

# CSD87503Q3E 30V N 沟道 NexFET™ 功率 MOSFET

## 1 特性

- 双 N 沟道共源极 MOSFET
- 针对 5V 栅极驱动器进行了优化
- 低热阻
- 低  $Q_g$  和  $Q_{gd}$
- 无铅引脚镀层
- 符合 RoHS 标准
- 无卤素
- 小外形尺寸无引线 (SON) 3.3mm × 3.3mm 塑料封装

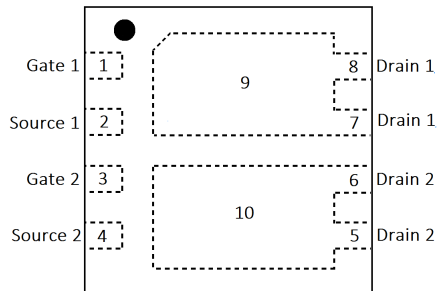
## 2 应用

- USB Type-C/PDVBUS 保护
- 电池保护
- 负载开关

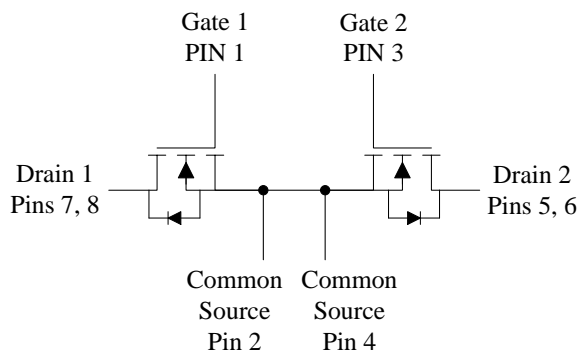
## 3 说明

CSD87503Q3E 是一款 30V、13.5mΩ、共源极、双路 N 沟道器件，专为 USB Type-C/PD 和电池保护而设计。此 3.3 × 3.3mm SON 器件具有低漏极至漏极导通电阻，可最大限度地减少损耗，且具有较少的组件数量，适用于空间受限的应用。

顶视图



电路图像



产品概要

$T_A = 25^\circ\text{C}$		值	单位
$V_{DS}$	漏源电压	30	V
$Q_g$	总栅极电荷 (4.5V)	13.4	nC
$Q_{gd}$	栅极电荷 (栅极到漏极)	5.8	nC
$R_{DD(on)}$	漏极到漏极导通电阻	$V_{GS} = 4.5\text{V}$	17.3
		$V_{GS} = 10\text{V}$	13.5
$V_{GS(th)}$	阈值电压	1.7	V

器件信息(1)

器件	数量	包装介质	封装	发货
CSD87503Q3E	2500	13 英寸卷带	SON 3.30mm × 3.30mm 塑料封装	卷带封装
CSD87503Q3ET	250	7 英寸卷带		

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

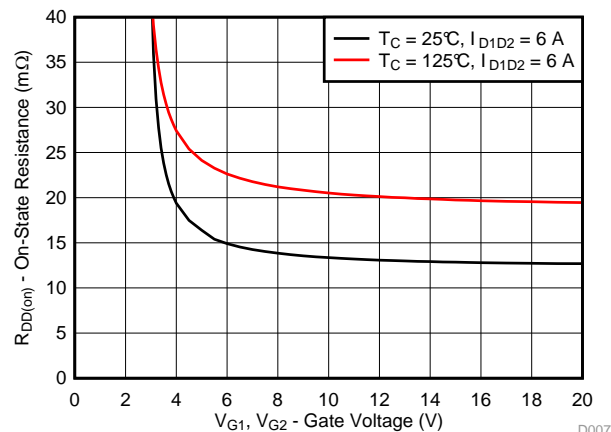
绝对最大额定值

$T_A = 25^\circ\text{C}$		值	单位
$V_{DS}$	漏源电压	30	V
$V_{GS}$	栅源电压	±20	V
$I_{D1, D2}$	持续漏极到漏极电流 (受封装限制)	10	A
$I_{DS}$	持续漏极到源极电流 (受封装限制)	1.5	A
$I_{D1, D2M}$	脉冲漏极到漏极电流 <sup>(1)</sup>	89	A
$P_D$	功率耗散 <sup>(2)</sup>	2.6	W
$P_D$	功耗, $T_C = 25^\circ\text{C}$	15.6	W
$T_J, T_{stg}$	工作结温、 储存温度	-55 至 150	°C

(1) 最大  $R_{\theta JC} = 8^\circ\text{C/W}$ ，脉冲持续时间  $\leq 100\mu\text{s}$ ，占空比  $\leq 1\%$ 。

(2) 典型  $R_{\theta JA} = 50^\circ\text{C/W}$  (当在 0.06 英寸 (1.52mm) 厚的 FR4 PCB 上将其安装在 1 平方英寸 (6.45cm<sup>2</sup>) 2oz (0.071mm) 厚的铜焊盘上时)。

$R_{DD(on)}$  与  $V_{GS}$  之间的关系



D007



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## 4 修订历史记录

日期	修订版本	说明
2017 年 9 月	*	初始发行版。

## 5 Specifications

### 5.1 Electrical Characteristics

 $T_A = 25^\circ\text{C}$  (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>STATIC CHARACTERISTICS</b>							
$BV_{DSS}$	Drain-to-source voltage <sup>(1)</sup>	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V	
$I_{DSS}$	Drain-to-source leakage current <sup>(1)</sup>	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$			1	$\mu\text{A}$	
$I_{GSS}$	Gate-to-source leakage current <sup>(1)</sup>	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA	
$V_{GS(th)}$	Gate-to-source threshold voltage <sup>(1)</sup>	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.3	1.7	2.1	V	
$R_{DD(on)}$	Drain-to-drain on-resistance	$V_{GS} = 4.5\text{ V}, I_{D1D2} = 6\text{ A}$		17.3	21.9	m $\Omega$	
		$V_{GS} = 10\text{ V}, I_{D1D2} = 6\text{ A}$		13.5	16.9		
$g_{fs}$	Transconductance	$V_{DS} = 3\text{ V}, I_{D1D2} = 6\text{ A}$		24		S	
<b>DYNAMIC CHARACTERISTICS</b>							
$C_{ISS}$	Input capacitance	$V_{GS} = 0\text{ V}, V_{D1D2} = 15\text{ V}, f = 1\text{ MHz}$		782	1020	pF	
$C_{OSS}$	Output capacitance			157	204	pF	
$C_{RSS}$	Reverse transfer capacitance			149	194	pF	
$R_g$	Series gate resistance <sup>(1)</sup>			1.5	3.0	$\Omega$	
$Q_g$	Gate charge total (4.5 V)	$V_{D1D2} = 15\text{ V}, I_{D1D2} = 6\text{ A}$		13.4	17.4	nC	
	Gate charge total (10 V)			32.9	42.8		
$Q_{gd}$	Gate charge gate-to-drain			5.8		nC	
$Q_{gs}$	Gate charge gate-to-source			4.8		nC	
$Q_{g(th)}$	Gate charge at $V_{th}$			1.0		nC	
$Q_{OSS}$	Output charge		$V_{D1D2} = 15\text{ V}, V_{GS} = 0\text{ V}$		4.3		nC
$t_{d(on)}$	Turnon delay time		$V_{D1D2} = 15\text{ V}, V_{GS} = 10\text{ V}, I_{D1D2} = 6\text{ A}, R_G = 0\ \Omega$		10		ns
$t_r$	Rise time				40		ns
$t_{d(off)}$	Turnoff delay time			25		ns	
$t_f$	Fall time			8		ns	
<b>DIODE CHARACTERISTICS</b>							
$V_{SD}$	Diode forward voltage <sup>(1)</sup>	$I_D = 0.5\text{ A}, V_{GS} = 0\text{ V}$		0.75	0.95	V	
$Q_{rr}$	Reverse recovery charge <sup>(1)</sup>	$V_{DS} = 15\text{ V}, I_F = 6\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		9.2		nC	
$t_{rr}$	Reverse recovery time <sup>(1)</sup>			14		ns	

(1) Parameter measured on both MOSFETs individually. Table values are for a single FET.

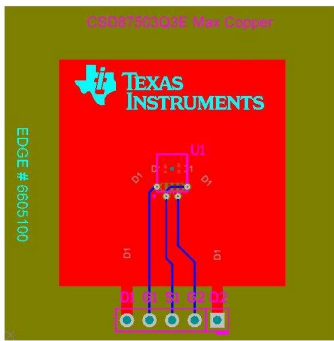
### 5.2 Thermal Information

 $T_A = 25^\circ\text{C}$  (unless otherwise stated)

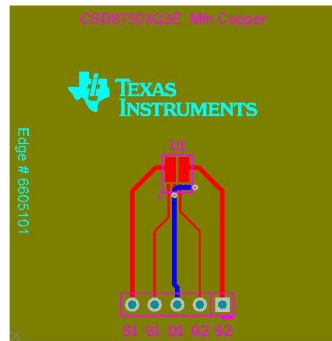
THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance <sup>(1)</sup>			8	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient thermal resistance <sup>(1)(2)</sup>			60	$^\circ\text{C}/\text{W}$

(1)  $R_{\theta JC}$  is determined with the device mounted on a 1-in<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz (0.071-mm) thick Cu pad on a 1.5-in × 1.5-in (3.81-cm × 3.81-cm), 0.06-in (1.52-mm) thick FR4 PCB.  $R_{\theta JC}$  is specified by design, whereas  $R_{\theta JA}$  is determined by the user's board design.

(2) Device mounted on FR4 material with 1-in<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz (0.071-mm) thick Cu.



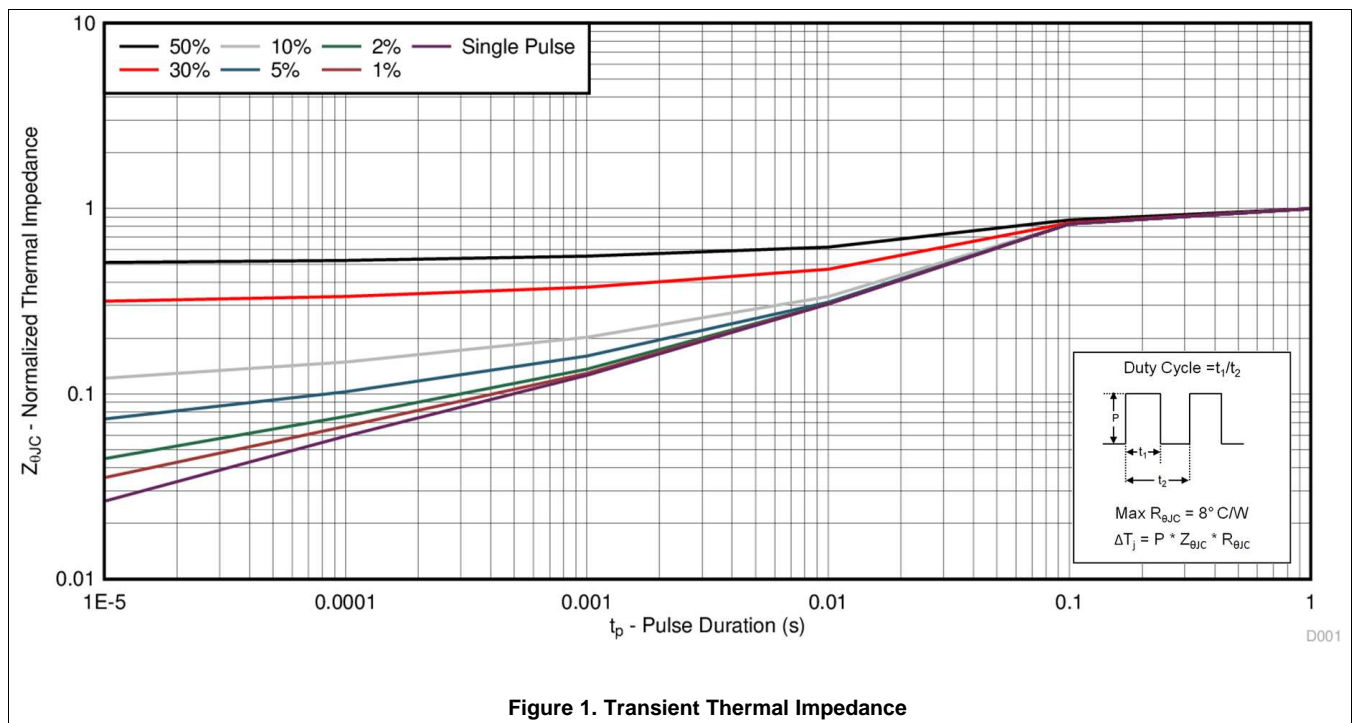
Max  $R_{\theta JA} = 60^{\circ}\text{C/W}$  when mounted on 1 in<sup>2</sup> (6.45 cm<sup>2</sup>) of 2-oz (0.071-mm) thick Cu.



Max  $R_{\theta JA} = 185^{\circ}\text{C/W}$  when mounted on a minimum pad area of 2-oz (0.071-mm) thick Cu.

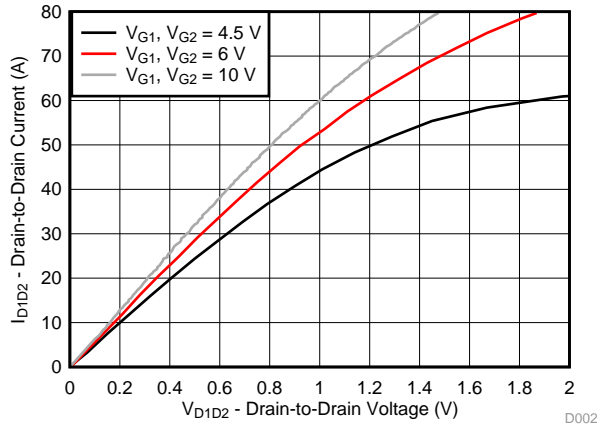
### 5.3 Typical MOSFET Characteristics

$T_A = 25^{\circ}\text{C}$  (unless otherwise stated)



Typical MOSFET Characteristics (continued)

T<sub>A</sub> = 25°C (unless otherwise stated)



Note: Measurement taken with both gates tied together

Figure 2. Saturation Characteristics

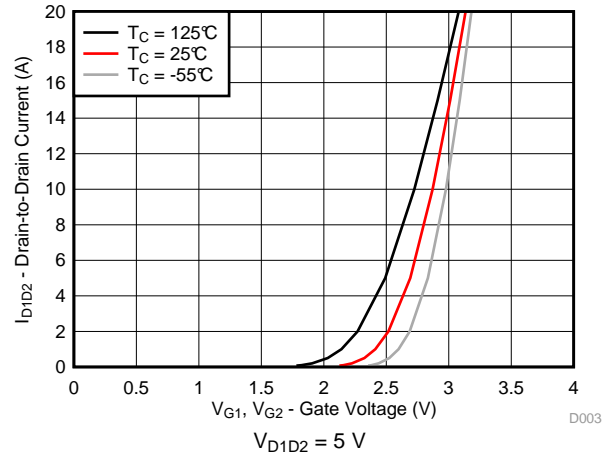


Figure 3. Transfer Characteristics

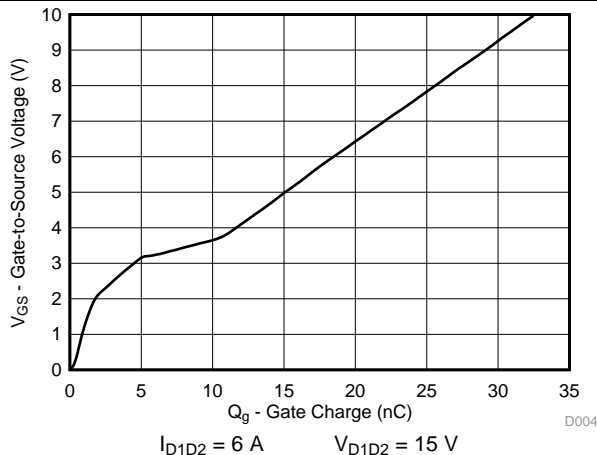


Figure 4. Gate Charge

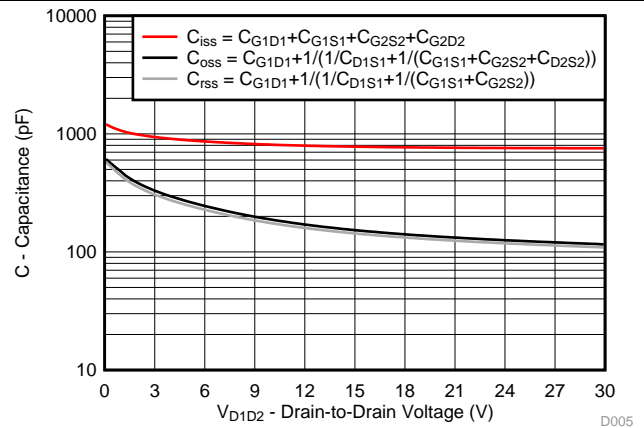


Figure 5. Capacitance

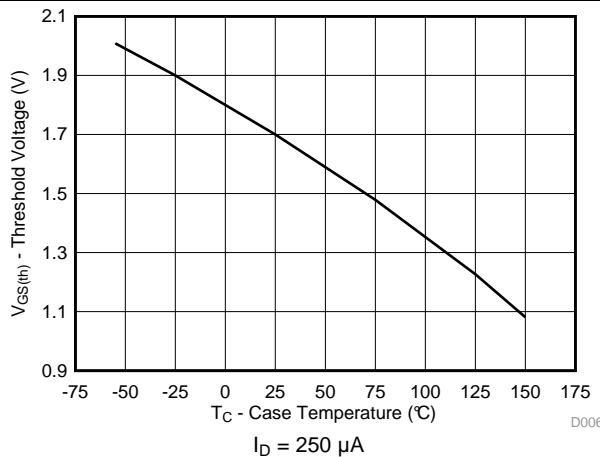


Figure 6. Threshold Voltage vs Temperature

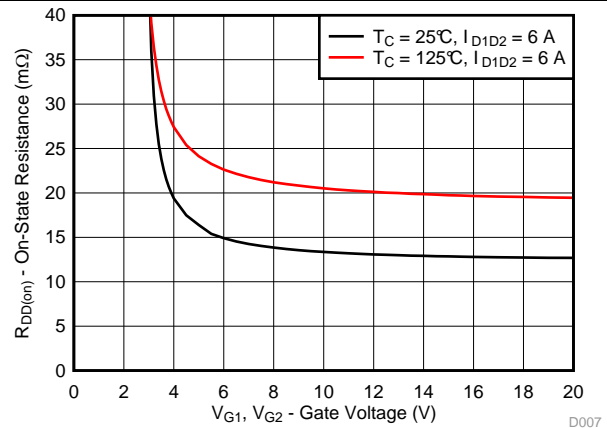


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

T<sub>A</sub> = 25°C (unless otherwise stated)

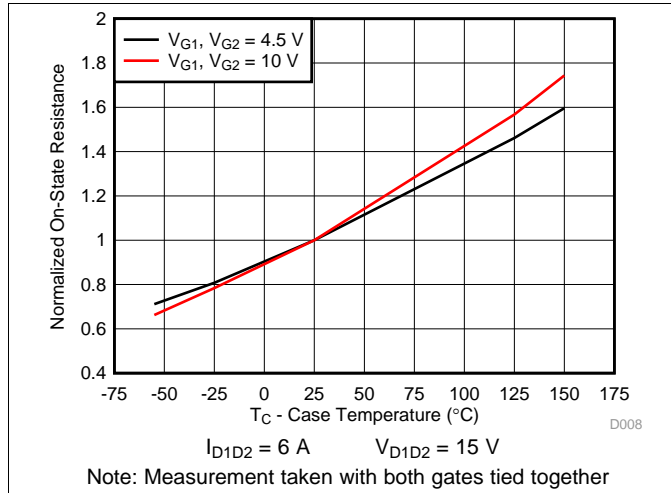


Figure 8. Normalized On-State Resistance vs Temperature

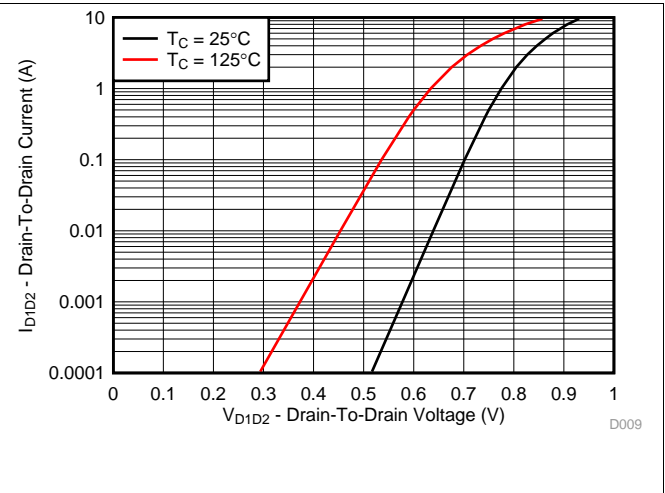


Figure 9. Typical Diode Forward Voltage

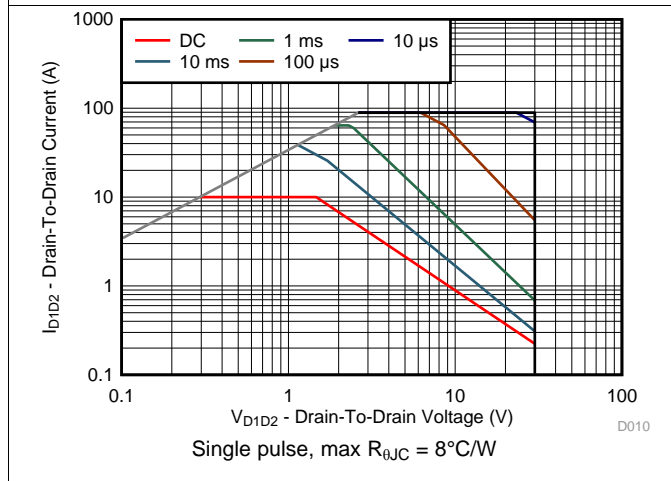


Figure 10. Maximum Safe Operating Area

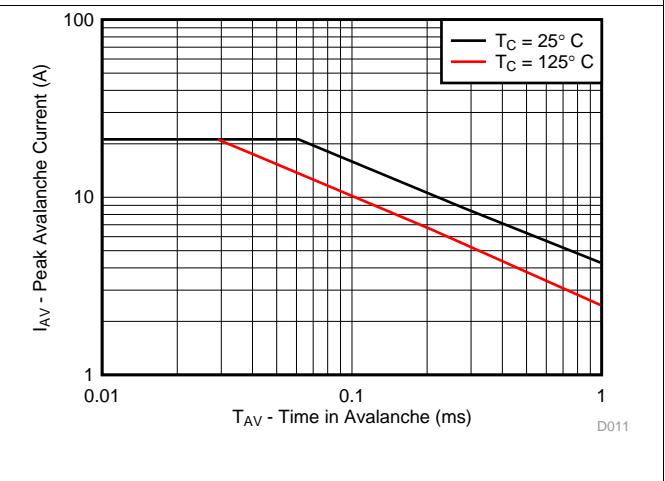


Figure 11. Single Pulse Unclamped Inductive Switching

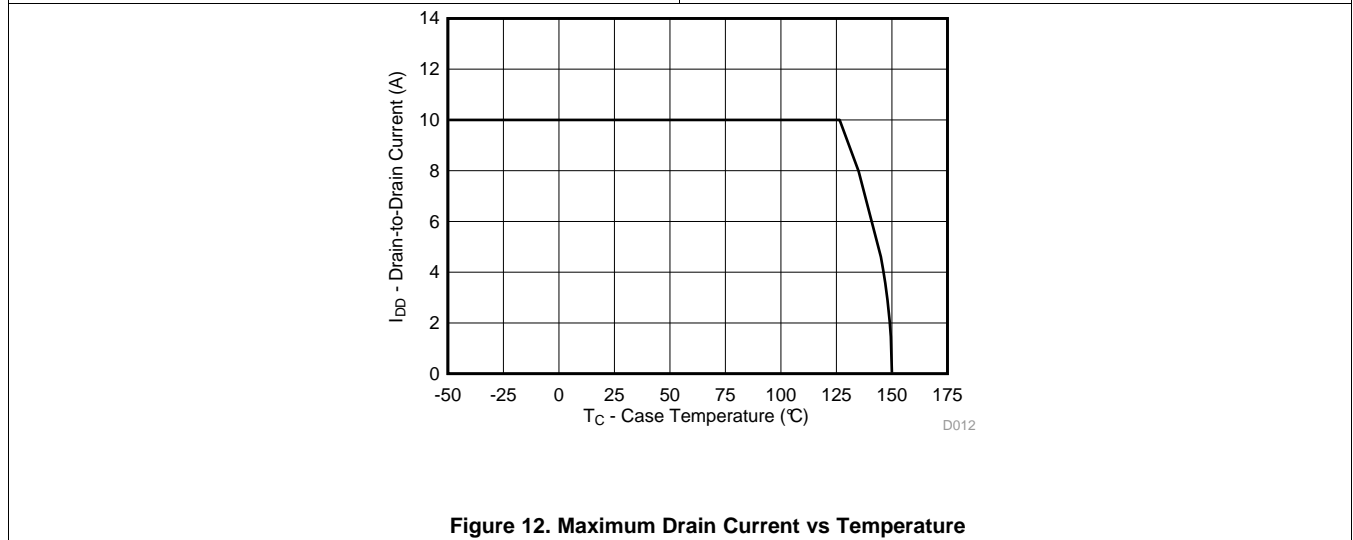


Figure 12. Maximum Drain Current vs Temperature

## 6 器件和文档支持

### 6.1 接收文档更新通知

要接收文档更新通知，请导航至 TI.com 上的器件产品文件夹。单击右上角的 [通知我](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 6.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

**TI E2E™ 在线社区** [TI 的工程师对工程师 \(E2E\) 社区](#)。此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

**设计支持** [TI 参考设计支持](#) 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

### 6.3 商标

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 6.4 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

### 6.5 Glossary

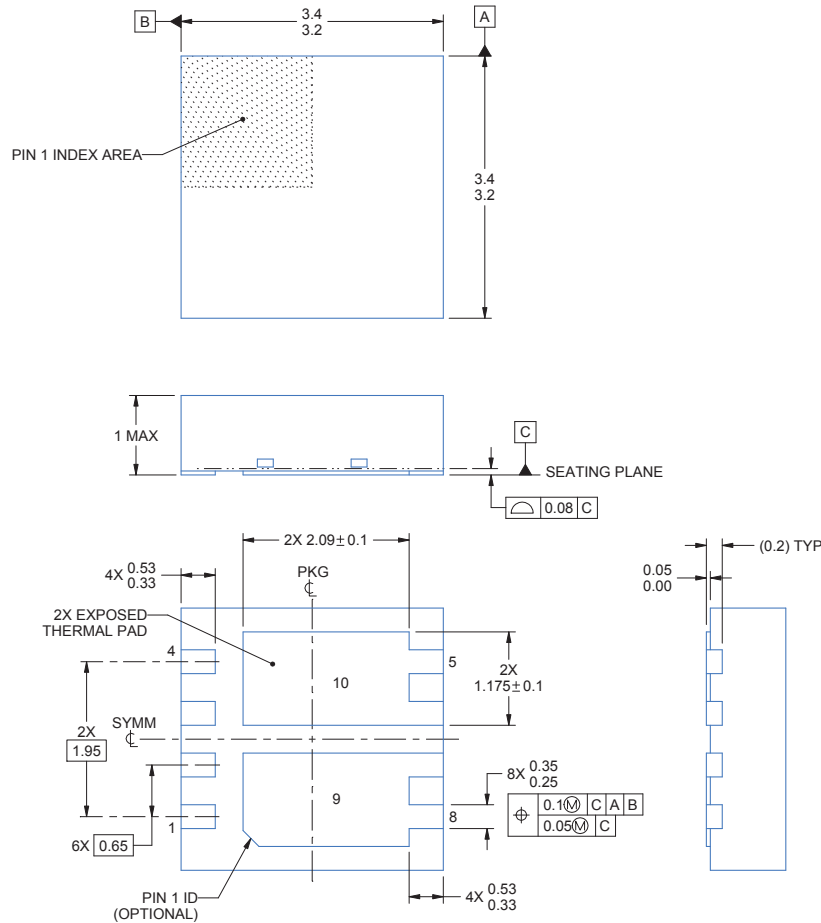
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 7 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航。

### 7.1 Q3 封装尺寸



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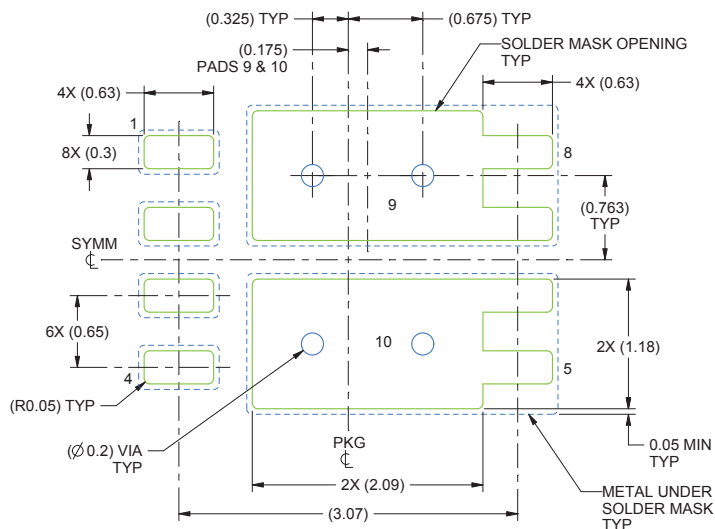
1. 所有线性尺寸的单位均为毫米。括号中的任何尺寸仅供参考。尺寸和公差值符合 ASME Y14.5M 标准。
2. 本图如有变更，恕不另行通知。
3. 封装散热盘必须在印刷电路板上焊接，包装散热和机械性能。

表 1. 引脚配置

位置	名称
引脚 1	栅极 1
引脚 2	共源极
引脚 3	栅极 2
引脚 4	共源极
引脚 5、6	漏极 2
引脚 7、8	漏极 1

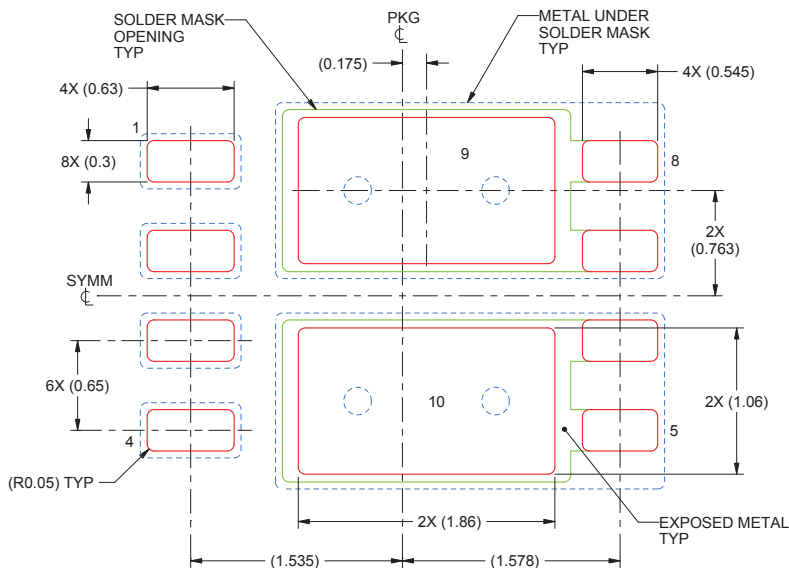


## 7.2 建议 PCB 布局



1. 此封装设计用于焊接到电路板的散热焊盘上。更多信息，请参见《[QFN/SON PCB 连接](#)》（文献编号：SLUA271）。
2. 根据具体应用决定是否选用通孔，请参见器件产品说明书。如需实施任意通孔，请参见此视图上的通孔位置。建议对焊锡膏下方的通孔进行填充、堵塞或包覆。
3. 本图如有变更，恕不另行通知。

## 7.3 建议模板开口



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PADS 9 & 10  
80% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

1. 具有漏斗形壁和圆角的激光切割孔可提供更佳的锡膏脱离。IPC-7525 可能提供替代设计建议。
2. 本图如有变更，恕不另行通知。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD87503Q3E	ACTIVE	VSON	DTD	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87503E	<a href="#">Samples</a>
CSD87503Q3ET	ACTIVE	VSON	DTD	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87503E	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD87503Q3E	VSON	DTD	8	2500	330.0	12.4	3.6	3.6	1.2	8.0	12.0	Q1
CSD87503Q3ET	VSON	DTD	8	250	178.0	13.5	3.6	3.6	1.2	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD87503Q3E	VSON	DTD	8	2500	364.0	357.0	31.0
CSD87503Q3ET	VSON	DTD	8	250	189.0	185.0	36.0

## 重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

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