

# 低偏移，1 至 5 差分 3.3V 低电压正射极耦合逻辑 (LVPECL) 扇出缓冲器

 查询样品: **LMK00725**

## 特性

- 5 个 3.3V 差分 LVPECL 输出
  - 附加抖动: 312.5MHz 时为 43fs RMS (典型值)
  - 噪声基底 ( $\geq 1\text{MHz}$  偏移): 312.5MHz 时为 -158dBc/Hz (典型值)
  - 输出频率: 650MHz (最大值)
  - 输出偏移: 35ps (最大值)
  - 部件间偏移: 100ps (最大值)
  - 传播延迟: 0.37ns (最大值)
- 两个差分输入对 (可由引脚选择)
  - CLKx, nCLK 输入对接受 LVPECL, 低压差分信号 (LVDS), 主机时钟信号电平 (HCSL), 短截线串联端接逻辑 (SSTL), 低压高速收发器逻辑 (LVHSTL) 或单端信号
- 同步时钟启用
- 电源: 3.3V  $\pm$  5%
- 封装: 20 引线薄型小尺寸封装 (TSSOP)
- 工业温度范围: -40°C 至 85°C
- 与 ICS85304-01 引脚兼容, 具有更低附加抖动和更宽温度范围

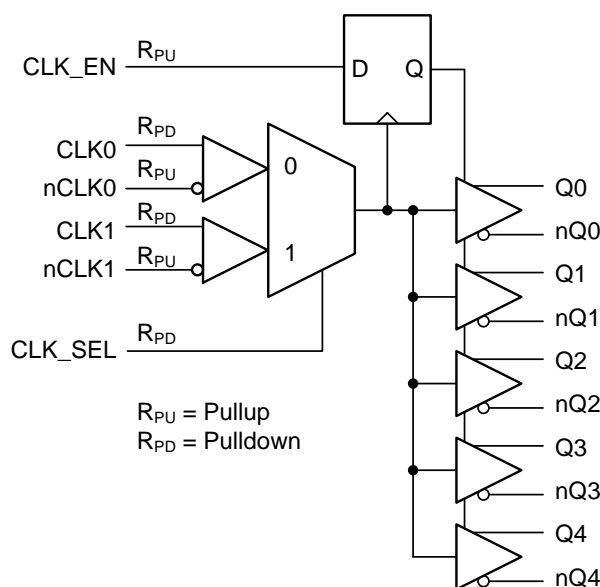
## 应用范围

- 无线和有线基础设施
- 网络和数据通信
- 服务器和计算
- 医疗成像
- 便携式测试和测量
- 高端 A/V

## 说明

LMK00725 是一款低偏移、高性能时钟扇出缓冲器，此缓冲器能够从可接受差分或单端输入的两个输入中的一个分发多达 5 个 3.3V LVPECL 输出。时钟使能输入在内部同步，以便在时钟使能引脚被置为有效或置为无效时消除输出上的欠幅脉冲或毛刺脉冲。低附加抖动和相位噪声，以及可靠输出和部件间偏移特性使得 LMK00725 成为对高性能和可重复性有严格要求的应用的理想选择。

## FUNCTIONAL BLOCK DIAGRAM


 (1)  $R_{PU} = 51\text{ k}\Omega$  pullup,  $R_{PD} = 51\text{ k}\Omega$  pulldown

**Figure 1.**

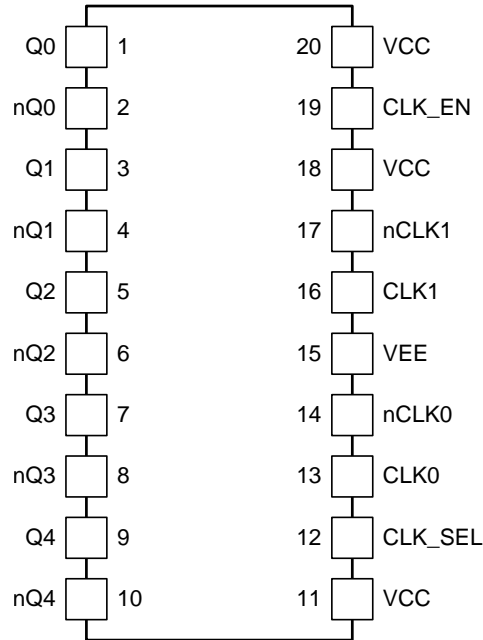

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**PINOUT DIAGRAM**



**Figure 2.**

**Table 1. PIN DESCRIPTIONS<sup>(1)(2)</sup>**

NO.	NAME	TYPE <sup>(1)</sup>	DESCRIPTION
1, 2	Q0, nQ0	O	LVPECL output pair 0
3, 4	Q1, nQ1	O	LVPECL output pair 1
5, 6	Q2, nQ2	O	LVPECL output pair 2
7, 8	Q3, nQ3	O	LVPECL output pair 3
9, 10	Q4, nQ4	O	LVPECL output pair 4
11, 18, 20	VCC	PWR	Power supply pins
12	CLK_SEL	I, R <sub>PD</sub>	Clock select input. LVCMOS / TTL compatible. 0 = Select CLK0, nCLK0 1 = Select CLK1, nCLK1
13	CLK0	I, R <sub>PD</sub>	Non-inverting differential clock input 0.
14	nCLK0	I, R <sub>PU</sub>	Inverting differential clock input 0.
15	VEE	PWR	Negative supply pin
16	CLK1	I, R <sub>PD</sub>	Non-inverting differential clock input 1.
17	nCLK1	I, R <sub>PU</sub>	Inverting differential clock input 1.
19	CLK_EN	I, R <sub>PU</sub>	Synchronous clock enable input. LVCMOS / TTL compatible. 0 = Qx outputs are forced low, nQx outputs are forced high. 1 = Clock outputs are enabled and follow clock input.

(1) G = Ground, I = Input, O = Output, P = Power, R<sub>PU</sub> = 51 kΩ pullup, R<sub>PD</sub> = 51 kΩ pulldown

(2) Please refer to [Recommendations for Unused Input and Output Pins](#), if applicable.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)(2)</sup>

Over operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
VCC	Supply Voltage	-0.3		3.6	V
V <sub>IN</sub>	Input Voltage Range	-0.3		VCC + 0.3	V
T <sub>STG</sub>	Storage Temperature Range	-65		150	°C
T <sub>J</sub>	Junction Temperature			150	°C
ESD	Electrostatic Discharge	Human Body Model (HBM)		2000	V
		Machine Model (MM)		150	
		Charged Device Model (CDM)		750	

- Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

## THERMAL CHARACTERISTICS

Over operating free-air temperature range (unless otherwise noted)

PARAMETER	$\theta_{JA}$	UNIT
Package Thermal Impedance, Junction to Air (0 LFPM)	107.2	°C/W

## RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VCC	Supply Voltage	VEE = GND	3.135	3.3	3.465	
I <sub>OUT</sub>	Output Current				30	mA
T <sub>A</sub>	Ambient Temperature		-40		85	°C
T <sub>J</sub>	Junction Temperature				125	°C

## POWER SUPPLY CHARACTERISTICS

Over operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
IEE	Power Supply Current through VEE			52	60	mA

## LVC MOS / TTL DC CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>IH</sub>	Input High Voltage		2		VCC + 0.3	V
V <sub>IL</sub>	Input Low Voltage		VEE - 0.3		0.4	V
I <sub>IH</sub>	Input High Current	VCC = V <sub>IN</sub> = 3.465 V				μA
		CLK_EN			5	
		CLK_SEL			150	
I <sub>IL</sub>	Input Low Current	VCC = 3.465V, V <sub>IN</sub> = 0 V				μA
		CLK_EN	-150			
		CLK_SEL	-5			
C <sub>IN</sub>	Input Capacitance			1		pF
R <sub>IN</sub>	Input Pullup or Pulldown Resistance			51		kΩ

## DIFFERENTIAL INPUT DC CHARACTERISTICS

Over operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>ID</sub>	Differential Input Voltage Swing (V <sub>IH</sub> -V <sub>IL</sub> ) <sup>(1)(2)</sup>		0.15		1.3	V
V <sub>ICM</sub>	Input Common Mode Voltage <sup>(1)(2)(3)</sup>		0.5		VCC – 0.85	V
I <sub>IH</sub>	Input High Current <sup>(4)</sup>	VCC = V <sub>IN</sub> = 3.465 V				μA
		nCLKx			5	
		CLKx			150	
I <sub>IL</sub>	Input Low Current <sup>(4)</sup>	VCC = 3.465V, V <sub>IN</sub> = 0 V				μA
		nCLKx	-150			
		CLKx	-5			

(1) V<sub>IL</sub> should not be less than -0.3V

(2) See [Figure 22](#)

(3) Input common mode voltage is defined as V<sub>IH</sub>

(4) For I<sub>IH</sub> and I<sub>IL</sub> measurements on CLKx (or nCLKx), care must be taken to comply with V<sub>ID</sub> and V<sub>ICM</sub> specifications using the appropriate bias on nCLKx (or CLKx)

## LVPECL OUTPUT CHARACTERISTICS

Over recommended operating free-air temperature range (unless otherwise noted), outputs terminated with 50Ω to VCC – 2V. All AC parameters measured at 500 MHz unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>OH</sub>	Output High Voltage	DC measurement	VCC – 1.4		VCC – 0.9	V
V <sub>OL</sub>	Output Low Voltage	DC measurement	VCC – 2.0		VCC – 1.6	V
V <sub>OD</sub>	Output Voltage Swing (V <sub>OH</sub> -V <sub>OL</sub> )	DC measurement	0.575		0.85	V
f <sub>OUT</sub>	Output Frequency <sup>(1)</sup>				650	MHz
t <sub>PD</sub>	Propagation Delay <sup>(1)(2)</sup>	f ≤ 650 MHz	0.17	0.25	0.37	ns
t <sub>SK(O)</sub>	Output Skew <sup>(1)(3)(4)</sup>				35	ps
t <sub>SK(PP)</sub>	Part-to-Part Skew <sup>(1)(4)(5)</sup>				100	ps
t <sub>R</sub> / t <sub>F</sub>	Output Rise/Fall Time <sup>(1)</sup>	20% to 80%, f=50 MHz		100	200	ps
J <sub>ADD</sub>	Additive Jitter <sup>(6)</sup>	f = 156.25 MHz, Input slew rate ≥ 3 V/ns, 10 KHz to 20 MHz integration band		75		fs RMS
		f = 312.5 MHz, Input slew rate ≥ 3 V/ns, 10 kHz to 20 MHz integration band		43		

(1) Parameter is specified by characterization. Not tested in production.

(2) Measured from the differential input crossing point to the differential output crossing point.

(3) Defined as skew between outputs at the same supply voltage and with equal loading conditions. Measured at the output differential crossing points.

(4) Parameter is defined in accordance with JEDEC Standard 65.

(5) Calculation for part-to-part skew is the difference between the fastest and slowest t<sub>PD</sub> across multiple devices, operating at the same supply voltage, same frequency, same temperature, with equal load conditions, and using the same type of inputs on each device. Measured at the output differential crossing points.

(6) Buffer Additive Jitter: J<sub>ADD</sub> = SQRT(J<sub>SYSTEM</sub> - J<sub>SOURCE</sub>), where J<sub>SYSTEM</sub> is the RMS jitter of the system output (source+buffer) and J<sub>SOURCE</sub> is the RMS jitter of the input source, and system output noise is not correlated to the input source noise. Additive jitter should be considered only when the input source noise floor is 3 dB or better than the buffer noise floor (NF). This is usually the case for high-quality ultra-low-noise oscillators. Please refer to [System-Level Phase Noise and Additive Jitter Measurement](#) for input source and measurement details.

**LVPECL OUTPUT CHARACTERISTICS (continued)**

Over recommended operating free-air temperature range (unless otherwise noted), outputs terminated with 50Ω to VCC – 2V. All AC parameters measured at 500 MHz unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
PN <sub>FLOOR</sub>	Phase Noise Floor <sup>(7)</sup>	f = 156.25 MHz, Input slew rate ≥ 3 V/ns, 10 kHz to 20 MHz integration band				dBc/Hz		
		10 kHz offset		-145				
		100 kHz offset		-153				
		1 MHz offset		-158				
		10 MHz offset		-159				
		20 MHz offset		-159				
				f = 312.5 MHz, Input slew rate ≥ 3 V/ns, 10 kHz to 20 MHz integration band				dBc/Hz
				10 kHz offset		-149		
				100 kHz offset		-154		
				1 MHz offset		-156		
10 MHz offset				-158				
20 MHz offset				-158				
ODC	Output Duty Cycle <sup>(8)</sup>	50% Input Duty Cycle	48	50	52	%		
PSRR	Power Supply Ripple Rejection <sup>(9)</sup>	f = 100 MHz, VCC ripple = 100 mVp-p @ 1 MHz		-80		dBc		

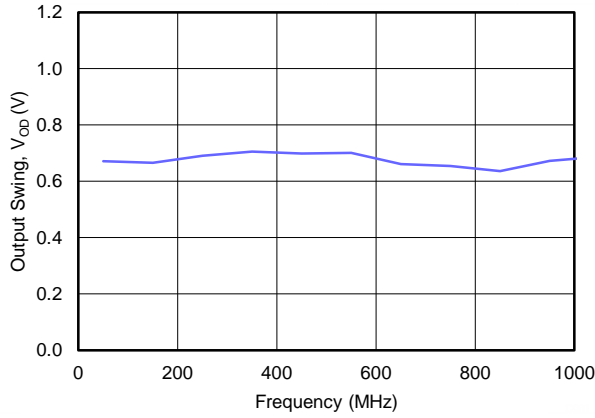
(7) Buffer Phase Noise Floor:  $PN_{FLOOR} \text{ (dBc/Hz)} = 10 \cdot \log_{10} [10^{(PN_{TOTAL}/10)} - 10^{(PN_{SOURCE}/10)}]$ , where  $PN_{TOTAL}$  is the phase noise floor of the system output (source+buffer) and  $PN_{SOURCE}$  is the phase noise floor of the input source. Buffer Phase Noise Floor should be considered only when the input source noise floor is 3 dB or better than the buffer noise floor ( $PN_{FLOOR}$ ). This is usually the case for high-quality ultra-low-noise oscillators. Please refer to [System-Level Phase Noise and Additive Jitter Measurement](#) for input source and measurement details.

(8) Parameter is specified by characterization. Not tested in production.

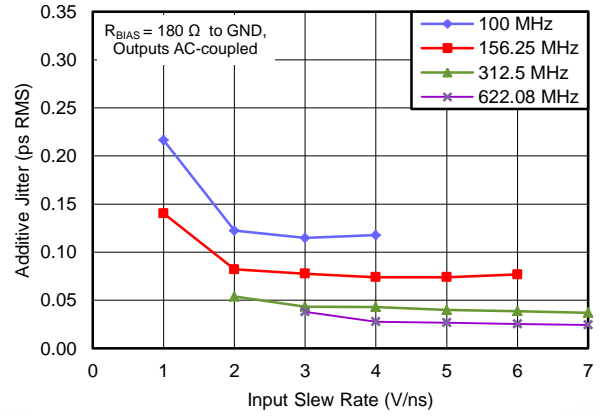
(9) Power supply ripple rejection, or PSRR, is defined as the single-sideband phase spur level (in dBc) modulated onto the clock output when a single-tone sinusoidal signal (ripple) is injected onto the VCC supply. Assuming no amplitude modulation effects and small index modulation, the peak-to-peak deterministic jitter (DJ) can be calculated using the measured single-sideband phase spur level (PSRR) as follows:  $DJ \text{ (ps p-p)} = [ (2 \times 10^{(PSRR/20)}) / (\pi \times f_{CLK}) ] \times 1E12$ .

### TYPICAL CHARACTERISTICS

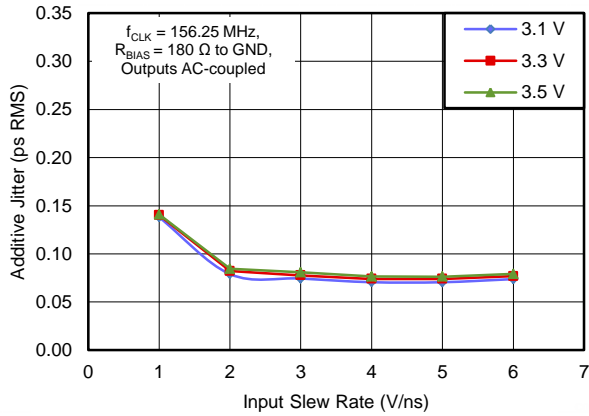
Unless otherwise noted:  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 3.3\text{ V}$ , Input slew rate  $\geq 3\text{ V/ns}$ , 10 kHz to 20 MHz integration band



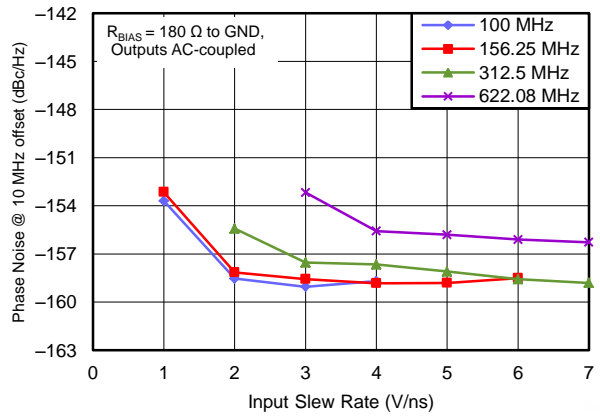
**Figure 3. Output Swing,  $V_{OD}$  (V) vs Frequency (MHz)**



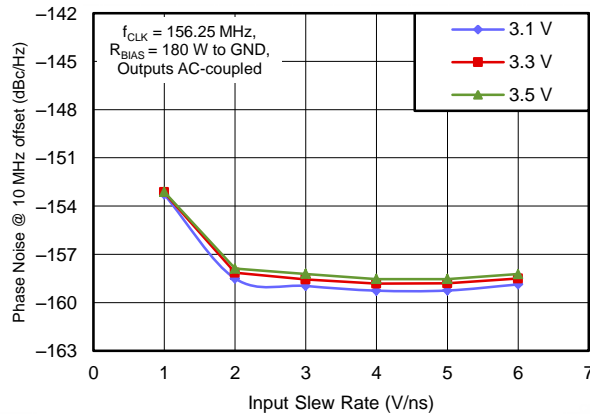
**Figure 4. Additive Jitter vs Input Slew Rate**



**Figure 5. Additive Jitter vs Input Slew Rate,  $f_{CLK} = 156.25\text{ MHz}$**



**Figure 6. Phase Noise Floor @ 10 MHz offset vs Input Slew Rate**



**Figure 7. Phase Noise Floor @ 10 MHz offset vs Input Slew Rate,  $f_{CLK} = 156.25\text{ MHz}$**

## FUNCTIONAL DESCRIPTIONS

### CONTROL INPUT FUNCTION

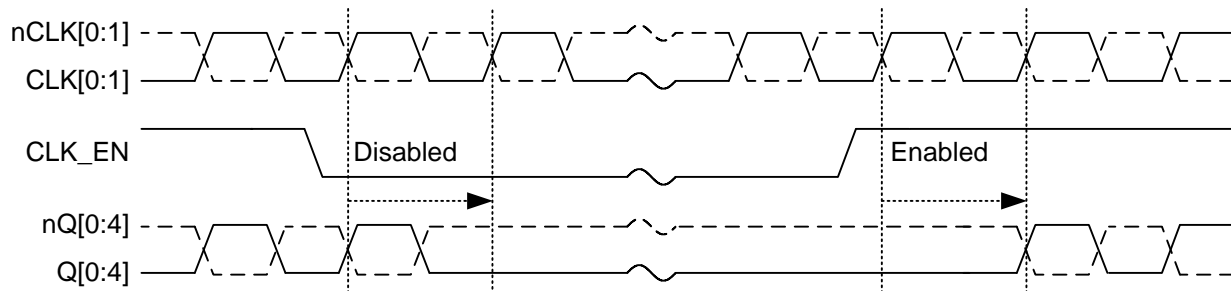
Over operating free-air temperature range (unless otherwise noted)

**Table 2.**

Inputs			Outputs	
CLK_EN	CLK_SEL	Selected Source	Qx	nQx
0	0	CLK0, nCLK0	Disabled; LOW	Disabled; HIGH
0	1	CLK1, nCLK1	Disabled; LOW	Disabled; HIGH
1	0	CLK0, nCLK0	Enabled	Enabled
1	1	CLK1, nCLK1	Enabled	Enabled

### CLOCK ENABLE TIMING

After CLK\_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in Figure 8. In the active mode, the output states are a function of the CLKx, nCLKx inputs as described in CLOCK INPUT FUNCTION.



**Figure 8. Clock Enable Timing Diagram**

### CLOCK INPUT FUNCTION

Over operating free-air temperature range (unless otherwise noted)

**Table 3.**

Inputs		Outputs		Input to Output Mode	Polarity
CLK0 or CLK1	nCLK0 or nCLK1	Qx	nQx		
0	1	LOW	HIGH	Differential to Differential	Non-inverting
1	0	HIGH	LOW	Differential to Differential	Non-inverting
0	Biased <sup>(1)</sup>	LOW	HIGH	Single-Ended to Differential	Non-inverting
1	Biased <sup>(1)</sup>	HIGH	LOW	Single-Ended to Differential	Non-inverting
Biased <sup>(1)</sup>	0	HIGH	LOW	Single-Ended to Differential	Inverting
Biased <sup>(1)</sup>	1	LOW	HIGH	Single-Ended to Differential	Inverting

(1) Refer to [Input DC Configuration During Device Test](#)

TEST LOAD CONFIGURATION

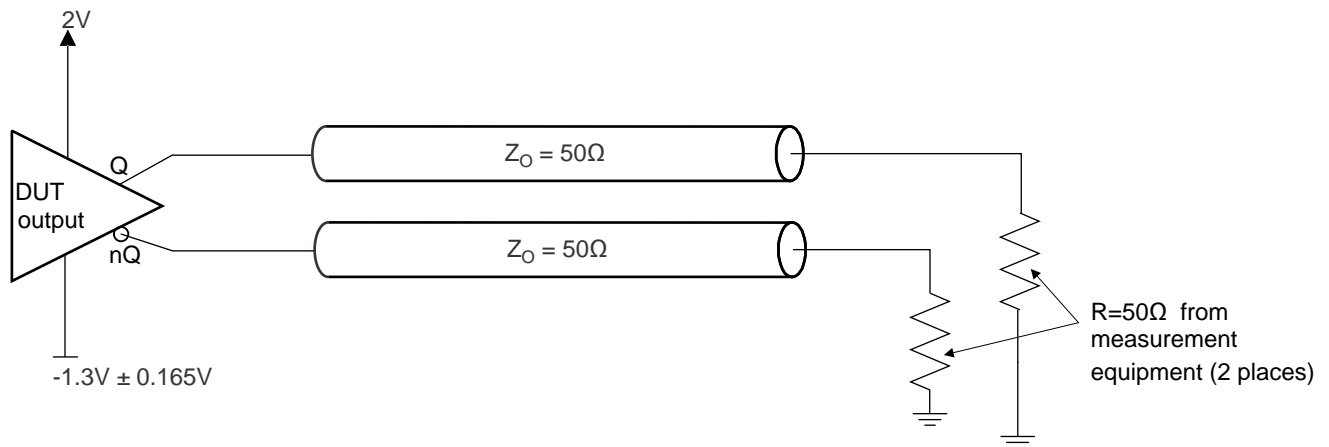


Figure 9. Output DC Configuration; Test Load Circuit



INPUT CLOCK INTERFACE CIRCUITS

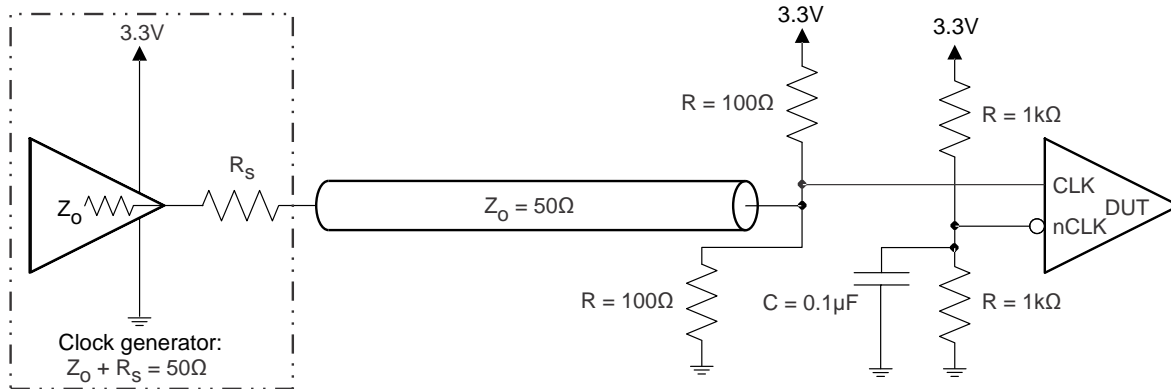


Figure 10. Single-Ended/LVCMOS Input DC Configuration During Device Test

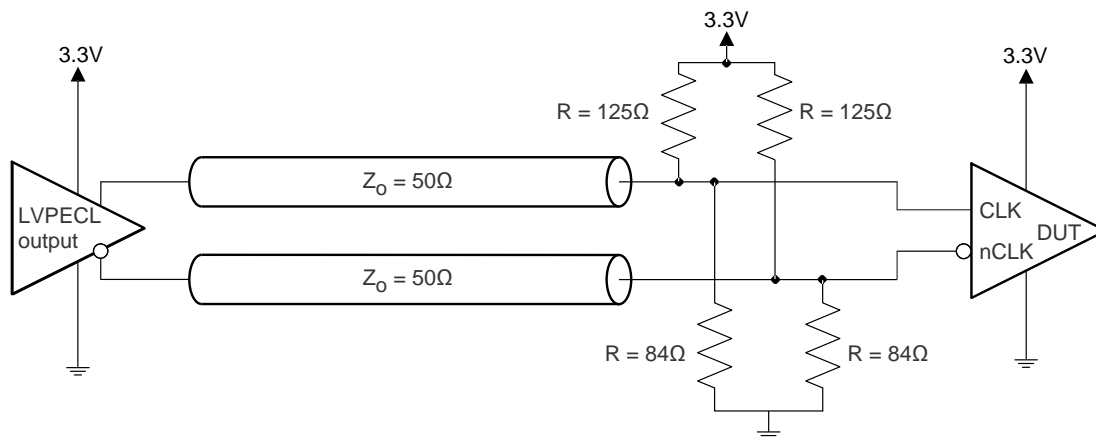


Figure 11. LVPECL Input Configuration During Device Test

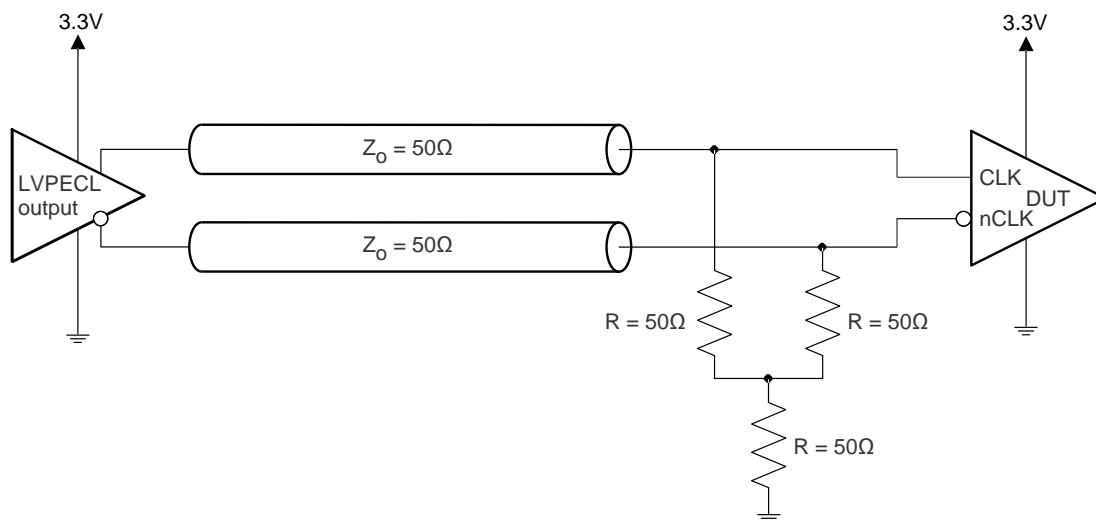


Figure 12. LVPECL Input Configuration During Device Test

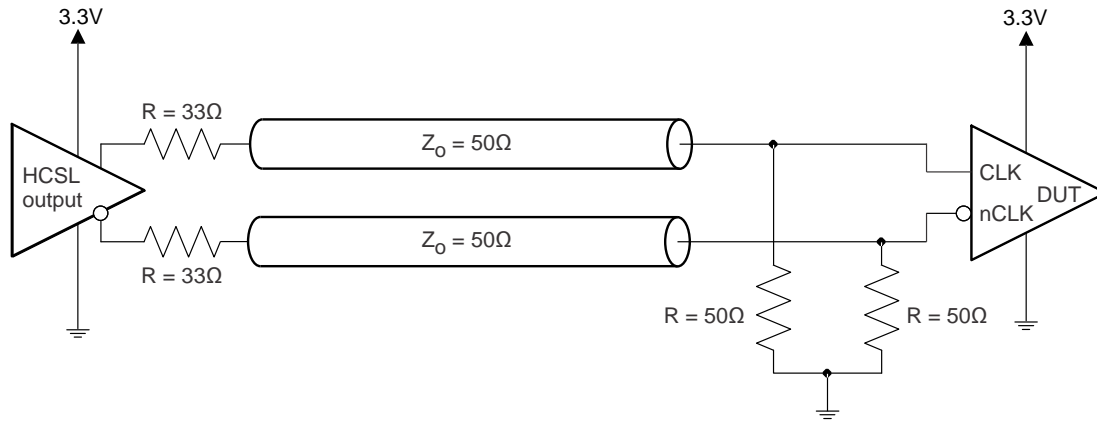


Figure 13. HCSL Input Configuration During Device Test

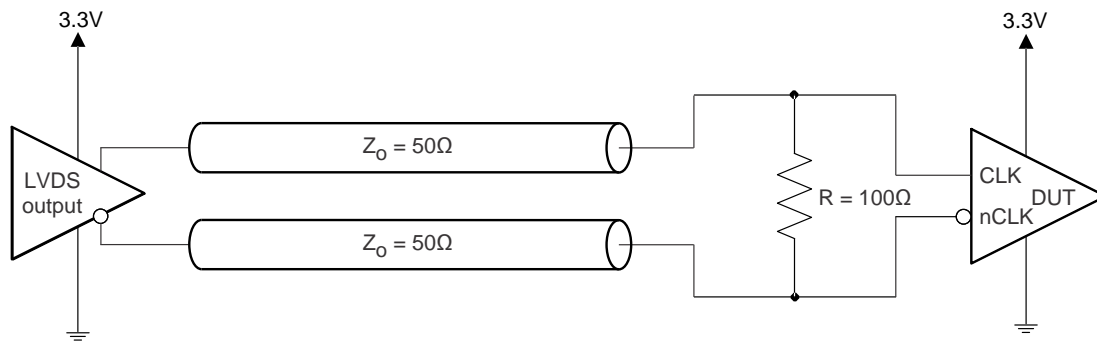


Figure 14. LVDS Input Configuration During Device Test

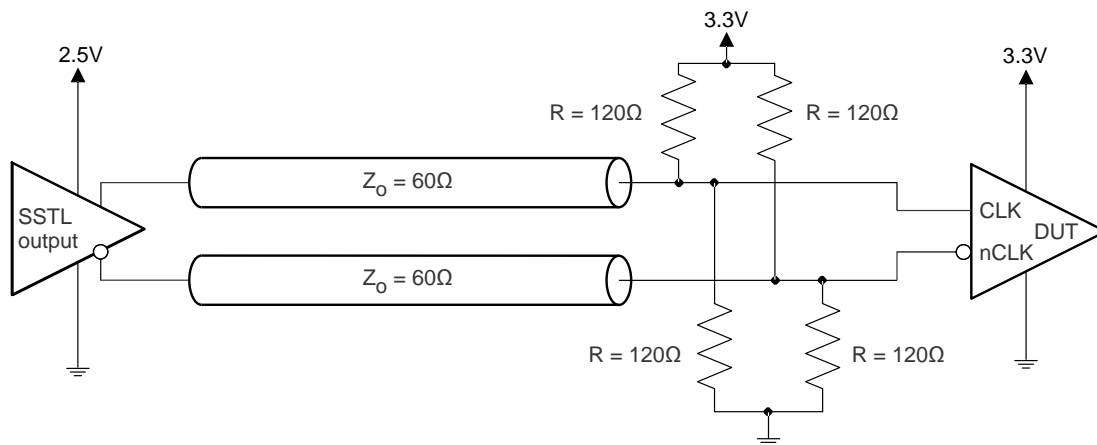


Figure 15. SSTL Input Configuration During Device Test

OUTPUT CLOCK INTERFACE CIRCUITS

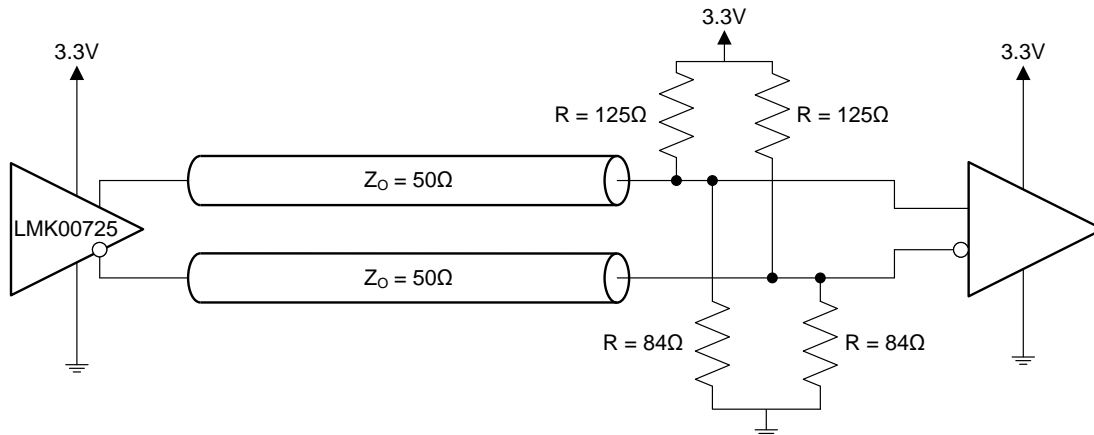


Figure 16. LVPECL Output DC Configuration: Typical Application Load

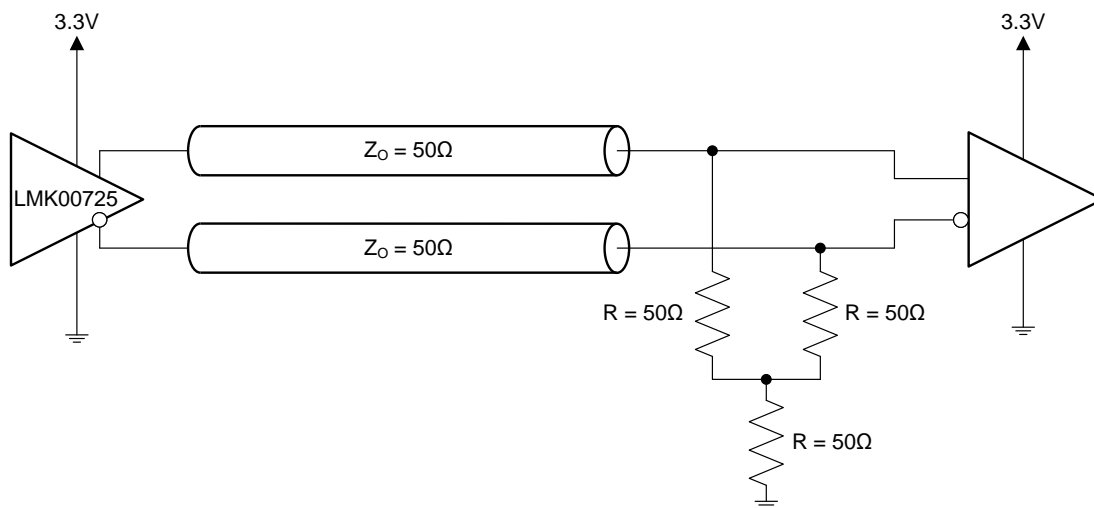
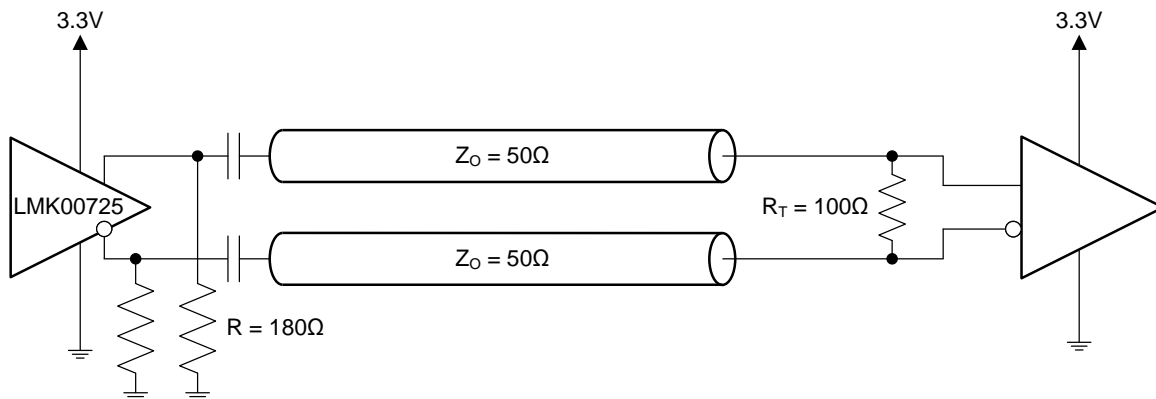


Figure 17. LVPECL Output DC Configuration: Typical Application Load



(1) R-bias can range from 120  $\Omega$  to 240  $\Omega$ , but 180  $\Omega$  is equivalent to loading outputs with 50  $\Omega$  to VCC - 2 V.

Figure 18. LVPECL Output AC Configuration: Typical Application Load

APPLICATION INFORMATION

Application Block Diagram Examples

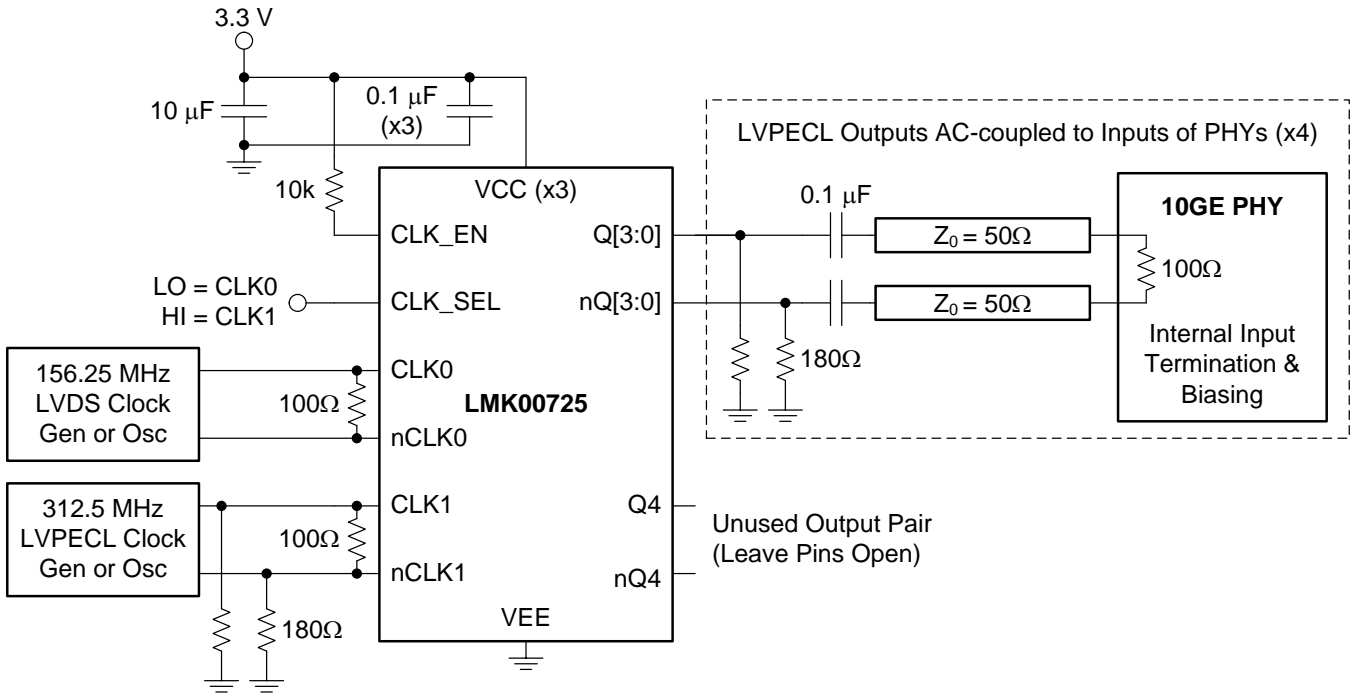


Figure 19. 10-Gigabit Ethernet PHY Clock Fanout with LVPECL Output AC Configuration

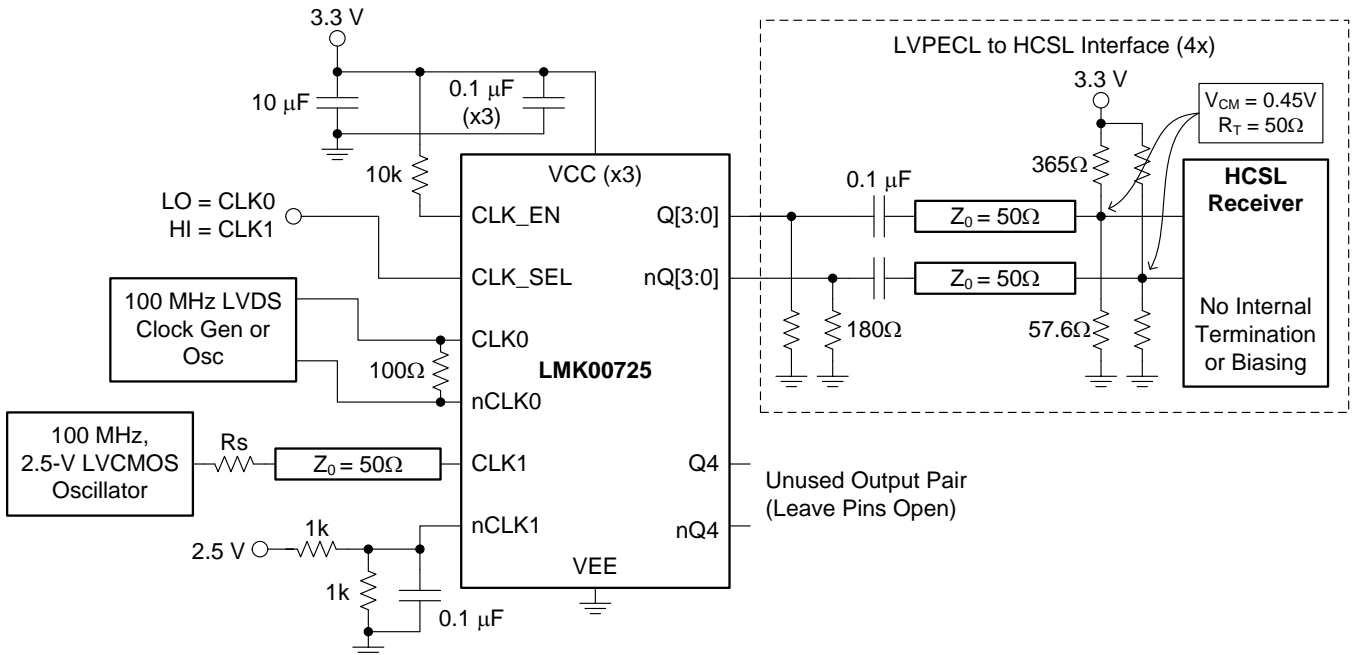


Figure 20. Interfacing LVPECL Outputs to HCSL Receiver Inputs

### Input Detail

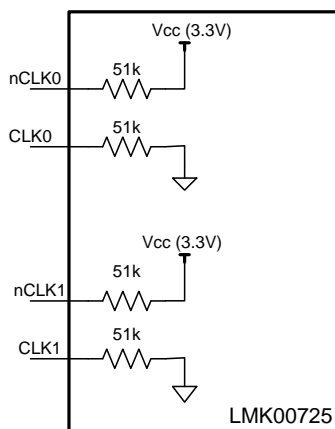
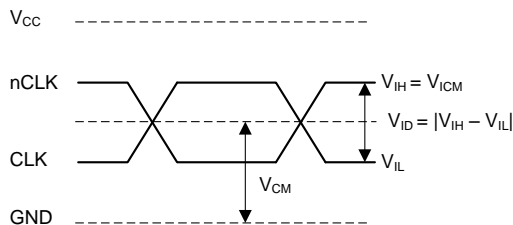


Figure 21. Clock Input Components

### Parameter Measurement Information



NOTE:  $V_{CM} = V_{ICM} - V_{ID}/2 = (V_{IH} + V_{IL})/2$

Figure 22. Differential Input Level

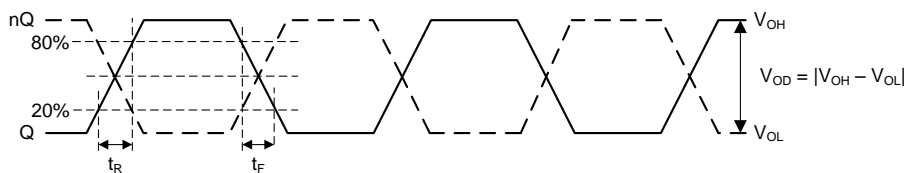


Figure 23. Output Voltage, and Rise and Fall Times

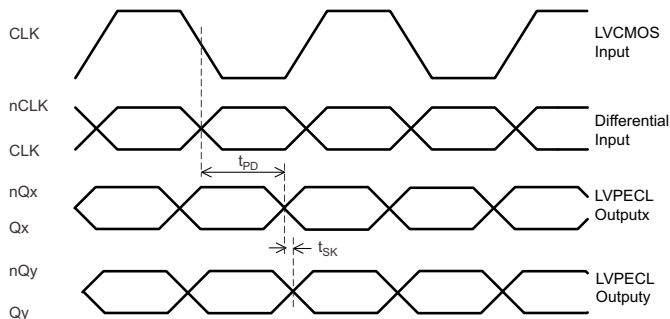


Figure 24. Differential and Single-Ended Output Skew and Propagation Delay

## Recommendations for Unused Input and Output Pins

- **CLK\_SEL and CLK\_EN:** These inputs have internal pull-up ( $R_{PU}$ ) or pull-down ( $R_{PD}$ ) according to [Figure 1](#) and can be left floating if unused. The floating state for CLK\_SEL is channel 0 selected, and the default for CLK-EN is normal output.
- **CLK/nCLK inputs:** See [Figure 21](#) for the internal connections. When using single ended input, take note of the internal pull-up and pull-down to make sure the unused input is properly biased. For single ended input, the [Figure 10](#) arrangement is recommended.
- **Outputs:** Unused outputs can be left floating or terminated. If left floating, it is recommended to not attach any traces to the output pins.

## Input Slew Rate Considerations

LMK00725 employs high-speed and low-latency circuit topology, allowing the device to achieve ultra-low additive jitter/phase noise and high-frequency operation. To take advantage of these benefits in the system application, it is optimal for the input signal to have a high slew rate of 3 V/ns or greater. Driving the input with a slower slew rate can degrade the additive jitter and noise floor performance. For this reason, a differential signal input is recommended over single-ended because it typically provides higher slew rate and common-mode-rejection. Refer to the “Additive RMS Jitter vs. Input Slew Rate” plots in the [TYPICAL CHARACTERISTICS](#) section. Also, using an input signal with very slow input slew rate, such as less than 0.05 V/ns, has the tendency to cause output switching noise to feed-back to the input stage and cause the output to chatter. This is especially true when driving either input in single-ended fashion with a very slow slew rate, such as a sine-wave input signal.

## System-Level Phase Noise and Additive Jitter Measurement

For high-performance devices, limitations of the equipment influence phase-noise measurements. The noise floor of the equipment is often higher than the noise floor of the device. The real noise floor of the device is probably lower. It is important to understand that system-level phase noise measured at the DUT output is influenced by the input source and the measurement equipment.

For [Figure 25](#) and [Figure 26](#) system-level phase noise plots, a Rohde & Schwarz SMA100A low-noise signal generator was cascaded with an Agilent 70429A K95 single-ended to differential converter block with ultra-low phase noise and fast edge slew rate (>3 V/ns) to provide a very low-noise clock input source to the LMK00725. An Agilent E5052 source signal analyzer with ultra-low measurement noise floor was used to measure the phase noise of the input source (SMA100A + 70429A K95) and system output (input source + LMK00725). The input source phase noise is shown by the light yellow trace, and the system output phase noise is shown by the dark yellow trace.

The additive phase noise or noise floor of the buffer ( $PN_{FLOOR}$ ) can be computed as follows:

$$PN_{FLOOR} \text{ (dBc/Hz)} = 10 * \log_{10} [10^{(PN_{SYSTEM}/10)} - 10^{(PN_{SOURCE}/10)}]$$

where

- $PN_{SYSTEM}$  is the phase noise of the system output (source+buffer)
  - $PN_{SOURCE}$  is the phase noise of the input source
- (1)

The additive jitter of the buffer ( $J_{ADD}$ ) can be computed as follows:

$$J_{ADD} = \text{SQRT}(J_{SYSTEM}^2 - J_{SOURCE}^2),$$

where

- $J_{SYSTEM}$  is the RMS jitter of the system output (source+buffer), integrated from 10 kHz to 20 MHz
  - $J_{SOURCE}$  is the RMS jitter of the input source, integrated from 10 kHz to 20 MHz
- (2)

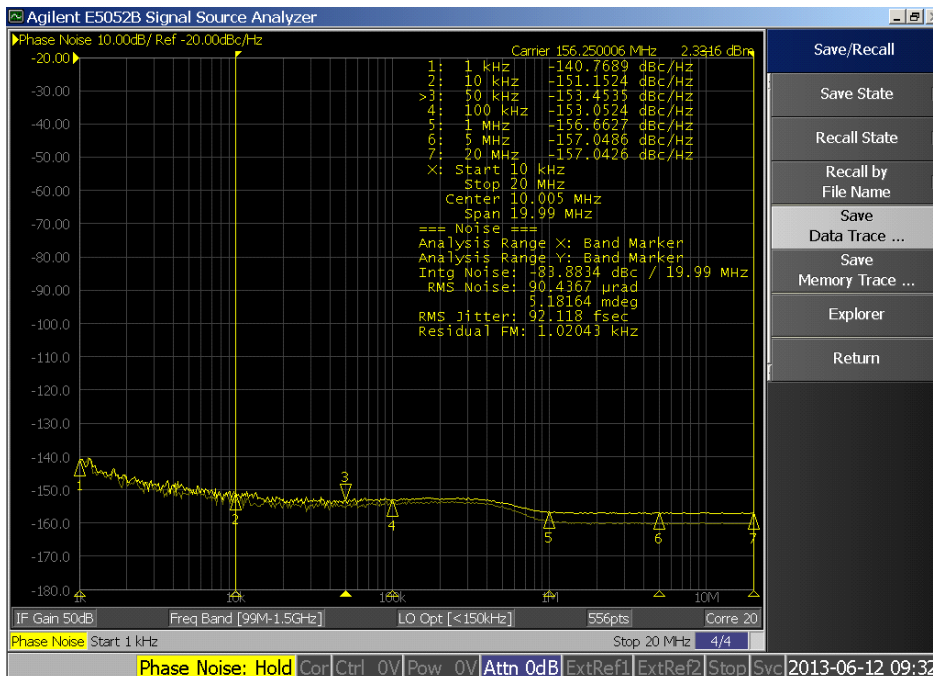


Figure 25. 156.25 MHz Input Phase Noise (66 fs rms, Light Yellow) and Output Phase Noise (92.1 fs rms, Dark Yellow). Additive Jitter = 65 fs rms (10 kHz to 20 MHz) @ 4 V/ns Input Slew Rate

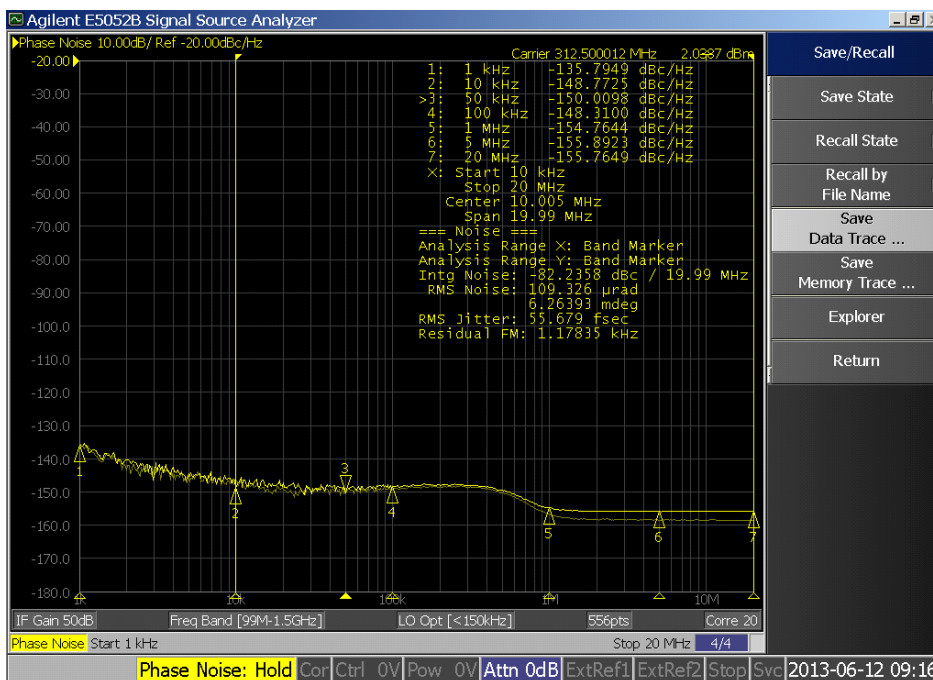


Figure 26. 312.5 MHz Input Phase Noise (43 fs rms, Light Yellow) and Output Phase Noise (55.7 fs rms, Dark Yellow). Additive Jitter = 36 fs rms (10 kHz to 20 MHz) @ 6 V/ns Input Slew Rate

## Power Considerations

The power dissipation of the LMK00725 consists of the quiescent power and load related power. Here is the expression for the total power which uses the values derived for "Quiescent Power" and "Load Power" further below:

$$P_{\text{Total}} = P_{\text{Q}} \text{ (worst case)} + P_{\text{L}} = 208 \text{ mW} + 30.2 \text{ mW} \times (\# \text{ of terminated outputs}) \quad (3)$$

For all 5 outputs terminated:

$$P_{\text{Total}} = 208 \text{ mW} + 27 \text{ mW} \times 5 = 343 \text{ mW} \quad (4)$$

### Quiescent Power:

$$P_{\text{Q}} = V_{\text{CC}} \times I_{\text{EE}} = 3.3\text{V} \times 60 \text{ mA} = 198 \text{ mW} \quad (5)$$

Considering a 5% tolerance on Vcc:

$$P_{\text{Q}} \text{ (worst case)} = 198 \text{ mW} \times 1.05 = 208 \text{ mW} \quad (6)$$

### Load Power:

Assuming 50% output duty cycle and 50 Ω load from each output (Q and nQ) to Vcc - 2 V (or 1.3 V) and output voltage levels of 1.1 V and 1.8 V below Vcc for V<sub>OH</sub> and V<sub>OL</sub> respectively:

$$P_{\text{L}} / \text{output\_pair} = P_{\text{high}} + P_{\text{low}} = \{1.1 \text{ V} \times [V_{\text{CC}} - 1.1 \text{ V} - (V_{\text{CC}} - 2 \text{ V})] / 50\Omega\} + \{1.8 \text{ V} \times [V_{\text{CC}} - 1.8 \text{ V} - (V_{\text{CC}} - 2 \text{ V})] / 50\Omega\} = 20 \text{ mW} + 7 \text{ mW} = 27 \text{ mW} \quad (7)$$

### NOTE

For dimensioning the power supply, consider the total power consumption. The total power consumption is the sum of device power consumption and the power consumption of the load.

## Thermal Management

Power consumption of the LMK00725 can be high enough to require attention to thermal management. For reliability and performance reasons, limit the die temperature to a maximum of 125°C. That is, as an estimate, T<sub>A</sub> (ambient temperature) plus device power consumption times θ<sub>JA</sub> should not exceed 125°C.

Assuming the conditions in the [Power Considerations](#) section and operating at an ambient temperature of 70°C with all outputs loaded, here is an estimate of the LMK00725 junction temperature:

$$T_{\text{J}} = T_{\text{A}} + P_{\text{Total}} \times \theta_{\text{JA}} = 70^\circ\text{C} + 343 \text{ mW} \times 107.2^\circ\text{C/W} = 70^\circ\text{C} + 37^\circ\text{C} = 107^\circ\text{C} \quad (8)$$

Here are some recommendations for improving heat flow away from the die:

- Use multi-layer boards
- Specify a higher copper thickness for the board
- Increase the number of vias from the top level ground plane under and around the device to internal layers and to the bottom layer with as much copper area flow on each level as possible
- Apply air flow
- Leave unused outputs floating



## Power-Supply Filtering

High-performance clock buffers are sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when jitter or phase noise is critical to applications.

Use of filter capacitors eliminates the low-frequency noise from power supply, where the bypass capacitors provide the very low-impedance path for high-frequency noise and guard the power-supply system against induced fluctuations. The bypass capacitors also provide instantaneous current surges as required by the device, and should have low ESR. To use the bypass capacitors properly, place them very close to the power supply pins and lay out traces with short loops to minimize inductance. TI recommends adding as many high-frequency bypass capacitors (such as 0.1- $\mu\text{F}$ , for example) as there are supply pins in the package. It is recommended, but not required, to insert a ferrite bead between the board power supply and the chip power supply to isolate the high-frequency switching noises generated by the clock driver, thereby preventing them from leaking into the board supply. Choosing an appropriate ferrite bead with very low DC resistance is important, because it is imperative to provide adequate isolation between the board supply and the chip supply. It is also imperative to maintain a voltage at the supply pins that is greater than the minimum voltage required for proper operation.

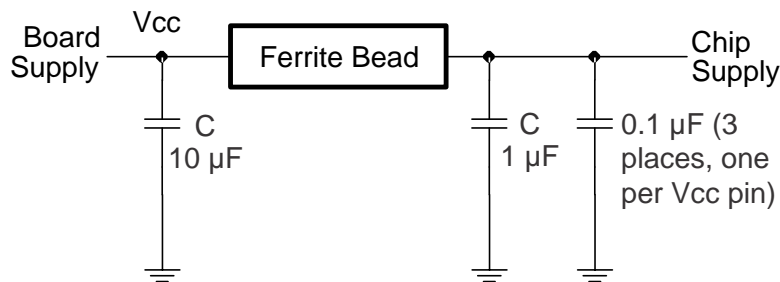


Figure 27. Power-Supply Decoupling

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMK00725PW	ACTIVE	TSSOP	PW	20	73	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMK00725	<a href="#">Samples</a>
LMK00725PWR	ACTIVE	TSSOP	PW	20	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMK00725	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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PW0020A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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