CSD16401Q5 25V N 沟道 NexFET™ 功率 MOSFET

1 特性

- 超低 Q_g 和 Q_{gd}
- 低热阻
- 雪崩额定值
- SON 5mm × 6mm 塑料封装

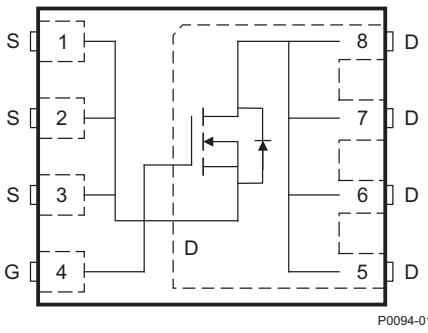
2 应用

- 用于网络、电信和计算系统等 应用 的负载点同步降压转换器
- 经优化可适用于同步 FET 应用

3 说明

这款采用 5mm × 6mm SON 封装的 25V、1.3mΩ NexFET™功率 MOSFET 旨在最大限度降低功率转换应用中的功率损耗。

俯视图



产品概要

T_A = 25°C		值		单位
V_{DS}	漏源电压	25		V
Q_g	总栅极电荷 (4.5V)	21		nC
Q_{gd}	栅极电荷（栅极到漏极）	5.2		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = 4.5V	1.8	mΩ
		V_{GS} = 10V	1.3	
$V_{GS(th)}$	阈值电压	1.5		V

器件信息(1)

器件	介质	数量	封装	发货
CSD16401Q5	13 英寸卷带	2500	SON 5.00mm × 6.00mm 塑料封装	卷带封装

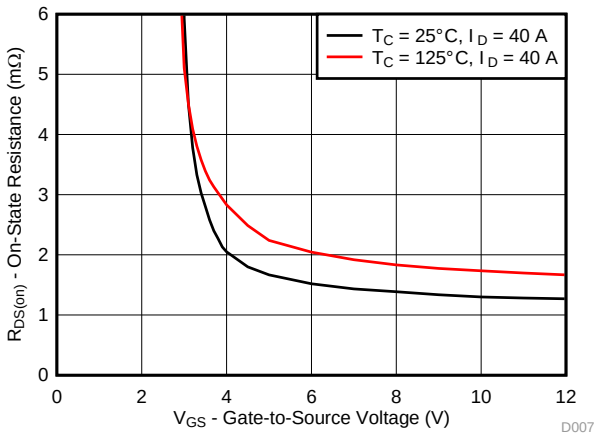
(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

绝对最大额定值

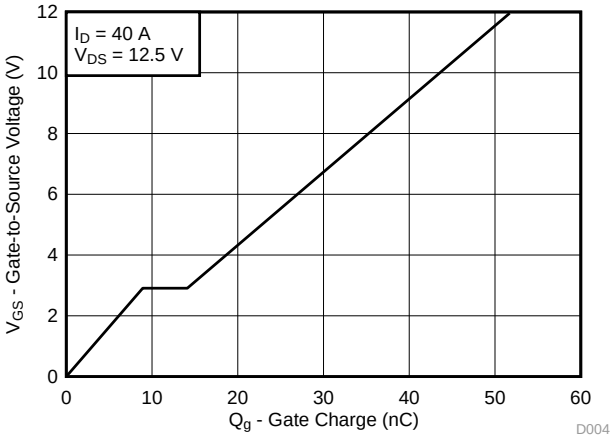
T_A = 25°C		值	单位
V_{DS}	漏源电压	25	V
V_{GS}	栅源电压	–12 至 16	V
I_D	持续漏极电流（受封装限制）	100	A
	持续漏极电流（受器件限制），T_C = 25°C	261	
	持续漏极电流(1)	38	
I_{DM}	脉冲漏极电流，T_A = 25°C(2)	240	A
P_D	功率耗散(1)	3.1	W
	功率耗散，T_C = 25°C	156	
T_J、T_{stg}	工作结温、贮存温度	–55 至 150	°C
E_{AS}	雪崩能量，单一脉冲 I_D = 100A，L = 0.1mH，R_G = 25Ω	500	mJ

(1) $R_{\theta JA}$ = 40°C/W，这是在一块 0.06in (1.52mm) 厚 FR4 PCB 上的 1in² (6.45cm²)、2oz (0.071mm) 厚覆铜焊盘上测得的值。
(2) 最大 $R_{\theta JC}$ = 0.8°C/W，脉冲持续时间 ≤ 100µs，占空比 ≤ 1%。

$R_{DS(ON)}$ 与 V_{GS} 间的关系



栅极电荷



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (August 2015) to Revision C **Page**

- Added V_{DS} = 5 V to Figure 3 4
- 已添加 *接收文档更新通知* 部分 7

Changes from Revision A (September 2010) to Revision B **Page**

- 已添加 在标题中添加了部件号 1
- 优化了 *说明* 1
- 添加了*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 1
- 更新了脉冲电流 1
- Updated Figure 1 to a normalized $R_{\theta JC}$ curve 4
- Updated the SOA in Figure 10 5

Changes from Original (August 2009) to Revision A **Page**

- 从 特性 列表中删除了环境项 1
- 删除了数据表末尾的*封装标记信息* 部分 10

5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise noted)

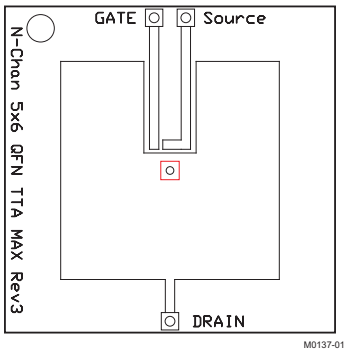
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_D = 250 µA	25			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 20 V			1	µA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = –12 V to 16 V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1.2	1.5	1.9	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 4.5 V, I_D = 40 A		1.8	2.3	mΩ
		V_{GS} = 10 V, I_D = 40 A		1.3	1.6	
g_{fs}	Transconductance	V_{DS} = 15 V, I_D = 40 A		168		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input capacitance	V_{GS} = 0 V, V_{DS} = 12.5 V, f = 1 MHz		3150	4100	pF
C_{OSS}	Output capacitance			2530	3300	pF
C_{RSS}	Reverse transfer capacitance			175	230	pF
R_g	Series gate resistance			1.2	2.4	Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 12.5 V, ID = 40 A		21	29	nC
Q_{gd}	Gate charge, gate-to-drain			5.2		nC
Q_{gs}	Gate charge, gate-to-source			8.3		nC
Qg(th)	Gate charge at Vth			4.8		nC
Q_{OSS}	Output charge	V_{DS} = 15 V, V_{GS} = 0 V		55		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 12.5 V, V_{GS} = 4.5 V, I_D = 40 A R_G = 2 Ω		16.6		ns
t_r	Rise time			30		ns
$t_{d(off)}$	Turnoff delay time			20		ns
t_f	Fall time			12.7		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_S = 40 A, V_{GS} = 0 V		0.85	1	V
Q_{rr}	Reverse recovery charge	V_{DD} = 15 V, I_F = 40 A, di/dt = 300 A/µs		72		nC
t_{rr}	Reverse recovery time	V_{DD} = 15 V, I_F = 40 A, di/dt = 300 A/µs		45		ns

5.2 Thermal Information

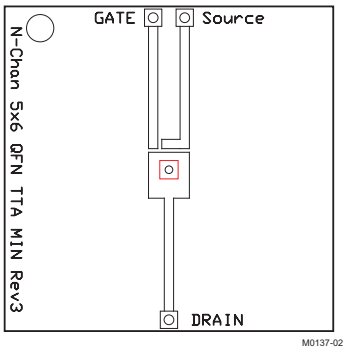
T_A = 25°C (unless otherwise noted)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal resistance, junction-to-case(1)			0.8	°C/W
$R_{\theta JA}$	Thermal resistance, junction-to-ambient(1)(2)			50	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-in (2.54-cm) square, 2-oz(0.071-mm) thick Cu pad on a 1.5-in × 1.5-in (3.81-cm × 3.81-cm), 0.06-in (1.52-mm) thick FR4 board. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1 in^2 (6.45 cm^2) of 2-oz (0.071-mm) thick Cu.



Max $R_{\theta JA}$ = 50°C/W when mounted on 1 in^2 (6.45 cm^2) of 2-oz (0.071-mm) thick Cu.



Max $R_{\theta JA}$ = 125°C/W when mounted on minimum pad area of 2-oz (0.071-mm) thick Cu.

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise noted)

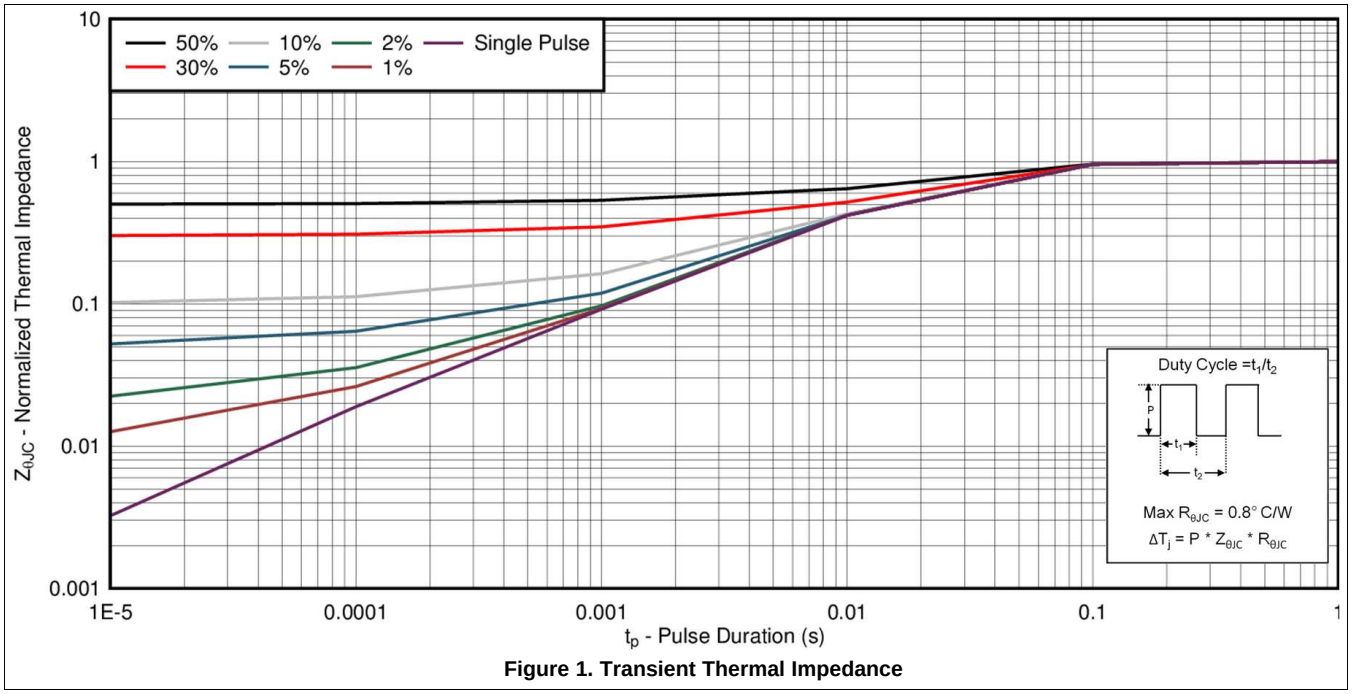


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise noted)

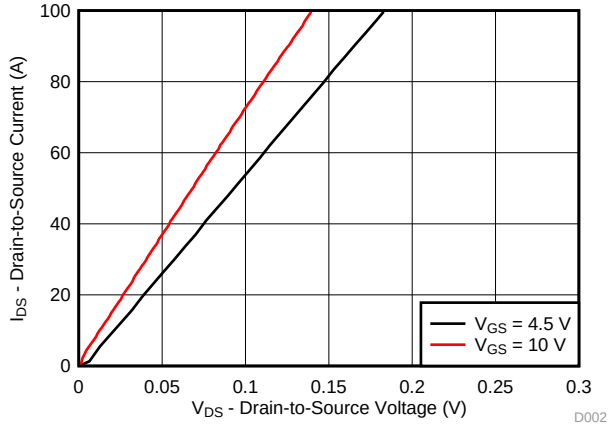


Figure 2. Saturation Characteristics

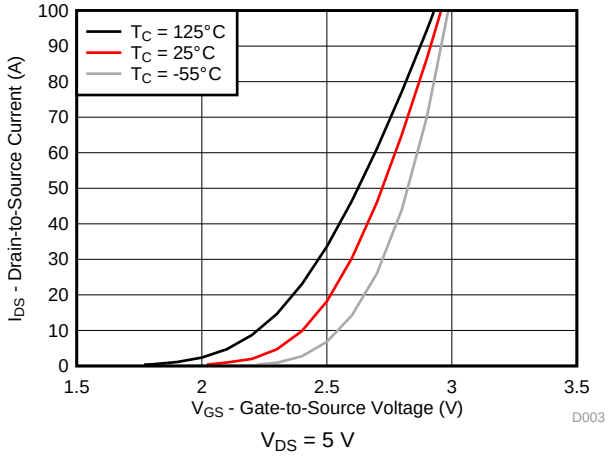


Figure 3. Transfer Characteristics

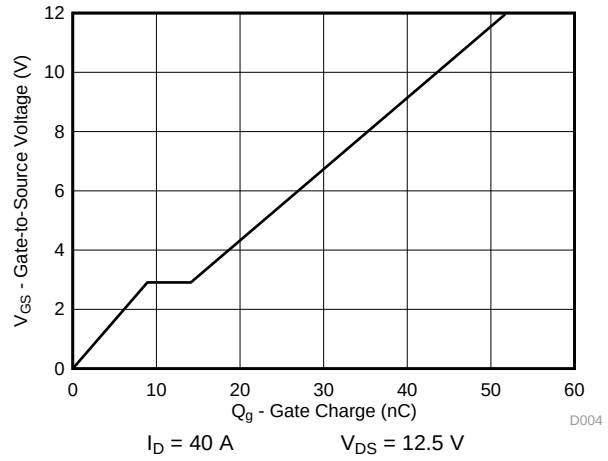


Figure 4. Gate Charge

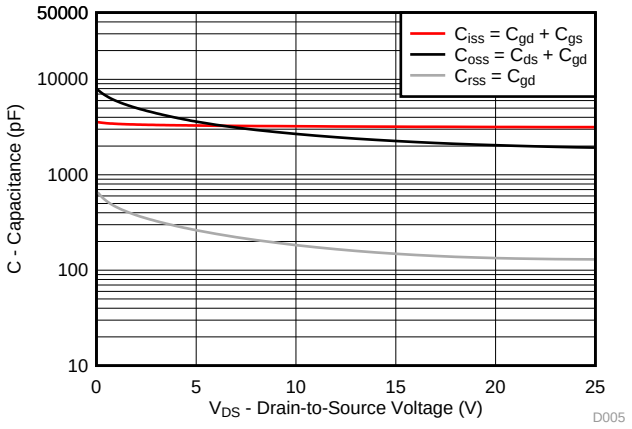


Figure 5. Capacitance

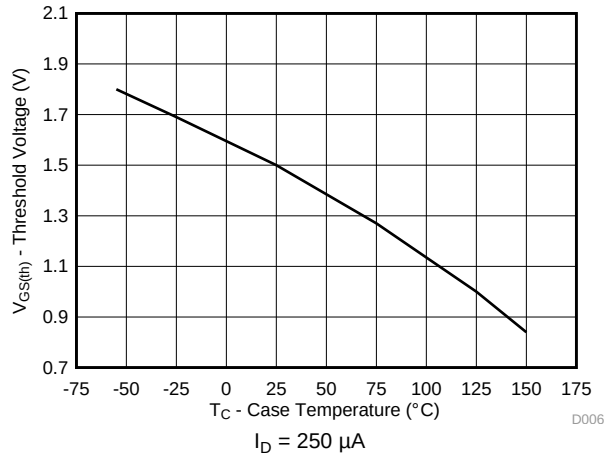


Figure 6. Threshold Voltage vs Temperature

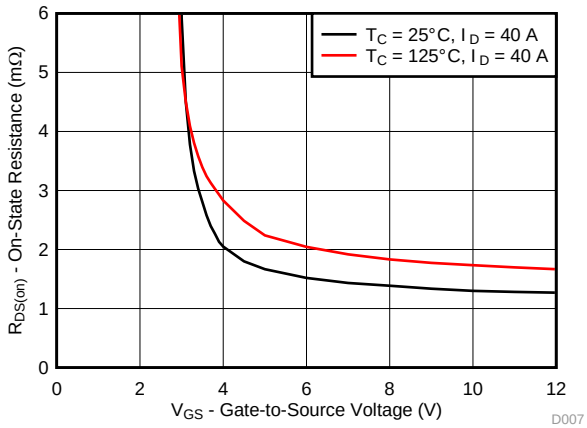
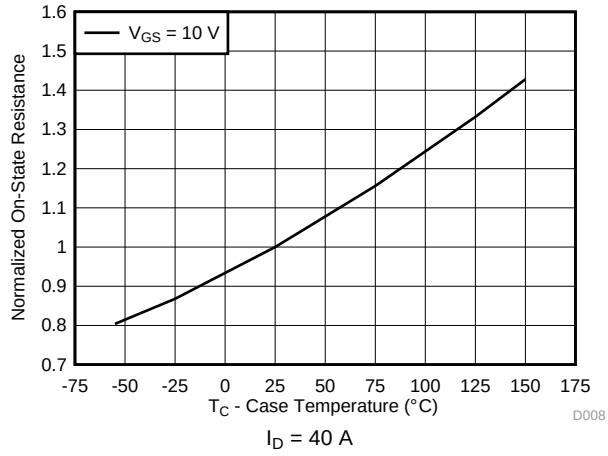


Figure 7. On-Resistance vs Gate Voltage

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise noted)



I_D = 40 A

Figure 8. On-Resistance vs Temperature

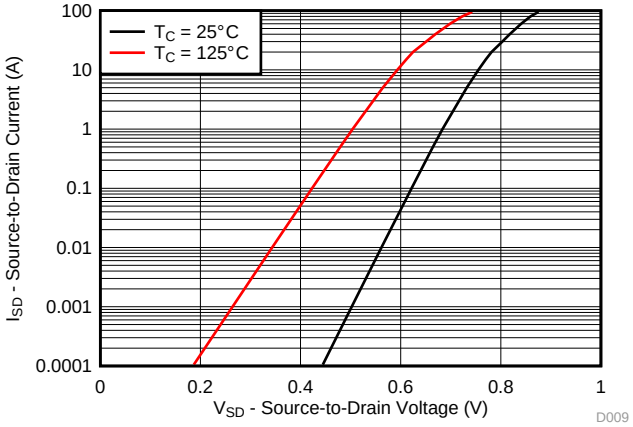
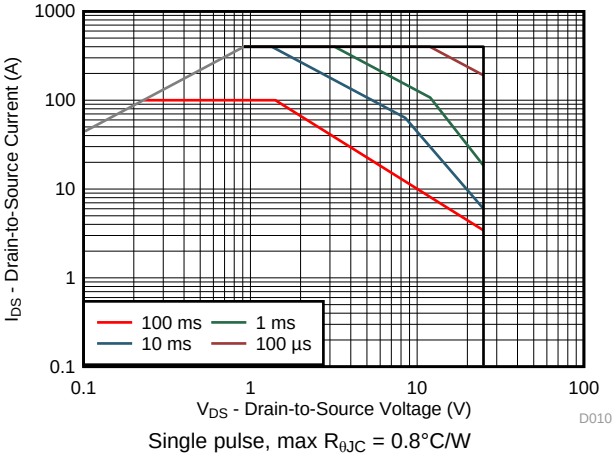


Figure 9. Typical Diode Forward Voltage



Single pulse, max $R_{\theta JC}$ = 0.8°C/W

Figure 10. Maximum Safe Operating Area

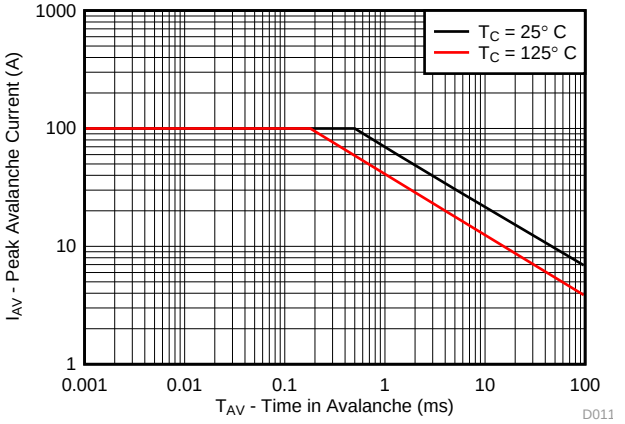


Figure 11. Single-Pulse Unclamped Inductive Switching

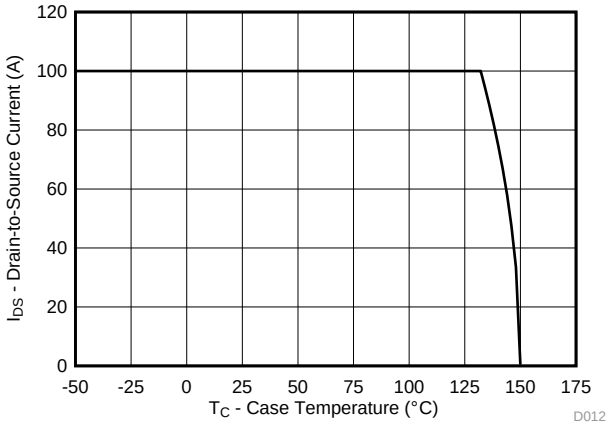


Figure 12. Maximum Drain Current vs Temperature

6 器件和文档支持

6.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

6.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** 此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

6.3 商标

NexFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

6.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.5 Glossary

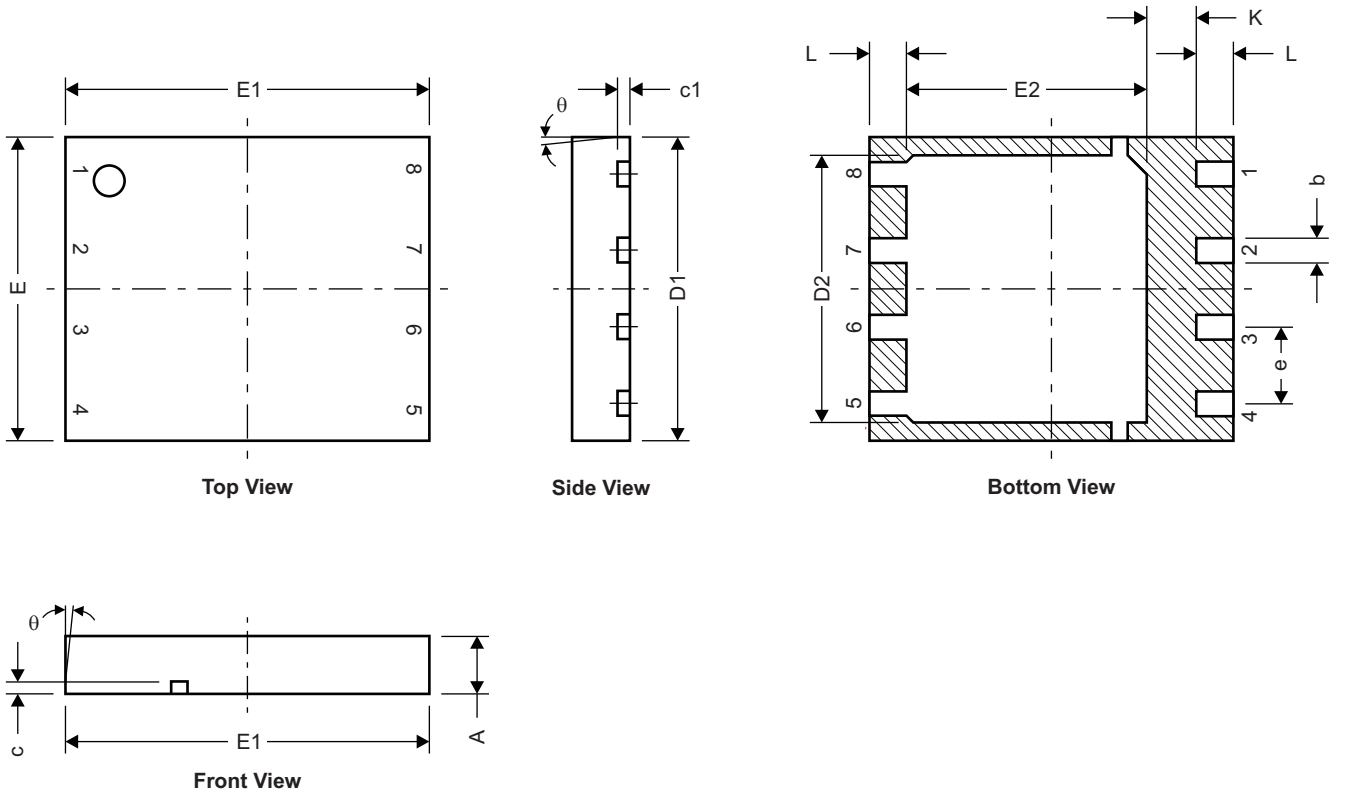
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

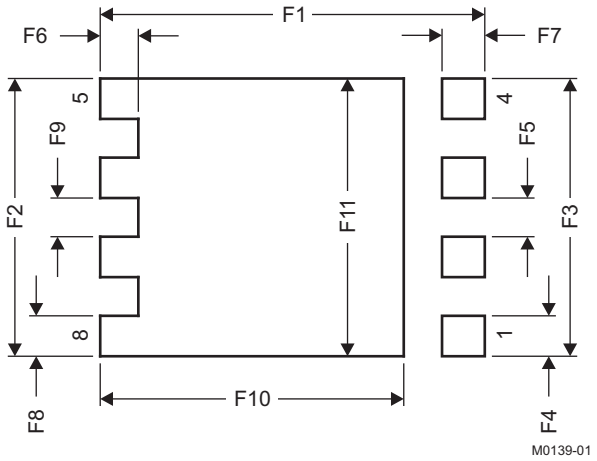
7.1 Q5 封装尺寸



M0140-01

DIM	毫米			英寸		
	最小值	典型值	最大值	最小值	典型值	最大值
A	0.950		1.050	0.037		0.039
b	0.360		0.460	0.014		0.018
c	0.150		0.250	0.006		0.010
c1	0.150		0.250	0.006		0.010
D1	4.900		5.100	0.193		0.201
D2	4.320		4.520	0.170		0.178
E	4.900		5.100	0.193		0.201
E1	5.900		6.100	0.232		0.240
E2	3.920		4.12	0.154		0.162
e		1.27			0.050	
K	0.760			0.030		
L	0.510		0.710	0.020		0.028
θ	0.00					

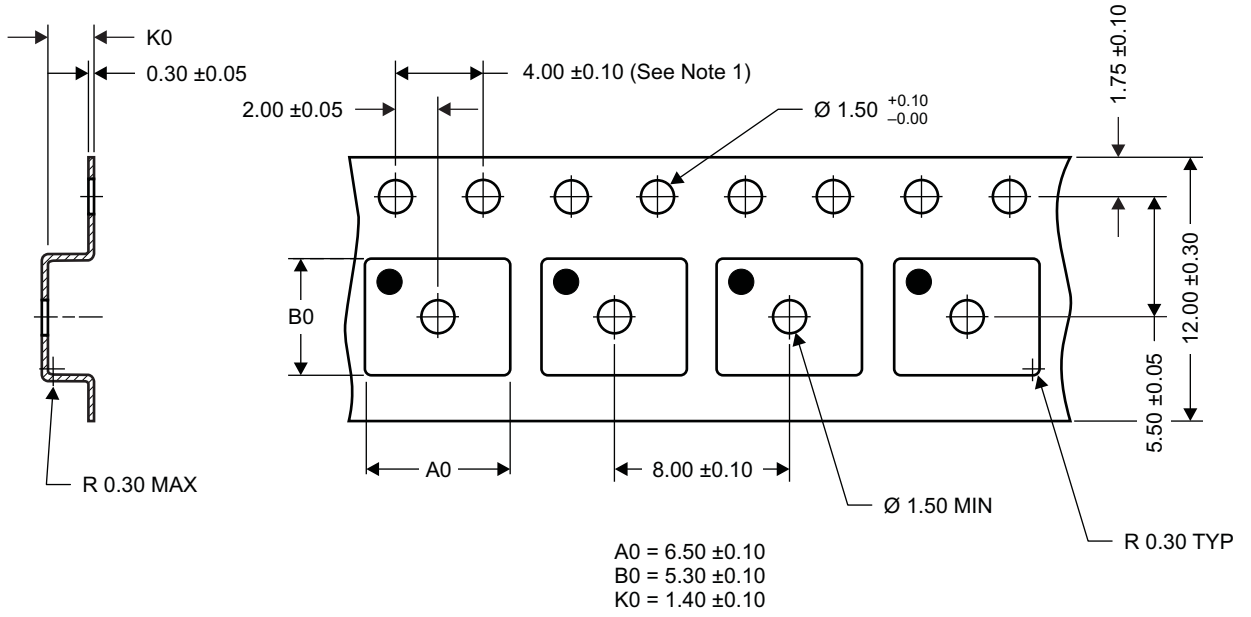
7.2 建议 PCB 布局



DIM	毫米		英寸	
	最小值	最大值	最小值	最大值
F1	6.205	6.305	0.244	0.248
F2	4.460	4.560	0.176	0.180
F3	4.460	4.560	0.176	0.180
F4	0.650	0.700	0.026	0.028
F5	0.620	0.670	0.024	0.026
F6	0.630	0.680	0.025	0.027
F7	0.700	0.800	0.028	0.031
F8	0.650	0.700	0.026	0.028
F9	0.620	0.670	0.024	0.026
F10	4.900	5.000	0.193	0.197
F11	4.460	4.560	0.176	0.180

如需了解针对 PCB 设计的建议电路布局，请参阅*《通过 PCB 布局技巧来减少振铃》*(SLPA005)。

7.3 Q5 卷带封装信息



注：

1. 10 个链齿孔间距的累积容差为 ±0.2。
2. 每 100mm 长度的翘曲不能超过 1mm，在 250mm 长度上不累积。
3. 材料：黑色抗静电聚苯乙烯。
4. 所有尺寸单位均为 mm（除非另外注明）。
5. 在高于卷带袋底部 0.3mm 的平面上测量得到 A0 和 B0 值。
6. 符合 MSL1 260°C（红外和对流）PbF 回流焊要求。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD16401Q5	ACTIVE	VSON-CLIP	DQH	8	2500	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD16401	Samples
CSD16401Q5T	ACTIVE	VSON-CLIP	DQH	8	250	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD16401	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

重要声明和免责声明

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