

SN74LVCC3245A 具有可调节输出电压和三态输出的八路总线收发器

1 特性

- 双向电压转换器
- A 端口的电压范围为 2.3V 至 3.6V，B 端口的电压范围为 3V 至 5.5V
- 控制输入 V_{IH} 和 V_{IL} 电平以 V_{CCA} 电压为基准
- 闩锁性能超过 250mA，符合 JESD 17 规范
- ESD 保护性能超过 JESD 22 规范要求
 - 2000V 人体放电模型 (A114-A)
 - 1000V 充电器件模型 (C101)

2 应用

- 电平转换
- USB 的连接
- 模拟和数字应用

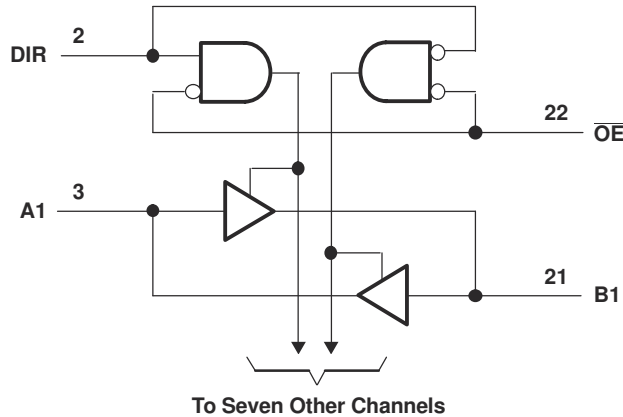
3 说明

SN74LVCC3245A 器件是一款包含两个独立电源轨的 8 位 (八路) 同相总线收发器。B 端口设计用于跟踪 V_{CCB} ，该端口可接受的电压范围为 3V 至 5.5V。A 端口设计用于跟踪 V_{CCA} ，其工作电压范围为 2.3V 至 3.6V。这样可实现从 3.3V 到 5V 的系统环境转换，反之亦然；以及从 2.5V 到 3.3V 的系统环境转换，反之亦然。

封装信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
SN74LVCC3245A	DB (SSOP, 24)	8.65mm × 3.90mm
	DW (SOIC, 24)	15.40mm × 7.50mm
	DBQ (SSOP, 24)	8.20mm × 5.30mm
	NS (SO, 24)	15.00mm × 5.30mm
	PW (TSSOP, 24)	7.80mm × 4.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



功能方框图



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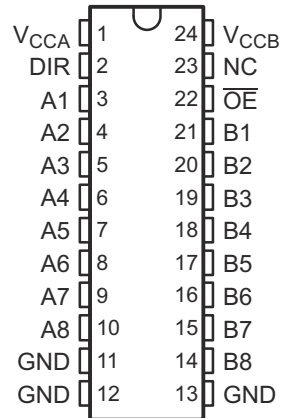
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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision P (December 2015) to Revision Q (December 2022)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• Added thermal information for DB and PW package.....	6
• Added inclusive terminology.....	15
Changes from Revision O (March 2005) to Revision P (December 2015)	Page
• 添加了应用部分、器件信息表、ESD 等级表、特性说明部分、器件功能模式、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分.....	1
• 删除了订购信息表.....	1

5 Pin Configuration and Functions



NC - No internal connection

See [# 12](#) for dimensions.

图 5-1. DB, DBQ, DW, NS, or PW Package, 24-Pin SSOP, SOIC, SO, or TSSOP (Top View)

表 5-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
A1	3	I/O	A1 port
A2	4	I/O	A2 port
A3	5	I/O	A3 port
A4	6	I/O	A4 port
A5	7	I/O	A5 port
A6	8	I/O	A6 port
A7	9	I/O	A7 port
A8	10	I/O	A8 port
B1	21	I/O	B1 port
B2	20	I/O	B2 port
B3	19	I/O	B3 port
B4	18	I/O	B4 port
B5	17	I/O	B5 port
B6	16	I/O	B6 port
B7	15	I/O	B7 port
B8	14	I/O	B8 port
DIR	2	I	Dir input
GND	11	—	Ground
	12		
	13		
NC	23	—	Unconnected
OE	22	I	Output Enable active low
V _{CCA}	1	—	A port power
V _{CCB}	24	—	B port power

(1) I = input, O = output, P = power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{CCA} V_{CCB}	Supply voltage	- 0.5	6	V
V_I	Input voltage	All A ports ⁽²⁾	$V_{CCA} + 0.5$	V
		All B ports ⁽³⁾	$V_{CCB} + 0.5$	
		Except I/O ports ⁽²⁾	$V_{CCA} + 0.5$	
V_O	Output voltage ⁽³⁾	All A ports	$V_{CCA} + 0.5$	V
		All B ports	$V_{CCB} + 0.5$	
I_{IK}	Input clamp current	$V_I < 0$	- 50	mA
I_{OK}	Output clamp current	$V_O < 0$	- 50	mA
I_O	Continuous output current		±50	mA
	Continuous current through V_{CCA} , V_{CCB} , or GND		±100	mA
T_J	Junction temperature		150	°C
$R_{\theta JA}$	Junction-to-ambient thermal resistance	DW	46	°C/W
		NS	65	
T_{stg}	Storage temperature	- 65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) This value is limited to 4.6 V maximum.
- (3) This value is limited to 6 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge		
	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000		

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		V_{CCA}	V_{CCB}	MIN	NOM	MAX	UNIT
V_{CCA}	Supply voltage			2.3	3.3	3.6	V
V_{CCB}	Supply voltage			3	5	5.5	V
V_{IHA}	High-level input voltage	2.3 V	3 V	1.7			V
		2.7 V	3 V	2			
		3 V	3.6 V	2			
		3.6 V	5.5 V	2			
V_{IHB}	High-level input voltage	2.3 V	3 V	2			V
		2.7 V	3 V	2			
		3 V	3.6 V	2			
		3.6 V	5.5 V	3.85			

6.3 Recommended Operating Conditions (continued)

		V _{CCA}	V _{CCB}	MIN	NOM	MAX	UNIT
V _{ILA}	Low-level input voltage	2.3 V	3 V			0.7	V
		2.7 V	3 V			0.8	
		3 V	3.6 V			0.8	
		3.6 V	5.5 V			0.8	
V _{ILB}	Low-level input voltage	2.3 V	3 V			0.8	V
		2.7 V	3 V			0.8	
		3 V	3.6 V			0.8	
		3.6 V	5.5 V			1.65	
V _{IH}	High-level input voltage (control terminals) (referenced to V _{CCA})	2.3 V	3 V	1.7			V
		2.7 V	3 V	2			
		3 V	3.6 V	2			
		3.6 V	5.5 V	2			
V _{IL}	Low-level input voltage (control terminals) (referenced to V _{CCA})	2.3 V	3 V			0.7	V
		2.7 V	3 V			0.8	
		3 V	3.6 V			0.8	
		3.6 V	5.5 V			0.8	
V _{IA}	Input voltage			0		V _{CCA}	V
V _{IB}	Input voltage			0		V _{CCB}	V
V _{OA}	Output voltage			0		V _{CCA}	V
V _{OB}	Output voltage			0		V _{CCB}	V
I _{OHA}	High-level output current	2.3 V	3 V			- 8	mA
		2.7 V	3 V			- 12	
		3 V	3 V			- 24	
		2.7 V	4.5 V			- 24	
I _{OHB}	High-level output current	2.3 V	3 V			- 12	mA
		2.7 V	3 V			- 12	
		3 V	3 V			- 24	
		2.7 V	4.5 V			- 24	
I _{OLA}	Low-level output current	2.3 V	3 V			8	mA
		2.7 V	3 V			12	
		3 V	3 V			24	
		2.7 V	4.5 V			24	
I _{OLB}	Low-level output current	2.3 V	3 V			12	mA
		2.7 V	3 V			12	
		3 V	3 V			24	
		2.7 V	4.5 V			24	
Δt/Δv	Input transition rise or fall rate					10	ns/V
T _A	Operating free-air temperature			- 40		85	°C

6.4 Thermal Information

THERMAL METRIC ^{(1) (4)}		SN74LVCC3245A			UNIT
		DB (SSOP)	DBQ (SSOP)	PW (TSSOP)	
		24 PINS	24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	90.7	61	100.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.9	44.8	44.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.7	34.5	55.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.8	9.5	6.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	49.3	37.2	55.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP	MAX	UNIT
V_{OHA}	$I_{OH} = -100 \mu A$	3 V	3 V	2.9	3		V
	$I_{OH} = -8 mA$	2.3 V	3 V	2			
	$I_{OH} = -12 mA$	2.7 V	3 V	2.2	2.5		
		3 V	3 V	2.4	2.8		
	$I_{OH} = -24 mA$	3 V	3 V	2.2	2.6		
2.7 V		4.5 V	2	2.3			
V_{OHB}	$I_{OH} = -100 \mu A$	3 V	3 V	2.9	3		V
	$I_{OH} = -12 mA$	2.3 V	3 V	2.4			
		2.7 V	3 V	2.4	2.8		
	$I_{OH} = -24 mA$	3 V	3 V	2.2	2.6		
2.7 V		4.5 V	3.2	4.2			
V_{OLA}	$I_{OL} = 100 \mu A$	3 V	3 V			0.1	V
	$I_{OL} = 8 mA$	2.3 V	3 V			0.6	
	$I_{OL} = 12 mA$	2.7 V	3 V		0.1	0.5	
		3 V	3 V		0.2	0.5	
V_{OLB}	$I_{OL} = 100 \mu A$	3 V	3 V			0.1	V
	$I_{OL} = 12 mA$	2.3 V	3 V			0.4	
		3 V	3 V		0.2	0.5	
	$I_{OL} = 24 mA$	2.7 V	4.5 V		0.2	0.5	
I_I	Control inputs	$V_I = V_{CCA}$ or GND	3.6 V	3.6 V	± 0.1	± 1	μA
			5.5 V		± 0.1	± 1	
I_{OZ} ⁽¹⁾	A or B ports	$V_O = V_{CCA/B}$ or GND, $V_I = V_{IL}$ or V_{IH}	3.6 V	3.6 V	± 0.5	± 5	μA
I_{CCA}	B to A	A port = V_{CCA} or GND, $I_O = 0$	3.6 V	Open	5	50	μA
		B port = V_{CCB} or GND, $I_O = 0$	3.6 V	3.6 V	5	50	
I_{CCB}	A to B		A port = V_{CCA} or GND, $I_O = 0$	3.6 V	3.6 V	5	50
		5.5 V			8	80	

6.5 Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CCA}	V _{CCB}	MIN	TYP	MAX	UNIT
ΔI_{CCA} (2)	A port	V _I = V _{CCA} - 0.6 V, Other inputs at V _{CCA} or GND, \overline{OE} at GND and DIR at V _{CCA}	3.6 V	3.6 V		0.35	0.5	mA
	\overline{OE}	V _I = V _{CCA} - 0.6 V, Other inputs at V _{CCA} or GND, DIR at V _{CCA}	3.6 V	3.6 V		0.35	0.5	
	DIR	V _I = V _{CCA} - 0.6 V, Other inputs at V _{CCA} or GND, \overline{OE} at GND	3.6 V	3.6 V		0.35	0.5	
ΔI_{CCB} (2)	B port	V _I = V _{CCB} - 2.1 V, Other inputs at V _{CCB} or GND, \overline{OE} at GND and DIR at GND	3.6 V	5.5 V		1	1.5	mA
C _i	Control inputs	V _I = V _{CCA} or GND	Open	Open		4		pF
C _{io}	A or B ports	V _O = V _{CCA/B} or GND	3.3 V	5 V		18.5		pF

(1) For I/O ports, the parameter I_{OZ} includes the input leakage current.

(2) This is the increase in supply current for each input that is at one of the specified voltage levels, rather than 0 V or the associated V_{CC}.

6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see 图 7-1 through 图 7-4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CCA} , V _{CCB}	MIN	MAX	UNIT
t _{PHL}	A	B	V _{CCA} = 2.5 V ± 0.2 V, V _{CCB} = 3.3 V ± 0.3 V	1	9.4	ns
			V _{CCA} = 2.7 V TO 3.6 V, V _{CCB} = 5 V ± 0.5 V	1	6	
			V _{CCA} = 2.7 V TO 3.6 V, V _{CCB} = 3.3 V ± 0.3 V	1	7.1	
t _{PLH}	A	B	V _{CCA} = 2.5 V ± 0.2 V, V _{CCB} = 3.3 V ± 0.3 V	1	9.1	ns
			V _{CCA} = 2.7 V TO 3.6 V, V _{CCB} = 5 V ± 0.5 V	1	5.3	
			V _{CCA} = 2.7 V TO 3.6 V, V _{CCB} = 3.3 V ± 0.3 V	1	7.2	
t _{PHL}	B	A	V _{CCA} = 2.5 V ± 0.2 V, V _{CCB} = 3.3 V ± 0.3 V	1	11.2	ns
			V _{CCA} = 2.7 V TO 3.6 V, V _{CCB} = 5 V ± 0.5 V	1	5.8	
			V _{CCA} = 2.7 V TO 3.6 V, V _{CCB} = 3.3 V ± 0.3 V	1	6.4	
t _{PLH}	B	A	V _{CCA} = 2.5 V ± 0.2 V, V _{CCB} = 3.3 V ± 0.3 V	1	9.9	ns
			V _{CCA} = 2.7 V TO 3.6 V, V _{CCB} = 5 V ± 0.5 V	1	7	
			V _{CCA} = 2.7 V TO 3.6 V, V _{CCB} = 3.3 V ± 0.3 V	1	7.6	
t _{PZL}	\overline{OE}	A	V _{CCA} = 2.5 V ± 0.2 V, V _{CCB} = 3.3 V ± 0.3 V	1	14.5	ns
			V _{CCA} = 2.7 V TO 3.6 V, V _{CCB} = 5 V ± 0.5 V	1	9.2	
			V _{CCA} = 2.7 V TO 3.6 V, V _{CCB} = 3.3 V ± 0.3 V	1	9.7	

6.6 Switching Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted) (see 图 7-1 through 图 7-4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCA}, V_{CCB}	MIN	MAX	UNIT
t_{PZH}	\overline{OE}	A	$V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}, V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1	12.9	ns
			$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}, V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$	1	9.5	
			$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}, V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1	9.5	
t_{PZL}	\overline{OE}	B	$V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}, V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1	13	ns
			$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}, V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$	1	8.1	
			$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}, V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1	9.2	
t_{PZH}	\overline{OE}	B	$V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}, V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1	12.8	ns
			$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}, V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$	1	8.4	
			$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}, V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1	9.9	
t_{PLZ}	\overline{OE}	A	$V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}, V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1	7.1	ns
			$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}, V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$	1	7	
			$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}, V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1	6.6	
t_{PHZ}	\overline{OE}	A	$V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}, V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1	7.3	ns
			$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}, V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$	1	7.8	
			$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}, V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1	6.9	
t_{PLZ}	\overline{OE}	B	$V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}, V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1	8.8	ns
			$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}, V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$	1	7.3	
			$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}, V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1	7.5	
t_{PHZ}	\overline{OE}	B	$V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}, V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1	8.9	ns
			$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}, V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$	1	7	
			$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}, V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1	7.9	

6.7 Operating Characteristics

$V_{CCA} = 3.3\text{ V}, V_{CCB} = 5\text{ V}, T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	38	pF
		Outputs disabled	4.5	

6.8 Typical Characteristics

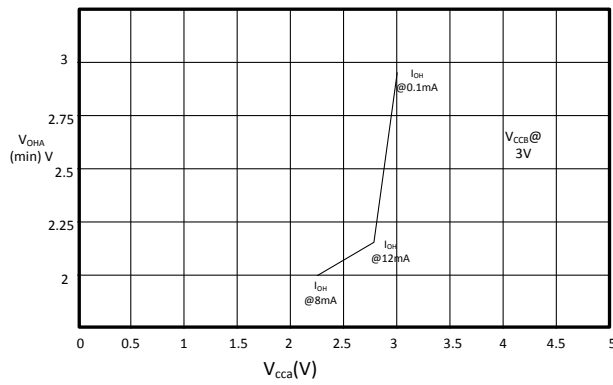
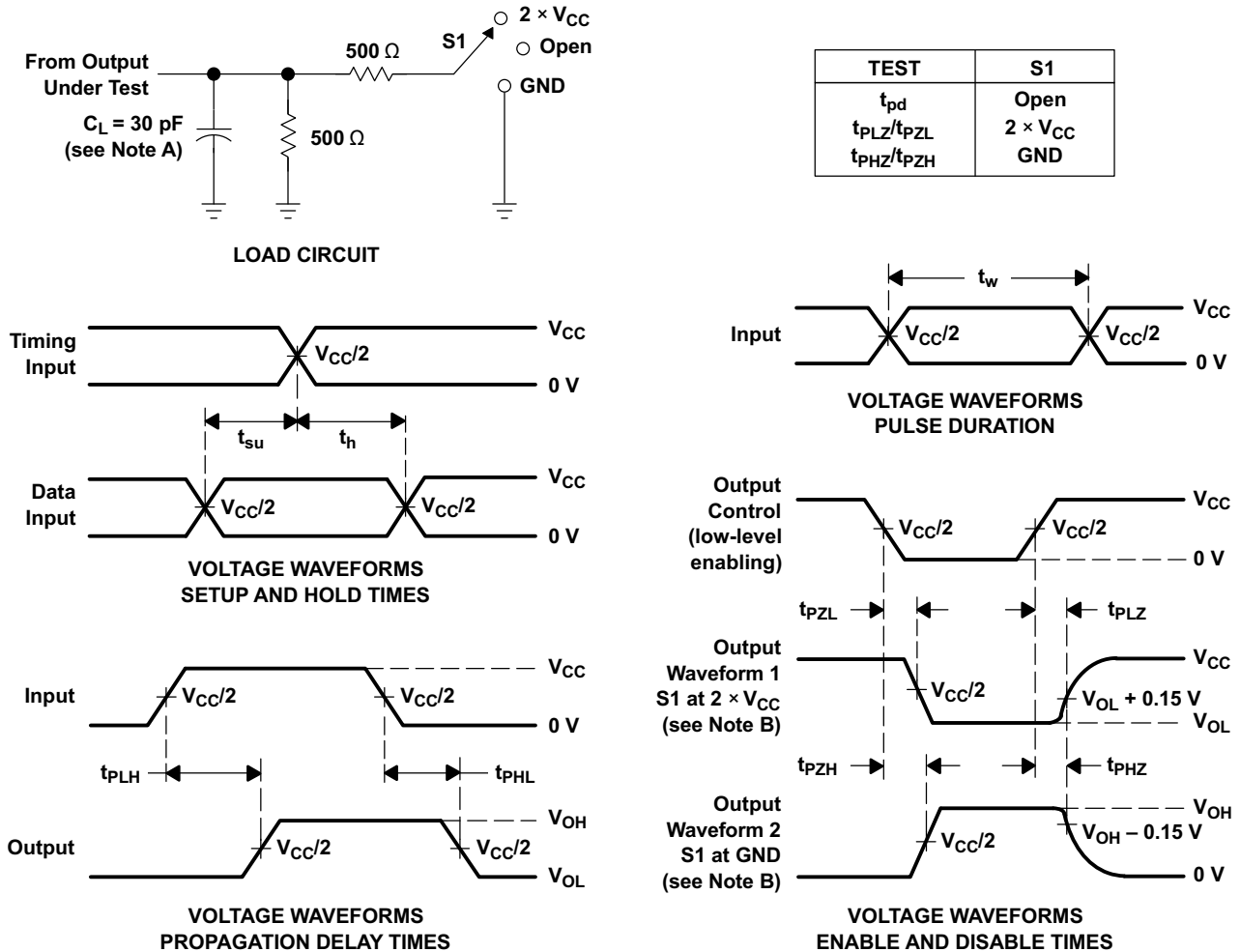


图 6-1. $V_{OHA}(\min)$ VS V_{CCA}

7 Parameter Measurement Information

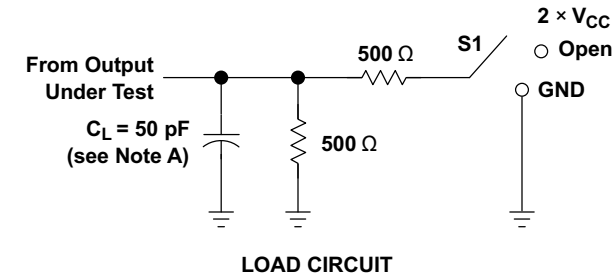
7.1 A Port ($V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$ and $V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$)



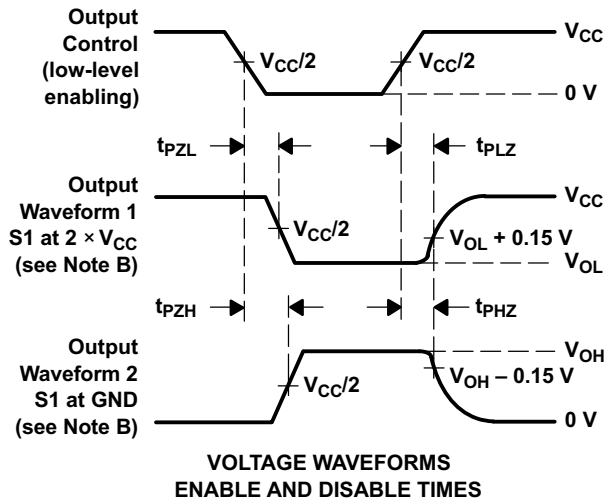
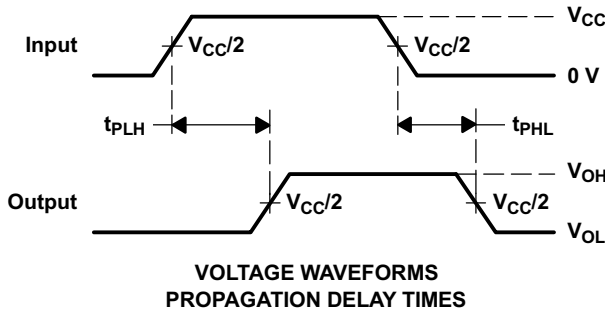
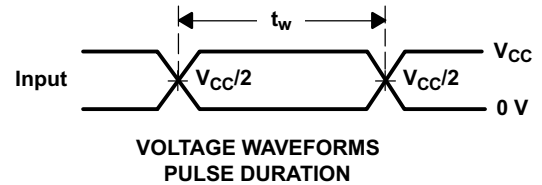
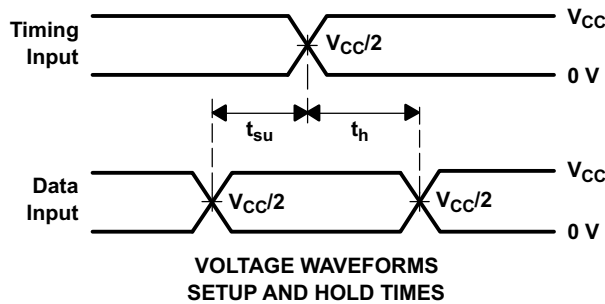
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

图 7-1. Load Circuit and Voltage Waveforms

7.2 B Port ($V_{CCA} = 2.5 V \pm 0.2 V$ and $V_{CCB} = 3.3 V \pm 0.3 V$)



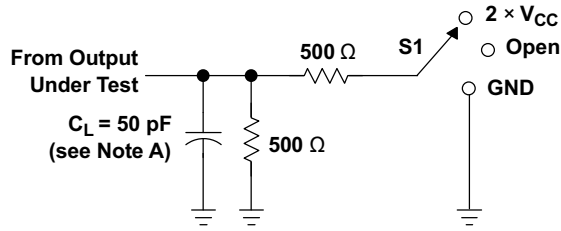
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

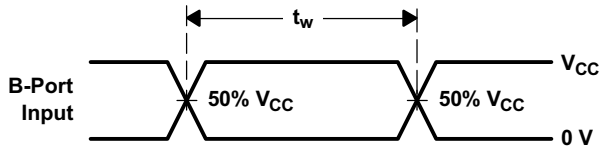
图 7-2. Load Circuit and Voltage Waveforms

7.3 B Port ($V_{CCA} = 3.6\text{ V}$ and $V_{CCB} = 5.5\text{ V}$)

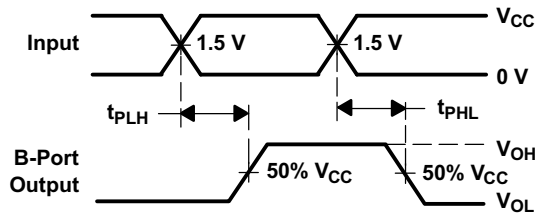


LOAD CIRCUIT

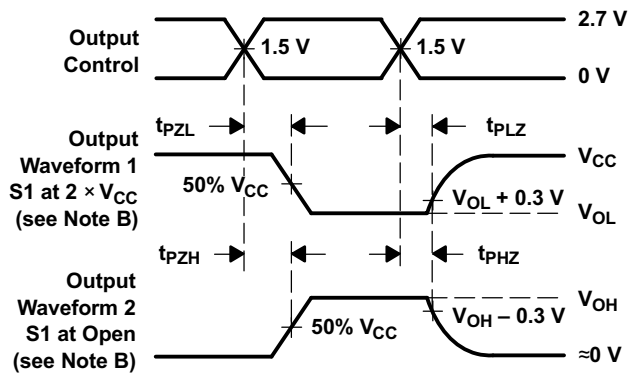
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	Open



**VOLTAGE WAVEFORMS
PULSE DURATION**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS**

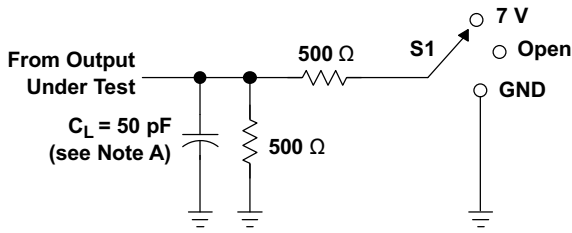


**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

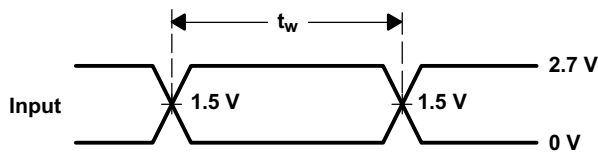
图 7-3. Load Circuit and Voltage Waveforms

7.4 A and B Port (V_{CCA} and $V_{CCB} = 3.6\text{ V}$)

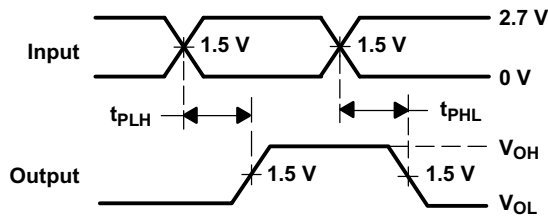


LOAD CIRCUIT

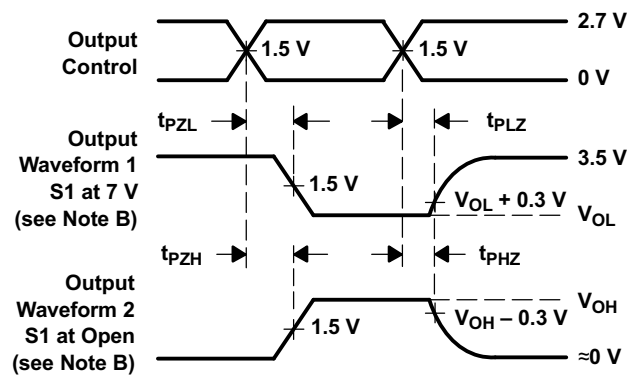
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

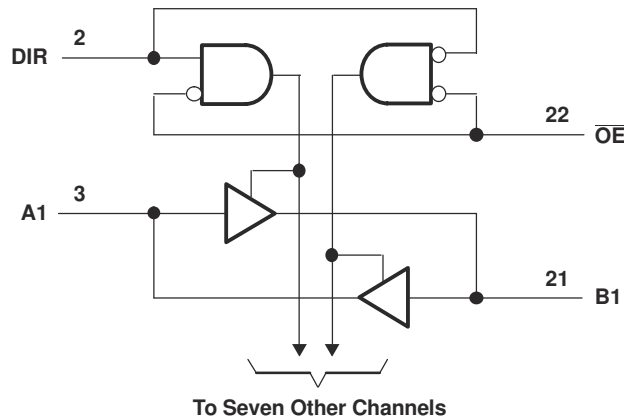
图 7-4. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74LVCC3245A device is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so the buses are effectively isolated. The control circuitry (DIR, \overline{OE}) is powered by V_{CCA} .

8.2 Functional Block Diagram



8.3 Feature Description

This device is a bidirectional level translator designed to operate from 2.3 V to 3.6 V on Port A and 3 V to 5.5 V on B port. The control inputs recommended operating specifications are referenced with respect to V_{CCA} Voltage.

8.4 Device Functional Modes

表 8-1 lists the functional modes of the SN74LVCC3245A.

表 8-1. Function Table (Each Transceiver)

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The SN74LVCC3245A device is a bidirectional level translator designed to operate from 2.3 V to 3.6 V on Port A and 3 V to 5.5 V on B port and designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input.

9.2 Typical Application

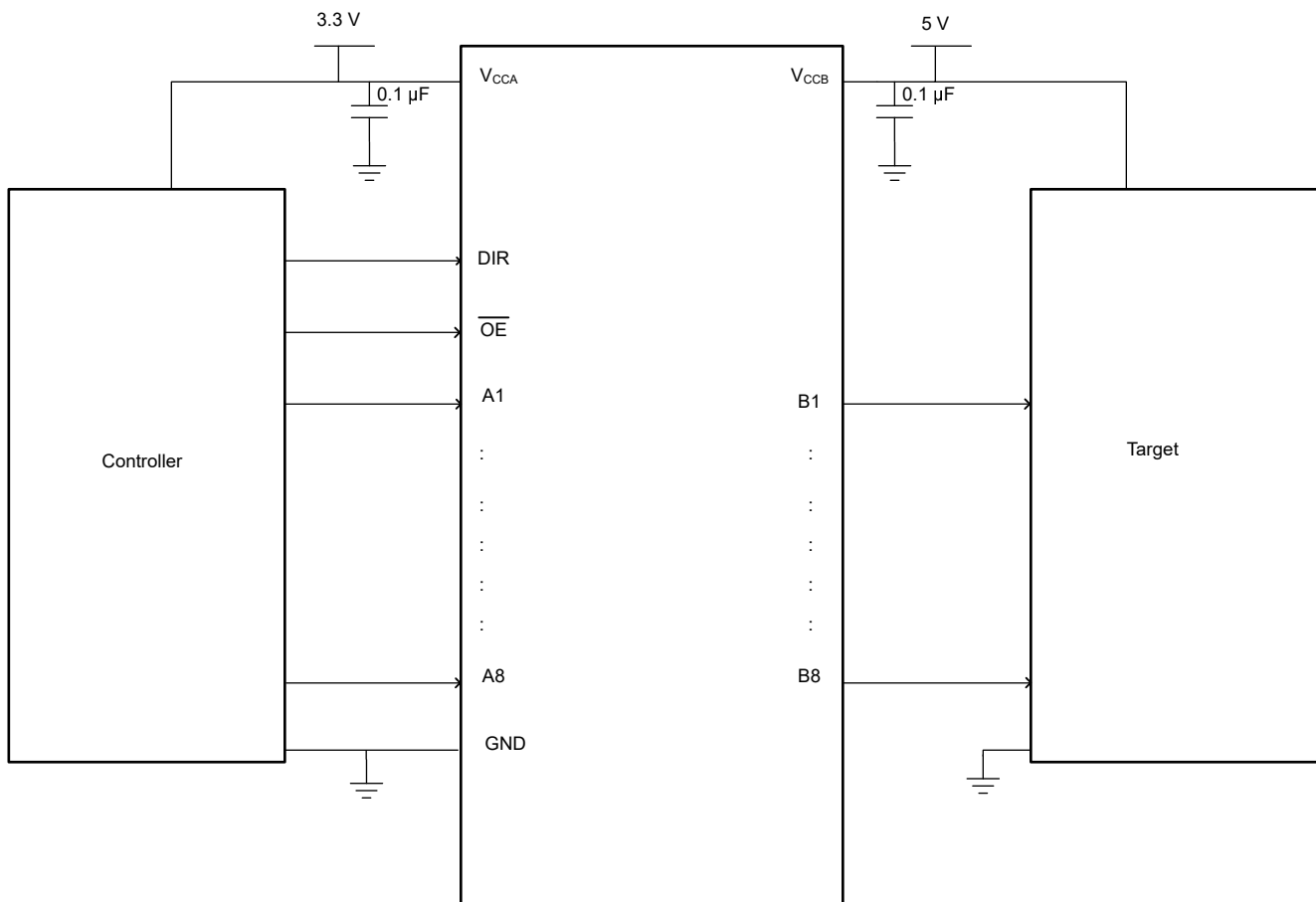


图 9-1. Typical Application

9.2.1 Design Requirements

This device can be used as bidirectional level translator depending on the DIR pin. The application describes the level translation of controller with signals at 3.3 V to target operating at 5 V. The OE pin is low and DIR pin is 3.3-V high.

9.2.2 Detailed Design Procedure

Use the procedure that follows for the design:

- Recommended Input Conditions
 - Rise time and fall time specs. See ($\Delta t / \Delta V$) in the [Recommended Operating Conditions](#) table.
 - Specified high and low levels. See (V_{IH} and V_{IL}) in the [Recommended Operating Conditions](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as (V_I max) in the [Recommended Operating Conditions](#) table at any valid V_{CC} .
- Absolute Maximum Output Conditions
 - Load currents should not exceed (I_O max) per output and should not exceed total current (continuous current through V_{CC} or GND) for the part. These limits are located in the [Absolute Maximum Ratings](#) table.
 - All the voltages on A and B ports should not exceed above V_{CCA} or V_{CCB} to prevent the biasing of Electrostatic discharge (ESD) diodes.

9.2.3 Application Curve

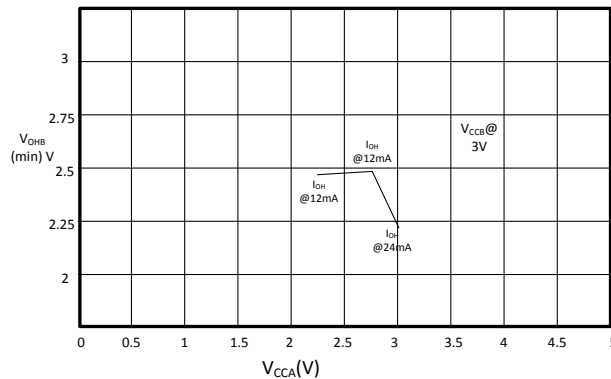


图 9-2. $V_{OHB}(\min)$ vs V_{CCA}

9 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- μ F capacitor is recommended and if there are multiple V_{CC} pins then 0.01- μ F or 0.022- μ F capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

10 Layout

10.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient.

10.2 Layout Example

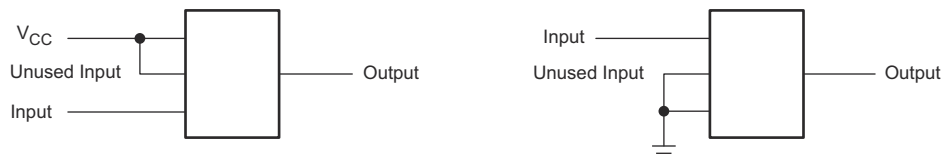


图 10-1. Layout Example

10.3 Power-Up Considerations

TI level-translation devices offer an opportunity for successful mixed-voltage signal design. A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device terminals. To guard against such power-up problems, take these precautions:

1. Connect ground before any supply voltage is applied.
2. Power up the control side of the device (V_{CCA} for all four of these devices).
3. Tie \overline{OE} to V_{CCA} with a pullup resistor so that it ramps with V_{CCA} .
4. Depending on the direction of the data path, DIR can be high or low. If DIR high is needed (A data to B bus), ramp it with V_{CCA} . Otherwise, keep DIR low.

For more information, refer to [Voltage-Level-Translation Devices](#) application note.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Implications of Slow or Floating CMOS Inputs](#)
- Texas Instruments, [Voltage-Level-Translation Devices](#)

11.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 支持资源

TI E2E™ [支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVCC3245ADBQR	ACTIVE	SSOP	DBQ	24	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVCC3245A	Samples
SN74LVCC3245ADBR	ACTIVE	SSOP	DB	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	Samples
SN74LVCC3245ADBRE4	ACTIVE	SSOP	DB	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	Samples
SN74LVCC3245ADBRG4	ACTIVE	SSOP	DB	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	Samples
SN74LVCC3245ADW	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A	Samples
SN74LVCC3245ADWE4	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A	Samples
SN74LVCC3245ADWG4	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A	Samples
SN74LVCC3245ADWR	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	LVCC3245A	Samples
SN74LVCC3245ADWRG4	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A	Samples
SN74LVCC3245ANSR	ACTIVE	SO	NS	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A	Samples
SN74LVCC3245APW	ACTIVE	TSSOP	PW	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	Samples
SN74LVCC3245APWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	Samples
SN74LVCC3245APWRE4	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	Samples
SN74LVCC3245APWRG4	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	Samples
SN74LVCC3245APWT	ACTIVE	TSSOP	PW	24	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	Samples
SN74LVCC3245APWTG4	ACTIVE	TSSOP	PW	24	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVCC3245A :

- Enhanced Product : [SN74LVCC3245A-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVCC3245ADBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVCC3245ADBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
SN74LVCC3245ADWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74LVCC3245ADWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74LVCC3245ADWRG4	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74LVCC3245ANSR	SO	NS	24	2000	330.0	24.4	8.3	15.4	2.6	12.0	24.0	Q1
SN74LVCC3245APWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
SN74LVCC3245APWT	TSSOP	PW	24	250	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVCC3245ADBQR	SSOP	DBQ	24	2500	356.0	356.0	35.0
SN74LVCC3245ADBR	SSOP	DB	24	2000	356.0	356.0	35.0
SN74LVCC3245ADWR	SOIC	DW	24	2000	364.0	364.0	27.0
SN74LVCC3245ADWR	SOIC	DW	24	2000	350.0	350.0	43.0
SN74LVCC3245ADWRG4	SOIC	DW	24	2000	350.0	350.0	43.0
SN74LVCC3245ANSR	SO	NS	24	2000	367.0	367.0	45.0
SN74LVCC3245APWR	TSSOP	PW	24	2000	356.0	356.0	35.0
SN74LVCC3245APWT	TSSOP	PW	24	250	356.0	356.0	35.0

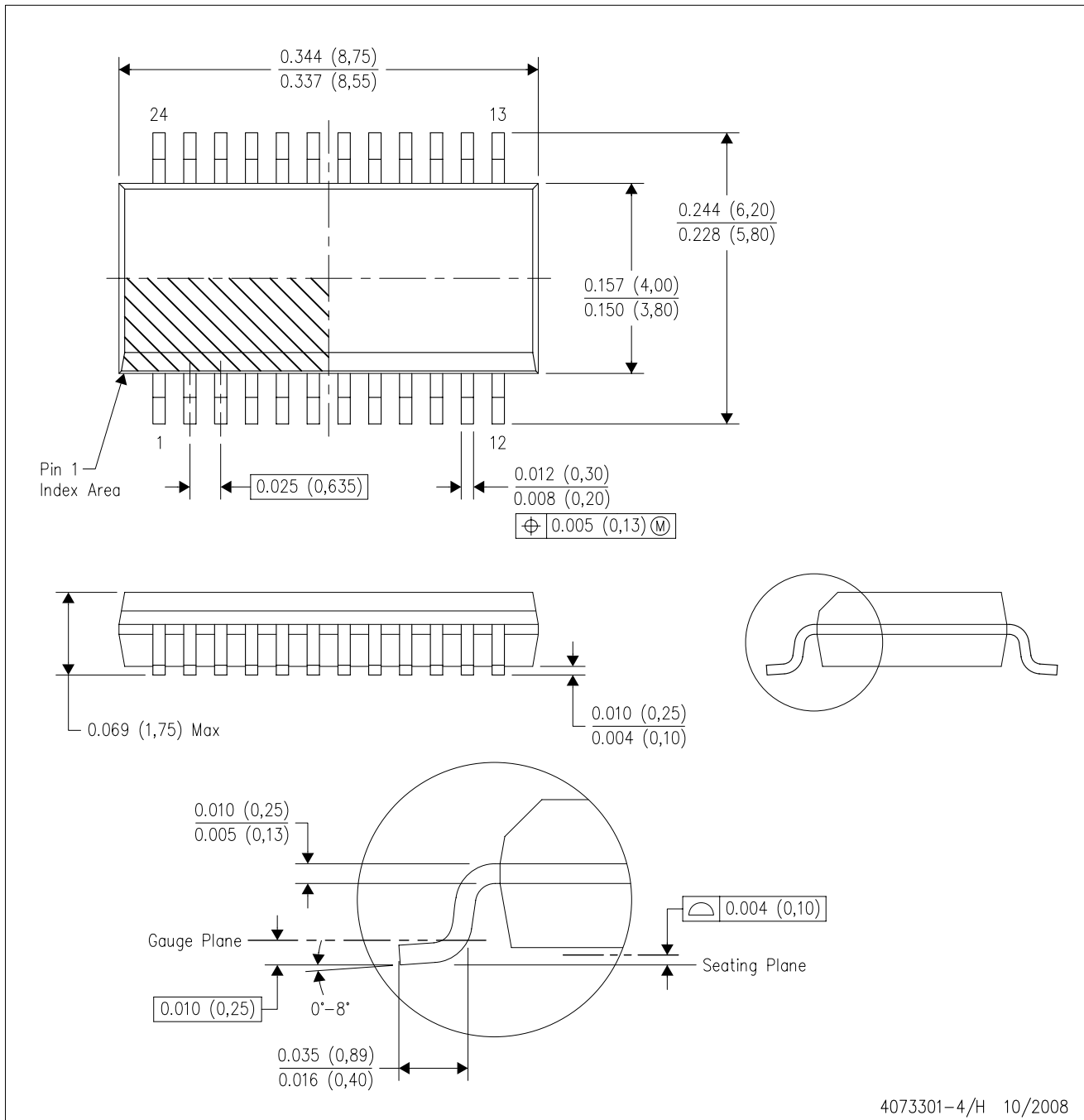
TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LVCC3245ADW	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74LVCC3245ADWE4	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74LVCC3245ADWG4	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74LVCC3245APW	PW	TSSOP	24	60	530	10.2	3600	3.5

DBQ (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
 - D. Falls within JEDEC MO-137 variation AE.

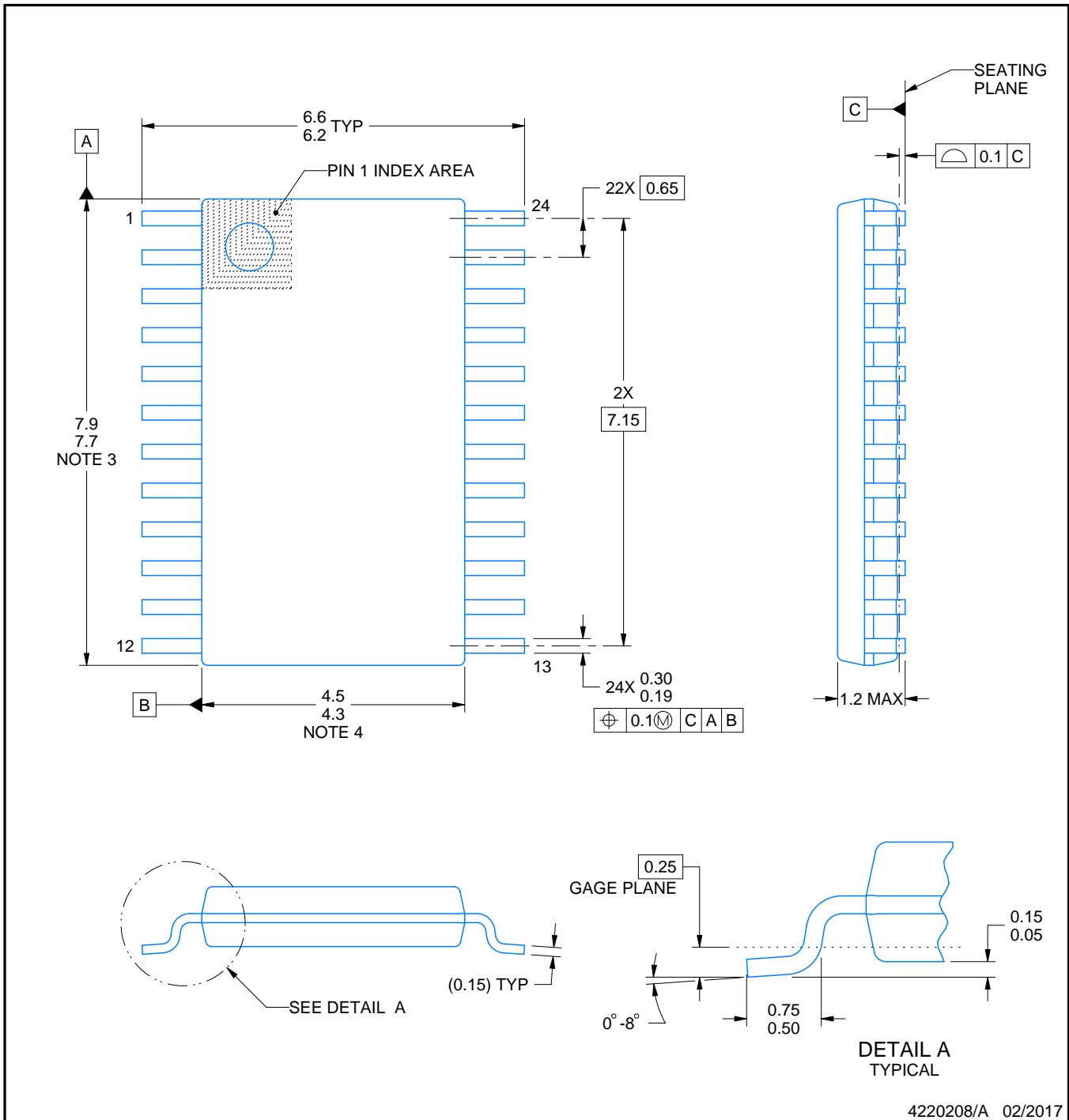
PW0024A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220208/A 02/2017

NOTES:

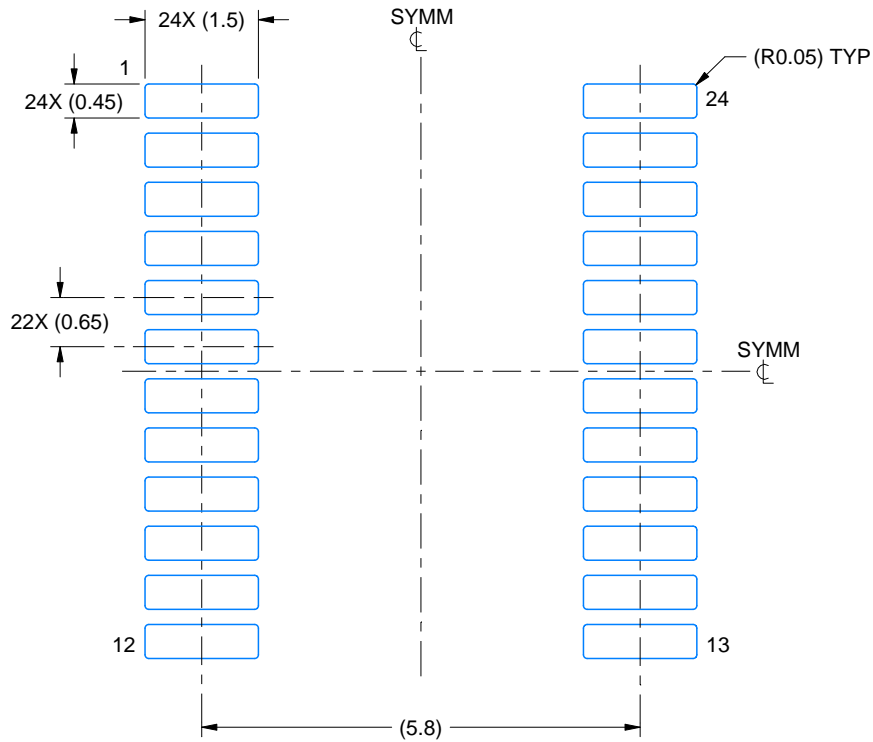
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

DW (R-PDSO-G24)

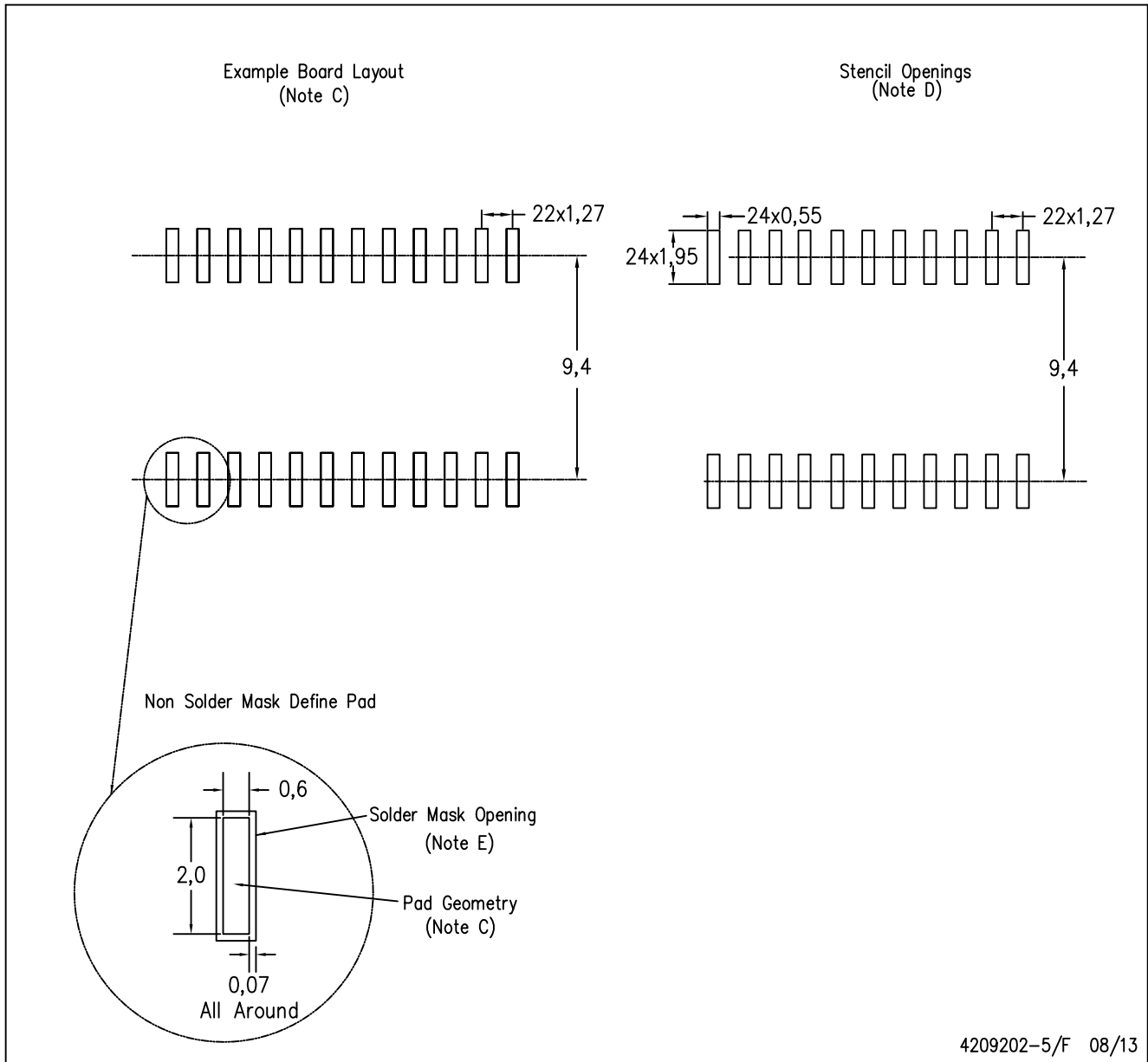
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



4209202-5/F 08/13

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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