1-Bit, 10MHz, 2nd-Order, Isolated Delta-Sigma Modulator

Check for Samples: AMC1203

FEATURES

- **16-Bit Resolution**
- **SNR: 80.5dB min**
- **THD: –88dB max (AMC1203B)**
- **±280mV Input Range with +5V Supply**
- **Internal 2.5V Reference Voltage: 1% Accuracy**
- **Gain Error: ±1% (AMC1203B)**
- **UL1577, IEC60747-5-2 (VDE0884, Rev. 2), and IEC61010-1 Approved**
  - **Isolation: 4000V_{PEAK}, Working Voltage: 560V**
  - **Transient Immunity: 15kV/µs**
- **Typical 25-Year Life at Rated Working Voltage (see Application Report SLLA197)**
- **Specified Temperature Range: –40°C to +105°C**

APPLICATIONS

- **Shunt Based Current Sensing in:**
  - **Motor Control**
  - **Uninterruptible Power Supplies**
  - **Power Inverters**
  - **Industrial Process Control**

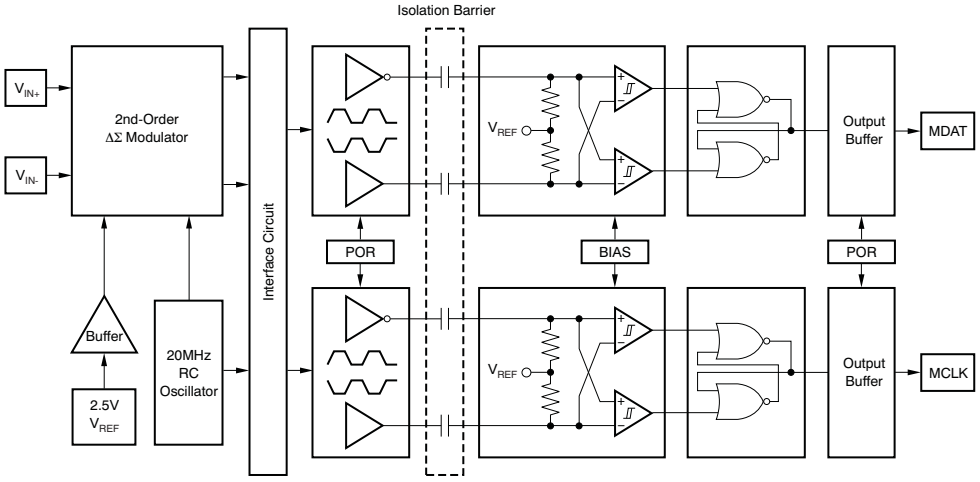
DESCRIPTION

The AMC1203 is a 1-bit, 10MHz, isolated delta-sigma (ΔΣ) modulator with an output buffer separated from the input interface circuitry by a silicon dioxide (SiO_2) isolation barrier. This barrier provides galvanic isolation of up to 4000V_{PEAK}. Used in conjunction with isolated power supplies, these devices prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry.

The AMC1203 modulator operates from a +5V supply with a dynamic range of 95dB. The differential inputs are ideal for direct connection to shunt resistors or other low-level signal sources. With the appropriate digital filter and modulator rate, the device can be used to achieve 16-bit analog-to-digital (A/D) conversion with no missing codes. An effective resolution of 14 bits and an SNR of 85dB (typical) can be maintained with a $sinc^3$ filter with a decimation ratio of 256.

The modulator output is translated to a balanced signal and then transferred by the capacitive isolation barrier. Across the isolation barrier, a differential comparator receives the logic transition information, and then sets or resets a flip-flop and the output circuit accordingly.

The AMC1203 is available in SOP-8 gull-wing, SOP-8, and SOIC-16 packages. The AMC1203 is characterized for operation over the ambient temperature range of –40°C to +105°C.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
AMC1203	SOP-8 Gull-Wing	DUB	–40°C to +105°C	AMC1203	AMC1203DUB	Tube, 50
					AMC1203DUBR	Tape and Reel, 350
	SOP-8	PSA	–40°C to +105°C	1203	AMC1203PSA	Tube, 95
					AMC1203PSAR	Tape and Reel, 2000
	SOIC-16	DW	–40°C to +105°C	AMC1203	AMC1203DW	Tube, 40
					AMC1203DWR	Tape ad Reel, 2000
AMC1203B	SOP-8 Gull-Wing	DUB	–40°C to +105°C	AMC1203	AMC1203BDUB	Tube, 50
					AMC1203BDUBR	Tape and Reel, 350
	SOP-8	PSA	–40°C to +105°C	1203	AMC1203BPSA	Tube, 95
					AMC1203BPSAR	Tape and Reel, 2000
	SOIC-16	DW	–40°C to +105°C	AMC1203	AMC1203BDW	Tube, 40
					AMC1203BDWR	Tape and Reel, 2000

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

PARAMETER		AMC1203	UNIT
Supply voltage, V_{DD1} to GND1 or V_{DD2} to GND2		–0.3 to +6	V
Analog input voltage at V_{IN+}, $V_{IN–}$		GND1 – 0.3 to V_{DD1} + 0.3	V
Input current to any pin except supply pins		±10	mA
Continuous total power dissipation		See Dissipation Ratings Table	
Maximum junction temperature, T_J		+150	°C
Electrostatic discharge (ESD), all pins	Human body model (HBM) JEDEC standard 22, test method A114-C.01	±3000	V
	Charged device Model (CDM) JEDEC standard 22, test method C101	±1500	V
	Machine Model (MM) JEDEC standard 22, test method A115A	±200	V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS(1)

Over recommended operating conditions, unless otherwise noted.

PARAMETER			SOP-8 GULL-WING	SOP-8	SOIC-16	UNIT
θ_{JA}	Junction-to-air thermal resistance	Low-K	127	246	104	°C/W
		High-K	78	164	58	°C/W
θ_{JC}	Junction-to-case thermal resistance		61	32	25	°C/W
P_D	Device power dissipation (max)		110	110	110	mW

(1) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range, unless otherwise noted.

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD1} to GND1 or V_{DD2} to GND2	4.5	5.0	5.5	V
Common-mode operating range, V_{CM}	0		V_{DD1}	V
Differential input voltage, $(V_{IN+}) – (V_{IN–})$	–280		280	mV
Operating junction temperature range, T_J (see the Thermal Characteristics table)	–40		+125	°C

DISSIPATION RATINGS(1)

PACKAGE	DERATING FACTOR ABOVE T_A = +25°C	$T_A \le$ +25°C POWER RATING	T_A = +70°C POWER RATING	T_A = +85°C POWER RATING	T_A = +125°C POWER RATING
SOP-8 Gull-Wing	7.9mW/°C	984mW	629mW	511mW	354mW
SOP-8	4.1mW/°C	508mW	325mW	264mW	182mW
SOIC-16	9.6mW/°C	1201mW	769mW	625mW	432mW

(1) Based on Low-K thermal resistance.

REGULATORY INFORMATION

VDE	UL
Certified according to IEC 60747-5-2	Recognized under 1577 Component Recognition Program
File Number: 40014131	File Number: E181974

IEC 60747-5-2 ISOLATION CHARACTERISTICS

Over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	VALUE	UNIT
V_{IORM}	Maximum working insulation voltage		560	V
V_{PD}	Input to output test voltage	Method A, after input or safety test (subgroup 2 or 3), $V_{PD} = V_{IORM} \times 1.2$, t = 10s, partial discharge < 5pC	672	V
		Method A, after environmental test (subgroup 1), $V_{PD} = V_{IORM} \times 1.6$, t = 10s, partial discharge < 5pC	896	V
		Method B1, routine and initial test, $V_{PD} = V_{IORM} \times 1.875$, 100% production test with t = 1s, partial discharge < 5pC	1050	V
V_{IOTM}	Transient overvoltage	t = 60s	4000	V
R_S	Isolation resistance	V_{IO} = 500V at T_S	$> 10^9$	Ω
PD	Pollution degree		2	

PACKAGE CHARACTERISTICS(1)

Over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (clearance)	Shortest terminal to terminal distance through air	DUB	7			mm
			DW	8			mm
			PSA	6.3			mm
L(I02)	Minimum external tracking (creepage)	Shortest terminal to terminal distance across the package surface	DUB	7			mm
			DW	8			mm
			PSA	6.3			mm
CTI	Tracking resistance (comparative tracking index)	DIN IEC 60112 / VDE 0303 Part 1		≥ 175			V
	Minimum internal gap (internal clearance)	Distance through the insulation		0.008			mm
R_{IO}	Isolation resistance	Input to output, V_{IO} = 500V, all pins on each side of the barrier tied together creating a two-terminal device, T_A < +85°C			> 10^{12}		Ω
		Input to output, V_{IO} = 500V, +100°C ≤ T_A < T_A max			> 10^{11}		Ω
C_{IO}	Barrier capacitance input to output	V_I = 0.8V_{PP} at 1MHz			1.2		pF
C_I	Input capacitance to ground	V_I = 0.8V_{PP} at 1MHz			3		pF

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of the board design to ensure that the mounting pads of the isolator on the printed circuit board do not reduce this distance. Creepage and clearance on a printed circuit board become equal according to the measurement techniques shown in the *Isolation Glossary* . Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

IEC SAFETY LIMITING VALUES

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output (I/O) circuitry. A failure of the I/O circuitry can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.
The safety-limiting constraint is the operating virtual junction temperature range specified in the Absolute Maximum Ratings table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the Thermal Characteristics table is that of a device installed in the JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages* and is conservative. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	θ_{JA} = 246°C/W, V_I = 5.5V, T_J = +150°C, T_A = +25°C			90	mA
T_C	Maximum case temperature				+150	°C

IEC 61000-4-5 RATINGS

PARAMETER		TEST CONDITIONS	VALUE	UNIT
V_{IOSM}	Surge immunity	1.2/50µs voltage surge and 8/20µs current surge	±6000	V

IEC 60664-1 RATINGS

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	IIIa
Installation classification	Rated mains voltage ≤ 150 V_{RMS}	I-IV
	Rated mains voltage < 300 V_{RMS}	I-III

ELECTRICAL CHARACTERISTICS

At T_A = –40°C to +105°C, V_{DD1} = 4.5V to 5.5V, V_{DD2} = 4.5V to 5.5V, V_{IN+} = –280mV to +280mV, $V_{IN–}$ = 0V, and sinc^3 filter with OSR = 256, unless otherwise noted.

PARAMETER		TEST CONDITIONS	AMC1203 MIN	AMC1203 TYP(1)	AMC1203 MAX	UNIT
RESOLUTION			16			Bits
DC ACCURACY						
INL	Integral linearity error(2)	AMC1203		±3	±9	LSB
		AMC1203B		±2	±6	LSB
DNL	Differential nonlinearity(3)		–1		+1	LSB
V_{OS}	Offset error(4)		–1	±0.1	1	mV
TCV_{OS}	Offset error thermal drift			±1.5	±5	µV/°C
G_{ERR}	Gain error	AMC1203	–2	±0.2	2	%
		AMC1203B	–1	±0.2	1	%
TCG_{ERR}	Gain error thermal drift			±20		ppm/°C
PSRR	Power-supply rejection ratio			80		dB
ANALOG INPUTS						
FSR	Full-scale differential voltage input range	$(V_{IN+}) – (V_{IN–})$	–320		320	mV
V_{CM}	Operating common-mode signal(3)		–0.1		5	V
C_I	Input capacitance to GND1	V_{IN+} or $V_{IN–}$		3		pF
C_{ID}	Differential input capacitance			6		pF
R_{ID}	Differential input resistance			28		kΩ
I_{IL}	Input leakage current		–5		5	nA
CMTI	Common-mode transient immunity	V_{CM} = 1kV	15			kV/µs
CMRR	Common-mode rejection ratio	V_{IN} from 0V to 5V at 0Hz		92		dB
		V_{IN} from 0V to 5V at 50kHz		105		dB
INTERNAL CLOCK						
t_{CLK}	Clock period	See Figure 2	83.33	100	125	ns
f_{CLK}	Clock frequency	See Figure 2	8	10	12	MHz
t_H	Clock high-time	See Figure 2	$(t_{CLK}/2) – 8$	50	$(t_{CLK}/2) + 8$	ns
t_{D1}	Data valid time after falling edge of clock	See Figure 2	–2	0	2	ns
AC ACCURACY						
SINAD	Signal-to-noise + distortion	f_{IN} = 1kHz	80	85		dB
SNR	Signal-to-noise ratio	f_{IN} = 1kHz	80.5	85		dB
THD	Total harmonic distortion	AMC1203, f_{IN} = 1kHz		–92	–84.5	dB
		AMC1203B, f_{IN} = 1kHz		–95	–88	
SFDR	Spurious-free dynamic range	AMC1203, f_{IN} = 1kHz	86	92		dB
		AMC1203B, f_{IN} = 1kHz	89	95		

(1) All typical values are at T_A = +25°C
(2) Integral nonlinearity is defined as the maximum deviation of the line through the inputs of the specified input range of the transfer curve of the specified VIN expressed either as number of LSBs, or as a percent of the specified 560mV input range.
(3) Ensured by design.
(4) Maximum values, including temperature drift, are ensured over the full specified temperature range.

ELECTRICAL CHARACTERISTICS (continued)

At T_A = –40°C to +105°C, V_{DD1} = 4.5V to 5.5V, V_{DD2} = 4.5V to 5.5V, V_{IN+} = –280mV to +280mV, $V_{IN–}$ = 0V, and sinc^3 filter with OSR = 256, unless otherwise noted.

PARAMETER		TEST CONDITIONS	AMC1203			UNIT
			MIN	TYP(1)	MAX	
DIGITAL OUTPUTS						
V_{OH}	High-level output voltage	I_{OH} = –8mA	V_{DD2} – 0.8	4.6		V
		I_{OH} = –4mA	V_{DD2} – 0.4	4.8		V
V_{OL}	Low-level output voltage	I_{OL} = 8mA		0.3	0.8	V
		I_{OL} = 4mA		0.2	0.4	V
POWER SUPPLY						
V_{DD}	Supply voltage	V_{DD1} and V_{DD2}	4.5	5.0	5.5	V
I_{DD1}	Analog supply current			6	8	mA
I_{DD2}	Digital supply current			10	12	mA
P_D	Power dissipation			80	110	mW

EQUIVALENT INPUT CIRCUIT

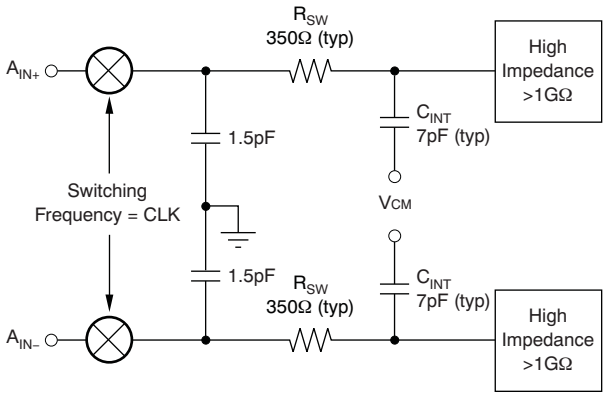


Figure 1. Equivalent Analog Input Circuit

PIN CONFIGURATION

DUB or PSA PACKAGE
SOP-8 Gull-Wing or SOP-8
(TOP VIEW)

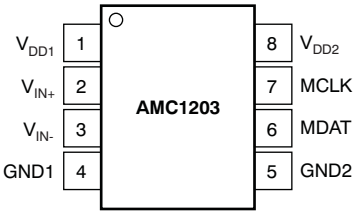


Table 1. SOP-8 PIN DESCRIPTIONS

PIN		
NO.	NAME	DESCRIPTION
1	V_{DD1}	Analog power supply
2	V_{IN+}	Noninverting analog input
3	$V_{IN–}$	Inverting analog input
4	GND1	Analog ground
5	GND2	Digital ground
6	MDAT	Modulator data output
7	MCLK	Modulator clock output
8	V_{DD2}	Digital power supply

DW PACKAGE
SOIC-16
(TOP VIEW)

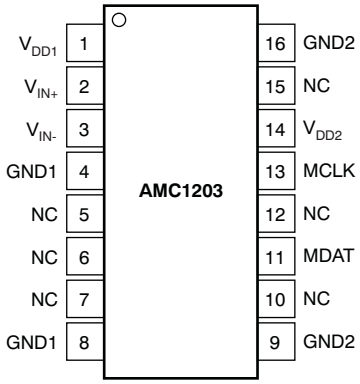


Table 2. SOIC-16 PIN DESCRIPTIONS

PIN		
NO.	NAME	DESCRIPTION
1	V_{DD1}	Analog power supply
2	V_{IN+}	Noninverting analog input
3	$V_{IN–}$	Inverting analog input
4, 8(1)	GND1	Analog ground
5, 6, 7, 10, 12, 15	NC	No internal connection—can be tied to any potential or left unconnected
9, 16(1)	GND2	Digital ground
11	MDAT	Modulator data output
13	MCLK	Modulator clock output
14	V_{DD2}	Digital power supply

(1) Both pins are connected internally via a low-impedance path; thus only one of the pins must be tied to the ground plane.

TIMING INFORMATION

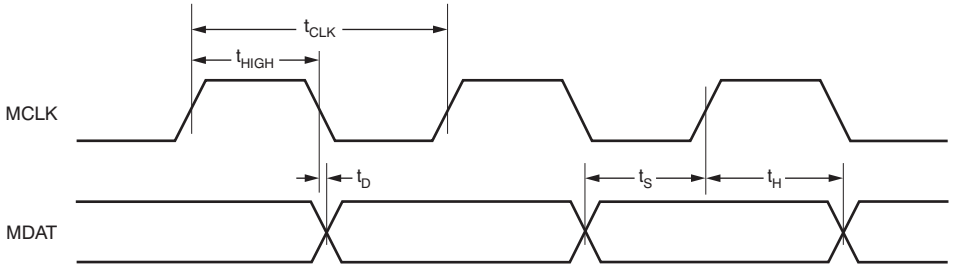


Figure 2. Modulator Output Mode Timing

TIMING CHARACTERISTICS FOR MODULATOR OUTPUT MODE

Over recommended operating free-air temperature range at –40°C to +105°C, V_{DD1} = +5V, and V_{DD2} = +5V, unless otherwise noted.

PARAMETER		MIN	TYP	MAX	UNIT
t_{CLK}	MCLK clock period	83.33	100	125	ns
t_{HIGH}	MCLK clock high time	(t_{CLK}/2) – 8	t_P/2	(t_{CLK}/2) + 8	ns
t_D	Data delay after falling edge of MCLK	–2	0	2	ns
t_S	Data setup time prior to rising edge of MCLK	31.5			ns
t_H	Data hold time after rising edge of MCLK	31.5			ns

TYPICAL CHARACTERISTICS

At V_{DD1} = V_{DD2} = 5V, V_{IN+} = –280mV to +280mV, $V_{IN–}$ = 0V, and sinc^3 filter with OSR = 256, unless otherwise noted.

INTEGRAL NONLINEARITY vs INPUT SIGNAL AMPLITUDE

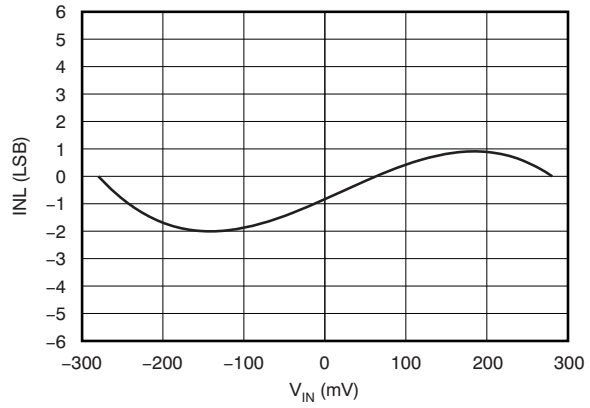


Figure 3.

INTEGRAL NONLINEARITY vs TEMPERATURE

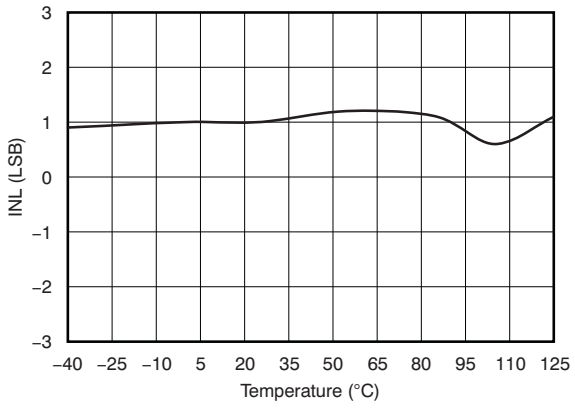


Figure 4.

OFFSET ERROR vs SUPPLY VOLTAGE

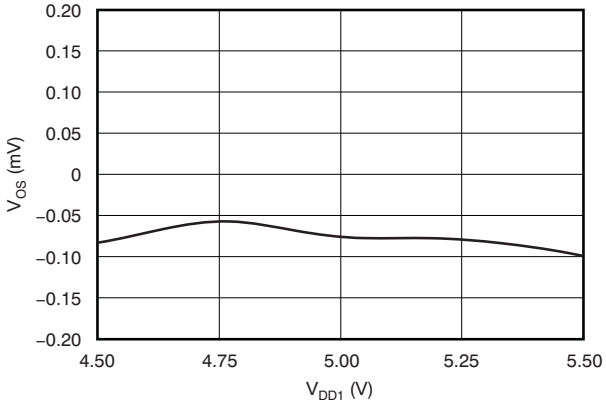


Figure 5.

OFFSET ERROR vs TEMPERATURE

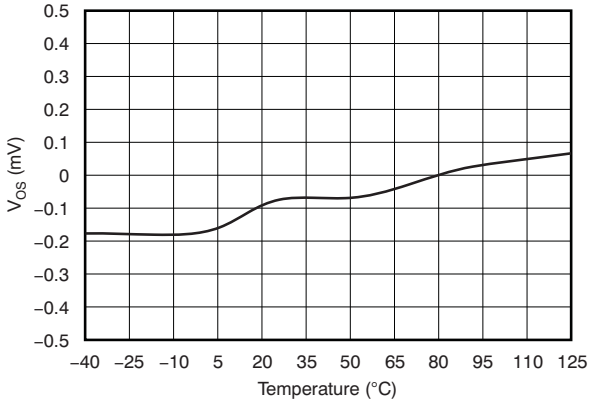


Figure 6.

GAIN ERROR vs TEMPERATURE

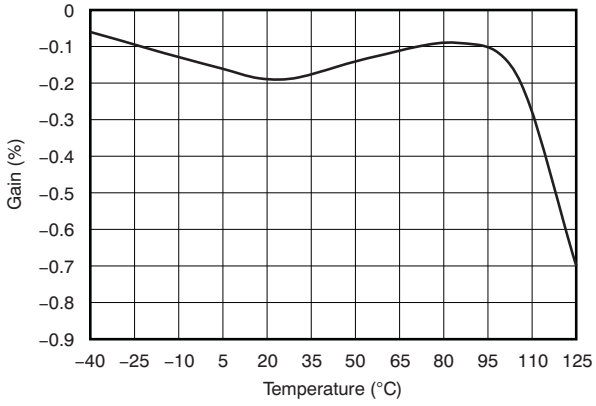


Figure 7.

EFFECTIVE NUMBER OF BITS vs OVERSAMPLING RATIO

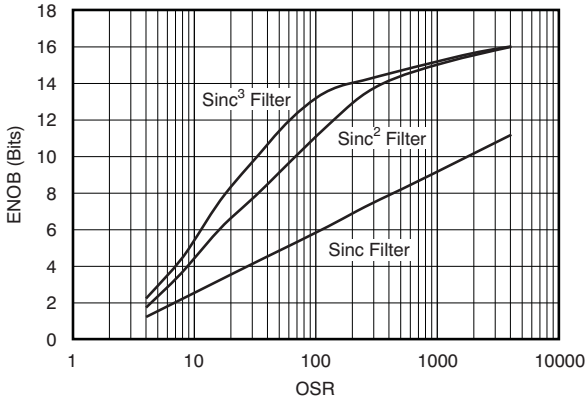


Figure 8.

TYPICAL CHARACTERISTICS (continued)

At V_{DD1} = V_{DD2} = 5V, V_{IN+} = –280mV to +280mV, $V_{IN–}$ = 0V, and $sinc^3$ filter with OSR = 256, unless otherwise noted.

SIGNAL-TO-NOISE RATIO vs INPUT SIGNAL AMPLITUDE

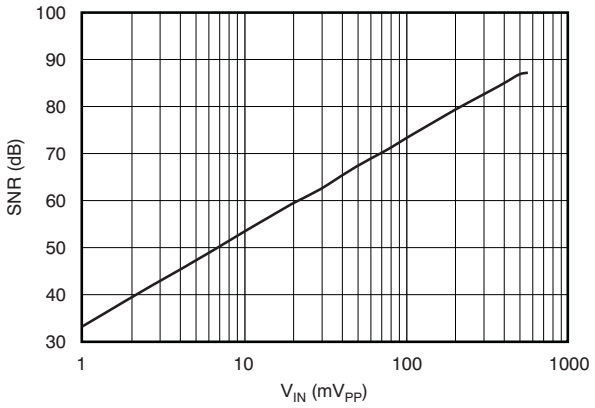


Figure 9.

SIGNAL-TO-NOISE RATIO vs TEMPERATURE

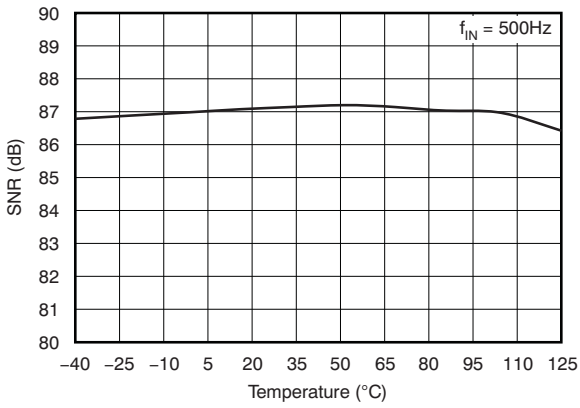


Figure 10.

SIGNAL-TO-NOISE RATIO vs INPUT SIGNAL FREQUENCY

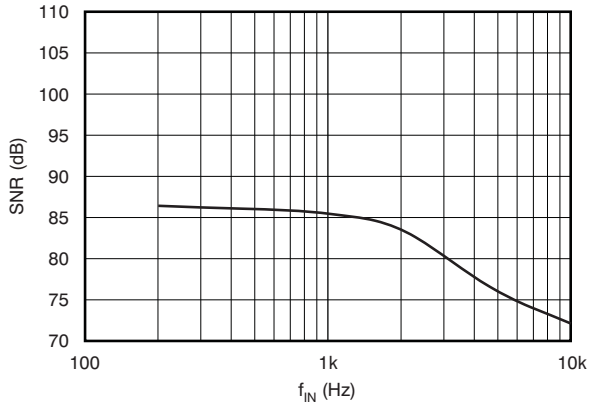


Figure 11.

SIGNAL-TO-NOISE RATIO vs TEMPERATURE

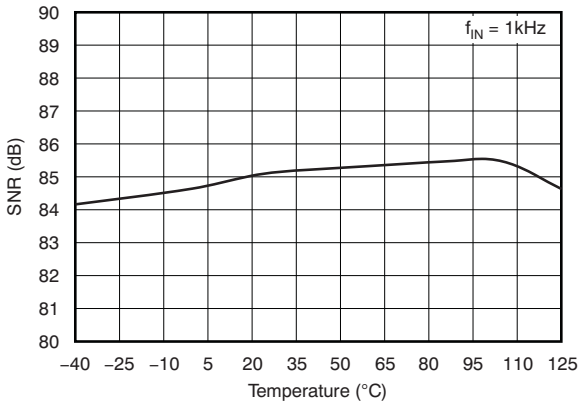


Figure 12.

TOTAL HARMONIC DISTORTION vs INPUT SIGNAL FREQUENCY

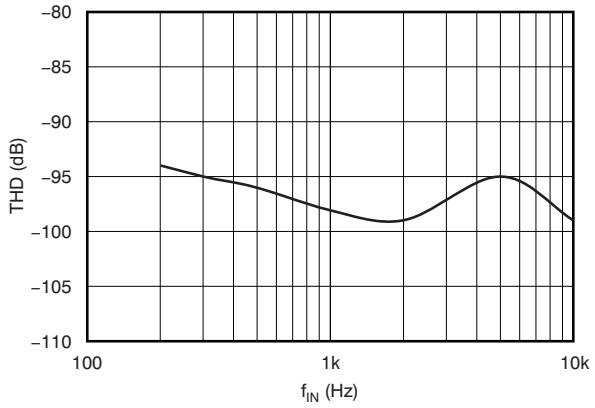


Figure 13.

TOTAL HARMONIC DISTORTION vs TEMPERATURE

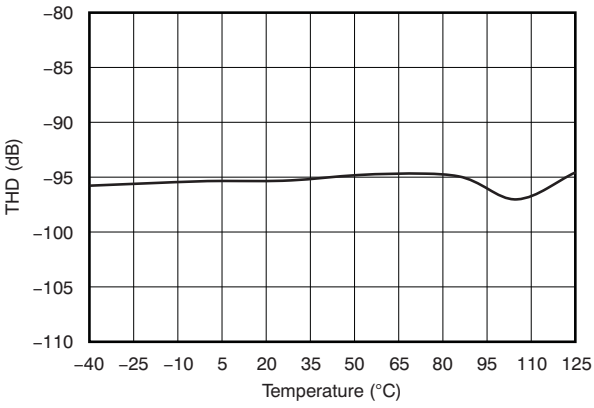


Figure 14.

TYPICAL CHARACTERISTICS (continued)

At V_{DD1} = V_{DD2} = 5V, V_{IN+} = –280mV to +280mV, $V_{IN–}$ = 0V, and sinc^3 filter with OSR = 256, unless otherwise noted.

FREQUENCY SPECTRUM
(4096 Point FFT, f_{IN} = 500Hz, 0.56V_{PP})

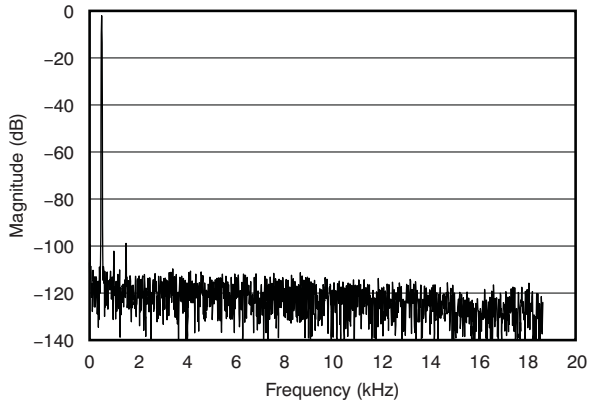


Figure 15.

FREQUENCY SPECTRUM
(4096 Point FFT, f_{IN} = 1kHz, 0.56V_{PP})

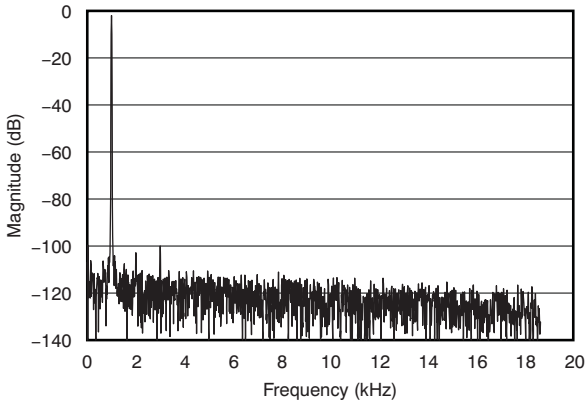


Figure 16.

COMMON-MODE REJECTION RATIO
vs INPUT SIGNAL FREQUENCY

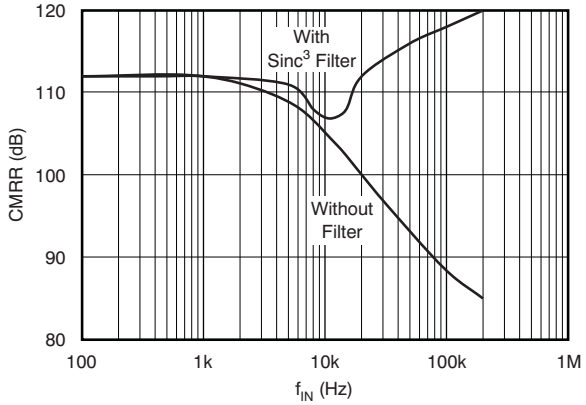


Figure 17.

POWER-SUPPLY REJECTION RATIO
vs FREQUENCY

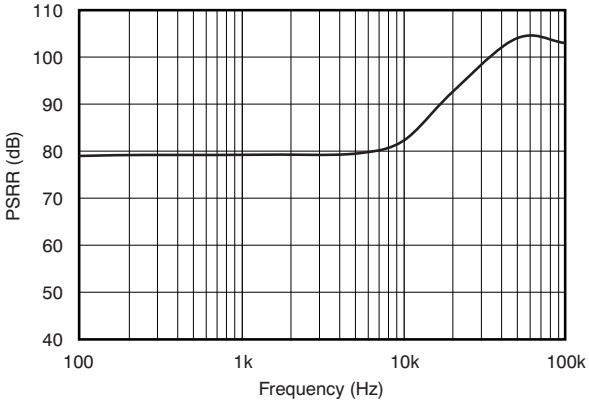


Figure 18.

INTERNAL CLOCK FREQUENCY
vs SUPPLY VOLTAGE

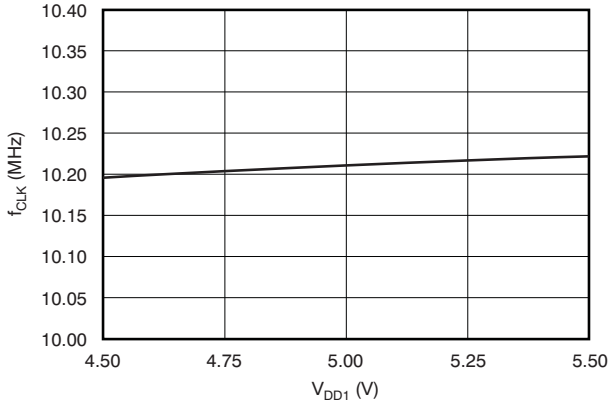


Figure 19.

INTERNAL CLOCK FREQUENCY
vs TEMPERATURE

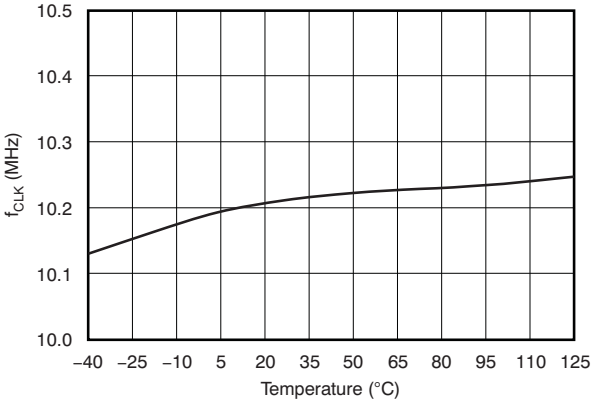


Figure 20.

TYPICAL CHARACTERISTICS (continued)

At V_{DD1} = V_{DD2} = 5V, V_{IN+} = –280mV to +280mV, $V_{IN–}$ = 0V, and $sinc^3$ filter with OSR = 256, unless otherwise noted.

ANALOG SUPPLY CURRENT vs TEMPERATURE

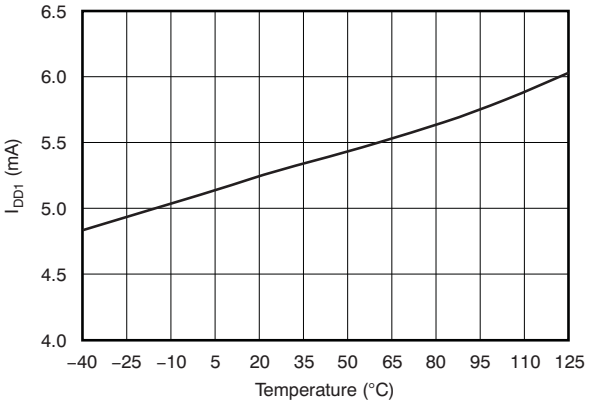


Figure 21.

DIGITAL SUPPLY CURRENT vs TEMPERATURE

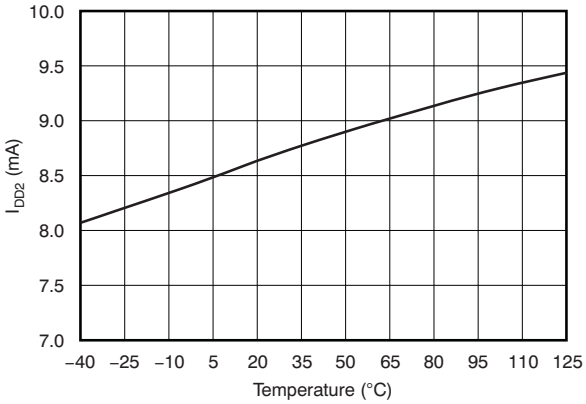


Figure 22.

GENERAL DESCRIPTION

The AMC1203 is a single-channel, 2nd-order, CMOS, delta-sigma modulator, designed for medium- to high-resolution A/D conversions from dc to 39kHz with an oversampling ratio (OSR) of 256. The isolated output of the converter (MDAT) provides a stream of digital ones and zeros. The time average of this serial output is proportional to the analog input voltage.

The modulator shifts the quantization noise to high frequencies; therefore, a low-pass digital filter should be used at the output of the device to increase the overall performance. This filter is also used to convert from the 1-bit data stream at a high sampling rate into a higher-bit data word at a lower rate (decimation). A digital signal processor (DSP), microcontroller (µC) or field programmable gate array (FPGA) can be used to implement the filter. Another option is using a suitable application-specific device, such as the AMC1210, a four-channel digital sinc-filter. Figure 23 shows two AMC1203s and one ADS1205 (dual-channel, non-isolated modulator) connected to an AMC1210, building the entire analog front-end of a resolver-based motor-control application. For detailed information on the ADS1205 and AMC1210, please visit our home page at www.ti.com.

The overall performance (speed and accuracy) depends on the selection of an appropriate OSR and filter type. A higher OSR results in higher accuracy while operating at lower refresh rate. Alternatively, a lower OSR results in lower accuracy, but provides data at a higher refresh rate. This system allows flexibility with the digital filter design and is capable of A/D conversion results that have a dynamic range exceeding 95dB with OSR = 256.

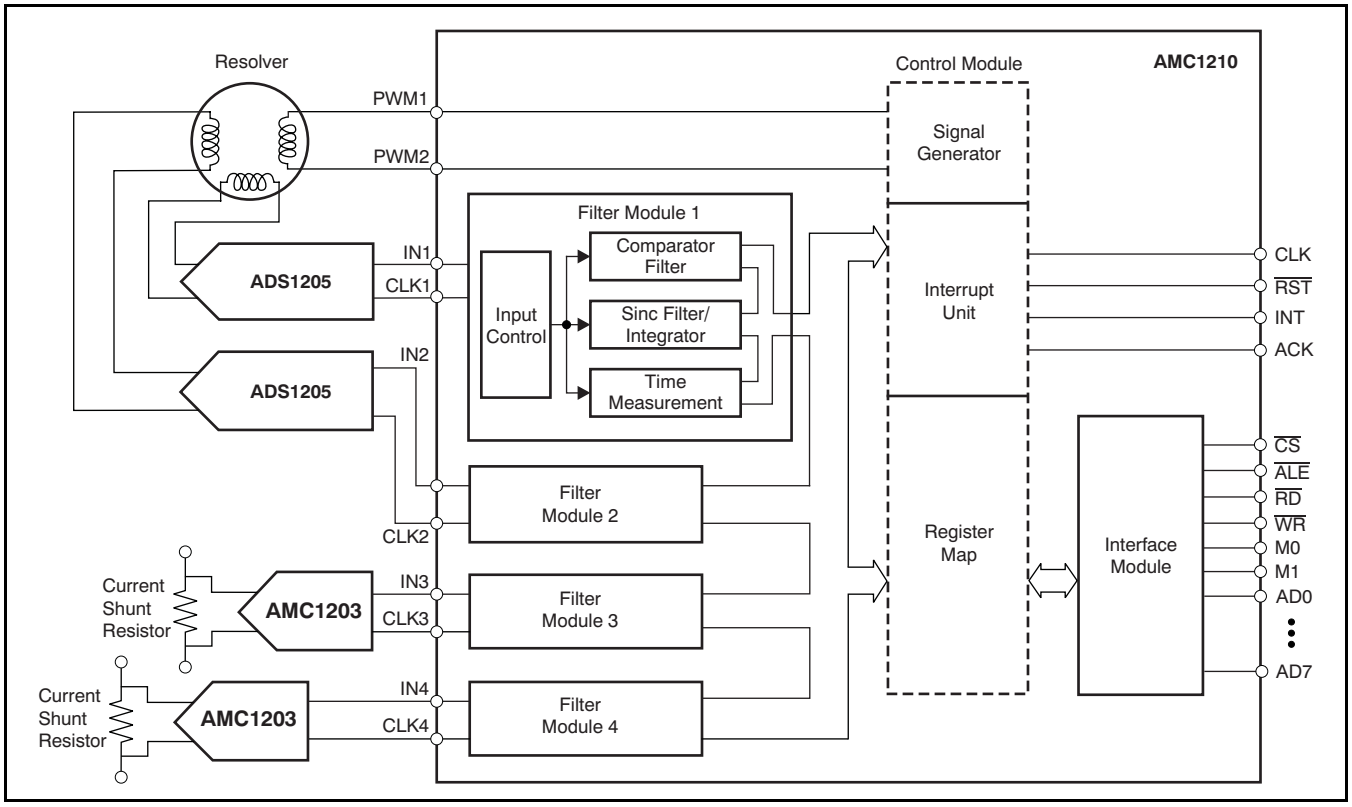


Figure 23. Example of a Resolver-Based Motor-Control Application

THEORY OF OPERATION

The differential analog input of the AMC1203 is implemented with a switched-capacitor circuit. This switched-capacitor circuit implements a 2nd-order modulator stage that digitizes the input signal into a 1-bit output stream. The internally-generated clock signal (sourcing the capacitor circuit and the modulator) is available as an output signal on the MCLK pin. The analog input signal is continuously sampled by the modulator and compared to an internal voltage reference. A digital stream, accurately representing the analog input voltage over time, appears at the output of the converter.

ANALOG INPUT

The input design topology of the AMC1203 is based on a fully-differential, switched-capacitor architecture with a dynamic input impedance of 28kΩ at 10MHz, as Figure 1 shows. This input stage provides the mechanism to achieve low system noise, high common-mode rejection (92dB), and excellent power-supply rejection.

The input impedance becomes a consideration in designs with high input-signal source impedance. This high-impedance may cause degradation in gain, linearity, and THD. The importance of this effect, however, depends on the desired system performance.

There are two restrictions on the analog input signals, V_{IN+} and V_{IN-}. If the input voltage exceeds the range GND – 0.3V to V_{DD} + 0.3V, the input current must be limited to 10mA, because the input protection diodes on the front end of the converter begin to turn on. In addition, the linearity and the noise performance of the device is ensured only when the differential analog voltage resides within ±280mV.

MODULATOR

The modulator topology of the AMC1203 is fundamentally a 2nd-order, switched-capacitor, delta-sigma modulator, such as the one conceptualized in Figure 24. The analog input voltage ($X_{(t)}$) and the output of the 1-bit digital-to-analog converter (DAC) are differentiated, providing an analog voltage (X_2) at the input of the first integrator or modulator stage. The output of the first integrator is further differentiated with the DAC output, and the resulting voltage (X_3) feeds the input of the second integrator stage. When the value of the integrated signal (X_4) at the output of the second stage equals the comparator reference voltage, the output of the comparator switches from high to low, or vice versa, depending on its previous state. In this case, the 1-bit DAC responds on the next clock pulse by changing its analog output voltage (X_6), causing the integrators to progress in the opposite direction, while forcing the value of the integrator output to track the average of the input.

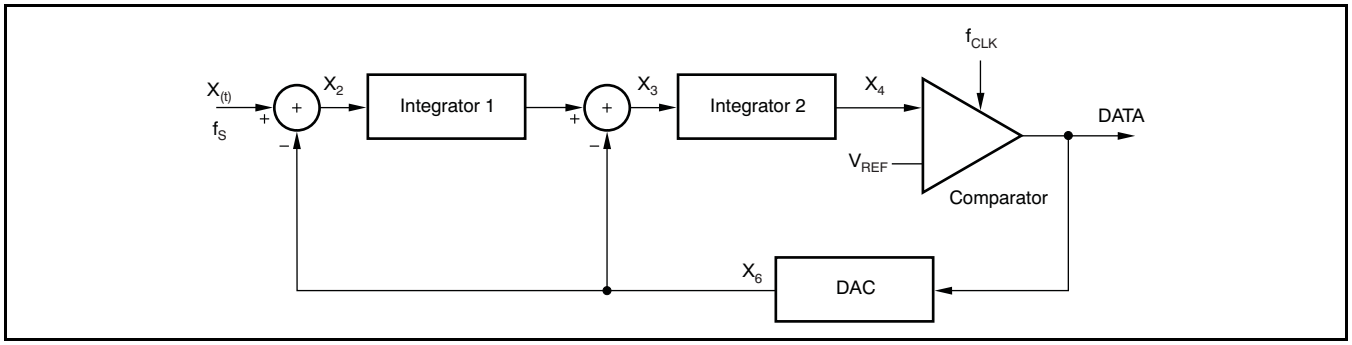


Figure 24. Block Diagram of the 2nd-Order Modulator

DIGITAL OUTPUT

A differential input signal of 0V ideally produces a stream of ones and zeros that are high 50% of the time and low 50% of the time. A differential input of +280mV produces a stream of ones and zeros that are high 87.5% of the time. A differential input of –280mV produces a stream of ones and zeros that are high 12.5% of the time. The input voltage versus the output modulator signal is shown in Figure 27.

The system clock of the AMC1203 is 20 MHz by default, and is generated internally using an RC circuit. The system clock is divided by two for the modulator clock; thus, the default clock frequency of the modulator is 10MHz. This clock is also available on the output terminal MCLK, whereas the data are provided at the MDAT output pin. The data are changing at the falling edge of MCLK, so data can safely be latched with the rising edge; see the Timing Characteristics.

FILTER USAGE

The modulator generates a bit stream that is processed by a digital filter to get a digital word similar to the conversion result of a conventional analog-to-digital converter (ADC). A very simple filter, built with minimal effort and hardware, is a sinc^3 filter:

$$H(z) = \left(\frac{1 - z^{-OSR}}{1 - z^{-1}} \right)^3 \quad (1)$$

This filter provides the best output performance at the lowest hardware size (count of digital gates). For an OSR in the range of 16 to 256, this filter is a good choice. All the characterizations in this document are also done with a sinc^3 filter with OSR=256 and an output word width of 16 bits.

In a sinc^3 filter response (shown in Figure 25 and Figure 26), the location of the first notch occurs at the frequency of output data rate $f_{DATA} = f_{CLK}/OSR$. The –3dB point is located at half the Nyquist frequency or $f_{DATA}/4$.

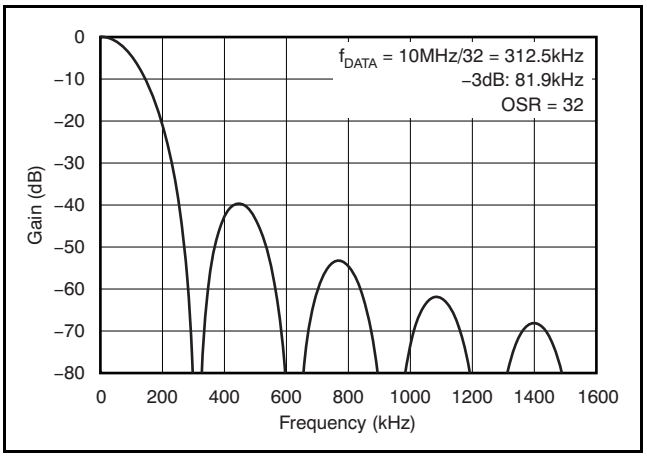


Figure 25. Frequency Response of the Sinc^3 Filter

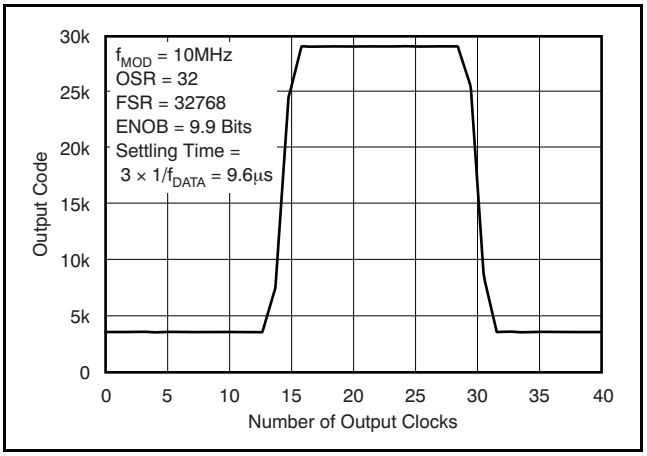


Figure 26. Pole Response of the Sinc^3 Filter

Performance can be improved, for example, by using a cascaded filter structure. The first decimation stage could be built using a sinc^3 filter with a low OSR and the second stage using a high-order filter.

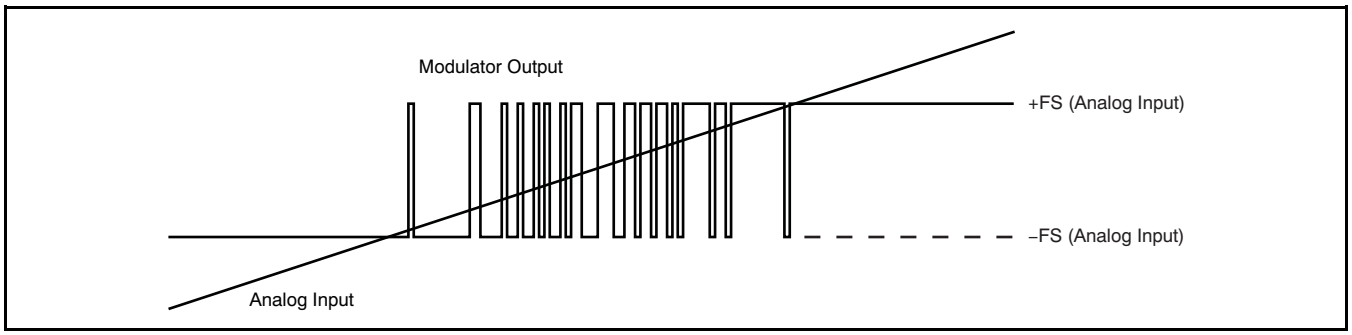


Figure 27. Analog Input vs Modulator Output

The effective number of bits (ENOB) is often used to compare the performance of ADCs and delta-sigma modulators. Figure 28 shows the ENOB of the AMC1203 with different oversampling ratios. In this data sheet, this number is calculated from the SNR using following formula:

$$SNR = 1.76dB + 6.02dB \times ENOB \quad (2)$$

In motor-control applications, a very fast response time for the over-current detection is required. The time for full settling of the filter depends on its order (that is, a $sinc^3$ filter requires three data clocks for full settling (with $f_{DATA} = f_{MOD}/OSR$). Therefore, for over-current protection, filter types other than $sinc^3$ might be a better choice; an alternative is the $sinc^2$ filter. Figure 29 compares the settling times of different filter orders (sincfast is a modified $sinc^2$ filter):

$$H(z) = \left(\frac{1 - z^{-OSR}}{1 - z^{-1}}\right)^2 (1 + z^{-2OSR}) \quad (3)$$

For more information, see application note SBAA094, *Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications*, available for download at www.ti.com.

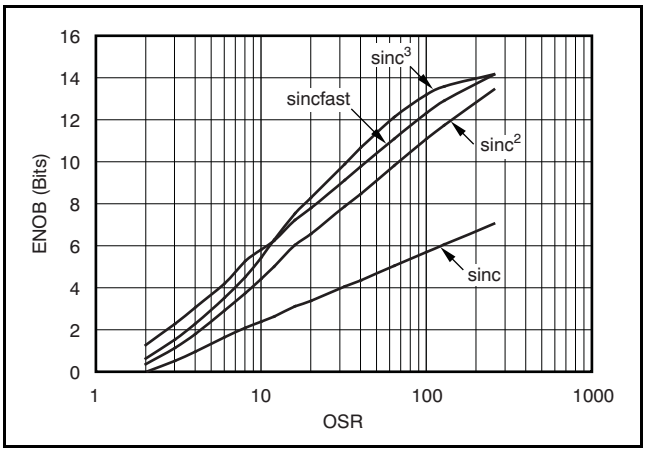


Figure 28. Measured Effective Number of Bits vs Oversampling Ratio

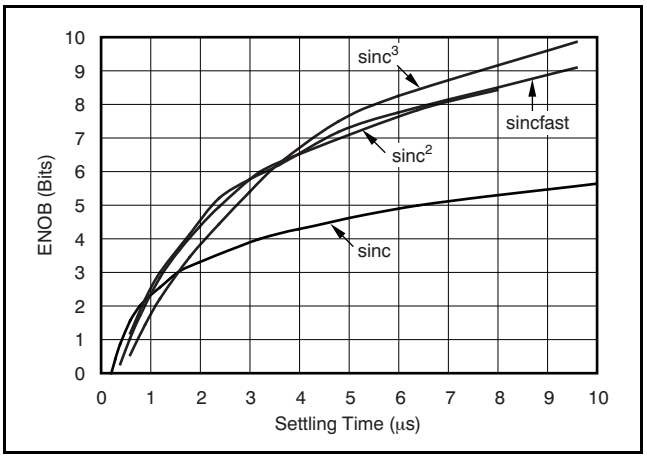


Figure 29. Measured Effective Number of Bits vs Settling Time

APPLICATION INFORMATION

A typical operation of the AMC1203 in a motor-control application is shown in Figure 30. Measurement of the motor phase current is done via the shunt resistor ®$_{SHUNT}$; in this case, a 2-terminal shunt). For better performance, the differential signal is filtered using RC filters (components R_2, R_3 and C_2). Optionally, C_3 and C_4 can be used to reduce charge dumping from the inputs. In this case, care should be taken when choosing the quality of these capacitors—mismatch in values of these capacitors will lead to a common-mode error at the input of the modulator.

The high-side power supply for the AMC1203 (V_{DD1}) is derived from the power supply of the upper gate driver. For lowest cost, a Zener diode can be used to limit the voltage to 5V ±10%. A decoupling capacitor of 0.1µF is recommended for filtering this power-supply path. This capacitor ©$_1$ in Figure 30) should be placed as close as possible to the V_{DD1} pin for best performance. If better filtering is required, an additional 1µF to 10µF capacitor can be used. The floating ground reference (GND1) is derived from the end of the shunt resistor, which is connected to the negative input of the AMC1203 ($V_{IN–}$). If a 4-terminal shunt is used, the inputs of the AMC1203 are connected to the inner leads, while GND1 is connected to one of the outer leads of the shunt. Both digital outputs, MCLK and MDAT, can be directly connected to a digital filter (that is, the AMC1210); see Figure 23.

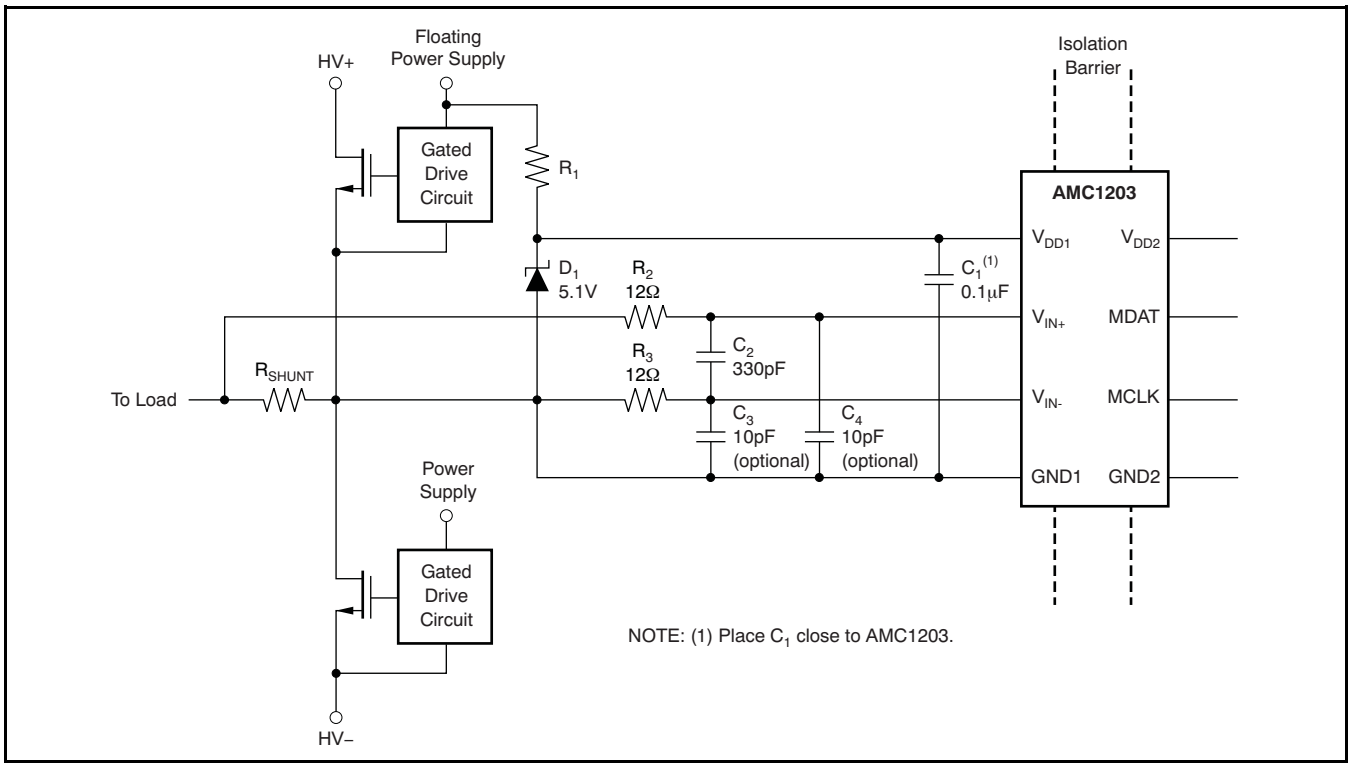
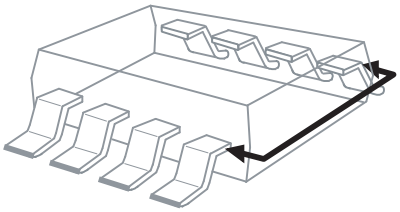


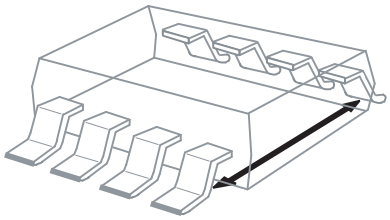
Figure 30. Typical Application Diagram

ISOLATION GLOSSARY

Creepage Distance: The shortest path between two conductive input to output leads measured along the surface of the insulation. The shortest distance path is found around the end of the package body.



Clearance: The shortest distance between two conductive input to output leads measured through air (line of sight).



Input-to Output Barrier Capacitance: The total capacitance between all input terminals connected together, and all output terminals connected together.

Input-to Output Barrier Resistance: The total resistance between all input terminals connected together, and all output terminals connected together.

Primary Circuit: An internal circuit directly connected to an external supply mains or other equivalent source that supplies the primary circuit electric power.

Secondary Circuit: A circuit with no direct connection to primary power that derives its power from a separate isolated source.

Comparative Tracking Index (CTI): CTI is an index used for electrical insulating materials. It is defined as the numerical value of the voltage that causes failure by tracking during standard testing. Tracking is the process that produces a partially conducting path of localized deterioration on or through the surface of an insulating material as a result of the action of electric discharges on or close to an insulation surface. The higher CTI value of the insulating material, the smaller the minimum creepage distance.

Generally, insulation breakdown occurs either through the material, over its surface, or both. Surface failure may arise from flashover or from the progressive degradation of the insulation surface by small localized sparks. Such sparks are the result of the breaking of a surface film of conducting contaminant on the insulation. The resulting break in the leakage current produces an overvoltage at the site of the discontinuity, and an electric spark is generated. These sparks often cause carbonization on insulation material and lead to a carbon track between points of different potential. This process is known as *tracking*.

Insulation:

Operational insulation—Insulation needed for the correct operation of the equipment.

Basic insulation—Insulation to provide basic protection against electric shock.

Supplementary insulation—Independent insulation applied in addition to basic insulation in order to ensure protection against electric shock in the event of a failure of the basic insulation.

Double insulation—Insulation comprising both basic and supplementary insulation.

Reinforced insulation—A single insulation system that provides a degree of protection against electric shock equivalent to double insulation.

Pollution Degree:

Pollution Degree 1—No pollution, or only dry, nonconductive pollution occurs. The pollution has no influence on device performance.

Pollution Degree 2—Normally, only nonconductive pollution occurs. However, a temporary conductivity caused by condensation is to be expected.

Pollution Degree 3—Conductive pollution, or dry nonconductive pollution that becomes conductive because of condensation, occurs. Condensation is to be expected.

Pollution Degree 4 – Continuous conductivity occurs as a result of conductive dust, rain, or other wet conditions.

Installation Category:

Overvoltage Category—This section is directed at insulation coordination by identifying the transient overvoltages that may occur, and by assigning four different levels as indicated in IEC 60664.

I: Signal Level: Special equipment or parts of equipment.

II: Local Level: Portable equipment, etc.

III: Distribution Level: Fixed installation.

IV: Primary Supply Level: Overhead lines, cable systems.

Each category should be subject to smaller transients than the previous category.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (May 2010) to Revision C **Page**

- Changed text in Features bullet from "Operating" to "Specified" for temperature range 1
- Changed Minimum Air Gap parameter in Package Characteristics table to show values for all packages 4
- Added V_{IOSM} symbol to Surge Immunity parameter in IEC 61000-4-5 Ratings table 4

Changes from Revision A (March 2009) to Revision B **Page**

- Deleted references to upcoming availability of SO-8 and SO-16 packages throughout document 1
- Renamed SO-8 to SOP-8 and SO-16 to SOIC-16 throughout document 1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AMC1203BDUB	ACTIVE	SOP	DUB	8	50	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 105	AMC1203 B	Samples
AMC1203BDUBR	ACTIVE	SOP	DUB	8	350	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 105	AMC1203 B	Samples
AMC1203BDW	ACTIVE	SOIC	DW	16	40	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 105	AMC1203 B	Samples
AMC1203BDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 105	AMC1203 B	Samples
AMC1203BPSA	ACTIVE	SOP	PSA	8	95	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	1203 B	Samples
AMC1203BPSAR	ACTIVE	SOP	PSA	8	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	1203 B	Samples
AMC1203DUB	ACTIVE	SOP	DUB	8	50	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 105	AMC1203	Samples
AMC1203DUBR	ACTIVE	SOP	DUB	8	350	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 105	AMC1203	Samples
AMC1203DW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 105	AMC1203	Samples
AMC1203DWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 105	AMC1203	Samples
AMC1203PSA	ACTIVE	SOP	PSA	8	95	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	1203	Samples
AMC1203PSAR	ACTIVE	SOP	PSA	8	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	1203	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

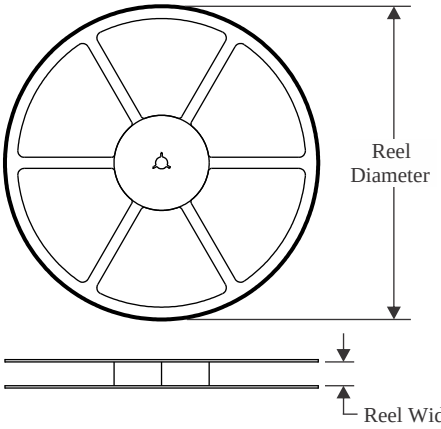
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

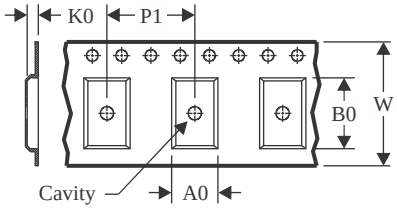
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

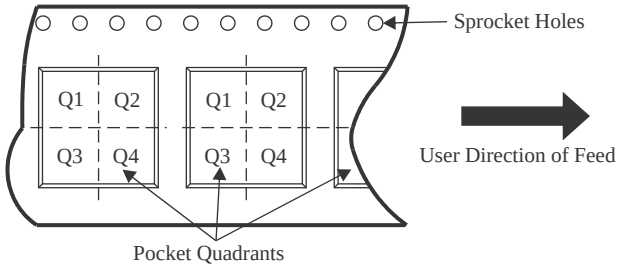


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

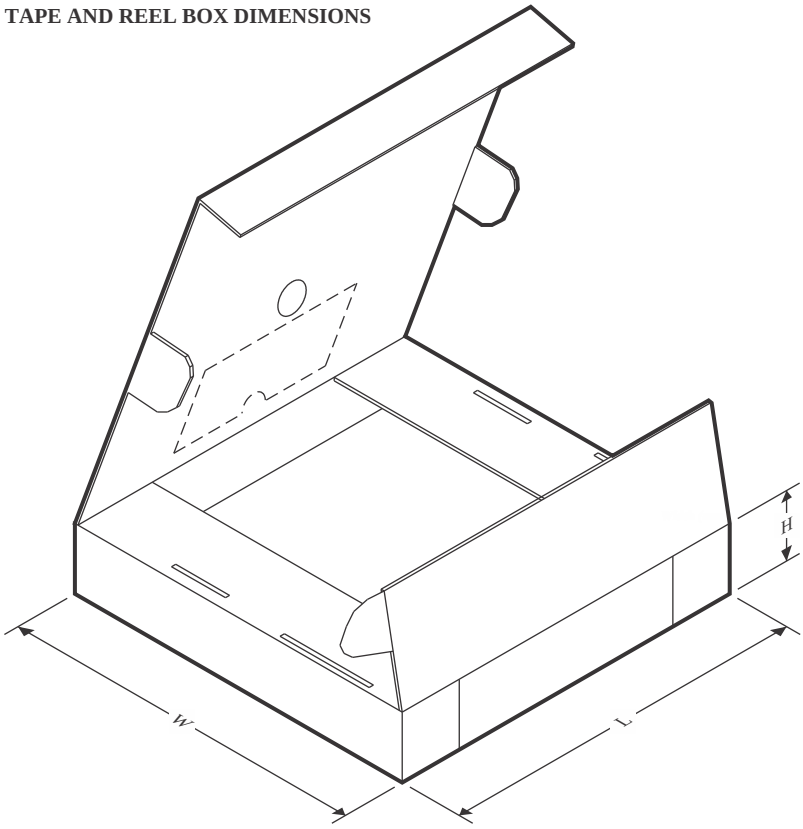
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC1203BDUBR	SOP	DUB	8	350	330.0	24.4	10.9	10.01	5.85	16.0	24.0	Q1
AMC1203BDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
AMC1203BPSAR	SOP	PSA	8	2000	330.0	16.4	8.3	5.7	2.3	12.0	16.0	Q1
AMC1203DUBR	SOP	DUB	8	350	330.0	24.4	10.9	10.01	5.85	16.0	24.0	Q1
AMC1203DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
AMC1203PSAR	SOP	PSA	8	2000	330.0	16.4	8.3	5.7	2.3	12.0	16.0	Q1

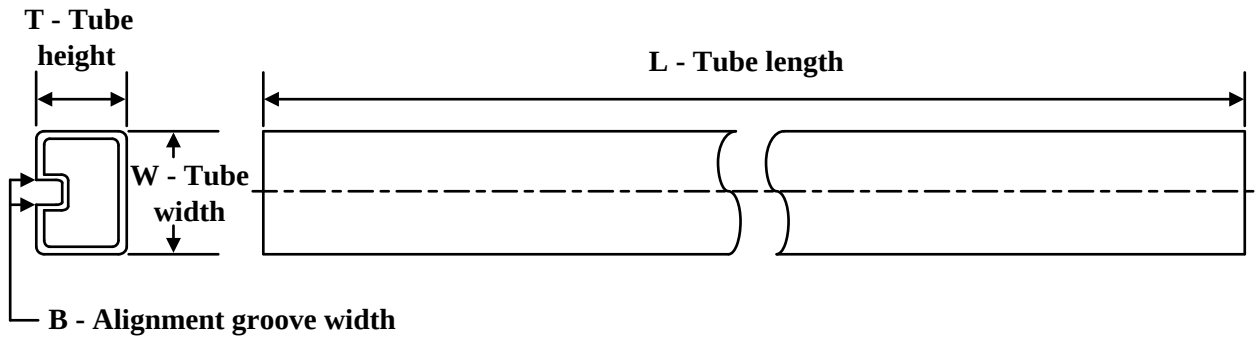
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC1203BDUBR	SOP	DUB	8	350	358.0	335.0	35.0
AMC1203BDWR	SOIC	DW	16	2000	350.0	350.0	43.0
AMC1203BPSAR	SOP	PSA	8	2000	406.0	348.0	63.0
AMC1203DUBR	SOP	DUB	8	350	346.0	346.0	41.0
AMC1203DWR	SOIC	DW	16	2000	350.0	350.0	43.0
AMC1203PSAR	SOP	PSA	8	2000	406.0	348.0	63.0

TUBE



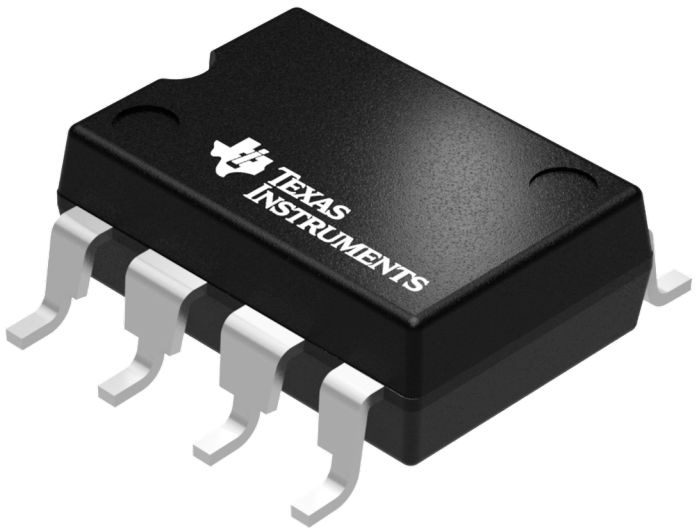
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
AMC1203BDUB	DUB	SOP	8	50	532.13	13.51	7.36	6.91
AMC1203BDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
AMC1203BPSA	PSA	SOP	8	95	530	10.5	4200	5.7
AMC1203DUB	DUB	SOP	8	50	532.13	13.51	7.36	6.91
AMC1203DW	DW	SOIC	16	40	506.98	12.7	4826	6.6
AMC1203PSA	PSA	SOP	8	95	530	10.5	4200	5.7

GENERIC PACKAGE VIEW

DUB 8 SOP - 4.85 mm max height

SMALL OUTLINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

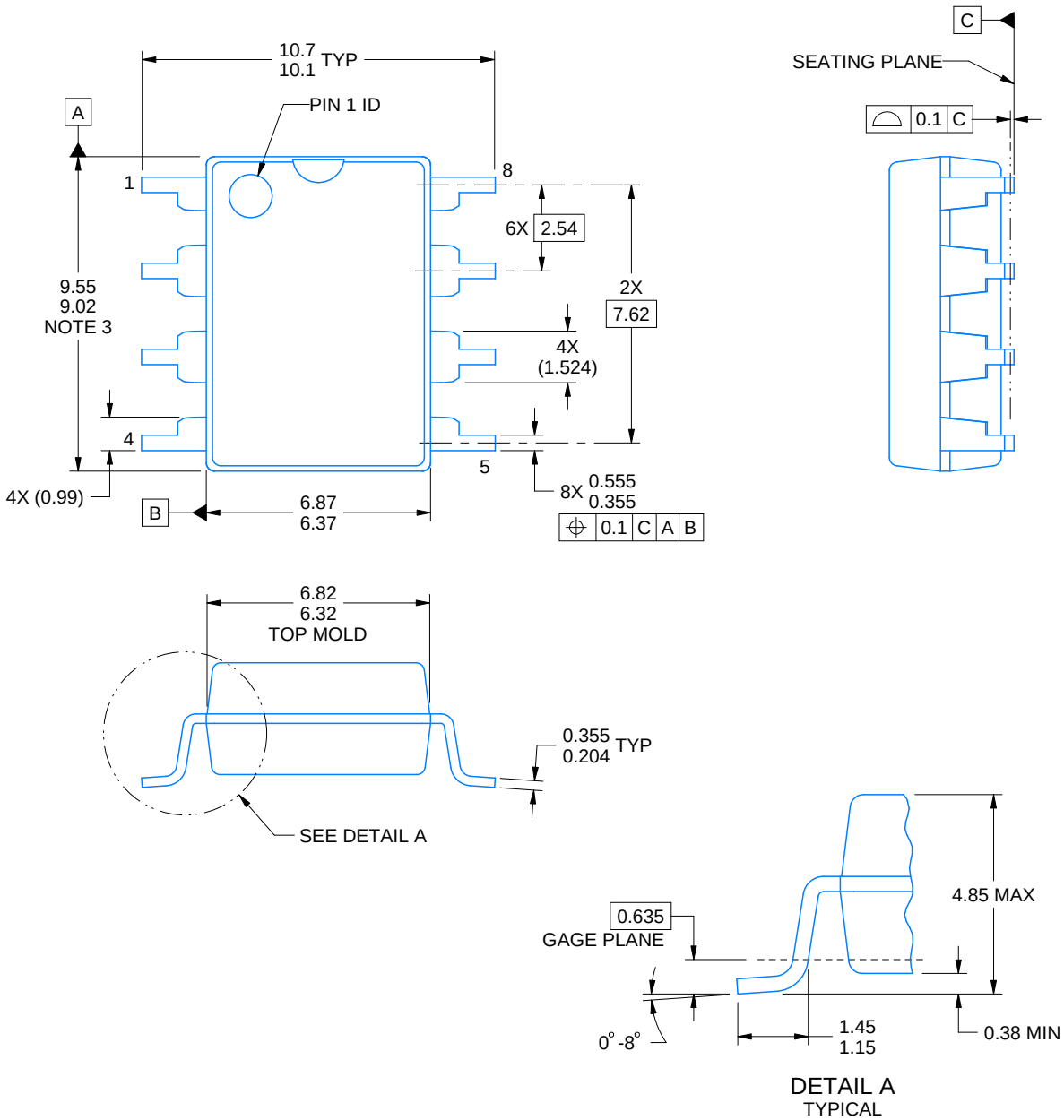
4207614/E

PACKAGE OUTLINE

DUB0008A

SOP - 4.85 mm max height

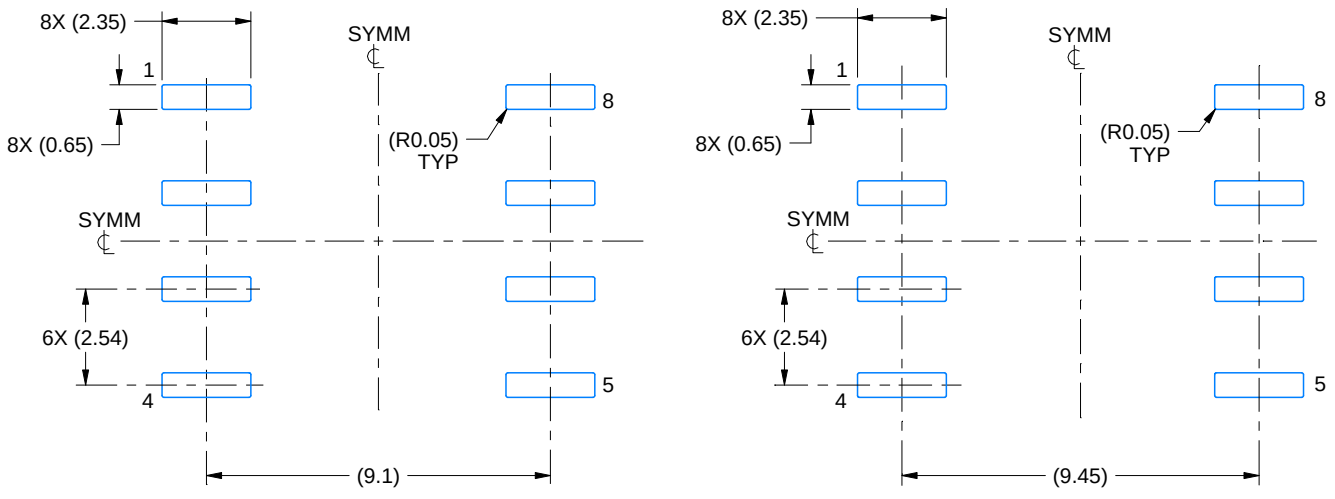
SMALL OUTLINE PACKAGE



4222355/G 04/2019

NOTES:

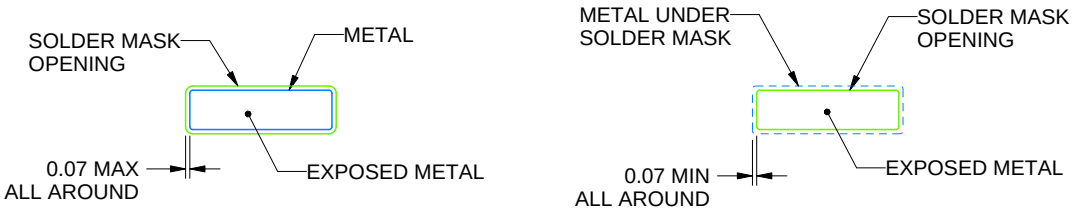
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.254 mm per side.



IPC-7351 NOMINAL
6.75 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
7.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLES
EXPOSED METAL SHOWN
SCALE:5X



NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4222355/G 04/2019

NOTES: (continued)

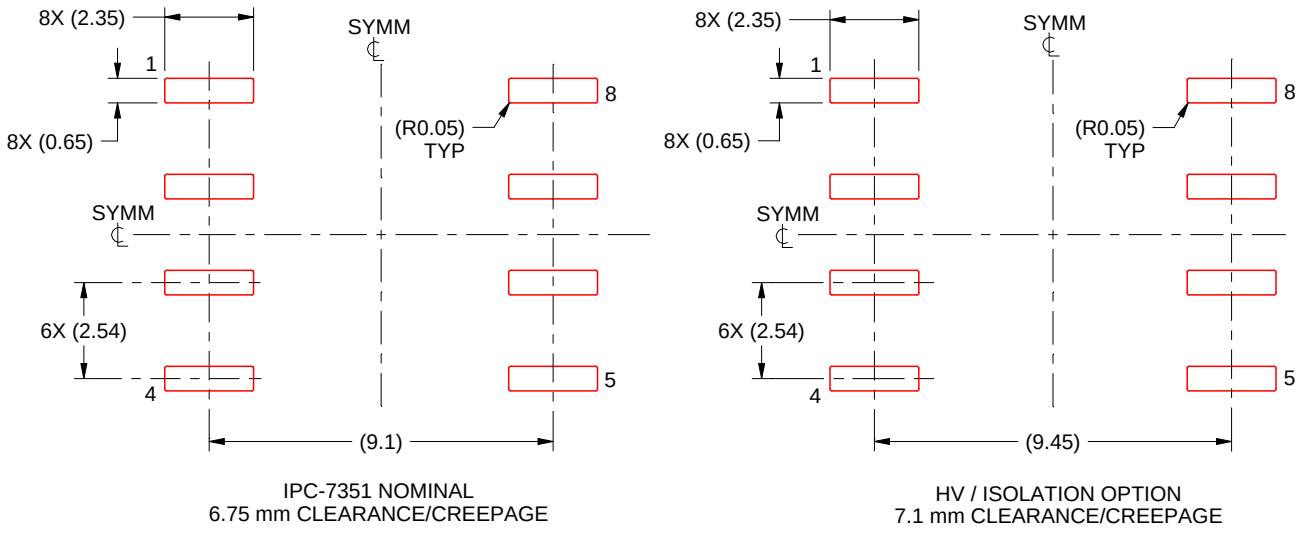
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DUB0008A

SOP - 4.85 mm max height

SMALL OUTLINE PACKAGE



IPC-7351 NOMINAL
6.75 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
7.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:5X

4222355/G 04/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

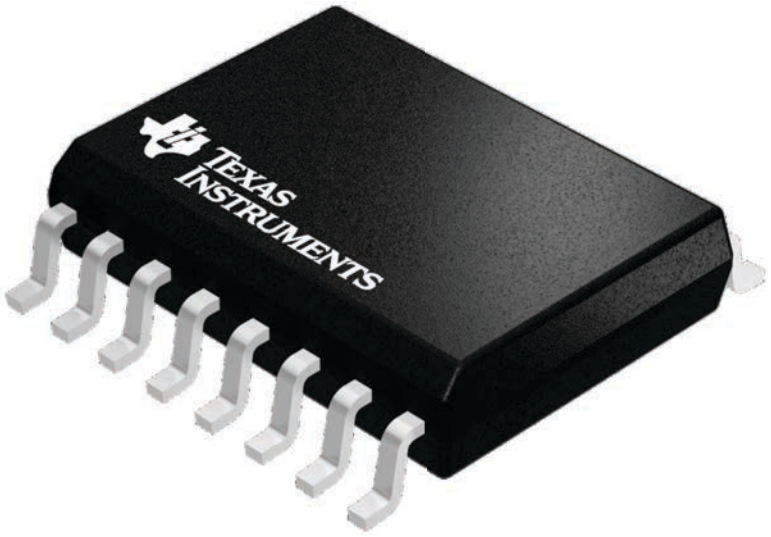
DW 16

SOIC - 2.65 mm max height

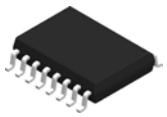
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

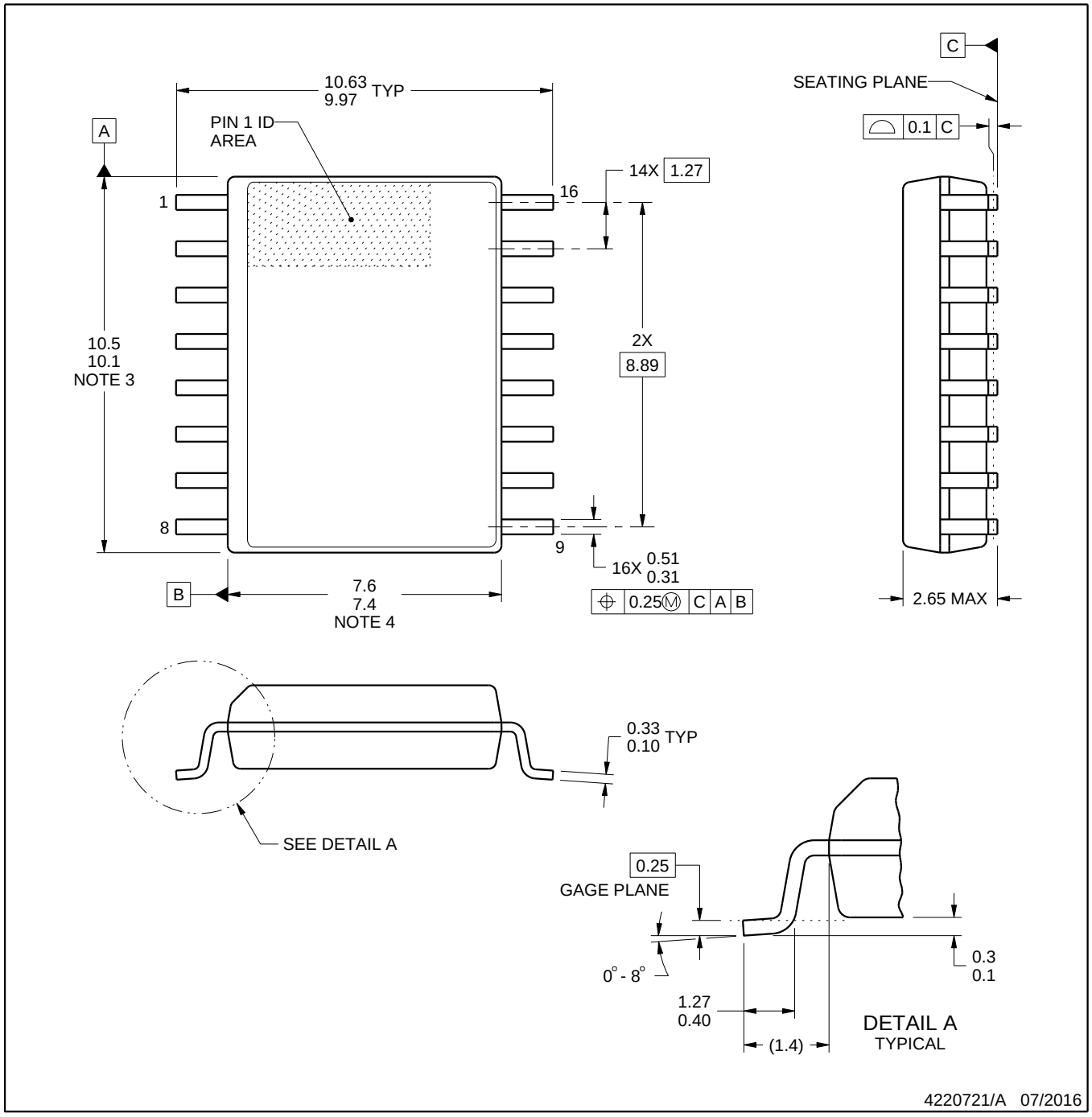


PACKAGE OUTLINE

DW0016A

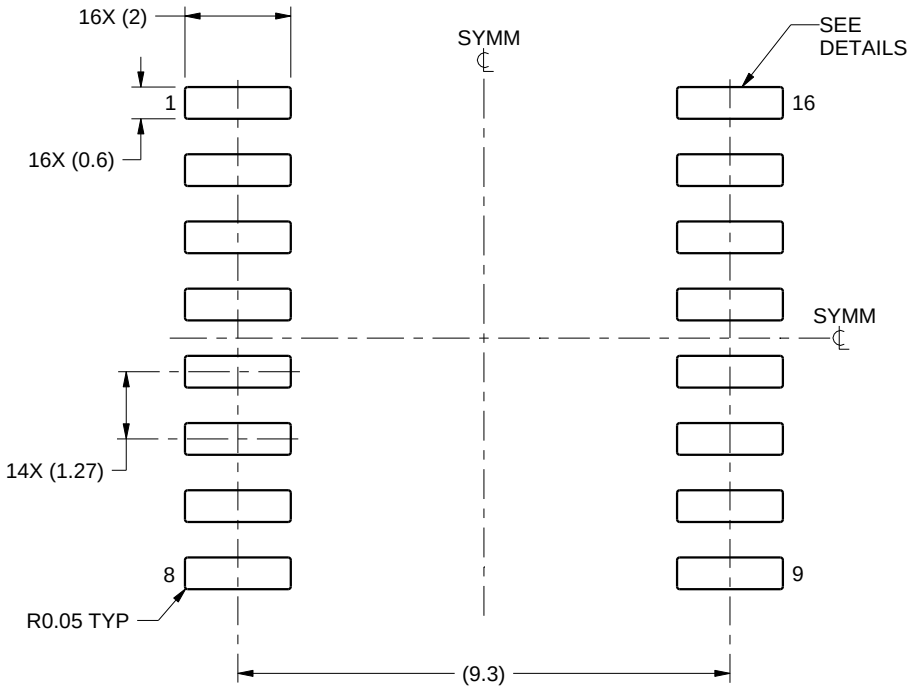
SOIC - 2.65 mm max height

SOIC

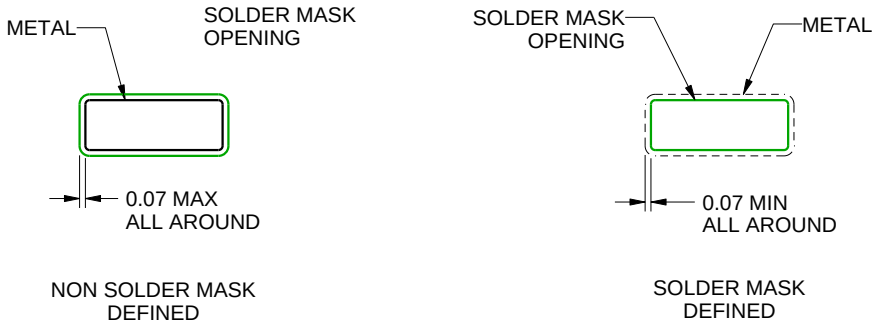


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

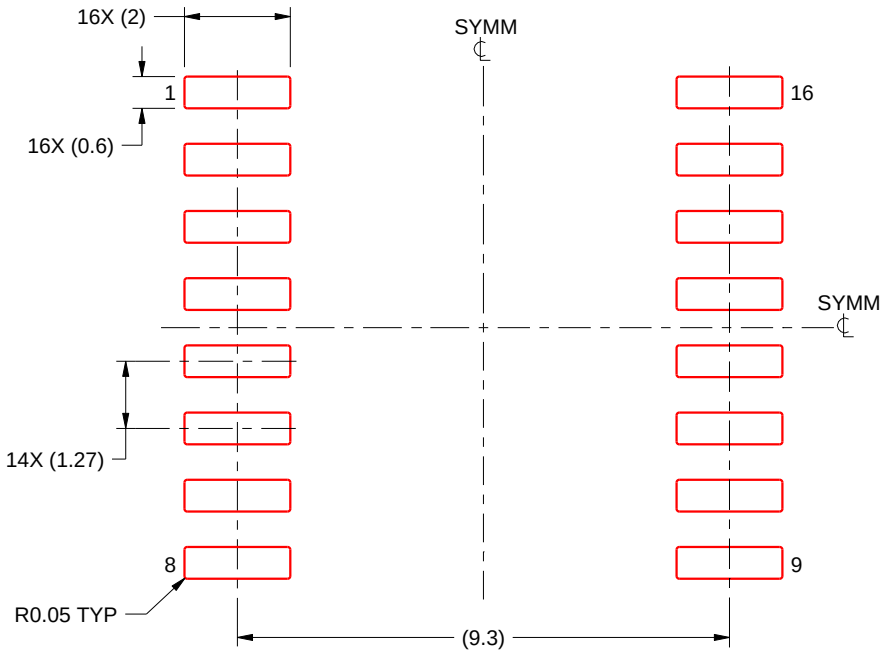


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



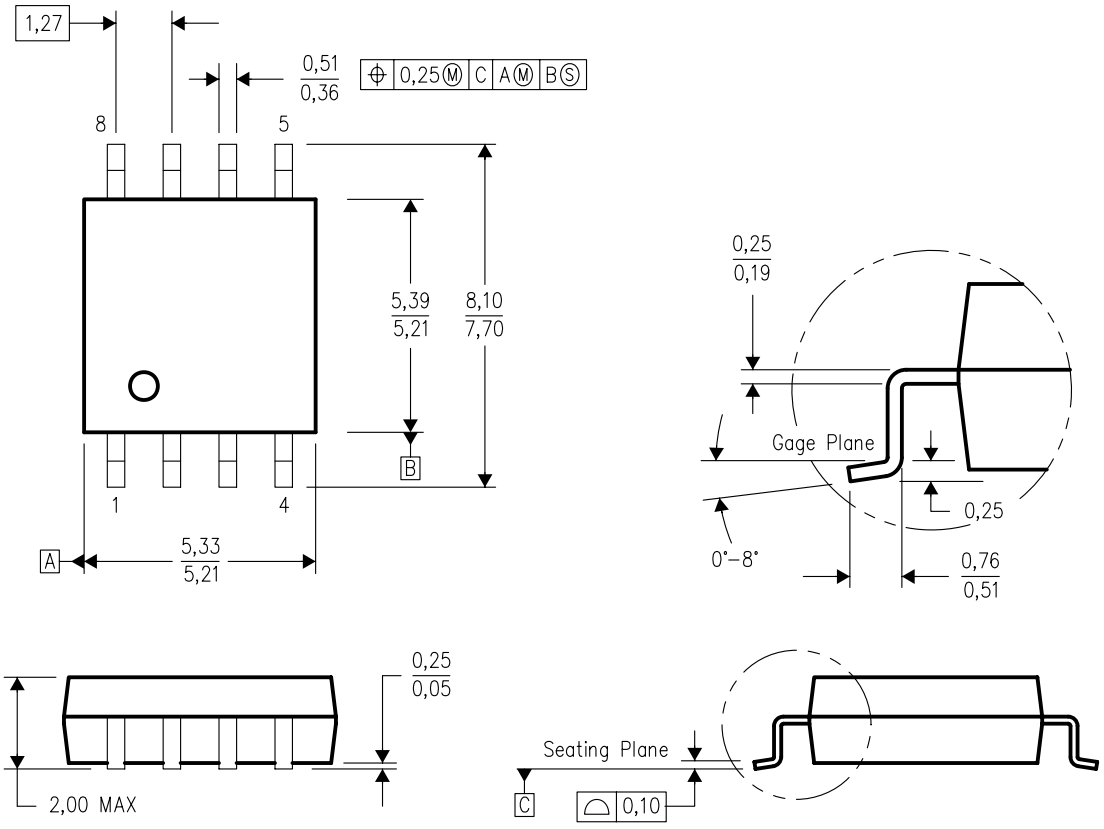
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PSA (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4209043/A 09/07

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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