LM5576/-Q1 SIMPLE SWITCHER® 75V 3A 降压开关稳压器

1 特性

- LM5576-Q1 是一款汽车级产品，符合 AEC-Q100 1 级标准（工作结温范围为 -40°C 至 +125°C）和 AEC-Q100 0 级标准（工作结温范围为 -40°C 至 +150°C）
- 集成了 75V 170mΩ N 沟道金属氧化物半导体场效应晶体管 (MOSFET)
- 超宽输入电压范围：6V 至 75V
- 可调节输出电压低至 1.225V
- 反馈基准精度：1.5% (Q1) 和 1.65% (Q0)
- 可使用单个电阻在 50kHz 至 500kHz 之间调节工作频率
- 主从频率同步
- 可调节软启动
- 仿真的电流模式控制架构
- 宽带宽误差放大器
- 内置保护
- HTSSOP-20EP（外露焊盘）

2 应用范围

- 汽车
- 工业用

3 说明

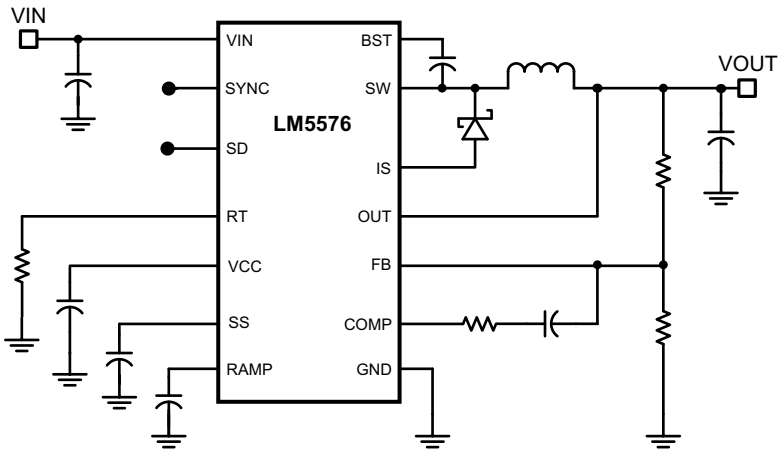
LM5576 是一款易于使用的 SIMPLE SWITCHER®降压稳压器。凭借这款稳压器，设计工程师能够使用最少的元件组设计并优化一个稳健的电源。LM5576 的工作输入电压范围为 6V 至 75V，并且集成有一个 170mΩ N 沟道 MOSFET，可提供 3A 的连续输出电流。该稳压器采用仿真的电流模式架构，兼具固有的线路稳定度、出色的负载瞬态响应以及简化的环路补偿特性，不存在电流模式稳压器中常会出现的低占空比限制。该器件的工作频率可在 50kHz 至 500kHz 范围内进行调节，从而实现解决方案尺寸和效率的最优化。为降低电磁干扰 (EMI)，LM(2)557x 系列的多款 IC 可通过频率同步引脚实现自同步或同步到外部时钟。LM5576 具备逐周期电流限制、短路保护、热关断以及远程关断等特性，能够确保自身的稳健性。该器件采用功耗增强型 HTSSOP-20 封装，特有一个外露芯片连接焊盘用于散热。LM5576 受整套的 WEBENCH®在线设计工具支持。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
LM5576	HTSSOP (20)	6.50mm x 4.40mm
LM5576-Q1		

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

简化应用电路原理图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision I (April 2013) to Revision J **Page**

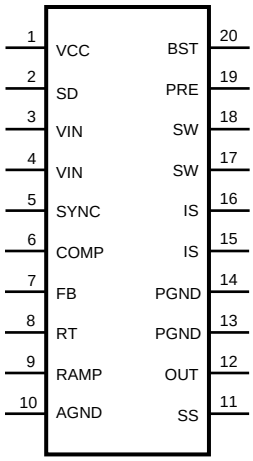
- 已添加 *引脚配置和功能*部分，*处理额定值*表，*特性 描述* 部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1

Changes from Revision H (April 2013) to Revision I **Page**

- Changed layout of National Data Sheet to TI format ... 26

5 Pin Configuration and Functions

20-Pin
HTSSOP Package
Top View



Pin Functions

PIN		I/O	DESCRIPTION	APPLICATION INFORMATION
NO.	NAME			
1	VCC	O	Output of the bias regulator	V_{CC} tracks V_{IN} up to 9 V. Beyond 9 V, V_{CC} is regulated to 7 Volts. A 0.1-uF to 1-uF ceramic decoupling capacitor is required. An external voltage (7.5 V – 14 V) can be applied to this pin to reduce internal power dissipation.
2	SD	I	Shutdown or UVLO input	If the SD pin voltage is below 0.7 V the regulator will be in a low power state. If the SD pin voltage is between 0.7 V and 1.225 V the regulator will be in standby mode. If the SD pin voltage is above 1.225 V the regulator will be operational. An external voltage divider can be used to set a line undervoltage shutdown threshold. If the SD pin is left open circuit, a 5-µA pull-up current source configures the regulator fully operational.
3, 4	V_{IN}	I	Input supply voltage	Nominal operating range: 6 V to 75 V
5	SYNC	I	Oscillator synchronization input or output	The internal oscillator can be synchronized to an external clock with an external pull-down device. Multiple LM5576 devices can be synchronized together by connection of their SYNC pins.
6	COMP	O	Output of the internal error amplifier	The loop compensation network should be connected between this pin and the FB pin.
7	FB	I	Feedback signal from the regulated output	This pin is connected to the inverting input of the internal error amplifier. The regulation threshold is 1.225 V.
8	RT	I	Internal oscillator frequency set input	The internal oscillator is set with a single resistor, connected between this pin and the AGND pin.
9	RAMP	O	Ramp control signal	An external capacitor connected between this pin and the AGND pin sets the ramp slope used for current mode control. Recommended capacitor range 50 pF to 2000 pF.
10	AGND	GROUND	Analog ground	Internal reference for the regulator control functions
11	SS	O	Soft-start	An external capacitor and an internal 10-µA current source set the time constant for the rise of the error amp reference. The SS pin is held low during standby, V_{CC} UVLO and thermal shutdown.
12	OUT	O	Output voltage connection	Connect directly to the regulated output voltage.

Pin Functions (continued)

PIN		I/O	DESCRIPTION	APPLICATION INFORMATION
NO.	NAME			
13, 14	PGND	GROUND	Power ground	Low side reference for the PRE switch and the IS sense resistor.
15, 16	IS	I	Current sense	Current measurement connection for the re-circulating diode. An internal sense resistor and a sample/hold circuit sense the diode current near the conclusion of the off-time. This current measurement provides the DC level of the emulated current ramp.
17, 18	SW	O	Switching node	The source terminal of the internal buck switch. The SW pin should be connected to the external Schottky diode and to the buck inductor.
19	PRE	I	Pre-charge assist for the bootstrap capacitor	This open drain output can be connected to SW pin to aid charging the bootstrap capacitor during very light load conditions or in applications where the output may be pre-charged before the LM5576 is enabled. An internal pre-charge MOSFET is turned on for 265 ns each cycle just prior to the on-time interval of the buck switch.
20	BST	I	Boost input for bootstrap capacitor	An external capacitor is required between the BST and the SW pins. A 0.022-µF ceramic capacitor is recommended. The capacitor is charged from V_{CC} via an internal diode during the off-time of the buck switch.
NA	EP	GROUND	Exposed Pad	Exposed metal pad on the underside of the device. It is recommended to connect this pad to the PWB ground plane, in order to aid in heat dissipation.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
V_{IN} to GND		76	V
BST to GND		90	V
PRE to GND		76	V
SW to GND (Steady State)		–1.5	V
BST to V_{CC}		76	V
SD, V_{CC} to GND		14	V
BST to SW		14	V
OUT to GND	Limited to V_{IN}		
SYNC, SS, FB, RAMP to GND		7	V

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. *Recommended Operating Conditions* are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see the *Electrical Characteristics*.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

6.2 Handling Ratings: LM5576

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)		2	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Handling Ratings: LM5576-Q1

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 (1)		2	kV

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.4 Recommended Operating Conditions

	MIN	MAX	UNIT
V_{IN}	6	75	V
Operation Junction Temperature (Q0)	−40	150	°C
Operation Junction Temperature (Q1)	−40	125	°C

6.5 Thermal Information

THERMAL METRIC (1)		LM5576 PWP 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.6 Electrical Characteristics

Typical values correspond to T_J = 25°C, V_{IN} = 48 V, R_T = 32.4kΩ. Minimum and maximum limits apply over –40°C to 125°C junction temperature range unless otherwise stated. (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STARTUP REGULATOR						
V_{CC} Reg	V_{CC} Regulator Output		6.85	7.15	7.45	V
	V_{CC} LDO Mode turn-off			9		V
	V_{CC} Current Limit	V_{CC} = 0 V		25		mA
VCC SUPPLY						
	V_{CC} UVLO Threshold	(V_{CC} increasing)	5.03	5.35	5.67	V
	V_{CC} Undervoltage Hysteresis			0.25		V
	Bias Current (Iin)	FB = 1.3 V		3.4	4.5	mA
	Shutdown Current (Iin)	SD = 0 V		57	85	µA
SHUTDOWN THRESHOLDS						
	Shutdown Threshold	(SD Increasing)	0.47	0.7	0.9	V
	Shutdown Hysteresis			0.1		V
	Standby Threshold	(Standby Increasing)	1.17	1.225	1.28	V
	Standby Hysteresis			0.1		V
	SD Pull-up Current Source			5		µA
SWITCH CHARACTERISTICS						
	Buck Switch Rds(on) (Q0)			170	380	mΩ
	Buck Switch Rds(on) (Q1)			170	340	mΩ
	BOOST UVLO			3.8		V
	BOOST UVLO Hysteresis			0.56		V
	Pre-charge Switch Rds(on)			70		Ω
	Pre-charge Switch on-time			265		ns
CURRENT LIMIT						
	Cycle by Cycle Current Limit (Q0)	RAMP = 0 V	3.6	4.2	5.5	A

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Texas Instruments' Average Outgoing Quality Level (AOQL).

Electrical Characteristics (continued)

Typical values correspond to T_J = 25°C, V_{IN} = 48 V, R_T = 32.4kΩ. Minimum and maximum limits apply over –40°C to 125°C junction temperature range unless otherwise stated.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Cycle by Cycle Current Limit (Q1)	RAMP = 0 V	3.6	4.2	5.1	A
	Cycle by Cycle Current Limit Delay	RAMP = 2.5 V		100		ns
SOFT-START						
	SS Current Source		7	10	14	µA
OSCILLATOR						
	Frequency1		180	200	220	kHz
	Frequency2	R_T = 11kΩ	425	485	545	kHz
	SYNC Source Impedance			11		kΩ
	SYNC Sink Impedance			110		Ω
	SYNC Threshold (falling)			1.3		V
	SYNC Frequency	R_T = 11kΩ	550			kHz
	SYNC Pulse Width Minimum		15			ns
RAMP GENERATOR						
	Ramp Current 1	V_{IN} = 60 V, V_{OUT}=10 V	235	275	315	µA
	Ramp Current 2	V_{IN} = 10 V, V_{OUT}=10 V	18	25	32	µA
PWM COMPARATOR						
	Forced Off-time (Q0)		390	500	590	ns
	Forced Off-time (Q1)		416	500	575	ns
	Min On-time			80		ns
	COMP to PWM Comparator Offset			0.7		V
ERROR AMPLIFIER						
	Feedback Voltage (Q0)	Vfb = COMP	1.207	1.225	1.243	V
	Feedback Voltage (Q1)	Vfb = COMP	1.207	1.225	1.243	V
	FB Bias Current			17		nA
	DC Gain			70		dB
	COMP Sink / Source Current		3			mA
	Unity Gain Bandwidth			3		MHz
DIODE SENSE RESISTANCE						
D_{SENSE}				42		mΩ
THERMAL SHUTDOWN						
Tsd	Thermal Shutdown Threshold (Q0)			180		°C
Tsd	Thermal Shutdown Threshold (Q1)			165		°C
	Thermal Shutdown Hysteresis			25		°C

6.7 Typical Characteristics

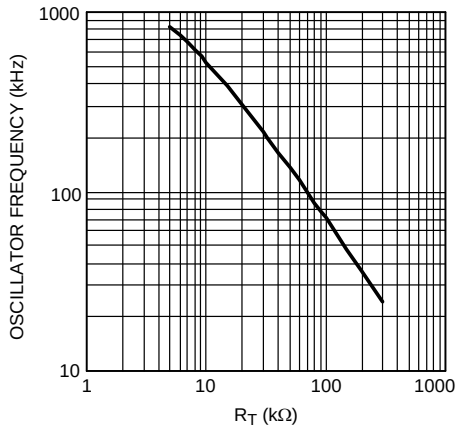


Figure 1. Oscillator Frequency vs R_T

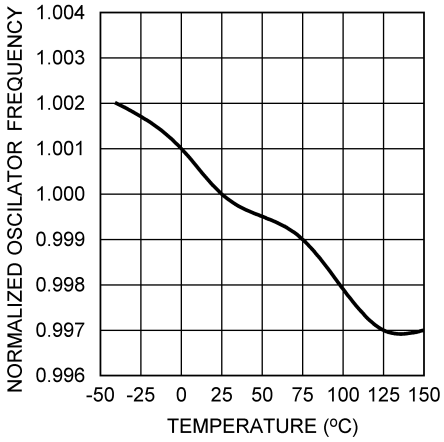


Figure 2. Oscillator Frequency vs Temperature (Q0) F_{OSC} = 200kHz

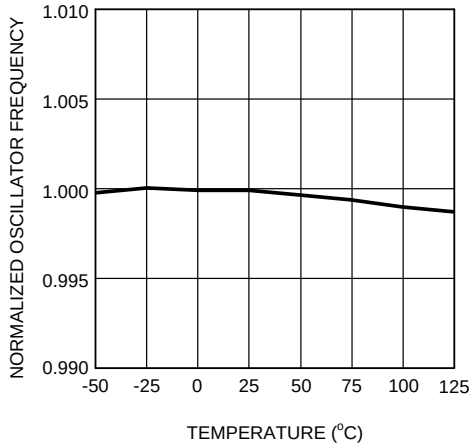


Figure 3. Oscillator Frequency vs Temperature (Q1) F_{OSC} = 200kHz

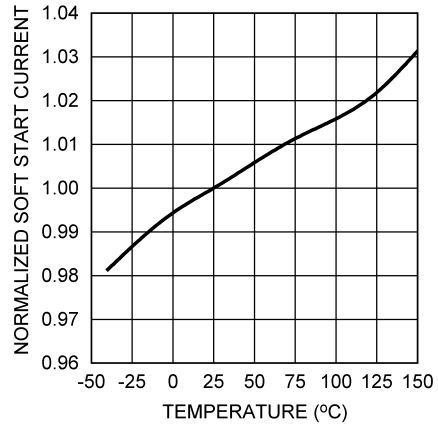


Figure 4. Soft Start Current vs Temperature (Q0)

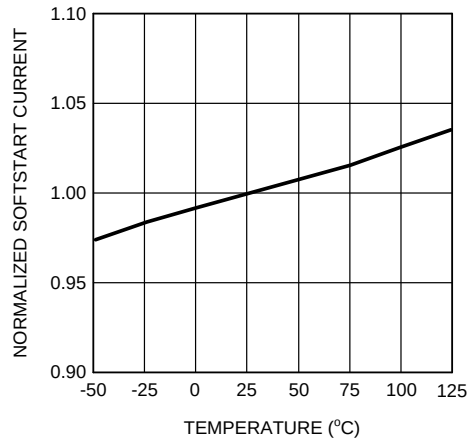


Figure 5. Soft Start Current vs Temperature (Q1)

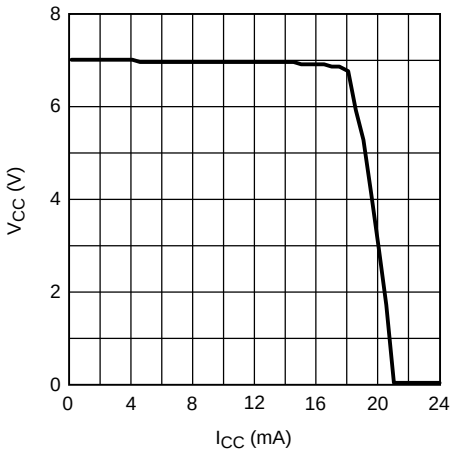


Figure 6. V_{CC} vs I_{CC} V_{IN} = 12 V

Typical Characteristics (continued)

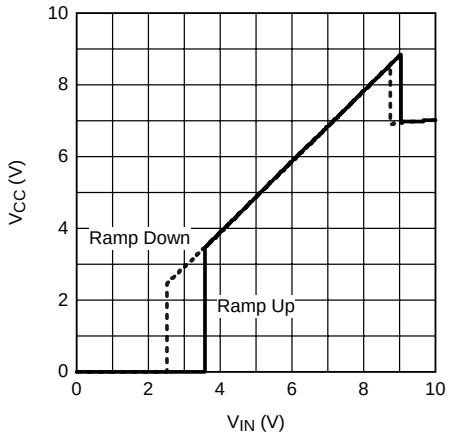


Figure 7. V_{CC} vs V_{IN} R_L = 7kω

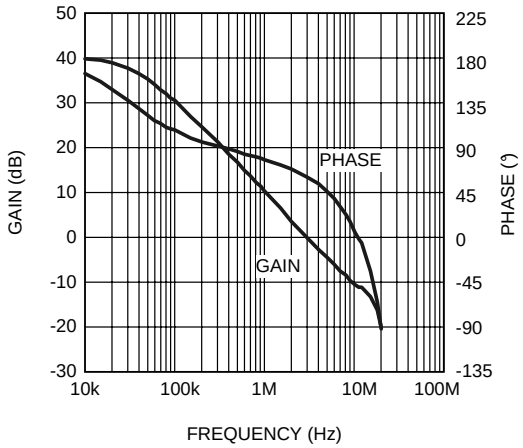


Figure 8. Error Amplifier Gain/Phase AVCL = 101

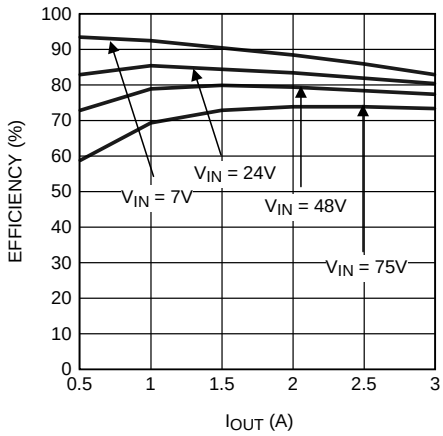


Figure 9. Demoboard Efficiency vs I_{OUT} and V_{IN}

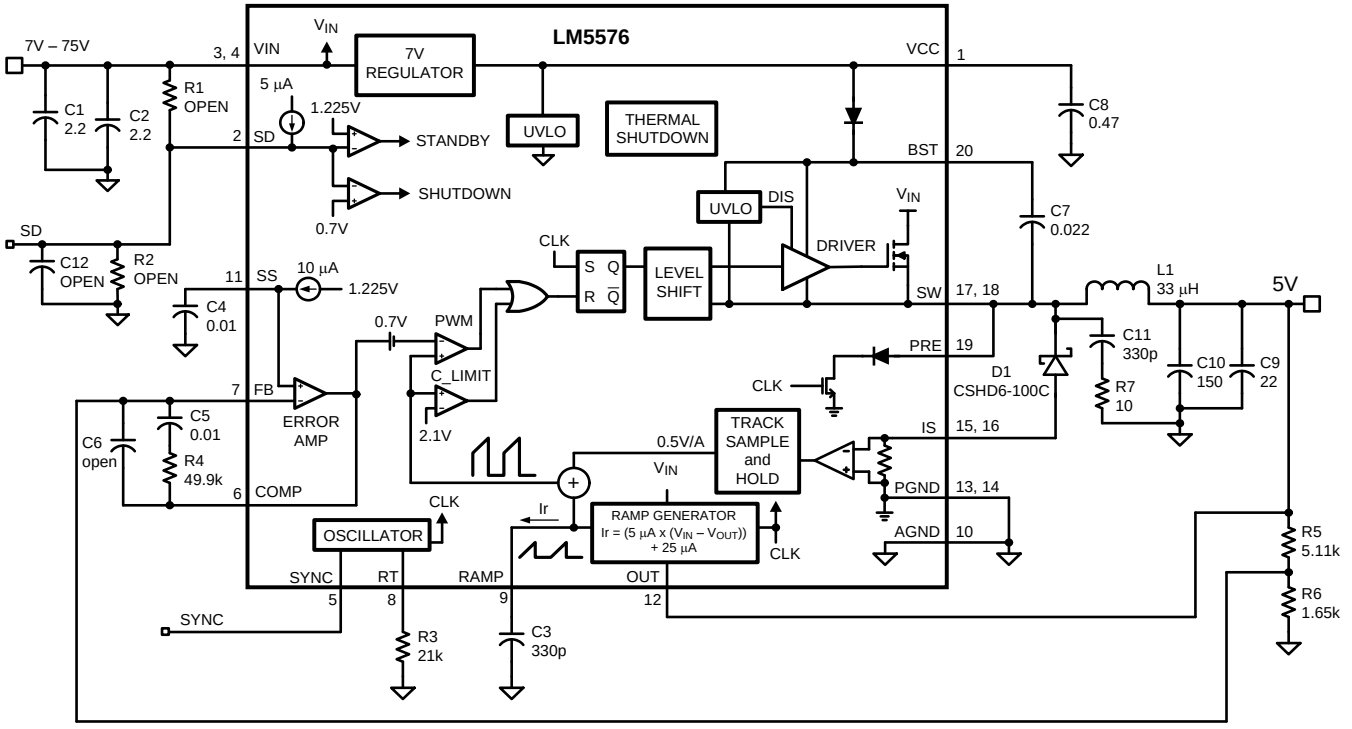
7 Detailed Description

7.1 Overview

The LM5576 switching regulator features all of the functions necessary to implement an efficient high voltage buck regulator using a minimum of external components. This easy to use regulator integrates a 75 V N-Channel buck switch with an output current capability of 3 Amps. The regulator control method is based on current mode control utilizing an emulated current ramp. Peak current mode control provides inherent line voltage feed-forward, cycle-by-cycle current limiting, and ease of loop compensation. The use of an emulated control ramp reduces noise sensitivity of the pulse-width modulation circuit, allowing reliable processing of very small duty cycles necessary in high input voltage applications. The operating frequency is user programmable from 50 kHz to 500 kHz. An oscillator synchronization pin allows multiple LM5576 regulators to self synchronize or be synchronized to an external clock. The output voltage can be set as low as 1.225 V. Fault protection features include, current limiting, thermal shutdown and remote shutdown capability. The device is available in the HTSSOP-20 package featuring an exposed pad to aid thermal dissipation.

The functional block diagram and typical application of the LM5576 are shown in the *Functional Block Diagram* section. The LM5576 can be applied in numerous applications to efficiently step-down a high, unregulated input voltage. The device is well suited for telecom, industrial and automotive power bus voltage ranges.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Shutdown / Standby

The LM5576 contains a dual level Shutdown (SD) circuit. When the SD pin voltage is below 0.7 V, the regulator is in a low current shutdown mode. When the SD pin voltage is greater than 0.7 V but less than 1.225 V, the regulator is in standby mode. In standby mode the V_{CC} regulator is active but the output switch is disabled. When the SD pin voltage exceeds 1.225 V, the output switch is enabled and normal operation begins. An internal 5 µA pull-up current source configures the regulator to be fully operational if the SD pin is left open.

Feature Description (continued)

An external set-point voltage divider from VIN to GND can be used to set the operational input range of the regulator. The divider must be designed such that the voltage at the SD pin will be greater than 1.225 V when V_{IN} is in the desired operating range. The internal 5 µA pull-up current source must be included in calculations of the external set-point divider. Hysteresis of 0.1 V is included for both the shutdown and standby thresholds. The SD pin is internally clamped with a 1 kΩ resistor and an 8 V zener clamp. The voltage at the SD pin should never exceed 14 V. If the voltage at the SD pin exceeds 8 V, the bias current will increase at a rate of 1 mA/V.

The SD pin can also be used to implement various remote enable / disable functions. Pulling the SD pin below the 0.7 V threshold totally disables the controller. If the SD pin voltage is above 1.225 V the regulator will be operational.

7.3.2 Soft-Start

The soft-start feature allows the regulator to gradually reach the initial steady state operating point, thus reducing start-up stresses and surges. The internal soft-start current source, set to 10 µA, gradually increases the voltage of an external soft-start capacitor connected to the SS pin. The soft-start capacitor voltage is connected to the reference input of the error amplifier. Various sequencing and tracking schemes can be implemented using external circuits that limit or clamp the voltage level of the SS pin.

In the event a fault is detected (over-temperature, V_{CC} UVLO, SD) the soft-start capacitor will be discharged. When the fault condition is no longer present a new soft-start sequence will commence.

7.3.3 Thermal Protection

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event the maximum junction temperature is exceeded. When activated, typically at 165°C (Q1 version) and 180°C (Q0 version), the controller is forced into a low power reset state, disabling the output driver and the bias regulator. This feature is provided to prevent catastrophic failures from accidental device overheating.

7.4 Device Functional Modes

7.4.1 High Voltage Start-Up Regulator

The LM5576 contains a dual-mode internal high voltage startup regulator that provides the $_{CC}$ bias supply for the PWM controller and boot-strap MOSFET gate driver. The input pin (VIN) can be connected directly to the input voltage, as high as 75 Volts. For input voltages below 9 V, a low dropout switch connects V_{CC} directly to V_{IN}. In this supply range, V_{CC} is approximately equal to V_{IN}. For V_{IN} voltage greater than 9 V, the low dropout switch is disabled and the V_{CC} regulator is enabled to maintain V_{CC} at approximately 7 V. The wide operating range of 6 V to 75 V is achieved through the use of this dual mode regulator.

The output of the V_{CC} regulator is current limited to 25 mA. Upon power up, the regulator sources current into the capacitor connected to the VCC pin. When the voltage at the VCC pin exceeds the V_{CC} UVLO threshold of 5.35 V and the SD pin is greater than 1.225 V, the output switch is enabled and a soft-start sequence begins. The output switch remains enabled until V_{CC} falls below 5.0 V or the SD pin falls below 1.125 V.

An auxiliary supply voltage can be applied to the VCC pin to reduce the IC power dissipation. If the auxiliary voltage is greater than 7.3 V, the internal regulator will essentially shut off, reducing the IC power dissipation. The V_{CC} regulator series pass transistor includes a diode between V_{CC} and V_{IN} that should not be forward biased in normal operation. Therefore the auxiliary V_{CC} voltage should never exceed the V_{IN} voltage.

In high voltage applications extra care should be taken to ensure the VIN pin does not exceed the absolute maximum voltage rating of 76 V. During line or load transients, voltage ringing on the V_{IN} line that exceeds the Absolute Maximum Ratings can damage the IC. Both careful PC board layout and the use of quality bypass capacitors located close to the VIN and GND pins are essential.

Device Functional Modes (continued)

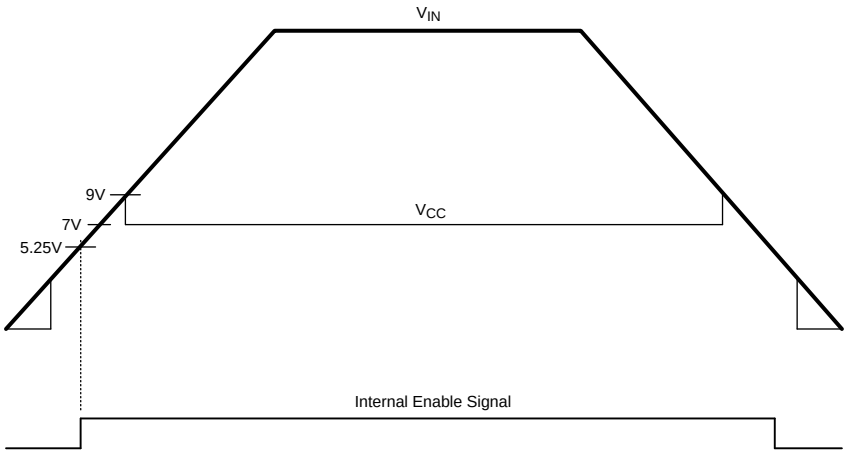


Figure 10. V_{IN} and V_{CC} Sequencing

7.4.2 Oscillator and Sync Capability

The LM5576 oscillator frequency is set by a single external resistor connected between the RT pin and the AGND pin. The R_T resistor should be located very close to the device and connected directly to the pins of the IC (RT and AGND).To set a desired oscillator frequency (F), the necessary value for the R_T resistor can be calculated from the following equation:

$$R_T = \frac{\frac{1}{F} - 580 \times 10^{-9}}{135 \times 10^{-12}} \quad (1)$$

The SYNC pin can be used to synchronize the internal oscillator to an external clock. The external clock must be of **higher frequency** than the free-running frequency set by the R_T resistor. A clock circuit with an open drain output is the recommended interface from the external clock to the SYNC pin. The clock pulse duration should be greater than 15 ns.

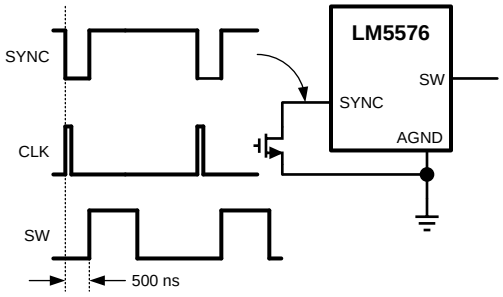


Figure 11. Sync From External Clock

Device Functional Modes (continued)

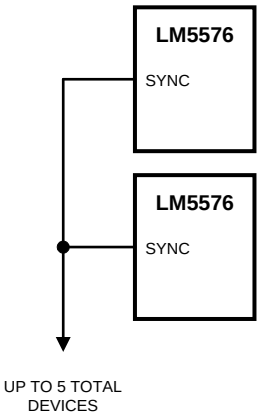


Figure 12. Sync From Multiple Devices

Multiple LM5576 devices can be synchronized together simply by connecting the SYNC pins together. In this configuration all of the devices will be synchronized to the highest frequency device. The diagram in Figure 13 illustrates the SYNC input/output features of the LM5576. The internal oscillator circuit drives the SYNC pin with a strong pull-down / weak pull-up inverter. When the SYNC pin is pulled low either by the internal oscillator or an external clock, the ramp cycle of the oscillator is terminated and a new oscillator cycle begins. Thus, if the SYNC pins of several LM5576 ICs are connected together, the IC with the highest internal clock frequency will pull the connected SYNC pins low first and terminate the oscillator ramp cycles of the other ICs. The LM5576 with the highest programmed clock frequency will serve as the master and control the switching frequency of the all the devices with lower oscillator frequency.

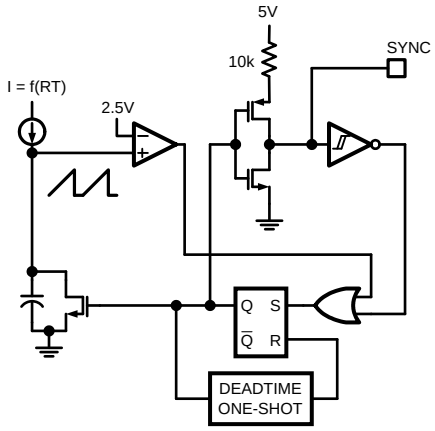


Figure 13. Simplified Oscillator Block Diagram and Sync I/O Circuit

7.4.3 Error Amplifier and PWM Comparator

The internal high gain error amplifier generates an error signal proportional to the difference between the regulated output voltage and an internal precision reference (1.225 V). The output of the error amplifier is connected to the COMP pin allowing the user to provide loop compensation components, generally a type II network, as illustrated in the *Functional Block Diagram* section. This network creates a pole at DC, a zero and a noise reducing high frequency pole. The PWM comparator compares the emulated current sense signal from the RAMP generator to the error amplifier output voltage at the COMP pin.

Device Functional Modes (continued)

7.4.4 Ramp Generator

The ramp signal used in the pulse width modulator for current mode control is typically derived directly from the buck switch current. This switch current corresponds to the positive slope portion of the output inductor current. Using this signal for the PWM ramp simplifies the control loop transfer function to a single pole response and provides inherent input voltage feed-forward compensation. The disadvantage of using the buck switch current signal for PWM control is the large leading edge spike due to circuit parasitics that must be filtered or blanked. Also, the current measurement may introduce significant propagation delays. The filtering, blanking time and propagation delay limit the minimum achievable pulsewidth. In applications where the input voltage may be relatively large in comparison to the output voltage, controlling small pulsewidths and duty cycles is necessary for regulation. The LM5576 utilizes a unique ramp generator, which does not actually measure the buck switch current but rather reconstructs the signal. Reconstructing or emulating the inductor current provides a ramp signal to the PWM comparator that is free of leading edge spikes and measurement or filtering delays. The current reconstruction is comprised of two elements; a sample & hold DC level and an emulated current ramp.

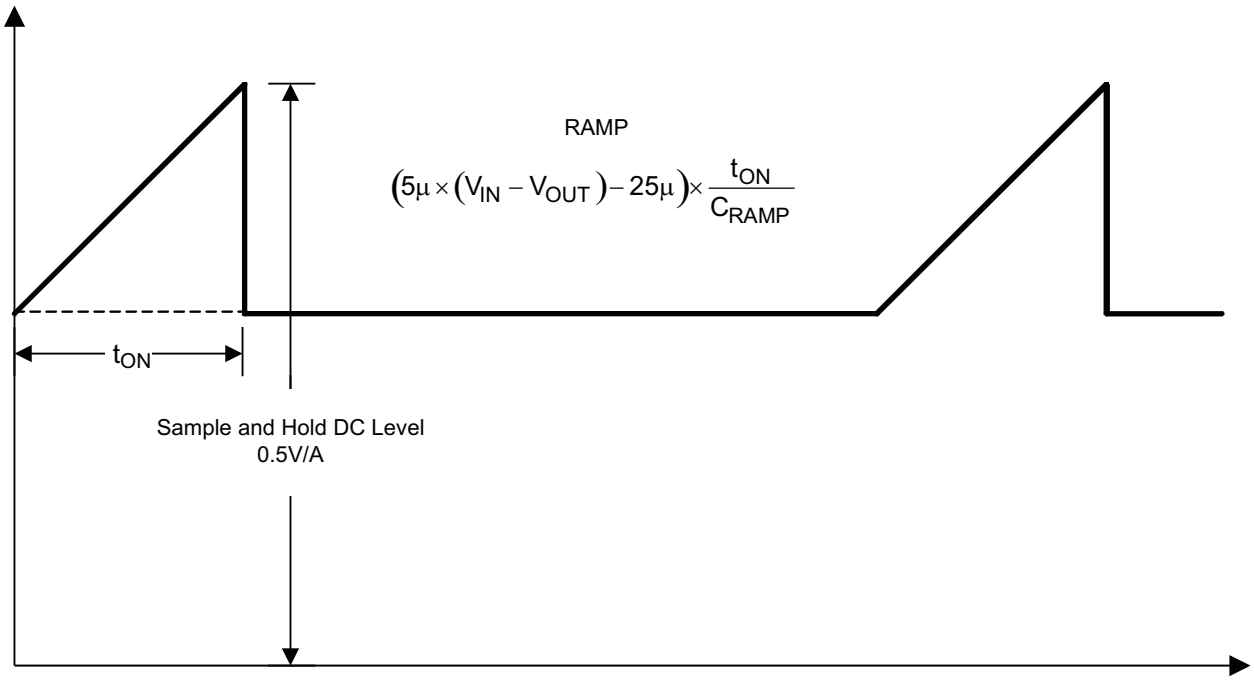


Figure 14. Composition of Current Sense Signal

The sample & hold DC level illustrated in Figure 14 is derived from a measurement of the re-circulating Schottky diode anode current. The re-circulating diode anode should be connected to the IS pin. The diode current flows through an internal current sense resistor between the IS and PGND pins. The voltage level across the sense resistor is sampled and held just prior to the onset of the next conduction interval of the buck switch. The diode current sensing and sample & hold provide the DC level of the reconstructed current signal. The positive slope inductor current ramp is emulated by an external capacitor connected from the RAMP pin to AGND and an internal voltage controlled current source. The ramp current source that emulates the inductor current is a function of the V_{IN} and V_{OUT} voltages per Equation 2:

$$I_{RAMP} = (5\ \mu \text{ x } (V_{IN} - V_{OUT})) + 25\ \mu A \quad (2)$$

Proper selection of the RAMP capacitor depends upon the selected value of the output inductor. The value of C_{RAMP} can be selected from:

$$C_{RAMP} = L \text{ x } 10^{-5} \quad (3)$$

where

- L is the value of the output inductor in Henrys

Device Functional Modes (continued)

With this value, the scale factor of the emulated current ramp will be approximately equal to the scale factor of the DC level sample and hold (0.5 V / A). The C_{RAMP} capacitor should be located very close to the device and connected directly to the pins of the IC (RAMP and AGND).

For duty cycles greater than 50%, peak current mode control circuits are subject to sub-harmonic oscillation. Sub-harmonic oscillation is normally characterized by observing alternating wide and narrow pulses at the switch node. Adding a fixed slope voltage ramp (slope compensation) to the current sense signal prevents this oscillation. The 25 µA of offset current provided from the emulated current source adds some fixed slope to the ramp signal. In some high output voltage, high duty cycle applications, additional slope may be required. In these applications, a pull-up resistor may be added between the V_{CC} and RAMP pins to increase the ramp slope compensation.

For V_{OUT} > 7.5 V:

Calculate optimal slope current, $I_{OS} = V_{OUT}$ x 5 µA/V.

For example, at V_{OUT} = 10 V, I_{OS} = 50 µA.

Install a resistor from the RAMP pin to V_{CC}:

$R_{RAMP} = V_{CC} / (I_{OS} - 25\ \mu A)$ (4)

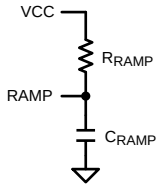


Figure 15. R_{RAMP} to V_{CC} for V_{OUT} > 7.5 V

Note that the emulated ramp signal on C_{RAMP} is applied to the current limit comparator as described in the Current Limit section below. Increasing the ramp slope will result in lower current limit threshold. This can lower the output current capability of the part to less than 3 A in some conditions. The resulting current limit threshold can be calculated by the following equation:

$$I_{CL} = \frac{V_{CL} - \frac{\left[\left(V_{IN} - V_{OUT}\right) \times g_m + Ioffset + \frac{Vcc}{R_{RAMP}}\right] \times D \times T}{C_{RAMP}}}{A \times Rs} + \frac{1}{2}\left[\frac{V_{OUT} \times T \times \left(1 - D\right)}{L}\right]$$

where

- V_{CL} = 2.1 V
- gm = 5 µA/V
- Ioffset = 25 µA
- A x Rs = 0.5 V/A
- V_{CC} = 7 V
- T = switching period
- D = duty cycle (approximately V_{OUT} / V_{IN})
- L = inductor value
- C_{RAMP} = ramp capacitor value
- R_{RAMP} = ramp resistor value (5)

If the recommended C_{RAMP} and R_{RAMP} values are used, then the following simplified equation calculates the current limit threshold:

Device Functional Modes (continued)

$$I_{CL} = \frac{V_{CL}}{A \times R_S} - \frac{1}{2}\left[\frac{V_{OUT} \times T \times (1+D)}{L}\right] \quad (6)$$

7.4.5 Maximum Duty Cycle / Input Drop-Out Voltage

There is a forced off-time of 500 ns implemented each cycle to ensure sufficient time for the diode current to be sampled. This forced off-time limits the maximum duty cycle of the buck switch. The maximum duty cycle will vary with the operating frequency.

D_{MAX} = 1 - Fs x 500ns

where

- Fs is the oscillator frequency (7)

Limiting the maximum duty cycle will raise the input dropout voltage. The input dropout voltage is the lowest input voltage required to maintain regulation of the output voltage. An approximation of the input dropout voltage is:

$$Vin_{MIN} = \frac{Vout + V_D}{1 - Fs \times 500\ ns}$$

where

- V_D is the voltage drop across the re-circulatory diode (8)

Operating at high switching frequency raises the minimum input voltage necessary to maintain regulation.

7.4.6 Boost Pin

The LM5576 integrates an N-Channel buck switch and associated floating high voltage level shift / gate driver. This gate driver circuit works in conjunction with an internal diode and an external bootstrap capacitor. A 0.022 µF ceramic capacitor, connected with short traces between the BST pin and SW pin, is recommended. During the off-time of the buck switch, the SW pin voltage is approximately -0.5 V and the bootstrap capacitor is charged from V_{CC} through the internal bootstrap diode. When operating with a high PWM duty cycle, the buck switch will be forced off each cycle for 500 ns to ensure that the bootstrap capacitor is recharged.

Under very light load conditions or when the output voltage is pre-charged, the SW voltage will not remain low during the off-time of the buck switch. If the inductor current falls to zero and the SW pin rises, the bootstrap capacitor will not receive sufficient voltage to operate the buck switch gate driver. For these applications, the PRE pin can be connected to the SW pin to pre-charge the bootstrap capacitor. The internal pre-charge MOSFET and diode connected between the PRE pin and PGND turns on each cycle for 265 ns just prior to the onset of a new switching cycle. If the SW pin is at a normal negative voltage level (continuous conduction mode), then no current will flow through the pre-charge MOSFET/diode. For output voltages above 5 V, a minimum load current may still be required to ensure that the SW voltage is pulled low enough to recharge the bootstrap capacitor.

7.4.7 Current Limit

The LM5576 contains a unique current monitoring scheme for control and over-current protection. When set correctly, the emulated current sense signal provides a signal which is proportional to the buck switch current with a scale factor of 0.5 V / A. The emulated ramp signal is applied to the current limit comparator. If the emulated ramp signal exceeds 2.1 V (4.2 A) the present current cycle is terminated (cycle-by-cycle current limiting). In applications with small output inductance and high input voltage the switch current may overshoot due to the propagation delay of the current limit comparator. If an overshoot should occur, the diode current sampling circuit will detect the excess inductor current during the off-time of the buck switch. If the sample & hold DC level exceeds the 2.1 V current limit threshold, the buck switch will be disabled and skip pulses until the diode current sampling circuit detects the inductor current has decayed below the current limit threshold. This approach prevents current runaway conditions due to propagation delays or inductor saturation since the inductor current is forced to decay following any current overshoot.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Bias Power Dissipation Reduction

Buck regulators operating with high input voltage can dissipate an appreciable amount of power for the bias of the IC. The V_{CC} regulator must step-down the input voltage V_{IN} to a nominal V_{CC} level of 7 V. The large voltage drop across the V_{CC} regulator translates into a large power dissipation within the regulator. There are several techniques that can significantly reduce this bias regulator power dissipation. Figure 16 and V_{CC} Figure 17 depict two methods to bias the IC from the output voltage. In each case the internal V_{CC} regulator is used to initially bias the VCC pin. After the output voltage is established, the VCC pin potential is raised above the nominal 7 V regulation level, which effectively disables the internal V_{CC} regulator. The voltage applied to the VCC pin should never exceed 14 V. The V_{CC} voltage should never be larger than the V_{IN} voltage.

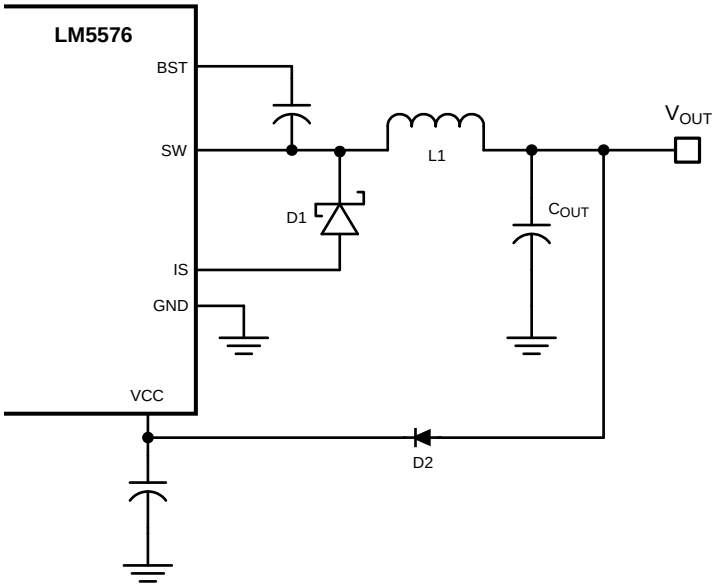


Figure 16. V_{CC} Bias From V_{OUT} for 8 V < V_{OUT} < 14 V

Application Information (continued)

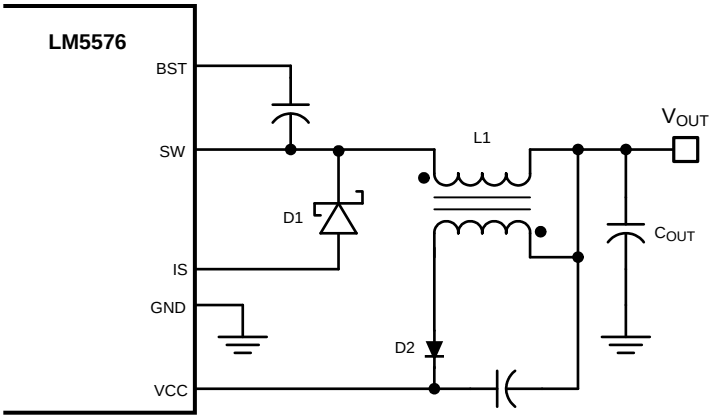


Figure 17. V_{CC} Bias With Additional Winding on the Output Inductor

8.2 Typical Application

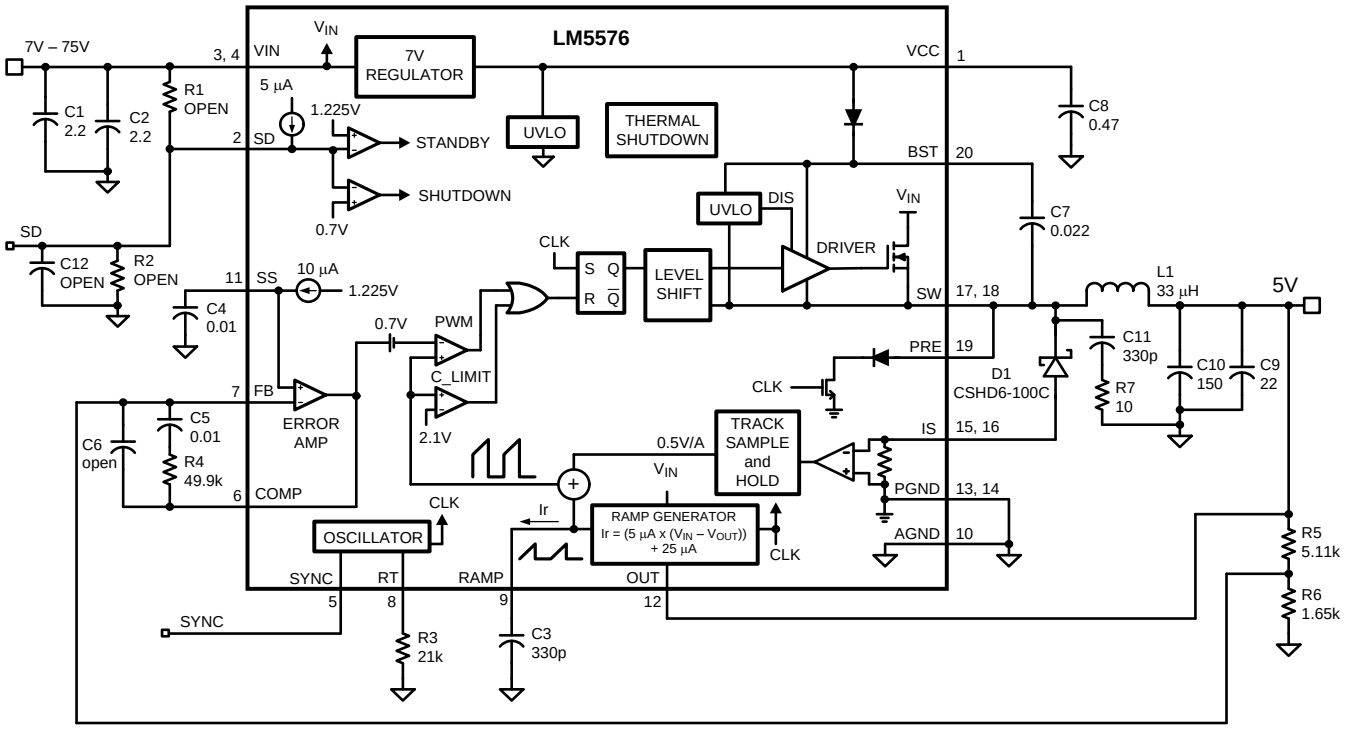


Figure 18. Typical Application

8.2.1 Design Requirements

The circuit shown in Figure 18 is configured for the following specifications:

- V_{OUT} = 5 V
- V_{IN} = 7 V to 75 V
- Fs = 300 kHz
- Minimum load current (for CCM) = 250 mA
- Maximum load current = 3 A

Typical Application (continued)

8.2.2 Detailed Design Procedure

8.2.2.1 External Components

The procedure for calculating the external components is illustrated with the following design example. The Bill of Materials for this design is listed in Table 1.

Table 1. 5 V, 3 A Demo Board Bill of Materials

ITEM		PART NUMBER	DESCRIPTION	VALUE
C	1	C4532X7R2A225M	CAPACITOR, CER, TDK	2.2 µ, 100 V
C	2	C4532X7R2A225M	CAPACITOR, CER, TDK	2.2 µ, 100 V
C	3	C0805C331G1GAC	CAPACITOR, CER, KEMET	330 p, 100 V
C	4	C2012X7R2A103K	CAPACITOR, CER, TDK	0.01 µ, 100 V
C	5	C2012X7R2A103K	CAPACITOR, CER, TDK	0.01 µ, 100 V
C	6	OPEN	NOT USED	
C	7	C2012X7R2A223K	CAPACITOR, CER, TDK	0.022 µ, 100 V
C	8	C2012X7R1C474M	CAPACITOR, CER, TDK	0.47 µ, 16 V
C	9	C3225X7R1C226M	CAPACITOR, CER, TDK	22 µ, 16 V
C	10	EEFHE0J151R	CAPACITOR, SP, PANASONIC	150 µ, 6.3 V
C	11	C0805C331G1GAC	CAPACITOR, CER, KEMET	330 p, 100 V
C	12	OPEN	NOT USED	
D	1	CSHD6-100C	DIODE, 100V, CENTRAL	
		6CWQ10FN	DIODE, 100V, IR (D1-ALT)	
L	1	DR127-330	INDUCTOR, COOPER	33 µH
R	1	OPEN	NOT USED	
R	2	OPEN	NOT USED	
R	3	CRCW08052102F	RESISTOR	21 kΩ
R	4	CRCW08054992F	RESISTOR	49.9 kΩ
R	5	CRCW08055111F	RESISTOR	5.11 kΩ
R	6	CRCW08051651F	RESISTOR	1.65 kΩ
R	7	CRCW2512100J	RESISTOR	10, 1 W
U	1	LM5576	REGULATOR, TEXAS INSTRUMENTS	

8.2.2.2 R3 (R_T)

R_T sets the oscillator switching frequency. Generally, higher frequency applications are smaller but have higher losses. Operation at 300 kHz was selected for this example as a reasonable compromise for both small size and high efficiency. The value of R_T for 300 kHz switching frequency can be calculated as follows:

$$R_T = \frac{\left(\left(\frac{1}{300 \times 10^3}\right) - 580 \times 10^{-9}\right)}{135 \times 10^{-12}} \quad (9)$$

The nearest standard value of 21 kΩ was chosen for R_T.

8.2.2.3 L1

The inductor value is determined based on the operating frequency, load current, ripple current, and the minimum and maximum input voltage ($V_{IN(min)}$, $V_{IN(max)}$).

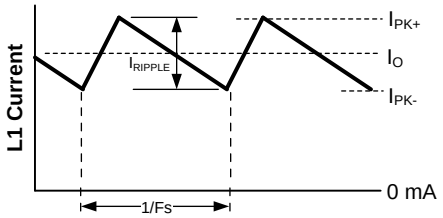


Figure 19. Inductor Current Waveform

To keep the circuit in continuous conduction mode (CCM), the maximum ripple current I_{RIPPLE} should be less than twice the minimum load current, or 0.5 Ap-p. Using this value of ripple current, the value of inductor (L1) is calculated using the following:

$$L1 = \frac{V_{OUT} \times \left(V_{IN(max)} - V_{OUT}\right)}{I_{RIPPLE} \times F_S \times V_{IN(max)}} \tag{10}$$

$$L1 = \frac{5V \text{ x } (75V - 5V)}{0.5A \text{ x } 300 \text{ kHz x } 75V} = 31\ \mu H \tag{11}$$

This procedure provides a guide to select the value of L1. The nearest standard value (33 µH) will be used. L1 must be rated for the peak current (I_{PK+}) to prevent saturation. During normal loading conditions, the peak current occurs at maximum load current plus maximum ripple. During an overload condition the peak current is limited to 4.2 A nominal (5.1 A maximum). The selected inductor (see Table 1) has a conservative 6.2 Amp saturation current rating. For this manufacturer, the saturation rating is defined as the current necessary for the inductance to reduce by 30%, at 20°C.

8.2.2.4 C3 (C_{RAMP})

With the inductor value selected, the value of C3 (C_{RAMP}) necessary for the emulation ramp circuit is:

$$C_{RAMP} = L \text{ x } 10^{-5} \tag{12}$$

Where:

L is in Henrys

With L1 selected for 33 µH the recommended value for C3 is 330 pF.

8.2.2.5 C9, C10

The output capacitors, C9 and C10, smooth the inductor ripple current and provide a source of charge for transient loading conditions. For this design a 22-µF ceramic capacitor and a 150-µF SP organic capacitor were selected. The ceramic capacitor provides ultra low ESR to reduce the output ripple voltage and noise spikes, while the SP capacitor provides a large bulk capacitance in a small volume for transient loading conditions. An approximation for the output ripple voltage is:

$$\Delta V_{OUT} = \Delta I_L \text{ x } \left(ESR + \frac{1}{8 \text{ x } F_S \text{ x } C_{OUT}}\right) \tag{13}$$

8.2.2.6 D1

A Schottky type re-circulating diode is required for all LM5576 applications. Ultra-fast diodes are not recommended and may result in damage to the IC due to reverse recovery current transients. The near ideal reverse recovery characteristics and low forward voltage drop are particularly important diode characteristics for high input voltage and low output voltage applications common to the LM5576. The reverse recovery characteristic determines how long the current surge lasts each cycle when the buck switch is turned on. The reverse recovery characteristics of Schottky diodes minimize the peak instantaneous power in the buck switch occurring during turn-on each cycle. The resulting switching losses of the buck switch are significantly reduced when using a Schottky diode. The reverse breakdown rating should be selected for the maximum V_{IN}, plus some safety margin.

The forward voltage drop has a significant impact on the conversion efficiency, especially for applications with a low output voltage. “Rated” current for diodes vary widely from various manufacturers. The worst case is to assume a short circuit load condition. In this case the diode will carry the output current almost continuously. For the LM5576 this current can be as high as 4.2 A. Assuming a worst case 1 V drop across the diode, the maximum diode power dissipation can be as high as 4.2 W. For the reference design a 100 V Schottky in a DPAK package was selected.

8.2.2.7 C1, C2

The regulator supply voltage has a large source impedance at the switching frequency. Good quality input capacitors are necessary to limit the ripple voltage at the VIN pin while supplying most of the switch current during the on-time. When the buck switch turns on, the current into the VIN pin steps to the lower peak of the inductor current waveform, ramps up to the peak value, then drops to zero at turn-off. The average current into VIN during the on-time is the load current. The input capacitance should be selected for RMS current rating and minimum ripple voltage. A good approximation for the required ripple current rating necessary is $I_{RMS} > I_{OUT} / 2$.

Quality ceramic capacitors with a low ESR should be selected for the input filter. To allow for capacitor tolerances and voltage effects, two 2.2-µF, 100 V ceramic capacitors will be used. If step input voltage transients are expected near the maximum rating of the LM5576, a careful evaluation of ringing and possible spikes at the device VIN pin should be completed. An additional damping network or input voltage clamp may be required in these cases.

8.2.2.8 C8

The capacitor at the VCC pin provides noise filtering and stability for the V_{CC} regulator. The recommended value of C8 should be no smaller than 0.1-µF, and should be a good quality, low ESR, ceramic capacitor. A value of 0.47-µF was selected for this design.

8.2.2.9 C7

The bootstrap capacitor between the BST and the SW pins supplies the gate current to charge the buck switch gate at turn-on. The recommended value of C7 is 0.022-µF, and should be a good quality, low ESR, ceramic capacitor.

8.2.2.10 C4

The capacitor at the SS pin determines the soft-start time, i.e. the time for the reference voltage and the output voltage, to reach the final regulated value. The time is determined from:

$$t_{SS} = \frac{C4 \times 1.225\,V}{10\,\mu A} \tag{14}$$

For this application, a C4 value of 0.01-µF was chosen which corresponds to a soft-start time of 1 ms.

8.2.2.11 R5, R6

R5 and R6 set the output voltage level, the ratio of these resistors is calculated from:

$$R5/R6 = (V_{OUT} / 1.225\ V) - 1 \tag{15}$$

For a 5 V output, the R5/R6 ratio calculates to 3.082. The resistors should be chosen from standard value resistors, a good starting point is selection in the range of 1.0 kΩ - 10 kΩ. Values of 5.11 kΩ for R5, and 1.65 kΩ for R6 were selected.

8.2.2.12 R1, R2, C12

A voltage divider can be connected to the SD pin to set a minimum operating voltage $V_{IN(min)}$ for the regulator. If this feature is required, the easiest approach to select the divider resistor values is to select a value for R1 (between 10 kΩ and 100 kΩ recommended) then calculate R2 from:

$$R2 = 1.225 \times \left(\frac{R1}{V_{IN(min)} + (5 \times 10^{-6} \times R1) - 1.225} \right) \quad (16)$$

Capacitor C12 provides filtering for the divider. The voltage at the SD pin should never exceed 8 V, when using an external set-point divider it may be necessary to clamp the SD pin at high input voltage conditions. The reference design utilizes the full range of the LM5576 (6V to 75V); therefore these components can be omitted. With the SD pin open circuit the LM5576 responds once the V_{CC} UVLO threshold is satisfied.

8.2.2.13 R7, C11

A snubber network across the power diode reduces ringing and spikes at the switching node. Excessive ringing and spikes can cause erratic operation and couple spikes and noise to the output. Voltage spikes beyond the rating of the LM5576 or the re-circulating diode can damage these devices. Selecting the values for the snubber is best accomplished through empirical methods. First, make sure the lead lengths for the snubber connections are very short. For the current levels typical for the LM5576 a resistor value between 5 and 20 Ohms is adequate. Increasing the value of the snubber capacitor results in more damping but higher losses. Select a minimum value of C11 that provides adequate damping of the SW pin waveform at high load.

8.2.2.14 R4, C5, C6

These components configure the error amplifier gain characteristics to accomplish a stable overall loop gain. One advantage of current mode control is the ability to close the loop with only two feedback components, R4 and C5. The overall loop gain is the product of the modulator gain and the error amplifier gain. The DC modulator gain of the LM5576 is as follows:

$$DC\ Gain_{(MOD)} = G_{m(MOD)} \times R_{LOAD} = 2 \times R_{LOAD} \quad (17)$$

The dominant low frequency pole of the modulator is determined by the load resistance (R_{LOAD},) and output capacitance (C_{OUT}). The corner frequency of this pole is:

$$f_{p(MOD)} = 1 / (2\pi\ R_{LOAD}\ C_{OUT}) \quad (18)$$

For R_{LOAD} = 5 Ω and C_{OUT} = 177 µF then $f_{p(MOD)}$ = 180 Hz

$DC\ Gain_{(MOD)}$ = 2 x 5 = 10 = 20 dB

For the design example of Figure 18 the following modulator gain vs. frequency characteristic was measured as shown in Figure 20.

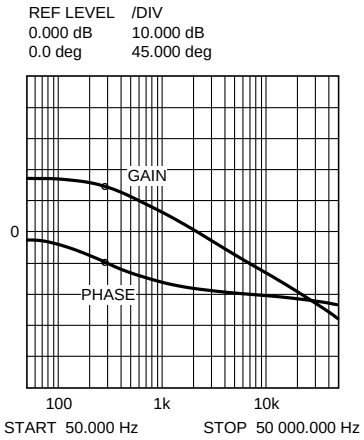


Figure 20. Gain and Phase of Modulator R = 5 Ohms and C = 177 µF Loadout

Components R4 and C5 configure the error amplifier as a type II configuration which has a pole at DC and a zero at f_Z = 1 / (2πR4C5). The error amplifier zero cancels the modulator pole leaving a single pole response at the crossover frequency of the loop gain. A single pole response at the crossover frequency yields a very stable loop with 90 degrees of phase margin.

For the design example, a target loop bandwidth (crossover frequency) of 20 kHz was selected. The compensation network zero (f_Z) should be selected at least an order of magnitude less than the target crossover frequency. This constrains the product of R4 and C5 for a desired compensation network zero 1 / (2π R4 C5) to be less than 2 kHz. Increasing R4, while proportionally decreasing C5, increases the error amp gain. Conversely, decreasing R4 while proportionally increasing C5, decreases the error amp gain. For the design example C5 was selected for 0.01-µF and R4 was selected for 49.9 kΩ. These values configure the compensation network zero at 320 Hz. The error amp gain at frequencies greater than f_Z is: R4 / R5, which is approximately 10 (20 dB).

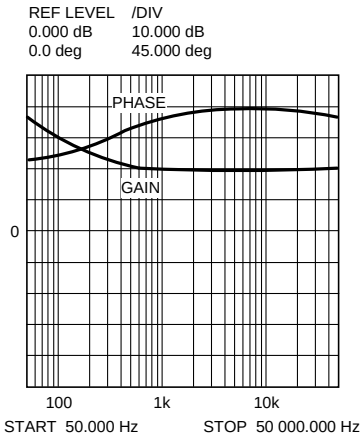


Figure 21. Error Amplifier Gain and Phase

The overall loop can be predicted as the sum (in dB) of the modulator gain and the error amp gain.

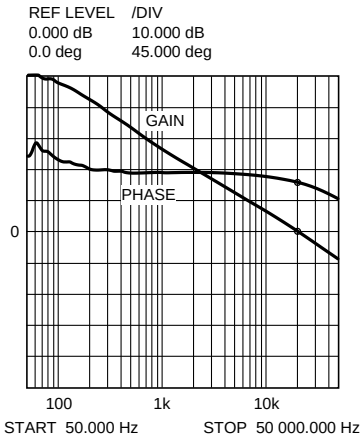


Figure 22. Overall Loop Gain and Phase

If a network analyzer is available, the modulator gain can be measured and the error amplifier gain can be configured for the desired loop transfer function. If a network analyzer is not available, the error amplifier compensation components can be designed with the guidelines given. Step load transient tests can be performed to verify acceptable performance. The step load goal is minimum overshoot with a damped response. C6 can be added to the compensation network to decrease noise susceptibility of the error amplifier. The value of C6 must be sufficiently small since the addition of this capacitor adds a pole in the error amplifier transfer function. This pole must be well beyond the loop crossover frequency. A good approximation of the location of the pole added by C6 is: f_{p2} = fz x C5 / C6.

8.2.3 Application Curves

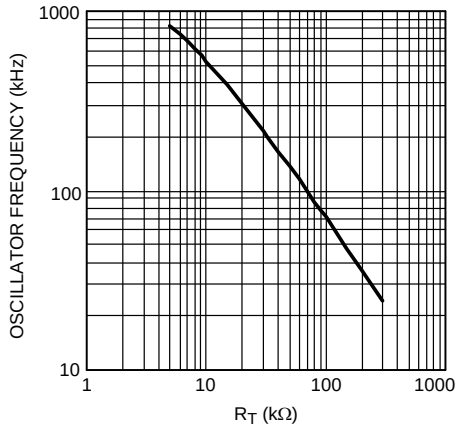


Figure 23. Oscillator Frequency vs R_T

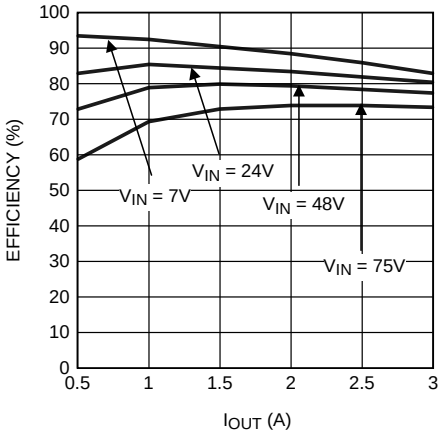


Figure 24. Demoboard Efficiency vs I_{OUT} and V_{IN}

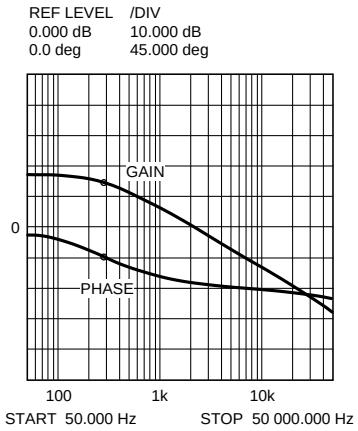


Figure 25. Gain and Phase Of Modulator R = 5 Ohms And C = 177 µF Loadout

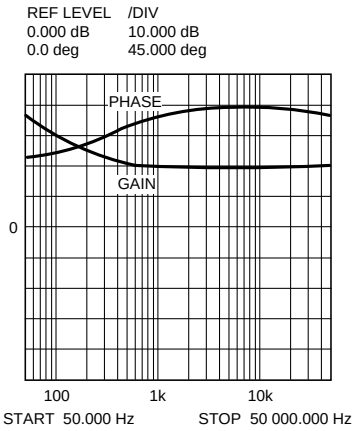


Figure 26. Error Amplifier Gain and Phase

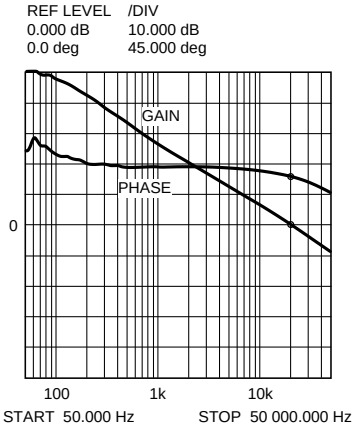


Figure 27. Overall Loop Gain and Phase

9 Power Supply Recommendations

The LM5576 is designed to operate from an input voltage supply range between 6 V and 75 V. This input supply should be able to withstand the maximum input current and maintain a voltage above 6 V. The resistance of the input supply rail should be low enough that an input current transient does not cause a high enough drop at the LM5576 supply voltage that can cause a false UVLO fault triggering and system reset. If the input supply is located more than a few inches from the LM5576 additional bulk capacitance may be required in addition to the ceramic bypass capacitors. The amount of bulk capacitance is not critical, but a 47-µF or 100-µF electrolytic capacitor is a typical choice.

10 Layout

10.1 Layout Guidelines

The circuit in Figure 18 serves as both a block diagram of the LM5576 and a typical application board schematic for the LM5576. In a buck regulator there are two loops where currents are switched very fast. The first loop starts from the input capacitors, to the regulator VIN pin, to the regulator SW pin, to the inductor then out to the load. The second loop starts from the output capacitor ground, to the regulator PGND pins, to the regulator IS pins, to the diode anode, to the inductor and then out to the load. Minimizing the loop area of these two loops reduces the stray inductance and minimizes noise and possible erratic operation. A ground plane in the PC board is recommended as a means to connect the input filter capacitors to the output filter capacitors and the PGND pins of the regulator. Connect all of the low power ground connections (C_{SS}, R_T, C_{RAMP}) directly to the regulator AGND pin. Connect the AGND and PGND pins together through the topside copper area covering the entire underside of the device. Place several vias in this underside copper area to the ground plane.

The two highest power dissipating components are the re-circulating diode and the LM5576 regulator IC. The easiest method to determine the power dissipated within the LM5576 is to measure the total conversion losses ($P_{IN} - P_{OUT}$) then subtract the power losses in the Schottky diode, output inductor and snubber resistor. An approximation for the Schottky diode loss is $P = (1\text{-}D) \times I_{OUT} \times V_{FWD}$. An approximation for the output inductor power is $P = I_{OUT}^2 \times R \times 1.1$, where R is the DC resistance of the inductor and the 1.1 factor is an approximation for the AC losses. If a snubber is used, an approximation for the damping resistor power dissipation is $P = V_{IN}^2 \times Fsw \times Csnub$, where Fsw is the switching frequency and Csnub is the snubber capacitor. The regulator has an exposed thermal pad to aid power dissipation. Adding several vias under the device to the ground plane will greatly reduce the regulator junction temperature. Selecting a diode with an exposed pad will aid the power dissipation of the diode.

The most significant variables that affect the power dissipated by the LM5576 are the output current, input voltage and operating frequency. The power dissipated while operating near the maximum output current and maximum input voltage can be appreciable. The operating frequency of the LM5576 evaluation board has been designed for 300 kHz. When operating at 3 A output current with a 70 V input the power dissipation of the LM5576 regulator is approximately 2.5 W.

The junction-to-ambient thermal resistance of the LM5576 will vary with the application. The most significant variables are the area of copper in the PC board, the number of vias under the IC exposed pad and the amount of forced air cooling provided. Referring to the evaluation board artwork, the area under the LM5576 (component side) is covered with copper and there are 5 connection vias to the solder side ground plane. Additional vias under the IC will have diminishing value as more vias are added. The integrity of the solder connection from the IC exposed pad to the PC board is critical. Excessive voids will greatly diminish the thermal dissipation capacity. The junction-to-ambient thermal resistance of the LM5576 mounted in the evaluation board varies from 45°C/W with no airflow to 25°C/W with 900 LFM (Linear Feet per Minute). With a 25°C ambient temperature and no airflow, the predicted junction temperature for the LM5576 will be 25 + (45 x 2.5) = 137.5°C. If the evaluation board is operated at 3 A output current and 70 V input voltage for a prolonged period of time the thermal shutdown protection within the IC will activate. The IC will turn off allowing the junction to cool, followed by restart with the soft-start capacitor reset to zero.

Layout Guidelines (continued)

One or more of the following modifications will prevent the thermal shutdown from being activated: apply forced air cooling, reduce the maximum input voltage, lower the maximum output current, reduce the operating frequency, add more heat sinking to the PC board. For example, applying forced air cooling of 225 LFM will reduce the LM5576 thermal resistance to approximately 30°C/W. The junction temperature will be reduced to 25 + (2.5 x 30) = 100°C. If the maximum input voltage for the application is 48 V, then the IC power dissipation reduces to 2 W (at 3 A output current). With the same forced air cooling the junction temperature reduces to 25 + (2 x 30) = 85°C.

10.2 Layout Example

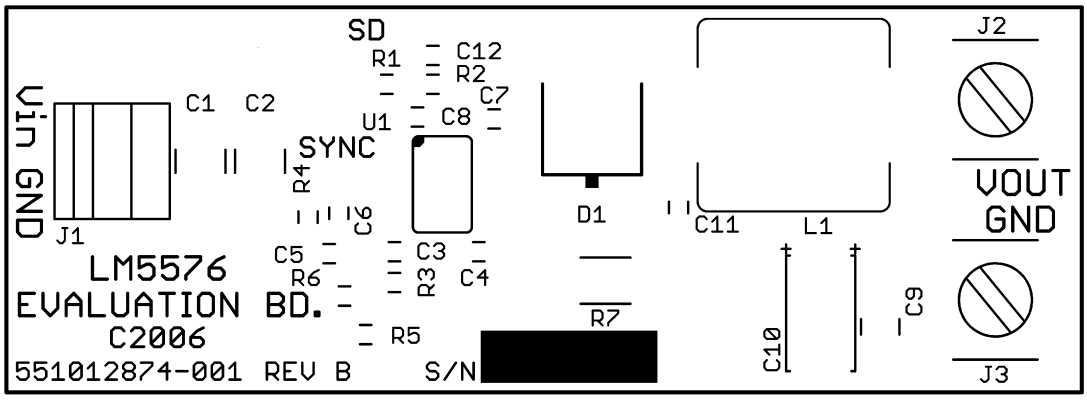


Figure 28. Silkscreen

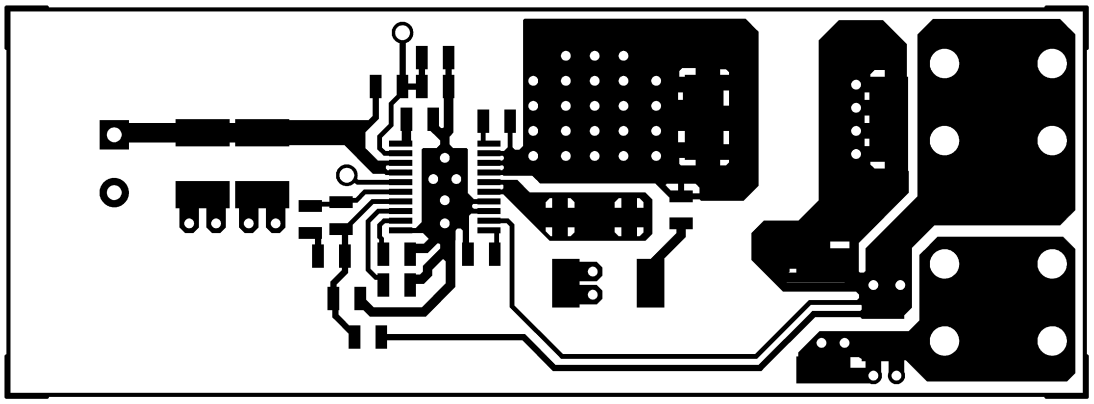


Figure 29. Component Side

Layout Example (continued)

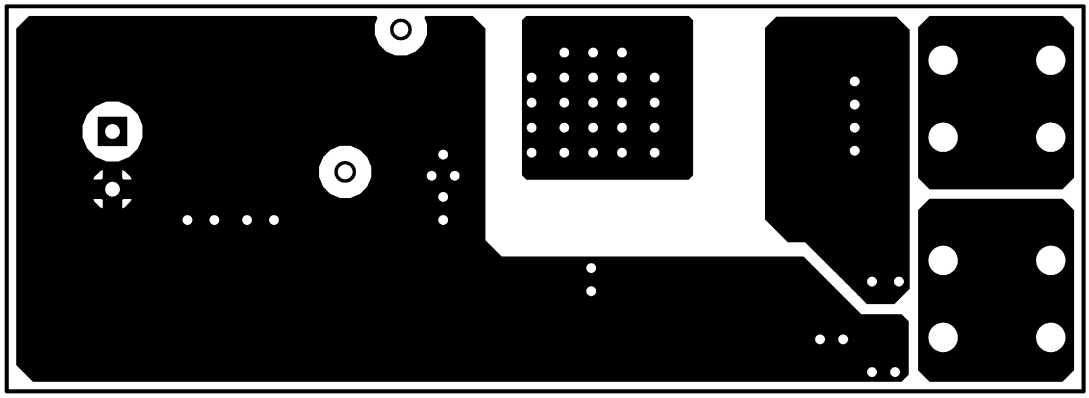


Figure 30. Solder Side

11 器件和文档支持

11.1 相关链接

下面的表格列出了快速访问链接。范围包括技术文档、支持和社区资源、工具和软件，以及样片或购买的快速访问。

表 2. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
LM5576	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
LM5576-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.2 商标

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11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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