1. FEATURES

- Nanopower supply current: 240nA/channel
- Offset voltage: 2.2mV (max)
- TcVos: 2μV/°C
- Unity gain-bandwidth: 4.2kHz
- Wide supply range: 1.6V to 5.5V
- Low input bias current: 0.1pA
- Unity-gain stable
- Rail-to-rail input and output
- EMI protection

2. APPLICATIONS

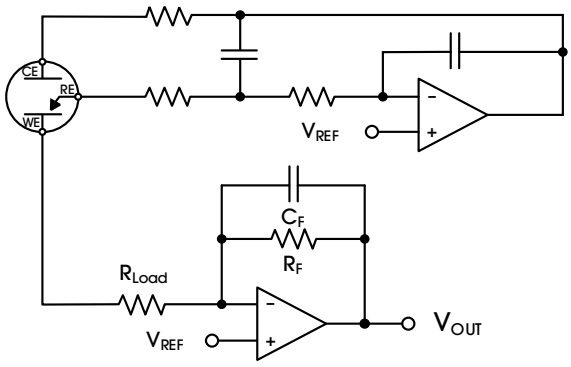
- CO and O2 gas detectors
- PIR motion detectors
- Ionization smoke alarms
- Thermostats
- IoT remote sensors
- Active RFID readers and tags
- Portable medical equipment
- Monitor and alarms
- Wearable devices

3. DESCRIPTION

The OPA501 is one of the ultra-low-power family operational amplifiers provided by AnalogySemi. With just 240nA of quiescent current and operating voltage ranged between 1.6V and 5.5V, the OPA501 operational amplifier is applicable to most battery-powered circumstances and stable even without additional boost topology. Keeping low power consumption and 4.2kHz of bandwidth, the OPA501 device works rather well with equipment such as CO detectors, smoke detectors, and PIR motion detectors. In addition, the OPA501 operational amplifier has CMOS input stages with typically femto-amp bias currents. EMI protection is incorporated into the OPA501 design in order to enhance overall system reliability by reducing system sensitivity to undesirable RF signals from mobile phones, Wi-Fi, radio transmitters, and tag readers.

The OPA501 operational amplifier is offered in the SOT23-5 package and specified from –40°C to 125°C, which makes it suitable for various rugged environment. See Table 1 for the order information.

Nanopower Amplifier in Electrochemical Sensor



Nanopower Amplifier in PIR Motion Detector

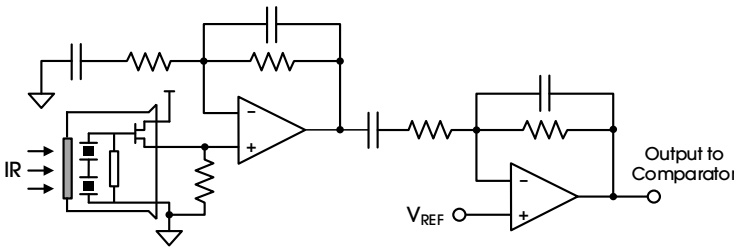


Table 1 lists the order information.

Table 1. Order Information

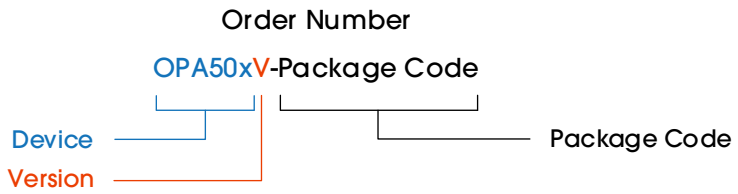
Order Number[1]	CH(#)	Package	Marking	I_Q per CH (Typ) (nA)	GBW (kHz)	Slew Rate (Typ) (V/ms)	Noise nV/√Hz (100Hz)	Operating Temp (°C)	Package Option
OPA501BSOT235	1	SOT23-5	OPA501	240	4.2	1.3	347	-40-125	T/R-3000

Table 2. Family Selection Guide

Order Number[1]	CH(#)	Package	Marking	I_Q per CH (Typ) (nA)	GBW (kHz)	Slew Rate (Typ) (V/ms)	Noise nV/√Hz (100Hz)	Operating Temp (°C)	Package Option
OPA503ASOT235	1	SOT23-5	OPA503	570	11	3	214	-40-125	T/R-3000
OPA504ASOT236	1	SOT23-6	OPA504	570	11	3	214	-40-125	T/R-3000
OPA505ASOT235	1	SOT23-5	OPA505	3200	65	20	100	-40-125	T/R-3000
OPA506ASOT236	1	SOT23-6	OPA506	3200	65	20	100	-40-125	T/R-3000

Devices can be ordered via the following two ways:
1. Place orders directly on our website (www.analogysemi.com), or;
2. Contact our sales team by mailing to sales@analogysemi.com.

Note:



4. PIN CONFIGURATION AND FUNCTIONS

Figure 1 illustrates the pin configuration.

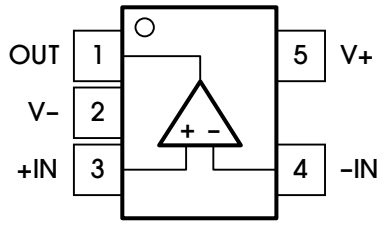


Figure 1. Pin Configuration

Table 3 lists the pin functions.

Table 3. Pin Functions

POSITION	NAME	TYPE	DESCRIPTION
1	OUT	Output	Output
2	V–	Power	Negative (lowest) power supply
3	+IN	Input	Positive (non-inverting) input
4	–IN	Input	Negative (inverting) input
5	V+	Power	Positive (highest) power supply

5. SPECIFICATIONS

5.1 ABSOLUTE MAXIMUM RATINGS

Table 4 lists the absolute maximum ratings of the OPA501. Over operating free-air temperature range, unless otherwise noted.

Table 4. Absolute Maximum Ratings

PARAMETER	DESCRIPTION		MIN	MAX	UNITS
Voltage	Supply		–0.3	6	V
	Signal input pins(2)(3)	Common-mode	(V–) – 0.3	(V+) + 0.3	
		Differential	(V–) – 0.3	(V+) + 0.3	
Current	Signal input pins		–10	10	mA
	Output short-circuit(4)		Continuous		
Temperature	Operating, T_A		–40	125	°C
	Junction, T_J			150	
	Storage, T_{stg}		–65	150	

Note 1: Stresses beyond those listed under Table 4 may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Table 6. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
Note 2: Not to exceed –0.3V or +6.0V on ANY pin, referred to V–.
Note 3: Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3V beyond the supply rails should be current-limited to 10mA or less.
Note 4: Short-circuit to V_S / 2, one amplifier per package. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

5.2 ESD RATINGS

Table 5 lists the ESD ratings of the OPA501.

Table 5. ESD Ratings

PARAMETER	SYMBOL	DESCRIPTION	VALUE	UNITS
Electrostatic Discharge	$V_{(ESD)}$	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±6000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±2000	

Note 1: The JEDEC document JEP155 indicates that 500V HBM allows safe manufacturing with a standard ESD control process.
Note 2: The JEDEC document JEP157 indicates that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 RECOMMENDED OPERATING CONDITIONS

Table 6 lists the recommended operating conditions for the OPA501. Over operating free-air temperature range, unless otherwise noted.

Table 6. Recommended Operating Conditions

PARAMETER	MIN	NOM	MAX	UNITS
Operating Voltage Range	1.6		5.5	V
Specified Temperature Range	–40		125	°C

5.4 THERMAL INFORMATION

Table 7 lists the thermal information for the OPA501.

Table 7. Thermal Information

PARAMETER	SYMBOL	SOT23-5	UNITS
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$	168	°C/W
Junction-to-Case (Top) Thermal Resistance	$R_{\theta JC(top)}$	103	°C/W
Junction-to-Board Thermal Resistance	$R_{\theta JB}$	39	°C/W
Junction-to-Top Characterization Parameter	ψ_{JT}	10	°C/W
Junction-to-Board Characterization Parameter	ψ_{JB}	36	°C/W
Junction-to-Case (Bottom) Thermal Resistance	$R_{\theta JC(bot)}$	66	°C/W

5.5 ELECTRICAL CHARACTERISTICS

Table 8 lists the electrical characteristics of OPA501. T_A = 25°C, V_S = 1.8V to 5V, V_{CM} = V_{OUT} = V_S / 2, and R_L ≥ 10MΩ to V_S / 2, unless otherwise noted.

Table 8. Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_S = 1.8V, 3.3V, and 5V, V_{CM} = V_S / 2 or V_{CM} = (V+) – 0.9V		±0.4	±2.2	mV
Input Offset Drift	$\Delta V_{OS}/\Delta T$	T_A = –40°C to 125°C		2		μV/°C
Power-Supply Rejection Ratio	PSRR	V_S = 1.8V to 5V, V_{CM} = VDD/2		10	73	μV/V
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		0		VDD	V
Common-Mode Rejection Ratio	CMRR	(V–) ≤ V_{CM} ≤ (V+) – 0.9V, V_S = 5V	79	95		dB
		(V–) ≤ V_{CM} ≤ (V+), V_S = 5V	63	79		dB
INPUT BIAS CURRENT						
Input Bias Current	I_B	V_S = 1.8V, V_{CM} = V_S / 2		±100		fA
Input Offset Current	I_{OS}	V_S = 1.8V, V_{CM} = V_S / 2		±100		
INPUT IMPEDANCE						
Differential(1)				3.3		pF
Common Mode(1)				7.2		
NOISE						
Input Voltage Noise	E_n	f = 0.1Hz to 10Hz		17.6		μV_{PP}
Input Voltage Noise Density	e_n	f = 100Hz		347		$nV/\sqrt{Hz}$
		f = 1kHz		417		
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	(V–) + 0.3V ≤ V_O ≤ (V+) – 0.3V, R_L = 100kΩ		114		dB
OUTPUT						
Voltage Output Swing from Positive Rail	V_{OH}	V_S = 1.8V, R_L = 100kΩ to (V+) / 2		2	10	mV
Voltage Output Swing from Negative Rail	V_{OL}	V_S = 1.8V, R_L = 100kΩ to (V+) / 2		1.5	10	
Short-Circuit Current	I_{SC}	V_S = 3.3V, short to V_S / 2		5		mA
FREQUENCY RESPONSE						
Gain-Bandwidth Product	GBP	C_L = 20pF, R_L = 10MΩ, V_S = 5V		4.2		kHz
Slew Rate (10% to 90%)	SR	G = 1, Rising Edge, C_L = 20pF, V_S = 5V		1.3		V/ms
		G = 1, Falling Edge, C_L = 20pF, V_S = 5V		2.6		
POWER SUPPLY						
Quiescent Current		V_{CM} = V–, I_O = 0, V_S = 3.3V		240	365	nA

Note: Guaranteed by design.

5.6 TYPICAL CHARACTERISTICS

T_A = 25°C, V_S = 3.3V, R_L = 10MΩ to V_S / 2, C_L = 20pF, V_{CM} = V_S / 2V, unless otherwise specified.

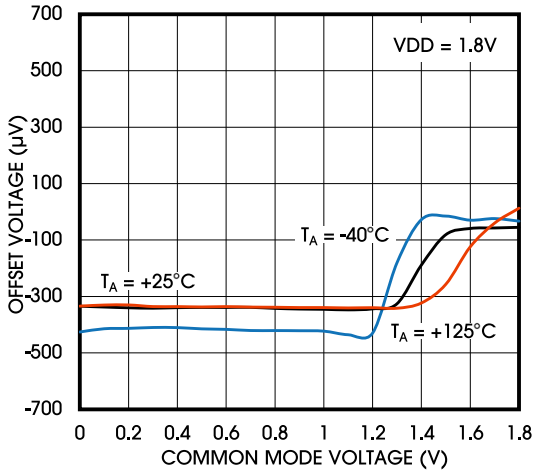


Figure 2. Typical Offset Voltage vs. Common Mode Voltage, 1.8V

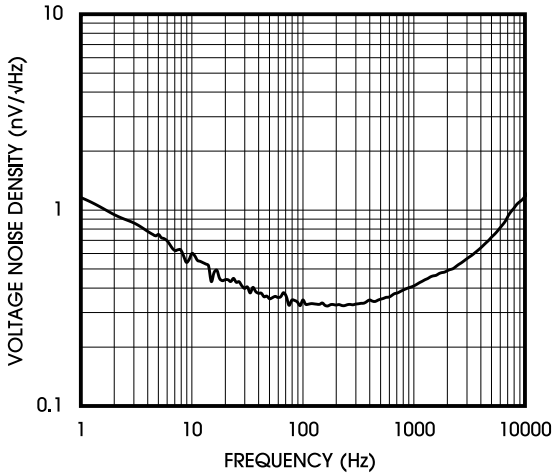


Figure 3. Input Voltage Noise vs Frequency

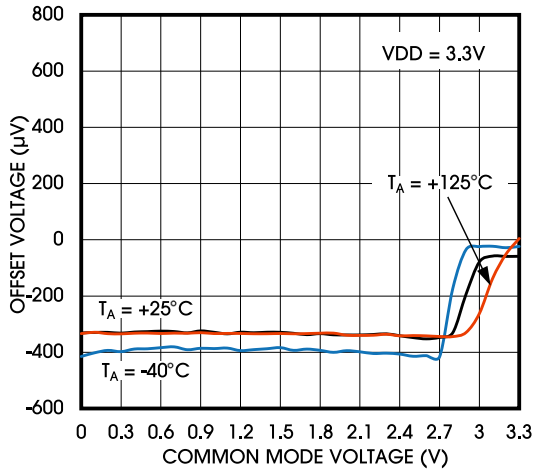


Figure 4. Typical Offset Voltage vs. Common Mode Voltage, 3.3V

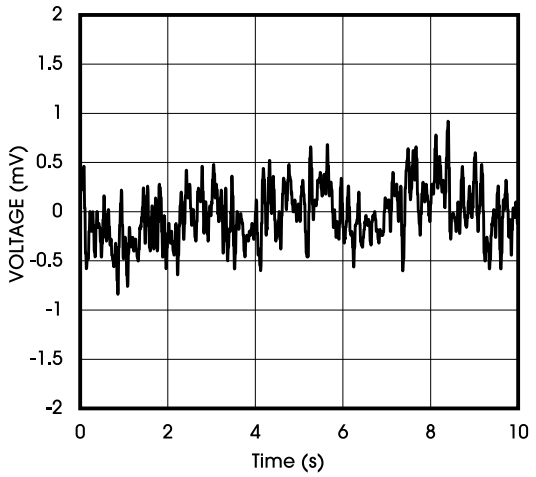


Figure 5. Integrated Noise

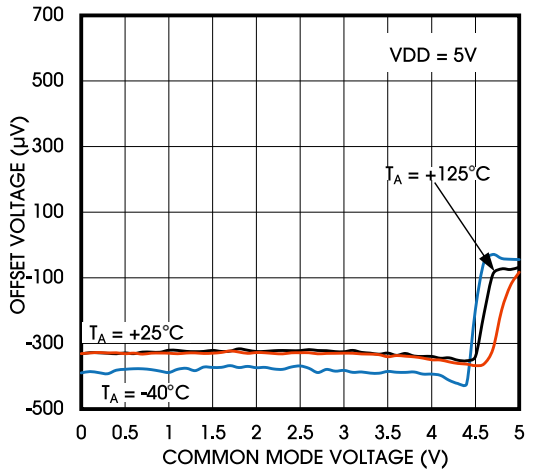


Figure 6. Typical Offset Voltage vs. Common Mode Voltage, 5V

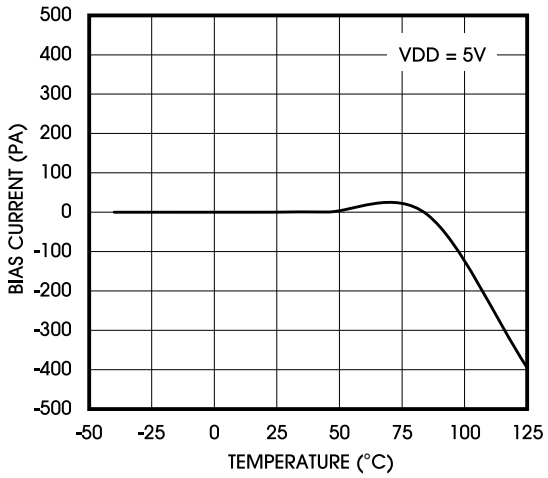


Figure 7. Input Bias Current vs. Temperature

5.7 TYPICAL CHARACTERISTICS (CONTINUED)

T_A = 25°C, V_S = 3.3V, R_L = 10MΩ to V_S / 2, C_L = 20pF, V_{CM} = V_S / 2V, unless otherwise specified.

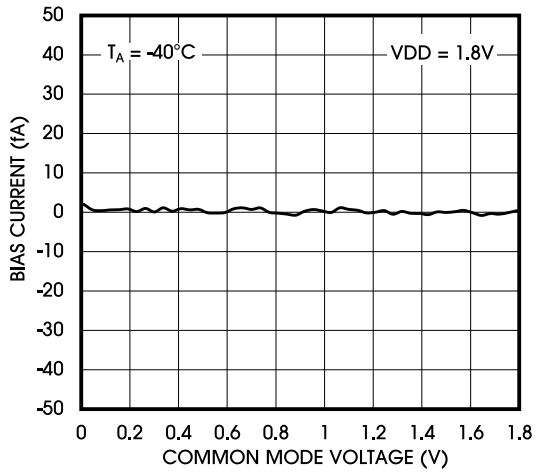


Figure 8. Input Bias Current vs. Common Mode Voltage

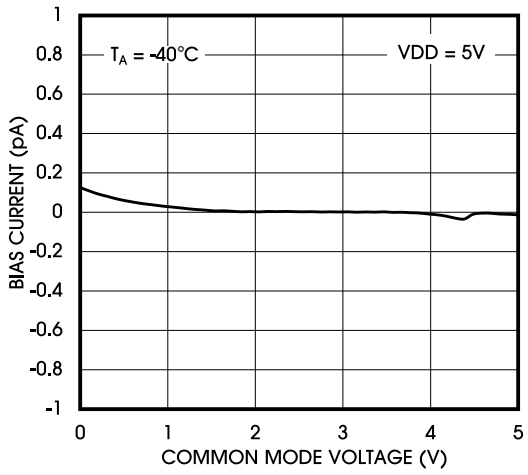


Figure 9. Input Bias Current vs. Common Mode Voltage

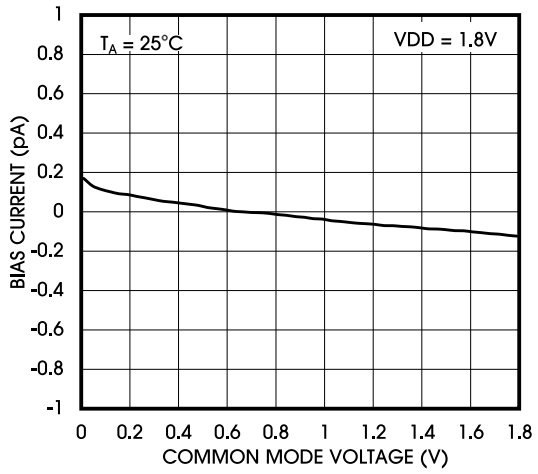


Figure 10. Input Bias Current vs. Common Mode Voltage

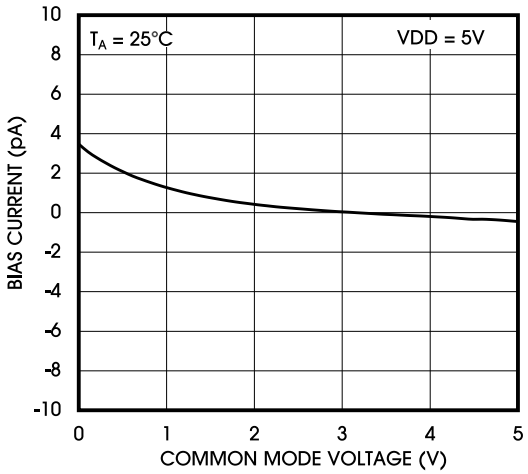


Figure 11. Input Bias Current vs. Common Mode Voltage

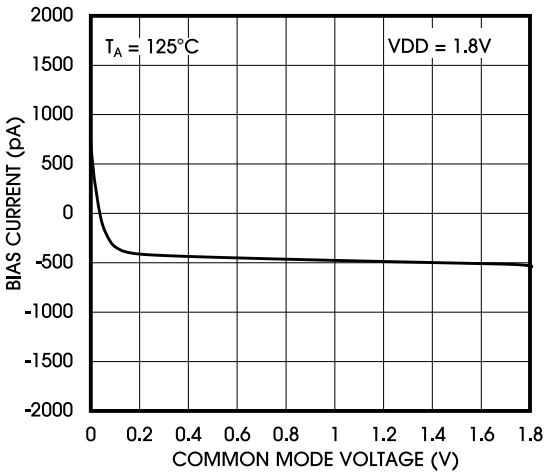


Figure 12. Input Bias Current vs. Common Mode Voltage

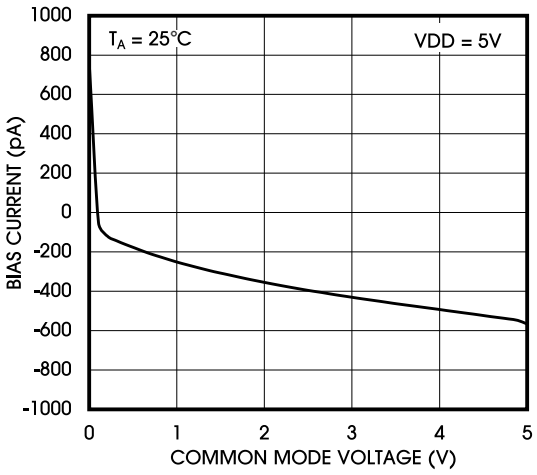


Figure 13. Input Bias Current vs. Common Mode Voltage

5.8 TYPICAL CHARACTERISTICS (CONTINUED)

T_A = 25°C, V_S = 3.3V, R_L = 10MΩ to V_S / 2, C_L = 20pF, V_{CM} = V_S / 2V, unless otherwise specified.

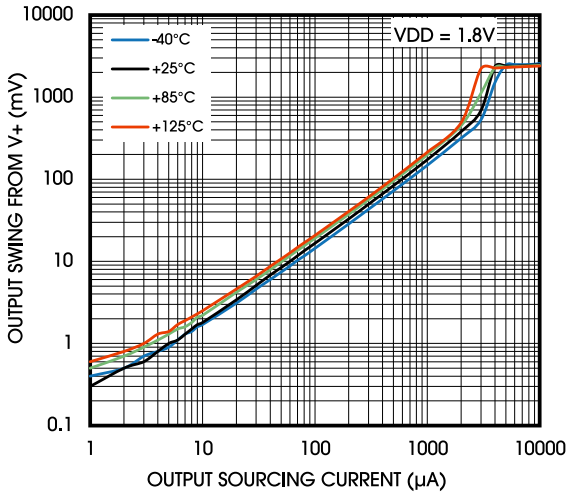


Figure 14. Output Swing vs. Sourcing Current, 1.8V

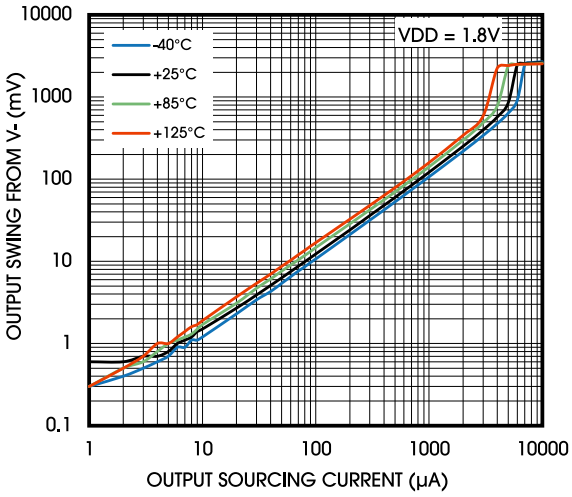


Figure 15. Output Swing vs. Sinking Current, 1.8V

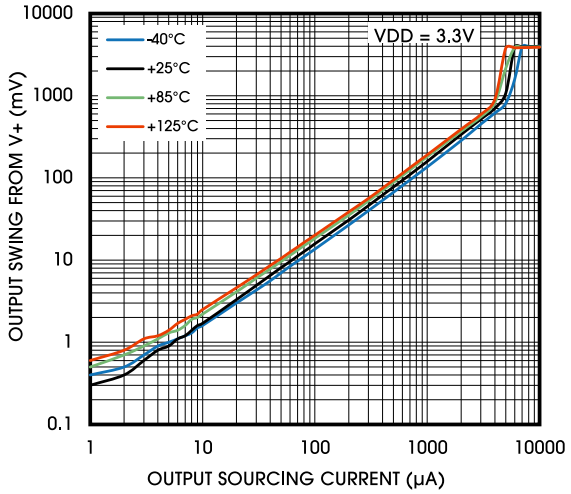


Figure 16. Output Swing vs. Sourcing Current, 3.3V

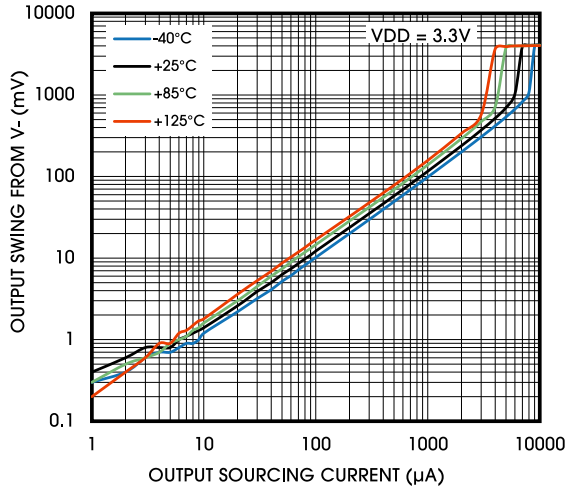


Figure 17. Output Swing vs. Sinking Current, 3.3V

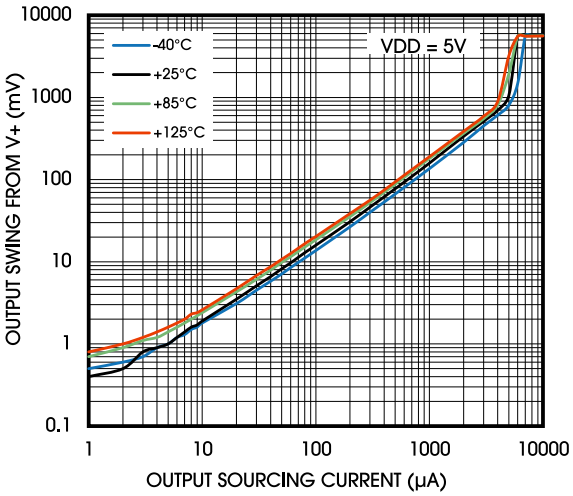


Figure 18. Output Swing vs. Sourcing Current, 5V

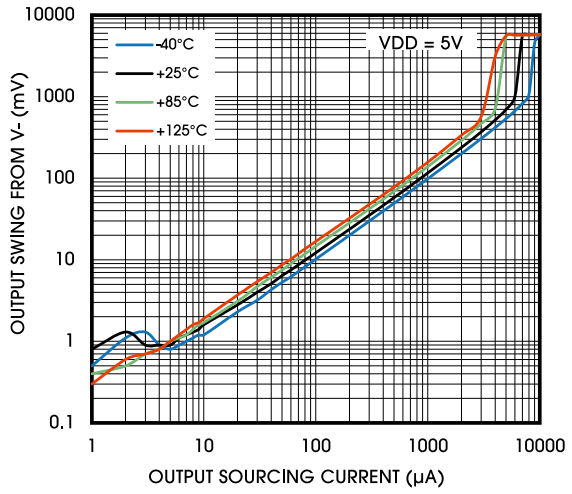


Figure 19. Output Swing vs. Sinking Current, 5V

5.9 TYPICAL CHARACTERISTICS (CONTINUED)

T_A = 25°C, V_S = 3.3V, R_L = 10MΩ to V_S / 2, C_L = 20pF, V_{CM} = V_S / 2V, unless otherwise specified.

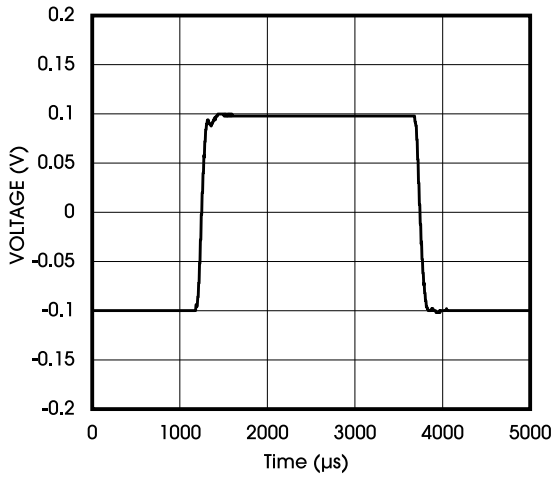


Figure 20. Small Signal Pulse Response, 1.8V

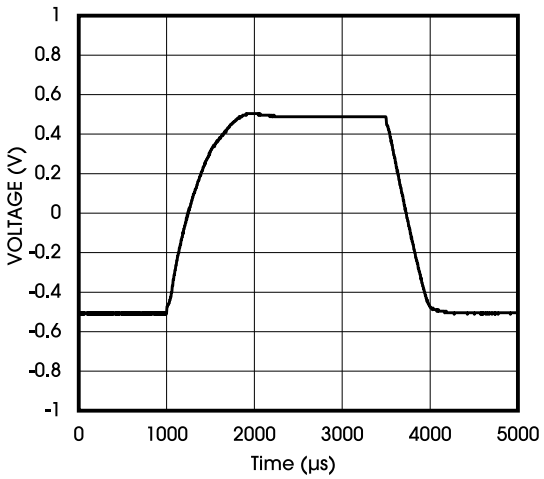


Figure 21. Large Signal Pulse Response, 1.8V

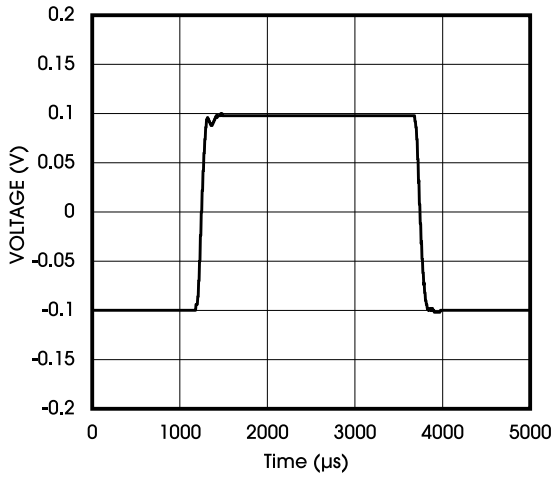


Figure 22. Small Signal Pulse Response, 3.3V

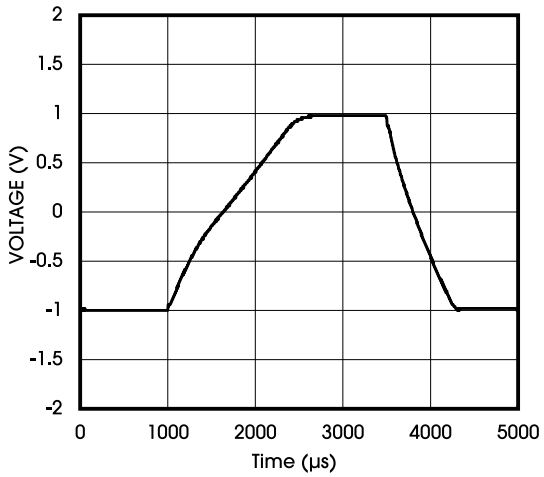


Figure 23. Large Signal Pulse Response, 3.3V

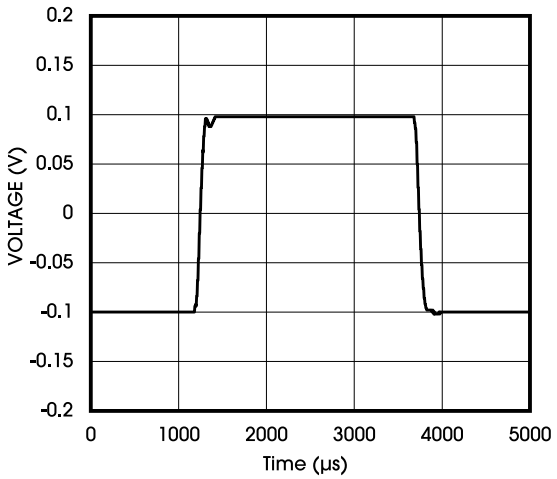


Figure 24. Small Signal Pulse Response, 5V

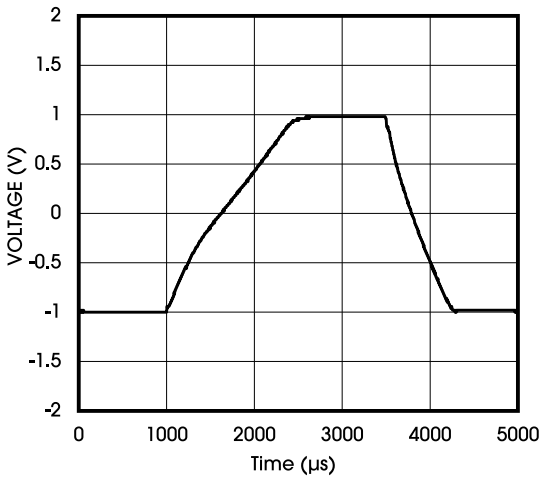


Figure 25. Large Signal Pulse Response, 5V

5.10 TYPICAL CHARACTERISTICS (CONTINUED)

T_A = 25°C, V_S = 3.3V, R_L = 10MΩ to V_S / 2, C_L = 20pF, V_{CM} = V_S / 2V, unless otherwise specified.

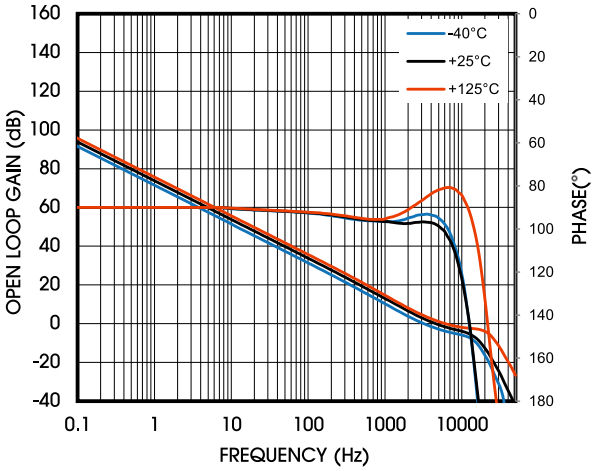


Figure 26. Open Loop Gain and Phase, 3.3V, 10MΩ Load

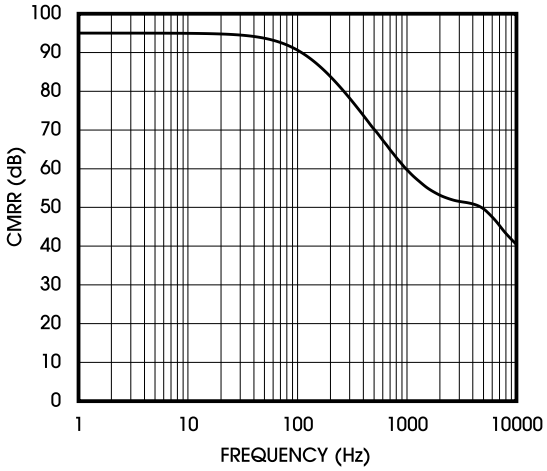


Figure 27. CMRR vs Frequency

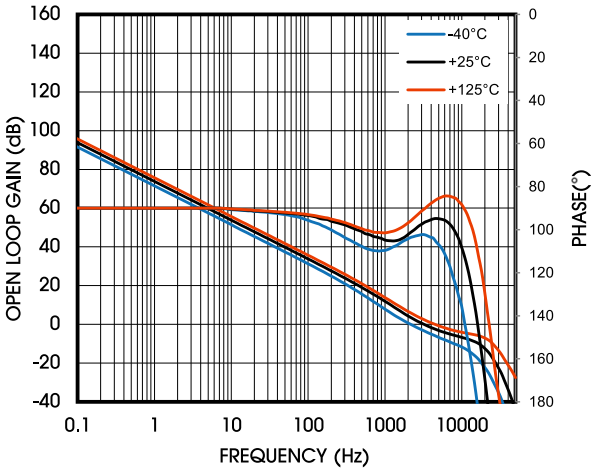


Figure 28. Open Loop Gain and Phase, 3.3V, 1MΩ Load

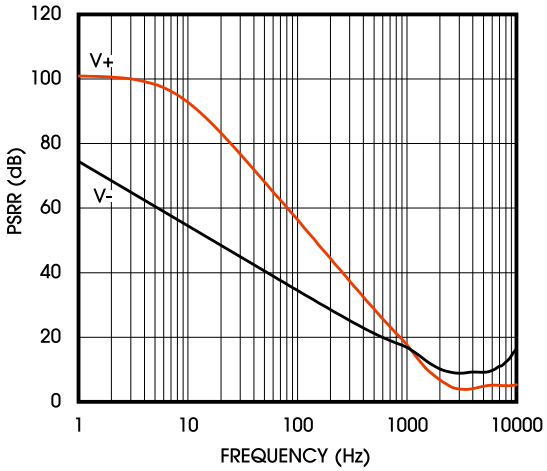


Figure 29. PSRR vs Frequency

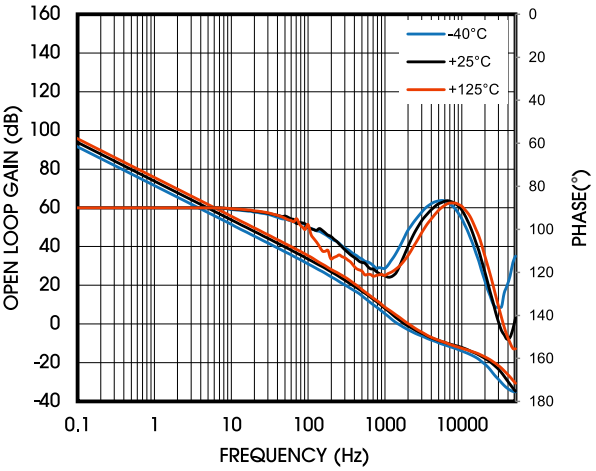


Figure 30. Open Loop Gain and Phase, 3.3V, 100kΩ Load

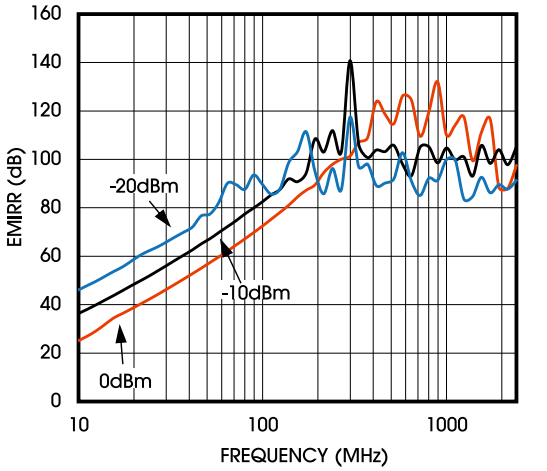


Figure 31. EMIRR Performance Supply Current vs. Supply Voltage

5.11 TYPICAL CHARACTERISTICS (CONTINUED)

T_A = 25°C, V_S = 3.3V, R_L = 10MΩ to V_S / 2, C_L = 20pF, V_{CM} = V_S / 2V, unless otherwise specified.

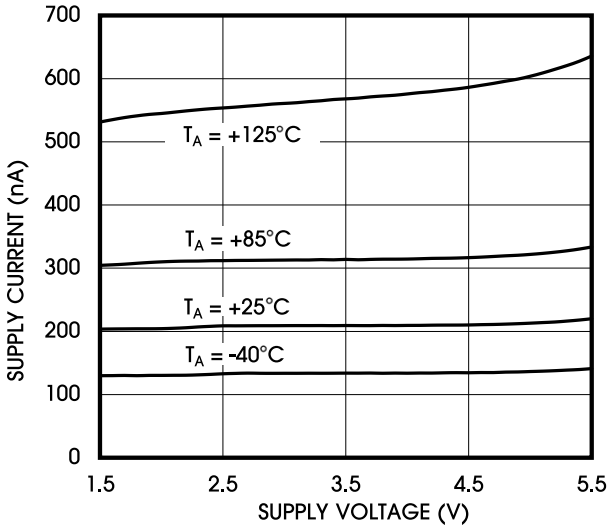


Figure 32. Supply Current vs. Supply Voltage

6. DETAILED DESCRIPTION

6.1 OVERVIEW

The OPA501 nanopower CMOS operational amplifier is designed for long-life battery-powered and energy harvested applications. They can operate on a single supply with operation as low as 1.6V. Low input bias current make it an ideal choice for sensor interface, in particular for sensors that operate with low voltage and at low frequency. The common-mode range extends to the power supply, making it ideal for single-supply applications. EMI protection has been employed internally to reduce the effects of EMI.

6.2 FEATURE DESCRIPTION

6.2.1 RAIL-TO-RAIL INPUT

The OPA501 features a rail-to-rail input with 100fA bias current, making it ideal for sensor like CO and O^2 gas detectors. Low input bias current contributes less error to sensor. See Figure 7 through Figure 13 for typical input bias current.

6.2.2 RAIL-TO-RAIL OUTPUT STAGE

The OPA501 output voltage swings 2mV from rails at 1.8V supply, which provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages. The Maximum Output Voltage Swing graph defines the maximum swing possible under a particular output load. See Figure 14 through Figure 19.

6.2.3 POWER SUPPLY

Connect a 100nF capacitor as close as possible to the V+/ V– pin, to reduce ripple of power supply. Care need be taken while selecting the capacitor, as the OPA501 is nanopower component, in low power application, static leakage current of ceramic capacitor cannot be ignored, especially at high temperature. Usually high-voltage ceramic capacitor has low static leakage current, use a high-voltage ceramic capacitor or film capacitor when static leakage current matters.

When designing for ultralow power, choose system feedback components carefully. To minimize quiescent current consumption, select large-value feedback resistors. Any large resistors will react with stray capacitance in the circuit and the input capacitance of the operational amplifier. These parasitic RC combinations can affect the stability of the overall system. A feedback capacitor may be required to assure stability and limit overshoot or gain peaking. When possible, use AC coupling and AC feedback to reduce static current draw through the feedback elements. Use film or ceramic capacitors since large electrolytic may have large static leakage currents in the nanoamps.

6.2.4 DRIVING CAPACITIVE LOAD

The OPA501 is internally compensated for stable unity gain operation, with a 4.2kHz typical gain bandwidth. However, the unity gain follower is the most sensitive configuration to capacitive load. The combination of a capacitive load placed directly on the output of an amplifier along with the amplifier's output impedance creates a phase lag, which reduces the phase margin of the amplifier. If the phase margin is significantly reduced, the response will be under damped, which causes peaking in the transfer and, when there is too much peaking, the op amp might start oscillating.

In order to drive heavy (> 50pF) capacitive loads, an isolation resistor, R_{ISO}, should be used. By using this isolation resistor, the capacitive load is isolated from the amplifier's output. The larger the value of R_{ISO}, the more stable the amplifier will be. If the value of R_{ISO} is sufficiently large, the feedback loop will be stable, independent of the value of C_L. However, larger values of R_{ISO} result in reduced output swing and reduced output current drive. The recommended value for R_{ISO} is 30-50kΩ.

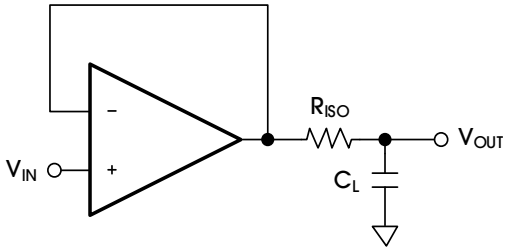


Figure 33. Resistive Isolation of Capacitive Load

6.2.5 PCB LAYOUT RECOMMENDATION

Take care about layout routing. Parasitic capacitor on the input and output can significantly lower phase margin and bandwidth. For some applications like unit gain, if there is ground shield in inner layer or bottom layer, fine routing is recommended, or use bottom layer instead of inner layer as ground shield. Furthermore, the routing of input and output should be as short as possible.

7. PACKAGE INFORMATION

The OPA501 is available in the SOT23-5 package. Figure 34 shows the package view.

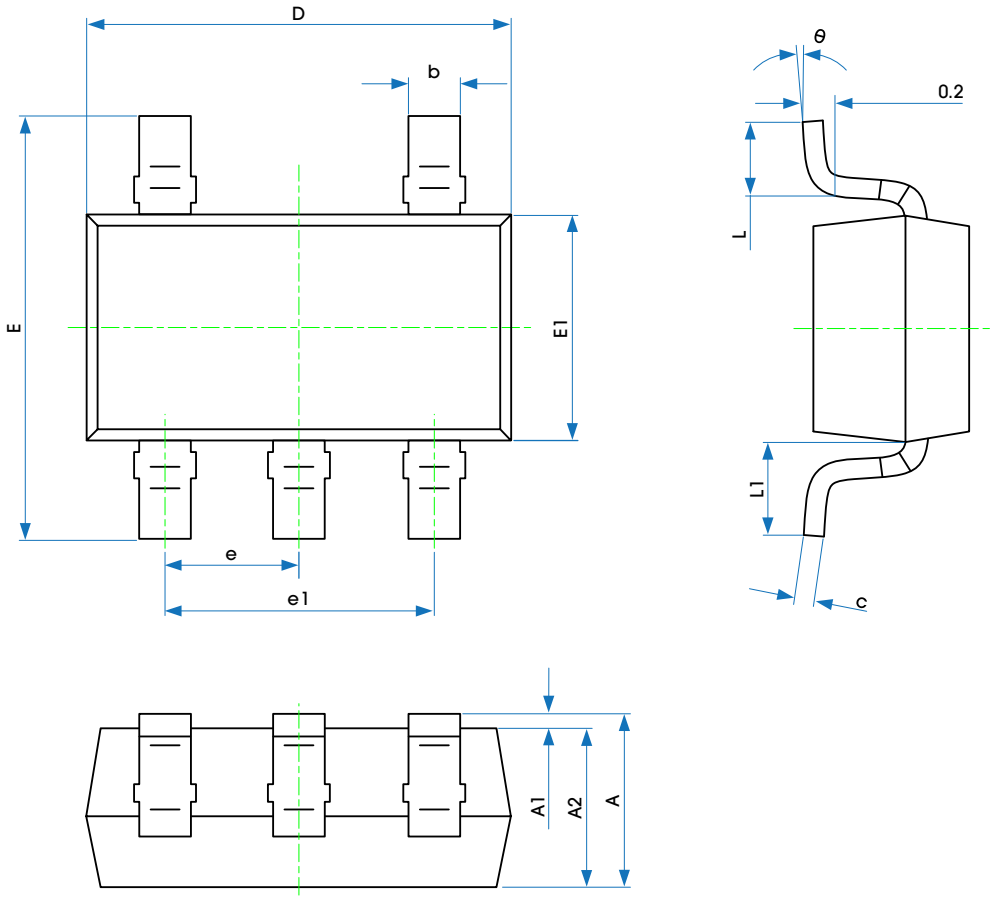


Figure 34. Package View

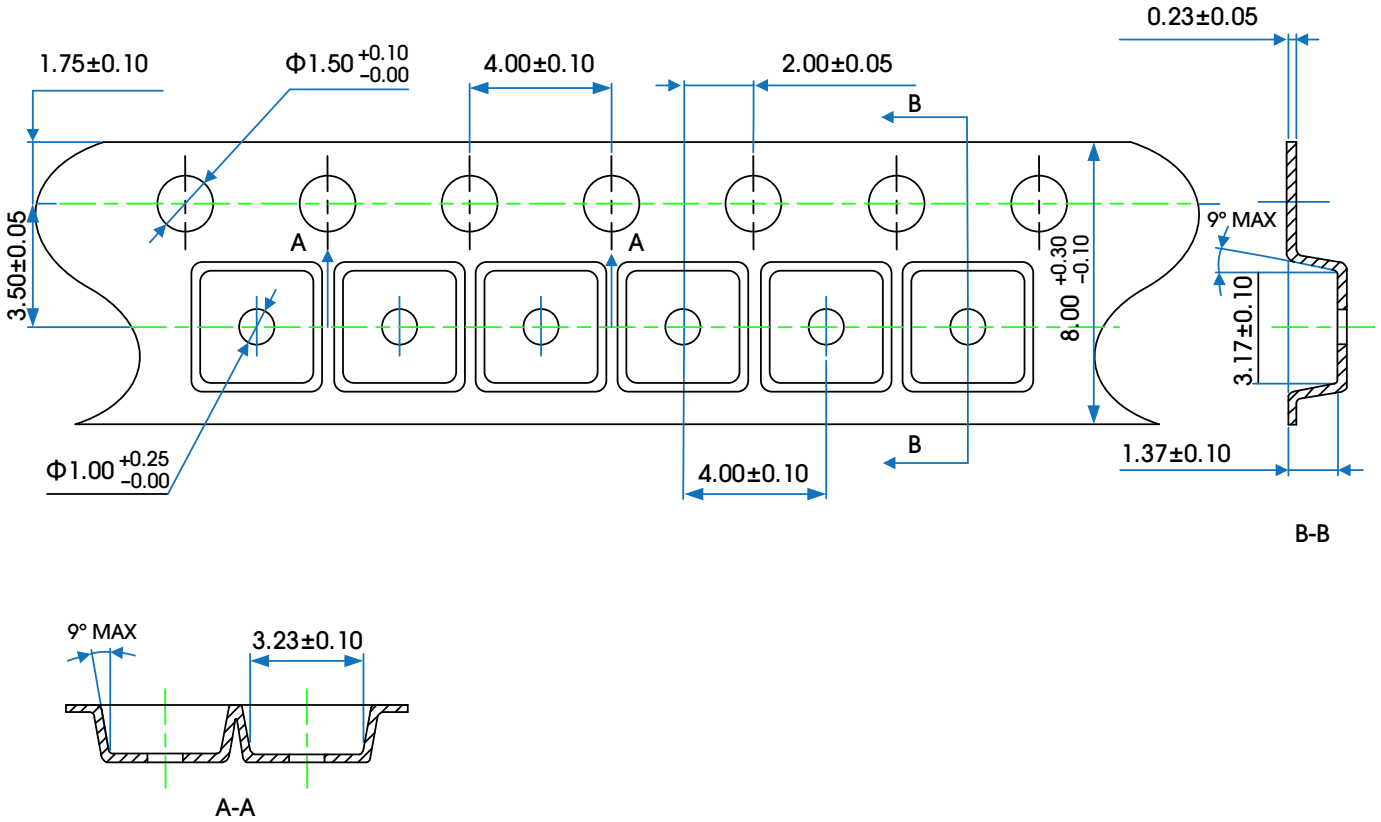
Table 9 provides detailed information about the dimensions.

Table 9. Dimensions

SYMBOL	DIMENSIONS IN MILLIMETERS		DIMENSIONS IN INCHES	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	2.650	2.950	0.104	0.116
E1	1.500	1.700	0.059	0.067
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
L1	0.600 REF.		0.024 REF.	
θ	0°	8°	0°	8°

8. TAPE AND REEL INFORMATION

Figure 35 illustrates the carrier tape.



Notes:
1. Cover tape width: 5.50 ± 0.10.
2. Cumulative tolerance of 10 sprocket hole pitch: ±0.20 (max).
3. Camber: not to exceed 2mm in 250mm.
4. Mold#: SOT23-5.
5. All dimensions: mm.
6. Direction of view:

Figure 35. Carrier Tape Drawing

Table 10 provides information about tape and reel.

Table 10. Tape and Reel Information

PACKAGE TYPE	REEL	QTY/REEL	REEL/ INNER BOX	INNER BOX/ CARTON	QTY/CARTON	INNER BOX SIZE (MM)	CARTON SIZE (MM)
SOT23-5	7''	3000	10	4	120000	210*208*203	440*440*230

Figure 36 shows the product loading orientation—pin 1 is assigned on the lower left corner.

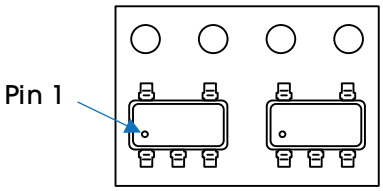


Figure 36. Product Loading Orientation

REVISION HISTORY

REVISION	DATE	DESCRIPTION
Rev A	30 March 2022	Rev A release.
Rev B	31 March 2022	Updated the PACKAGE OPTION columns in Table 1 and Table 2.