AiP74HC/HCT74
Dual D-type flip-flop with set and reset; positive-edge trigger

Product Specification

Specification Revision History:

Version	Date	Description
2012-05-A1	2012-05	New
2021-11-A2	2021-11	Modify Ordering Information; Modify ambient temperature to -40℃ ~+105℃ and add electrical characteristics of -40℃~+105℃
2021-12-A3	2021-12	Modify Ordering Information

1、General Description

The AiP74HC/HCT74 are dual positive edge triggered D-type flip-flop. They have individual data (nD), clock (nCP), set ($n\overline{SD}$) and reset ($n\overline{RD}$) inputs, and complementary nQ and $n\overline{Q}$ outputs. Data at the nD-input, that meets the set-up and hold time requirements on the LOW-to-HIGH clock transition, is stored in the flip-flop and appears at the nQ output. Schmitt-trigger action in the clock input, makes the circuit highly tolerant to slower clock rise and fall times. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

Features:

- Input levels:
  For AiP74HC74: CMOS level
  For AiP74HCT74: TTL level
- Symmetrical output impedance
- Low power dissipation
- Balanced propagation delays
- Specified from -40℃ to +105℃
- Packaging information: DIP14/SOP14/TSSOP14

Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
AiP74HC74DA14.TB	DIP14	74HC74	25 PCS/tube	40 tube/box	1000 PCS/box	Dimensions of plastic enclosure: 19.0mm×6.4mm Pin spacing: 2.54mm
AiP74HCT74DA14.TB	DIP14	74HCT74	25 PCS/tube	40 tube/box	1000 PCS/box	Dimensions of plastic enclosure: 19.0mm×6.4mm Pin spacing: 2.54mm
AiP74HC74SA14.TB	SOP14	74HC74	50 PCS/tube	200 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 8.7mm×3.9mm Pin spacing: 1.27mm
AiP74HCT74SA14.TB	SOP14	74HCT74	50 PCS/tube	200 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 8.7mm×3.9mm Pin spacing: 1.27mm
AiP74HC74TA14.TB	TSSOP14	74HC74	94 PCS/tube	200 tube/box	18800 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm
AiP74HCT74TA14.TB	TSSOP14	74HCT74	94 PCS/tube	200 tube/box	18800 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
AiP74HC74SA14.TR	SOP14	74HC74	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 8.7mm×3.9mm Pin spacing: 1.27mm
AiP74HCT74SA14.TR	SOP14	74HCT74	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 8.7mm×3.9mm Pin spacing: 1.27mm
AiP74HC74TA14.TR	TSSOP14	74HC74	5000 PCS/reel	10000 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm
AiP74HCT74TA14.TR	TSSOP14	74HCT74	5000 PCS/reel	10000 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram

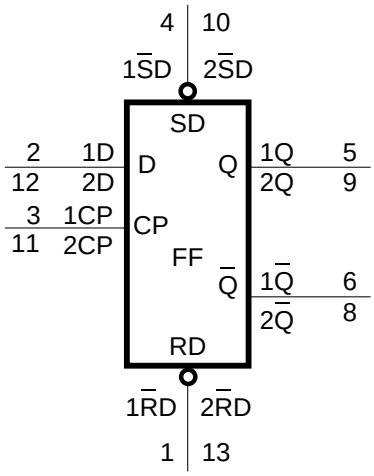


Figure 1. Logic symbol

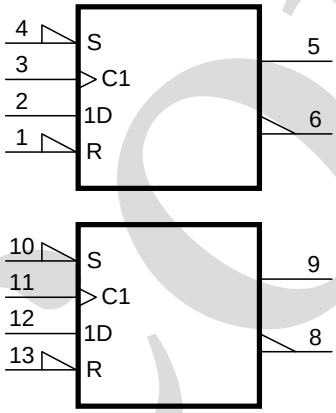


Figure 2. IEC logic symbol

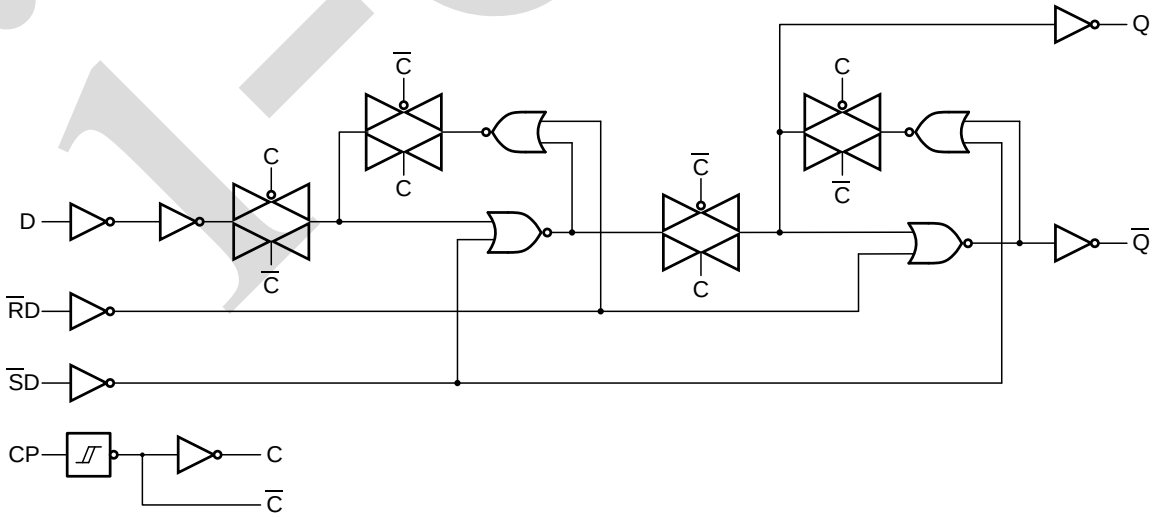


Figure 3. Logic diagram for one flip-flop

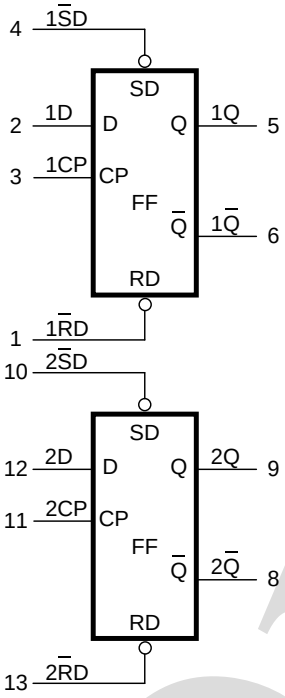
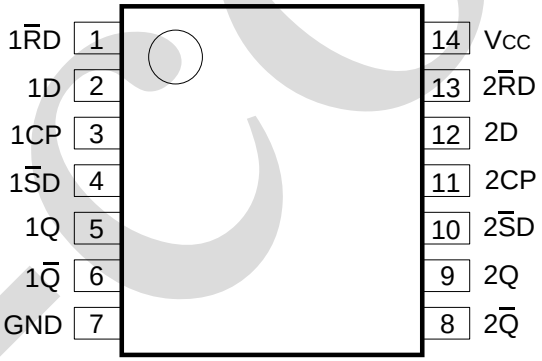


Figure 4. Functional diagram

2.2、Pin Configurations



2.3、Pin Description

Pin No.	Pin Name	Description
1	$1\overline{RD}$	asynchronous reset-direct input (active LOW)
2	1D	data input
3	1CP	clock input (LOW-to-HIGH, edge-triggered)
4	$1\overline{SD}$	asynchronous set-direct input (active LOW)
5	1Q	output
6	$1\overline{Q}$	complement output
7	GND	ground (0V)
8	$2\overline{Q}$	complement output
9	2Q	output
10	$2\overline{SD}$	asynchronous set-direct input (active LOW)
11	2CP	clock input (LOW-to-HIGH, edge-triggered)
12	2D	data input
13	$2\overline{RD}$	asynchronous reset-direct input (active LOW)
14	V_{CC}	supply voltage

2.4、Function Table

Input				Output	
$n\overline{SD}$	**$n\overline{RD}$**	**nCP**	**nD**	**nQ**	**$n\overline{Q}$**
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

Input				Output	
$n\overline{SD}$	**$n\overline{RD}$**	**nCP**	**nD**	**nQ_{n+1}**	**$n\overline{Q}_{n+1}$**
H	H	↑	L	L	H
H	H	↑	H	H	L

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care;
↑=LOW-to-HIGH transition; Qn+1=state after the next LOW-to-HIGH CP transition.

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V_{CC}	-		-0.5	+7	V
input clamping current	I_{IK}	$V_I < -0.5V$ or $V_I > V_{CC}+0.5V$		-	±20	mA
output clamping current	I_{OK}	$V_O < -0.5V$ or $V_O > V_{CC}+0.5V$		-	±20	mA
output current	I_O	$-0.5V < V_O < V_{CC}+0.5V$		-	±25	mA
supply current	I_{CC}	-		-	100	mA
ground current	I_{GND}	-		-100	-	mA
total power dissipation	P_{tot}	-		-	500	mW
storage temperature	T_{stg}	-		-65	+150	℃
soldering temperature	T_L	10s	DIP	245		℃
			SOP	250		

Note:

[1] For DIP14 packages: above 70℃ the value of P_{tot} derates linearly with 12mW/K.

[2] For SOP14 packages: above 70℃ the value of P_{tot} derates linearly with 8mW/K.

[3] For (T)SSOP14 packages: above 60℃ the value of P_{tot} derates linearly with 5.5mW/K.

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
AiP74HC74						
supply voltage	V_{CC}	-	2.0	5.0	6.0	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
input transition rise and fall rate	Δt/ΔV	V_{CC}=2.0V	-	-	625	ns/V
		V_{CC}=4.5V	-	1.67	139	ns/V
		V_{CC}=6.0V	-	-	83	ns/V
ambient temperature	T_{amb}	-	-40	-	+105	℃
AiP74HCT74						
supply voltage	V_{CC}	-	4.5	5.0	5.5	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
input transition rise and fall rate	Δt/ΔV	V_{CC}=2.0V	-	-	-	ns/V
		V_{CC}=4.5V	-	1.67	139	ns/V
		V_{CC}=6.0V	-	-	-	ns/V
ambient temperature	T_{amb}	-	-40	-	+105	℃

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
AiP74HC74							
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	1.2	-	V
		V_{CC}=4.5V		3.15	2.4	-	V
		V_{CC}=6.0V		4.2	3.2	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	0.8	0.5	V
		V_{CC}=4.5V		-	2.1	1.35	V
		V_{CC}=6.0V		-	2.8	1.8	V
HIGH-level output voltage	V_{OH}	V_I=V_{IH} or V_{IL}	I_O=-4.0mA; V_{CC}=4.5V	3.84	4.32	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.34	5.81	-	V
LOW-level output voltage	V_{OL}	V_I=V_{IH} or V_{IL}	I_O=4.0mA; V_{CC}=4.5V	-	0.15	0.33	V
			I_O=5.2mA; V_{CC}=6.0V	-	0.16	0.33	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	40	uA
input capacitance	C_I	-		-	3.5	-	pF
AiP74HCT74							
HIGH-level input voltage	V_{IH}	V_{CC}=4.5V to 5.5V		2.0	1.6	-	V
LOW-level input voltage	V_{IL}	V_{CC}=4.5V to 5.5V		-	1.2	0.8	V
HIGH-level output voltage	V_{OH}	V_I=V_{IH} or V_{IL}	I_O=-4.0mA; V_{CC}=4.5V	3.84	4.32	-	V
LOW-level output voltage	V_{OL}	V_I=V_{IH} or V_{IL}	I_O=5.2mA; V_{CC}=4.5V	-	0.15	0.33	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=5.5V		-	-	±1.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V		-	-	40	uA
additional supply current	ΔI_{CC}	per input pin; V_I=V_{CC}-2.1V; I_O=0A; other inputs at V_{CC} or GND; V_{CC}=4.5V to 5.5V	per input pin; nD, nRD inputs	-	70	315	uA
			per input pin; nSD, nCP input	-	80	360	uA
input capacitance	C_I	-		-	3.5	-	pF

3.3.2、DC Characteristics 2

(T_{amb}=-40℃ to +105℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
AiP74HC74							
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
HIGH-level output voltage	V_{OH}	V_I=V_{IH} or V_{IL}	I_O=-4.0mA; V_{CC}=4.5V	3.7	-	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.2	-	-	V
LOW-level output voltage	V_{OL}	V_I=V_{IH} or V_{IL}	I_O=4.0mA; V_{CC}=4.5V	-	-	0.4	V
			I_O=5.2mA; V_{CC}=6.0V	-	-	0.4	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	80	uA
AiP74HCT74							
HIGH-level input voltage	V_{IH}	V_{CC}=4.5V to 5.5V		2.0	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=4.5V to 5.5V		-	-	0.8	V
HIGH-level output voltage	V_{OH}	V_I=V_{IH} or V_{IL}	I_O=-4.0mA; V_{CC}=4.5V	3.7	-	-	V
LOW-level output voltage	V_{OL}	V_I=V_{IH} or V_{IL}	I_O=5.2mA; V_{CC}=4.5V	-	-	0.4	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=5.5V		-	-	±1.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V		-	-	80	uA
additional supply current	ΔI_{CC}	per input pin; V_I=V_{CC}-2.1V; I_O=0A; other inputs at V_{CC} or GND; V_{CC}=4.5V to 5.5V	per input pin; nD, nRD inputs	-	-	343	uA
			per input pin; nSD, nCP input	-	-	392	uA

3.3.3、AC Characteristics 1

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
AiP74HC74							
nCP to nQ,$n\overline{Q}$ propagation delay	t_{pd}	see Figure 6[1]	V_{CC}=2.0V	-	47	220	ns
			V_{CC}=4.5V	-	17	44	ns
			V_{CC}=5.0V;C_L=15pF	-	14	-	ns
			V_{CC}=6.0V	-	14	37	ns
$n\overline{SD}$ to nQ,$n\overline{Q}$ propagation delay	t_{pd}	see Figure 7[1]	V_{CC}=2.0V	-	50	250	ns
			V_{CC}=4.5V	-	18	50	ns
			V_{CC}=5.0V;C_L=15pF	-	15	-	ns
			V_{CC}=6.0V	-	14	43	ns
$n\overline{RD}$ to nQ,$n\overline{Q}$ propagation delay	t_{pd}	see Figure 7[1]	V_{CC}=2.0V	-	52	250	ns
			V_{CC}=4.5V	-	19	50	ns
			V_{CC}=5.0V;C_L=15pF	-	16	-	ns
			V_{CC}=6.0V	-	15	43	ns
nQ,$n\overline{Q}$ transition time	t_t	see Figure 6[2]	V_{CC}=2.0V	-	19	95	ns
			V_{CC}=4.5V	-	7	19	ns
			V_{CC}=6.0V	-	6	16	ns
CP pulse width	t_W	see Figure 6	V_{CC}=2.0V	100	19	-	ns
			V_{CC}=4.5V	20	7	-	ns
			V_{CC}=6.0V	17	6	-	ns
$n\overline{SD}$, $n\overline{RD}$ pulse width	t_W	see Figure 7	V_{CC}=2.0V	100	19	-	ns
			V_{CC}=4.5V	20	7	-	ns
			V_{CC}=6.0V	17	6	-	ns
$n\overline{SD}$, $n\overline{RD}$ recovery time	t_{rec}	see Figure 7	V_{CC}=2.0V	40	3	-	ns
			V_{CC}=4.5V	8	1	-	ns
			V_{CC}=6.0V	7	1	-	ns
nD to nCP set-up time	t_{su}	see Figure 6	V_{CC}=2.0V	75	6	-	ns
			V_{CC}=4.5V	15	2	-	ns
			V_{CC}=6.0V	13	2	-	ns
nD to nCP hold time	t_h	see Figure 6	V_{CC}=2.0V	3	-6	-	ns
			V_{CC}=4.5V	3	-2	-	ns
			V_{CC}=6.0V	3	-2	-	ns
nCP maximum frequency	f_{max}	see Figure 6	V_{CC}=2.0V	4.8	23	-	MHz
			V_{CC}=4.5V	24	69	-	MHz
			V_{CC}=5.0V;C_L=15pF	-	76	-	MHz
			V_{CC}=6.0V	28	82	-	MHz
power dissipation capacitance	C_{PD}	C_L=50pF;f=1 MHz; V_I= GND to V_{CC}[3]		-	24	-	pF
AiP74HCT74							
nCP to nQ,$n\overline{Q}$ propagation delay	t_{pd}	see Figure 6[1]	V_{CC}=4.5V	-	18	44	ns
			V_{CC}=5.0V;C_L=15pF	-	15	-	ns

$n\overline{SD}$ to nQ,$n\overline{Q}$ propagation delay	t_{pd}	see Figure 7[1]	V_{CC}=4.5V	-	23	50	ns
			V_{CC}=5.0V;C_L=15pF	-	18	-	ns
$n\overline{RD}$ to nQ,$n\overline{Q}$ propagation delay	t_{pd}	see Figure 7[1]	V_{CC}=4.5V	-	24	50	ns
			V_{CC}=5.0V;C_L=15pF	-	18	-	ns
nQ,$n\overline{Q}$ transition time	t_t	see Figure 6[2]	V_{CC}=4.5V	-	7	19	ns
CP pulse width	t_W	see Figure 6	V_{CC}=4.5V	23	9	-	ns
$n\overline{SD}$, $n\overline{RD}$ pulse width	t_W	see Figure 7	V_{CC}=4.5V	20	9	-	ns
$n\overline{SD}$, $n\overline{RD}$ recovery time	t_{rec}	see Figure 7	V_{CC}=4.5V	8	1	-	ns
nD to nCP set-up time	t_{su}	see Figure 6	V_{CC}=4.5V	15	5	-	ns
nD to nCP hold time	t_h	see Figure 6	V_{CC}=4.5V	3	-3	-	ns
CP maximum frequency	f_{max}	see Figure 6	V_{CC}=4.5V	22	54	-	MHz
			V_{CC}=5.0V;C_L=15pF	-	59	-	MHz
power dissipation capacitance	C_{PD}	C_L=50pF;f=1 MHz; V_I= GND to V_{CC}-1.5V[3]		-	29	-	pF

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] t_t is the same as t_{THL} and t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D=(C_{PD}\times V_{CC}^2\times f_i\times N)+\sum(C_L\times V_{CC}^2\times f_o)$ where:

f_i=input frequency in MHz;

f_o=output frequency in MHz;

C_L=output load capacitance in pF;

V_{CC}=supply voltage in V;

N=number of inputs switching;

$\sum(C_L\times V_{CC}^2\times f_o)$=sum of outputs.

3.3.4、AC Characteristics 2

(T_{amb}=-40℃ to +105℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
AiP74HC74							
nCP to nQ,$n\overline{Q}$ propagation delay	t_{pd}	see Figure 6[1]	V_{CC}=2.0V	-	-	265	ns
			V_{CC}=4.5V	-	-	53	ns
			V_{CC}=6.0V	-	-	45	ns
$n\overline{SD}$ to nQ,$n\overline{Q}$ propagation delay	t_{pd}	see Figure 7[1]	V_{CC}=2.0V	-	-	300	ns
			V_{CC}=4.5V	-	-	60	ns
			V_{CC}=6.0V	-	-	51	ns
$n\overline{RD}$ to nQ,$n\overline{Q}$ propagation delay	t_{pd}	see Figure 7[1]	V_{CC}=2.0V	-	-	300	ns
			V_{CC}=4.5V	-	-	60	ns
			V_{CC}=6.0V	-	-	51	ns
nQ,$n\overline{Q}$ transition time	t_t	see Figure 6[2]	V_{CC}=2.0V	-	-	110	ns
			V_{CC}=4.5V	-	-	22	ns
			V_{CC}=6.0V	-	-	19	ns
CP pulse width	t_W	see Figure 6	V_{CC}=2.0V	120	-	-	ns
			V_{CC}=4.5V	24	-	-	ns
			V_{CC}=6.0V	20	-	-	ns
$n\overline{SD}$, $n\overline{RD}$ pulse width	t_W	see Figure 7	V_{CC}=2.0V	120	-	-	ns
			V_{CC}=4.5V	24	-	-	ns
			V_{CC}=6.0V	20	-	-	ns
$n\overline{SD}$, $n\overline{RD}$ recovery time	t_{rec}	see Figure 7	V_{CC}=2.0V	45	-	-	ns
			V_{CC}=4.5V	9	-	-	ns
			V_{CC}=6.0V	8	-	-	ns
nD to nCP set-up time	t_{su}	see Figure 6	V_{CC}=2.0V	90	-	-	ns
			V_{CC}=4.5V	18	-	-	ns
			V_{CC}=6.0V	15	-	-	ns
nD to nCP hold time	t_h	see Figure 6	V_{CC}=2.0V	3	-	-	ns
			V_{CC}=4.5V	3	-	-	ns
			V_{CC}=6.0V	3	-	-	ns
nCP maximum frequency	f_{max}	see Figure 6	V_{CC}=2.0V	4.0	-	-	MHz
			V_{CC}=4.5V	20	-	-	MHz
			V_{CC}=6.0V	24	-	-	MHz
AiP74HCT74							
nCP to nQ,$n\overline{Q}$ propagation delay	t_{pd}	see Figure 6[1]	V_{CC}=4.5V	-	-	53	ns
$n\overline{SD}$ to nQ,$n\overline{Q}$ propagation delay	t_{pd}	see Figure 7[1]	V_{CC}=4.5V	-	-	60	ns
$n\overline{RD}$ to nQ,$n\overline{Q}$ propagation delay	t_{pd}	see Figure 7[1]	V_{CC}=4.5V	-	-	60	ns
nQ,$n\overline{Q}$ transition time	t_t	see Figure 6[2]	V_{CC}=4.5V	-	-	22	ns

CP pulse width	t_W	see Figure 6	V_{CC}=4.5V	27	-	-	ns
$\overline{nSD}$, $\overline{nRD}$ pulse width	t_W	see Figure 7	V_{CC}=4.5V	24	-	-	ns
$\overline{nSD}$, $\overline{nRD}$ recovery time	t_{rec}	see Figure 7	V_{CC}=4.5V	9	-	-	ns
nD to nCP set-up time	t_{su}	see Figure 6	V_{CC}=4.5V	18	-	-	ns
nD to nCP hold time	t_h	see Figure 6	V_{CC}=4.5V	3	-	-	ns
CP maximum frequency	f_{max}	see Figure 6	V_{CC}=4.5V	18	-	-	MHz

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] t_t is the same as t_{THL} and t_{TLH}.

4、Testing Circuit

4.1、AC Testing Circuit

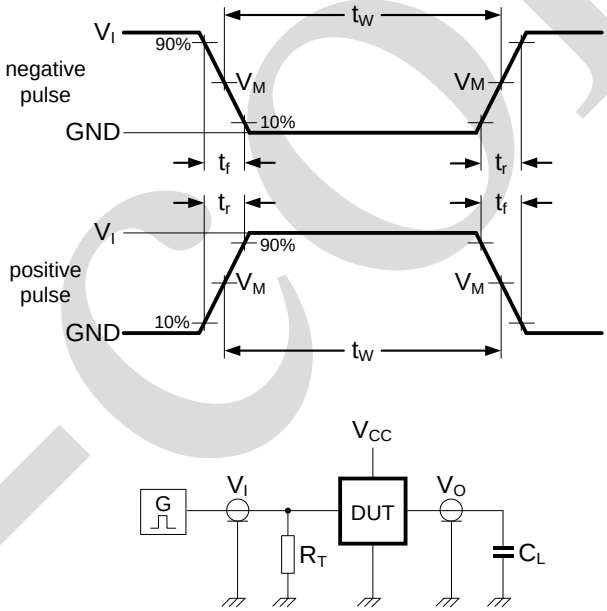


Figure 5. Test circuit for measuring switching times

Definitions for test circuit:

C_L=load capacitance including jig and probe capacitance.

R_T=termination resistance should be equal to the output impedance Z_o of the pulse generator.

4.2、AC Testing Waveforms

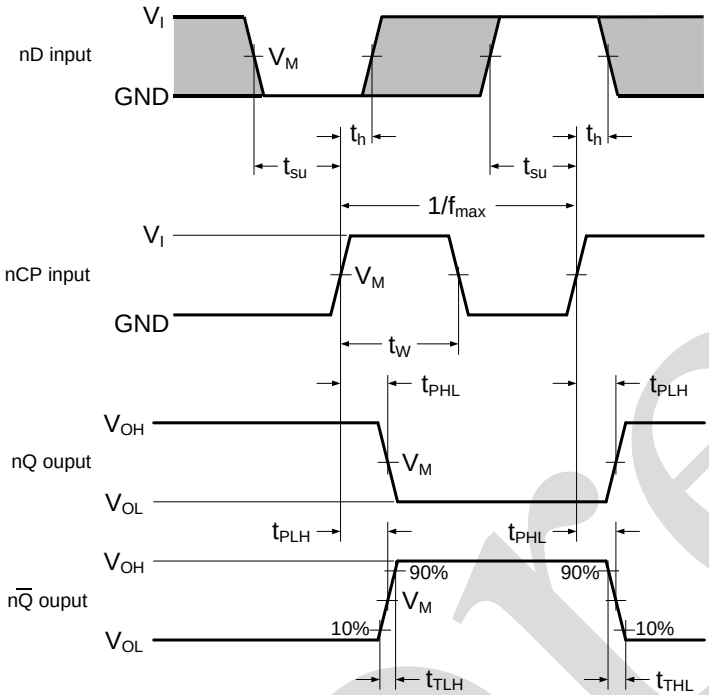


Figure 6. Input to output propagation delays

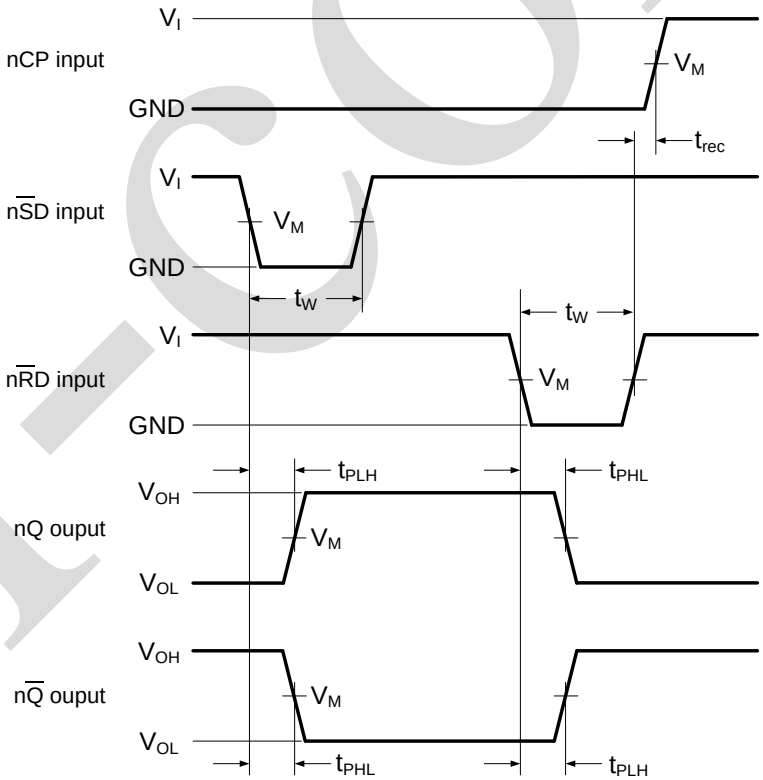


Figure 7. Set and reset propogation delays, pulse widths and recovery time

4.3、Measurement Points

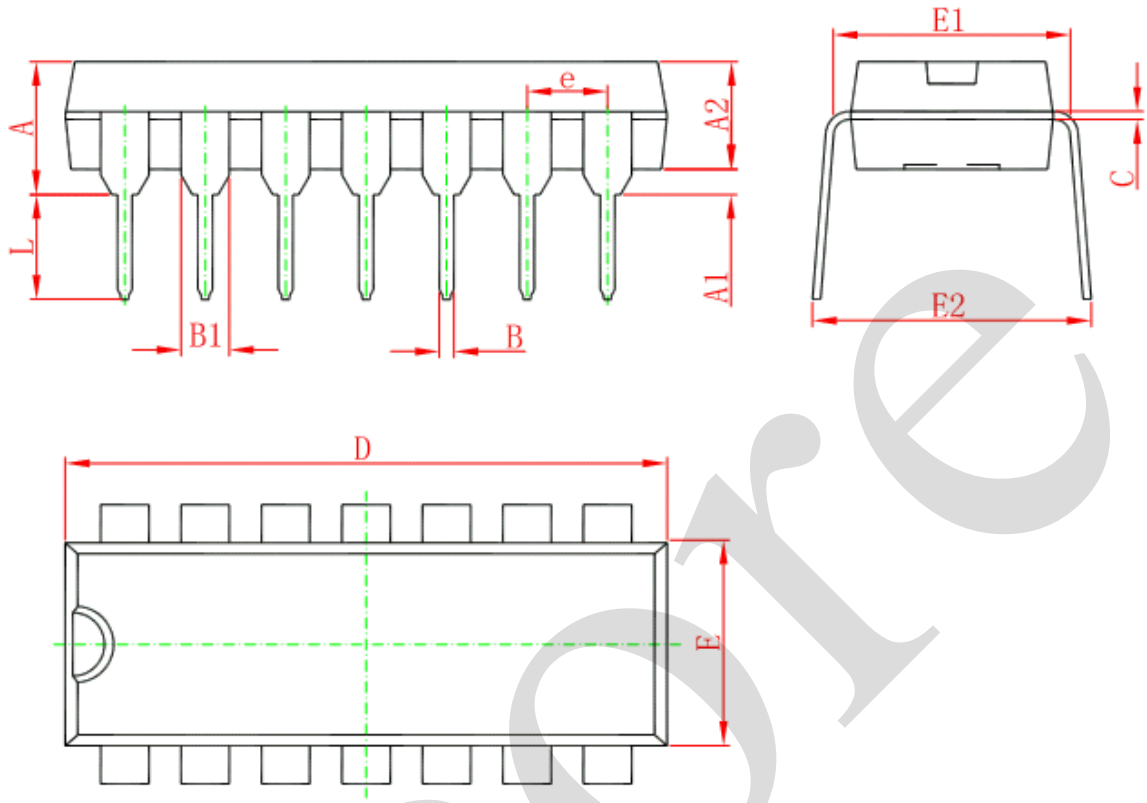
Type	Input	Output
	V_M	V_M
AiP74HC74	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
AiP74HCT74	1.3V	1.3V

4.4、Test Data

Type	Input		Load		Test
	V_I	t_r , t_f	C_L	R_L	
AiP74HC74	V_{CC}	6.0ns	15pF, 50pF	1kΩ	t_{PLH}, t_{PHL}
AiP74HCT74	3.0V	6.0ns	15pF, 50pF	1kΩ	t_{PLH}, t_{PHL}

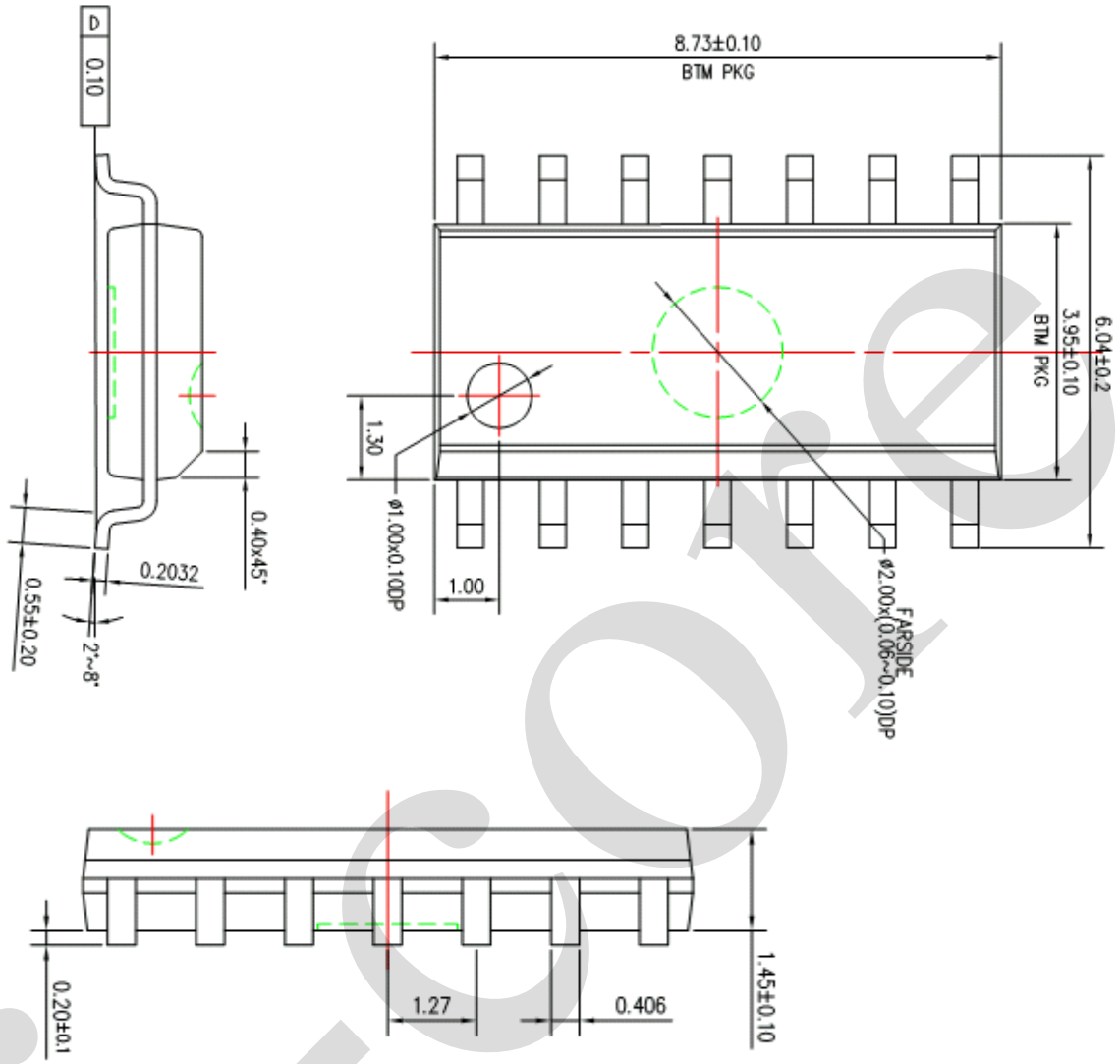
5、Package Information

5.1、DIP14

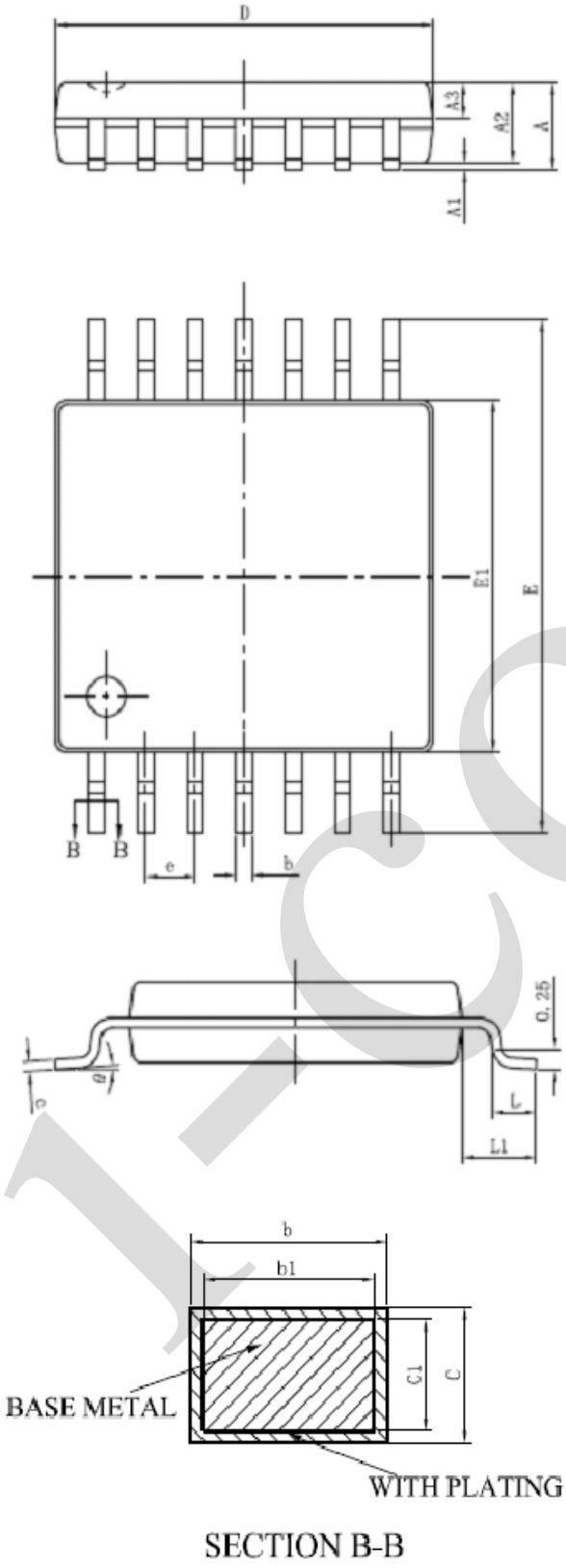


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524 (BSC)		0.060 (BSC)	
C	0.204	0.360	0.008	0.014
D	18.800	19.200	0.740	0.756
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540 (BSC)		0.100 (BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

5.2、SOP14


0.10
8.73±0.10
BTM PKG
6.04±0.2
3.95±0.10
BTM PKG
1.30
Ø1.00x0.100P
1.00
Ø2.00x(0.06~0.10)DP
FARSIDE
0.40x45°
0.2032
0.55±0.20
2°~8°
0.20±0.1
1.27
0.406
1.45±0.10

5.3、TSSOP14



SECTION B-B

SYMBOL	MILLIMETER	
	MIN	MAX
A	—	1.20
A1	0.05	0.15
A2	0.90	1.05
A3	0.39	0.49
b	0.20	0.30
b1	0.19	0.25
c	0.13	0.19
c1	0.12	0.14
D	4.86	5.06
E1	4.30	4.50
E	6.20	6.60
e	0.65BSC	
L	0.45	0.75
L1	1.00BSC	
θ	0	8°

6、Statements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

6.2、Notion

Recommended carefully reading this information before the use of this product;

The information in this document are subject to change without notice;

This information is using to the reference only, the company is not responsible for any loss;

The company is not responsible for the any infringement of the third party patents or other rights of the responsibility.