# RTL8812FR-CG

# Single-Chip 802.11ac/a/n 2T2R WLAN
## With PCI Express Interface

## DATASHEET
**(CONFIDENTIAL: Development Partners Only)**

**Rev. 0.1**
**13 , Feb., 2010**
**Track ID:**


**Realtek Semiconductor Corp.**
**No. 2, Innovation Road II, Hsinchu Science Park, Hsinchu 300, Taiwan**
**Tel.: +886-3-578-0211. Fax: +886-3-577-6047**
**www.realtek.com**

## COPYRIGHT



## DISCLAIMER

Realtek provides this document 'as is', without warranty of any kind. Realtek may make improvements and/or changes in this document or in the product described in this document at any time. This document could include technical inaccuracies or typographical errors.

## TRADEMARKS

Realtek is a trademark of Realtek Semiconductor Corporation. Other names mentioned in this document are trademarks/registered trademarks of their respective owners.

## USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

## ELECTROSTATIC DISCHARGE (ESD) WARNING

This product can be damaged by Electrostatic Discharge (ESD). When handling, care must be taken. Damage due to inappropriate handling is not covered by warranty.

Do not open the protective conductive packaging until you have read the following, and are at an approved anti-static workstation.

- Use an approved anti-static mat to cover your work surface.
- Use a conductive wrist strap attached to a good earth ground
- Always discharge yourself by touching a grounded bare metal surface or approved anti-static mat before picking up an ESD-sensitive electronic component
- If working on a prototyping board, use a soldering iron or station that is marked as ESD-safe
- Always disconnect the microcontroller from the prototyping board when it is being worked on

## REVISION HISTORY

| Revision | Release Date | Summary |
|---|---|---|
| 0.1 | 2018/06/13 | Preliminary release. |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |

# Table of Contents

# List of Tables



# List of Figures

# 1. General Description

The Realtek RTL8812FR-CG is a highly integrated single-chip that support 2-stream 802.11ac solutions with Multi-user MIMO (Multiple-Input, Multiple-Output) with Wireless LAN (WLAN) PCI Express network interface. It combines a WLAN MAC, a 2T2R capable WLAN baseband, and RF in a single chip.

The RTL8812FR-CG baseband implements Multi-user Multiple Input, Multiple Output (MU-MIMO) Orthogonal Frequency Division Multiplexing (OFDM) with two transmit and two receive paths (2T2R). Features include two spatial stream transmissions, short Guard Interval (GI) of 400ns, spatial spreading, and support for variant channel bandwidth. Moreover, RTL8812FR-CG provides one spatial stream space-time block code (STBC), Transmit Beamforming (TxBF) and Low Density Parity Check (LDPC) to extend the range of transmission. At the receiver, extended range and good minimum sensitivity is achieved by having receiver diversity up to 2 antennas. As the recipient, the RTL8812FR-CG also supports explicit sounding packet feedback that helps senders with beamforming capability.

For legacy compatibility, Direct Sequence Spread Spectrum (DSSS), Complementary Code Keying (CCK) and OFDM baseband processing are included to support all IEEE 802.11b, 802.11g and 802.11a data rates. Differential phase shift keying modulation schemes, DBPSK and DQPSK with data scrambling capability are available, and CCK provides support for legacy data rates, with long or short preamble. The high speed FFT/IFFT paths, combined with BPSK, QPSK, 16QAM, 64QAM and 256QAM modulation of the individual subcarriers, and rate compatible coding rate of 1/2, 2/3, 3/4, and 5/6, provide up to 866.7Mbps for IEEE 802.11ac MIMO OFDM.

The RTL8812FR-CG builds in an enhanced signal detector, an adaptive frequency domain equalizer, and a soft-decision Viterbi decoder to alleviate severe multi-path effects and mutual interference in the reception of multiple streams. For better detection quality, receive diversity with Maximal-Ratio-Combine (MRC) applying up to two receive paths, and Maximum-Likelihood Detection (MLD) are implemented. Robust interference detection and suppression are provided to protect against Bluetooth, cordless phone, and microwave oven interference.

Receive vector diversity for multi-stream application is implemented for efficient utilization of the MIMO channel. Efficient IQ-imbalance, DC offset, phase noise, frequency offset, and timing offset compensations are provided for the radio frequency front-end.

The RTL8812FR-CG supports fast receiver Automatic Gain Control (AGC) with synchronous and asynchronous control loops among antennas, antenna diversity functions, and adaptive transmit power control functions to obtain better performance in the analog portions of the transceiver.

The RTL8812FR-CG MAC supports 802.11e for multimedia applications, 802.11i and WAPI (Wireless Authentication Privacy Infrastructure) for security, and 802.11n/802.11ac for enhanced MAC protocol

efficiency. Using packet aggregation techniques such as A-MPDU with BA and A-MSDU, protocol efficiency is significantly improved. Power saving mechanisms such as Legacy Power Save, U-APSD, and MIMO power saving reduce the power wasted during idle time, and compensate for the extra power required to transmit MIMO OFDM. The RTL8812FR-CG provides simple legacy, 20MHz/40MHz/80MHz co-existence mechanisms to ensure backward and network compatibility.

# 2. Features

### General

- 56-pin QFN
- CMOS MAC, Baseband PHY and RF in a single chip for IEEE 802.11a/b/g/n/ac compatible WLAN
- Support 802.11ac 2x2,Wave-2 compliant with MU-MIMO
- Complete 802.11n MIMO solution for 5Ghz band
- Maximum PHY data rate up to 173.3 Mbps using 20MHz bandwidth, 400Mbps using 40MHz bandwidth, and 866.7Mbps using 80MHz bandwidth.
- Backward compatible with 802.11a/b/g devices while operating at 802.11n data rates
- Backward compatible with 802.11a/n devices while operating at 802.11ac data rates.

### Host Interface

- Complies with PCI Express Base Specification Revision 2.1

### Standards Supported

- IEEE 802.11a/b/g/n/ac compatible WLAN
- IEEE 802.11e QoS Enhancement (WMM)
- IEEE 802.11i (WPA, WPA2). Open, shared key, and pair-wise key authentication services
- IEEE 802.11h DFS, TPC, Spectrum Measurement
- IEEE 802.11k Radio Resource Measurement
- WAPI (Wireless Authentication Privacy Infrastructure) certified.

### MAC Features

- Frame aggregation for increased MAC efficiency (A-MSDU, A-MPDU)
- Low latency immediate Block Acknowledgement (BA)
- Long NAV for media reservation with CF-End for NAV release
- PHY-level spoofing to enhance legacy compatibility
- MIMO power saving mechanism
- Channel management and co-existence
- Multiple BSSID feature allows the RTL8812FR-CG to assume multiple MAC identities when used as a wireless bridge
- Transmit Opportunity (TXOP) Short Inter-Frame Space (SIFS) bursting for higher multimedia bandwidth
- WiFi Direct supports wireless peer to peer applications.

### Other Features

- Supports Wake-On-WLAN via Magic Packet and Wake-up frame
- Transmit Beamforming
- Support S3/S4 AES/TKIP group key update
- Support Network List Offload
- CCA on secondary through RTS/CTS handshake.
- Support TCP/UDP/IP checksum offload

### Peripheral Interfaces

- One configurable LED pins
- Generates 40MHz clock for peripheral chip.
- Single external power source 3.3V only

### PHY Features

- IEEE 802.11ac MIMO OFDM
- IEEE 802.11n MIMO OFDM
- Two Transmit and Two Receive paths
- 5MHz / 10MHz / 20MHz / 40MHz / 80MHz bandwidth transmission
- Support 5Ghz band channels
- Short Guard Interval (400ns)
- Sounding packet.
- DSSS with DBPSK and DQPSK, CCK modulation with long and short preamble
- OFDM with BPSK, QPSK, 16QAM, 64QAM and 256QAM modulation. Convolutional Coding Rate: 1/2, 2/3, 3/4, and 5/6

- Maximum data rate 54Mbps in 802.11g, 300Mbps in 802.11n and 866.7bps in 802.11ac.
- OFDM receive diversity with MRC using up to 2 receive paths. Switch diversity used for DSSS/CCK
- Support STBC
- Support LDPC
- Hardware antenna diversity
- Maximum-Likelihood Detection (MLD)
- Fast receiver Automatic Gain Control (AGC)
- On-chip ADC and DAC
- Build-in both 5GHz PA
- Build-in both 5GHz LNA

**Peripheral Interfaces**

- Flexible Crystal frequency selection(52, 48, 40, 38.4, 27, 26, 25, 24, 20, 19.2, 17.664, 16, 14.318, 13 and 12MHz)
- Support Crystal or external clock input

# 3. Application Diagrams

## *3.1. 11ac Dual-Band 2x2 RF Application*

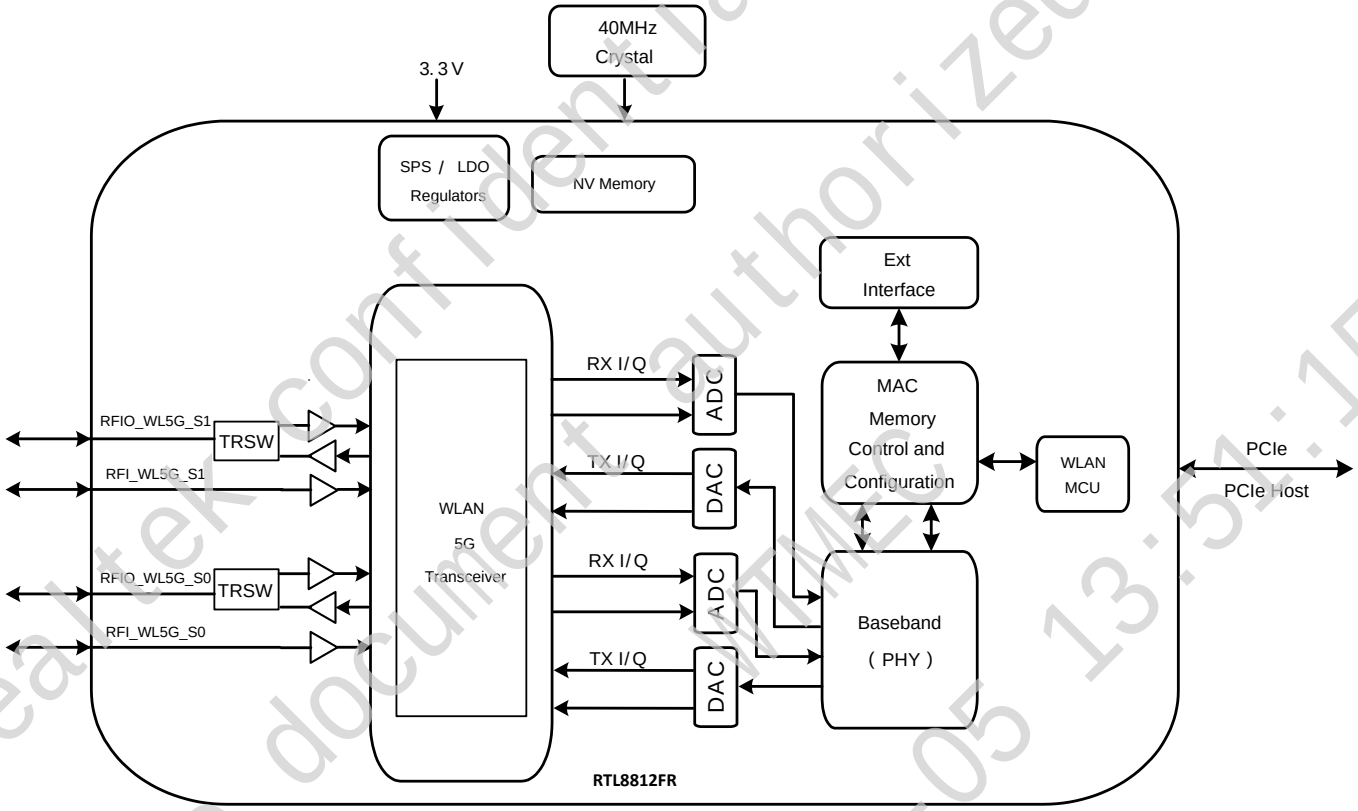



**Figure 1. Dual-Band MIMO 2x2 Solution(11ac 2x2 MAC/BB/RF + PA) Solution --- RTL8812FR-CG**

# 4. Pin Assignments

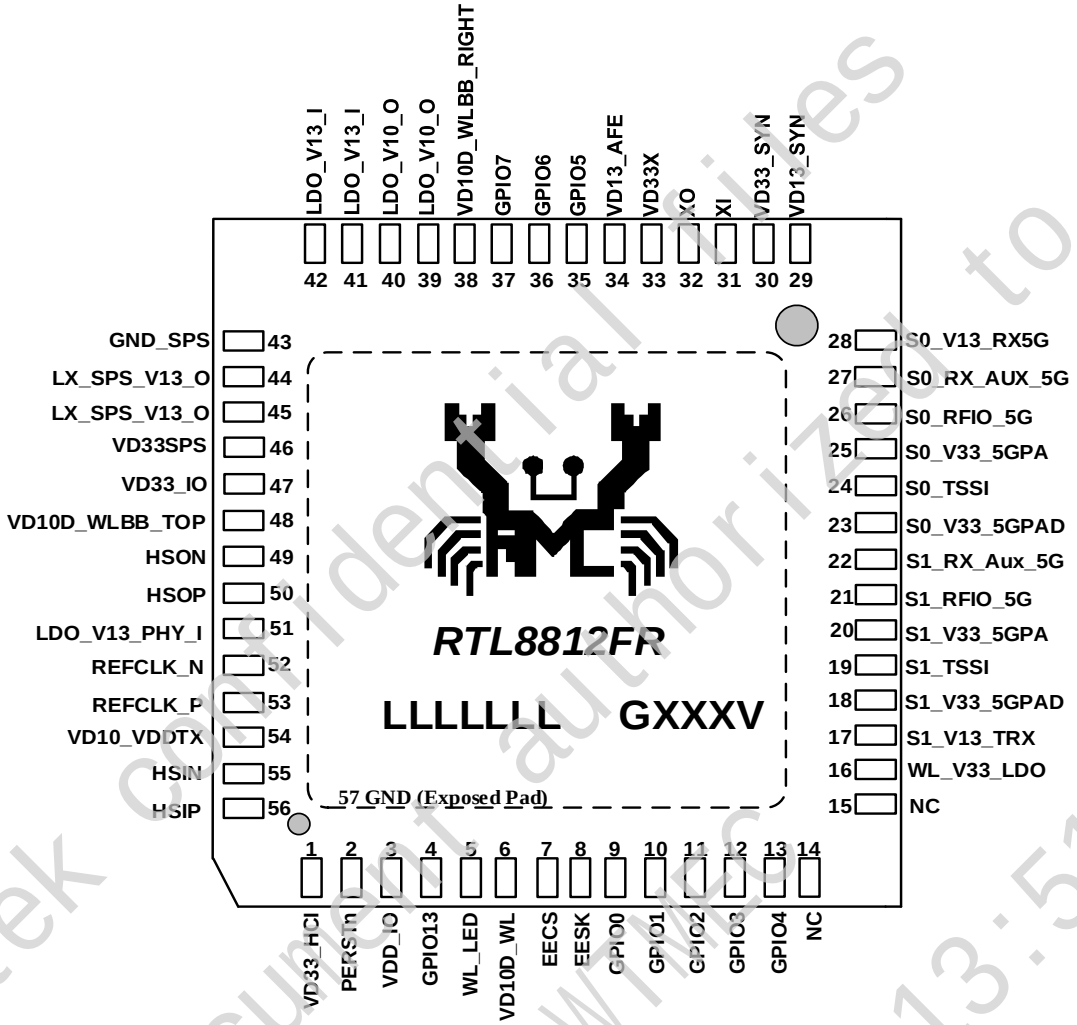



**Figure 2. Pin Assignments**

## 4.1. Package Identification & Mark Information

Green package is indicated by a 'G' in the location marked 'V' in Figure2The version is shown in the location marked 'V'.



# 5. Pin Descriptions

The following signal type codes are used in the tables:

| | | | |
|---|---|---|---|
| I: | Input | O: | Output |
| T/S: | Tri-State bi-directional input/output pin | S/T/S: | Sustained Tri-State |
| O/D: | Open Drain | P: | Power pin |
| N/A: | No Bonding pin | | |

## 5.1. Power On Trap Pin

**Table 1. Power-On Trap Pins**

| Symbol | Type | Pin No | Description |
|---|---|---|---|
| TEST_MODE_SEL | I | 13 | Shared with GPIO4<br>0: Normal operation mode<br>1: Test/debug mode |

## 5.2. PCI Express Transceiver Interface

**Table 2. PCI Express Transceiver Interface**

| Symbol | Type | Pin No | Description | Voltage |
|---|---|---|---|---|
| HSIN/HSIP | I | 55,56 | PCI Express Receive Differential Pair | |
| HSON/HSOP | O | 49,50 | PCI Express Transmit Differential Pair | |

| Symbol | Type | Pin No | Description | Voltage |
|---|---|---|---|---|
| REFCLK_N/REFCLK_P | I | 52,53 | PCI Express Differential Reference Clock Source: 100MHz ± 300ppm | |
| PERST# | I | 2 | PCI Express Reset Signal: active low.<br>When the PERST# is asserted at power-on state, the RTL8812FR-CG returns to a pre-defined reset state and is ready for initialization and configuration after the de-assertion of the PERST#. | 3.3V |

## 5.3. RF Interface

**Table 3. RF Interface**

| Symbol | Type | Pin No | Description |
|---|---|---|---|
| S1_TSSI | I | 19 | TSSI input from external PA/FEM |
| S1_RFIO_5G | ● /O | 21 | WLAN 5G RF input/output for path S1 |
| S1_RX_AUX_5G | I | 22 | WLAN 5G RF input for path S1 in external FEM configuration |
| S0_TSSI | I | 24 | TSSI input from external PA/FEM |
| S0_RFIO_5G | I/O | 26 | WLAN 5G RF input/output for path S0 |
| S0_RX_AUX_5G | I | 27 | WLAN 5G RF input for path S0 in external FEM configuration |

## 5.4. LED Interface

**Table 4. LED Interface**

| Symbol | Type | Pin No | Description |
|---|---|---|---|
| WL_LED | O | 5 | WL LED Pin (Active Low), shared with GPIO8 |

## 5.5. Clock and Other Pins

**Table 5. Clock and Other Pins**

| Symbol | Type | Pin No | Description |
|---|---|---|---|
| XI | I | 31 | 40MHz OSC Input<br>40MHz crystal reference clock input |
| XO | O | 32 | 40MHz Crystal reference clock output |
| EECS | I | 7 | RTC clock input |
| EESK | I | 8 | WLAN eFuse autoload |
| GPIO0 | IO | 9 | General Purpose Input/Output Pin |
| GPIO1 | IO | 10 | General Purpose Input/Output Pin |
| GPIO2 | IO | 11 | General Purpose Input/Output Pin |
| GPIO3 | IO | 12 | General Purpose Input/Output Pin |

| Symbol | Type | Pin No | Description |
|---|---|---|---|
| GPIO4 | IO | 13 | General Purpose Input/Output Pin |
| GPIO5 | IO | 35 | General Purpose Input/Output Pin |
| GPIO6 | IO | 36 | General Purpose Input/Output Pin |
| GPIO7 | IO | 37 | General Purpose Input/Output Pin |
| GPIO8 | IO | 5 | General Purpose Input/Output Pin |
| GPIO13 | IO | 4 | General Purpose Input/Output Pin |
| NC | | 14,15 | No connect. |

## 5.6. HCI Power Pins

**Table 6. HCI Power Pins**

| Symbol | Type | Pin No | Description |
|---|---|---|---|
| LDO_V13_PHY_I | P | 51 | LDO 1.3V PHY Input |
| VD10_VDDTX | P/I | 54 | 1.05V for analog circuits in interface |
| VD33_HCI | P | 1 | 3.3V for HCI |

## 5.7. Digital Power Pins

**Table 7. Digital Power Pins**

| Symbol | Type | Pin No | Description |
|---|---|---|---|
| VD33_IO | P | 47 | VDD3.3V for Digital IO (PERST#,WL_LED) |
| VDD_IO | P | 3 | VDD for GPIO[0:7], GPIO13 , EESK |
| VD10D_WLBB_TOP / VD10D_WLBB_RIGHT | P | 48,38 | 1.05V for WLAN BB digital power |
| VD10D_WL | P | 6 | 1.05V for WLAN digital power |

## 5.8. REGU Power Pins

**Table 8. REGU Power Pins**

| Symbol | Type | Pin No | Description |
|---|---|---|---|
| LX_SPS_V13_O | P | 44,45 | Switching Regulator 1.3V Output |
| VD33SPS | P | 46 | Switching Regulator Input<br>Or Linear Regulator input from 3.3V to 1.5V |
| LDO_V13_I | P | 41,42 | LDO 1.3V Input |
| LDO_V10_O | P | 39,40 | LDO 1.05 Output |
| GND_SPS | P | 43 | Switching Regulator Ground |

## 5.9. RF Power Pins

Table 9. RF Power Pins

| Symbol | Type | Pin No | Description |
|---|---|---|---|
| WL_V33_LDO | P | 16 | VDD 3.3V for internal LDO input |
| S1_V13_TRX | P | 17 | VDD 1.3V for S1 WLAN RF |
| S1_V33_5GPAD | P | 18 | VDD 3.3V for S1 5G WLAN PAD |
| S1_V33_5GPA | P | 20 | VDD 3.3V for S1 5G WLAN PA |
| S0_V33_5GPAD | P | 23 | VDD 3.3V for S0 5G WLAN PAD |
| S0_V33_5GPA | P | 25 | VDD 3.3V for S0 5G WLAN PA |
| S0_V13_RX5G | P | 28 | VDD 1.3V for S0 WLAN RF |
| V13_SYN | P | 29 | VDD 1.3V for WLAN synthesizer |
| V33_SYN | P | 30 | VDD 3.3V for WLAN synthesizer |
| VD33X | P | 33 | VDD 3.3V for Crystal |
| V13_AFE | P | 34 | VDD 1.3V for WLAN AFE |

# 6. Electrical and Thermal Characteristics

## *6.1. Temperature Limit Ratings*

**Table 10. Temperature Limit Ratings**

| Parameter | Minimum | Maximum | Units |
|---|---|---|---|
| Storage Temperature | -55 | +125 | °C |
| Ambient Operating Temperature | 0 | 70 | °C |
| Junction Temperature | 0 | 125 | °C |

## 6.2. DC Characteristics

### 6.2.1. Power Supply Characteristics

**Table 11. DC Characteristics**

| Symbol | Parameter | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| VD33 | 3.3V I/O Supply Voltage | 3.0 | 3.3 | 3.6 | V |
| VD10 | 1.05V Core Supply Voltage | 0.945 | 1.05 | 1.155 | V |

### 6.2.2. Digital IO Pin DC Characteristics

**Table 12. 3.3V IO DC Characteristics**

| Symbol | Parameter | Minimum | Normal | Maximum | Units |
|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | 2.0 | 3.3 | 3.6 | V |
| $V_{IL}$ | Input low voltage | -- | 0 | 0.9 | V |
| $V_{OH}$ | Output high voltage | 2.97 | -- | 3.3 | V |
| $V_{OL}$ | Output low voltage | 0 | -- | 0.33 | V |

**Table 13. 1.8V IO DC Characteristics**

| Symbol | Parameter | Minimum | Normal | Maximum | Units |
|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | 1.7 | 1.8 | 3.6 | V |
| $V_{IL}$ | Input low voltage | -- | 0 | 0.8 | V |
| $V_{OH}$ | Output high voltage | 1.62 | -- | 1.8 | V |
| $V_{OL}$ | Output low voltage | 0 | -- | 0.18 | V |

# 7. Interface Timing Specification

## *7.1. PCIe Bus during Power On Sequence*

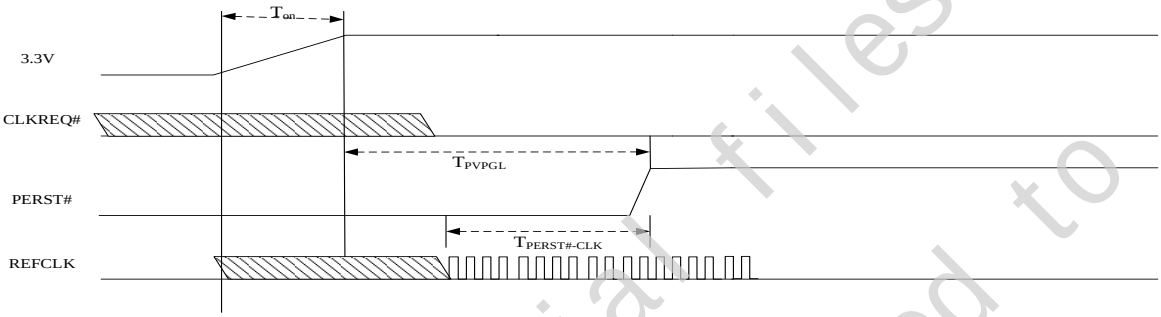



**Figure 3. RTL8812FR-CG PCIe Bus Power On Sequence**

**$T_{on}$:** The main power ramp up duration

**$T_{PVPGL}$:** Power valid to PERST# input inactive

**$T_{PERST\#-CLK}$:** Reference clock stable before PERST# inactive

| Symbol | Unit | Min | Typical | Max |
|---|---|---|---|---|
| $T_{on}$ | ms | 0.5 | 1.5 | 5 |
| $T_{PVPGL}$ | ms | Implementation specific;recommended 50ms | | -- |
| $T_{PERST\#-CLK}$ | us | 100 | | -- |

**Table 14. The typical timing range**

## 7.2. PCIe PERST# Timing Sequence

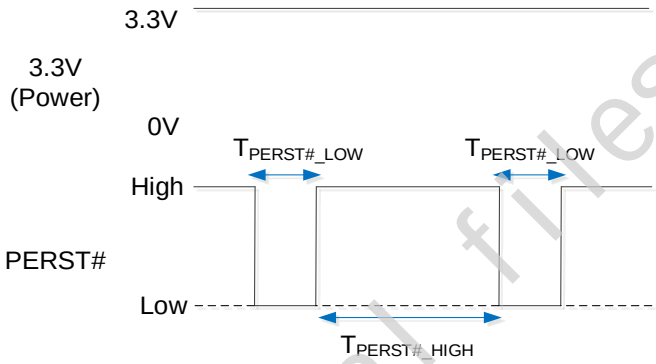



**Table 15. RTL8812FR-CG PCIE PERST# Timing Parameters**

| | Min | Typical | Max | Unit | Description |
|---|---|---|---|---|---|
| $T_{PERST\#\_LOW}$ | 6 | 10 | X | ms | PERST# low duration |
| $T_{PERST\#\_HIGH}$ | 400 | 500 | X | ms | PERST# high duration |

## 7.3. Power Off Sequence

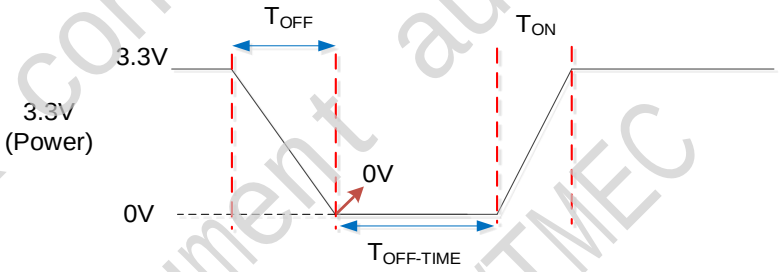



**Figure 4. RTL8812FR-CG Power Off Sequence**

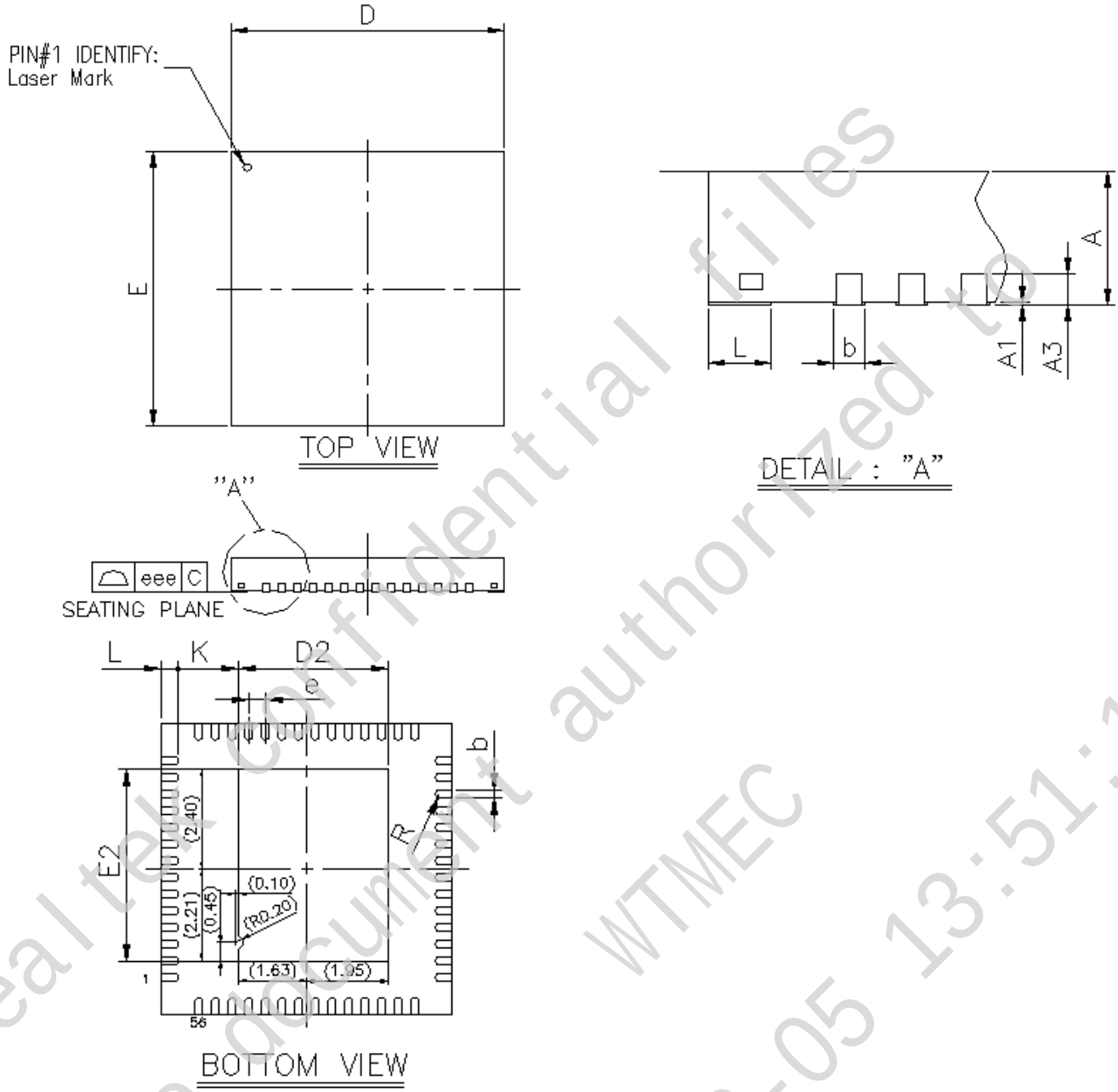
**Table 16. RTL8812FR-CG Power Off Timing Parameters**

| Symbol | Unit | Min | Typical | Max |
|---|---|---|---|---|
| $T_{OFF}$ | ms | 5 | 20 | 50 |
| $T_{OFF-TIME}$ | ms | 500 | -- | -- |
| $T_{ON}$ | ms | 0.5 | 1.5 | 5 |

## 7.4. Platform state transitions

| 3.3V Power range | 3.3V Ripple | 3.3V Noise | Rise time | |
|---|---|---|---|---|
| | | | Min | Max |
| +/-0.165V | 300mVpp @ switching frequency > 400KHz | | 0.5ms | 5ms |

# 8. Mechanical Dimensions




| Symbol | Dimension in mm | | | Dimension in inch | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | 0.80 | 0.85 | 0.90 | 0.031 | 0.033 | 0.035 |
| $A_1$ | 0.00 | 0.02 | 0.05 | 0.000 | 0.001 | 0.002 |
| $A_3$ | 0.2 REF | | | 0.008 REF | | |
| b | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| D/E | 7.00 BSC | | | 0.276 BSC | | |
| $D_2$ | 3.48 | 3.58 | 3.68 | 0.137 | 0.141 | 0.145 |
| $E_2$ | 4.51 | 4.61 | 4.71 | 0.178 | 0.181 | 0.185 |
| e | 0.40 BSC | | | 0.016 BSC | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| L | 0.30 | 0.40 | 0.50 | 0.012 | 0.016 | 0.020 |

Notes：

1. CONTROLLING DIMENSION：MILLIMETER(mm).
2. REFERENCE DOCUMENTL：JEDEC MO-220.

# 9. Ordering Information

**Table 17. Ordering Information**

| Part Number | Package | Status |
|---|---|---|
| RTL8812FR-CG | QNF56 , 'Green' Package | To be available |

Hsinchu 300, Taiwan, R.O.C.
Tel: 886-3-5780211  Fax: 886-3-5776047
www.realtek.com