SGM2056
1.2A, 7V, High PSRR, Ultra-Low Noise, Ultra-Low Dropout Linear Regulator

GENERAL DESCRIPTION

The SGM2056 is a high current, high PSRR, ultra-low noise and ultra-low dropout voltage linear regulator. It is capable of supplying 1.2A output current with typical dropout voltage of only 85mV. The operating input voltage range is from 1.1V to 7V. The adjustable output voltage range is from 0.8V to 5.5V by using an external resistor divider.

Other features include logic-controlled shutdown mode, short-circuit current limit and thermal shutdown protection. The SGM2056 has automatic discharge function to quickly discharge V_{OUT} in the disabled status.

The SGM2056 is available in a Green TDFN-3×3-8DL package. It operates over an operating temperature range of -40℃ to +125℃.

FEATURES

- **Operating Input Voltage Range: 1.1V to 7V**
- **Output Voltage Range: 0.8V to 5.5V**
- **1.2A Output Current**
- **Ultra-Low Dropout Voltage: 85mV (TYP) at 1.2A**
- **Ultra-Low Noise: 6.5μV_{RMS} (TYP) at V_{OUT} = 0.8V**
- **High PSRR: 50dB (TYP) at 500kHz**
- **Current Limiting and Thermal Protection**
- **With Output Automatic Discharge**
- **Programmable Soft-Start Output**
- **Support Power-Good Indicator Function**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in a Green TDFN-3×3-8DL Package**

APPLICATIONS

Portable Electronics
Wireless Devices
AD-DC/DC-DC Power Module

TYPICAL APPLICATION

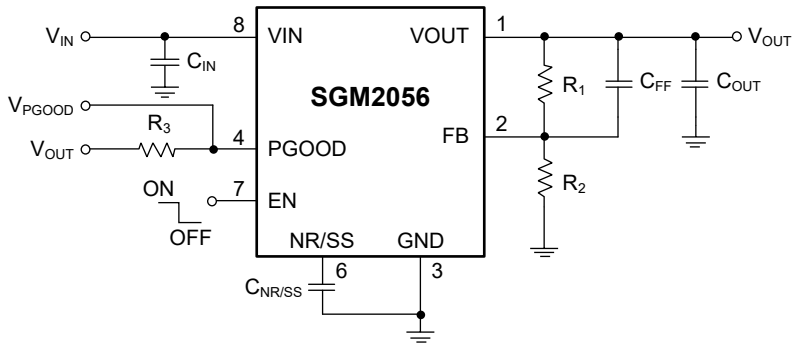


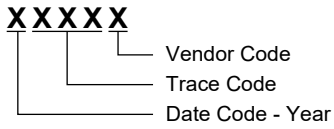
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM2056	TDFN-3×3-8DL	-40℃ to +125℃	SGM2056XTEU8G/TR	SGM 2056EU XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VIN, PGOOD, EN to GND ..... -0.3V to 8V
VOUT to GND ..... -0.3V to MIN(V_{IN} + 0.3V, 8V)
NR/SS, FB to GND ..... -0.3V to 3.6V
Package Thermal Resistance
TDFN-3×3-8DL, θ_{JA} ..... 65℃/W
TDFN-3×3-8DL, θ_{JB} ..... 27℃/W
TDFN-3×3-8DL, θ_{JC} ..... 50℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 5000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range ..... 1.1V to 7V
Enable Input Voltage Range ..... 0V to 7V
Input Effective Capacitance, C_{IN} ..... 10μF (MIN)
Output Effective Capacitance, C_{OUT} ..... 9μF to 1000μF
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

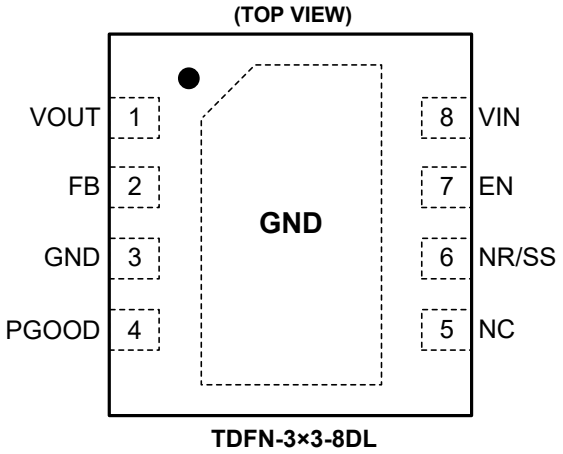
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	FUNCTION
1	VOUT	Regulator Output Pin. It is recommended to use a ceramic capacitor with effective capacitance in the range of 9μF to 1000μF to ensure stability. This ceramic capacitor should be placed as close as possible to VOUT pin.
2	FB	Feedback Voltage Input Pin. Connect this pin to the midpoint of an external resistor divider to adjust the output voltage. Place the resistors as close as possible to this pin.
3	GND	Ground.
4	PGOOD	Power-Good Indicator Output Pin. An open-drain, active-high output that indicates the status of V_{OUT}. When the output voltage reaches 89% of the target, the PG pin goes into a high-impedance state.
5	NC	No Internal Connection. Connect this pin to ground or leave it floating.
6	NR/SS	Noise-Reduction and Soft-Start Pin. Connecting an external capacitor $C_{NR/SS}$ between this pin and GND can reduce the output noise and slow down the V_{OUT} rise to achieve soft starting.
7	EN	Enable Control Input Pin. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator.
8	VIN	Input Voltage Supply Pin. It is recommended to use a 10μF or larger ceramic capacitor from VIN pin to ground to get good power supply decoupling. This ceramic capacitor should be placed as close as possible to VIN pin.
Exposed Pad	GND	Exposed Pad. Connect it to GND internally. Connect it to a large ground plane to maximize thermal performance. This pad is not an electrical connection point.

FUNCTIONAL BLOCK DIAGRAM

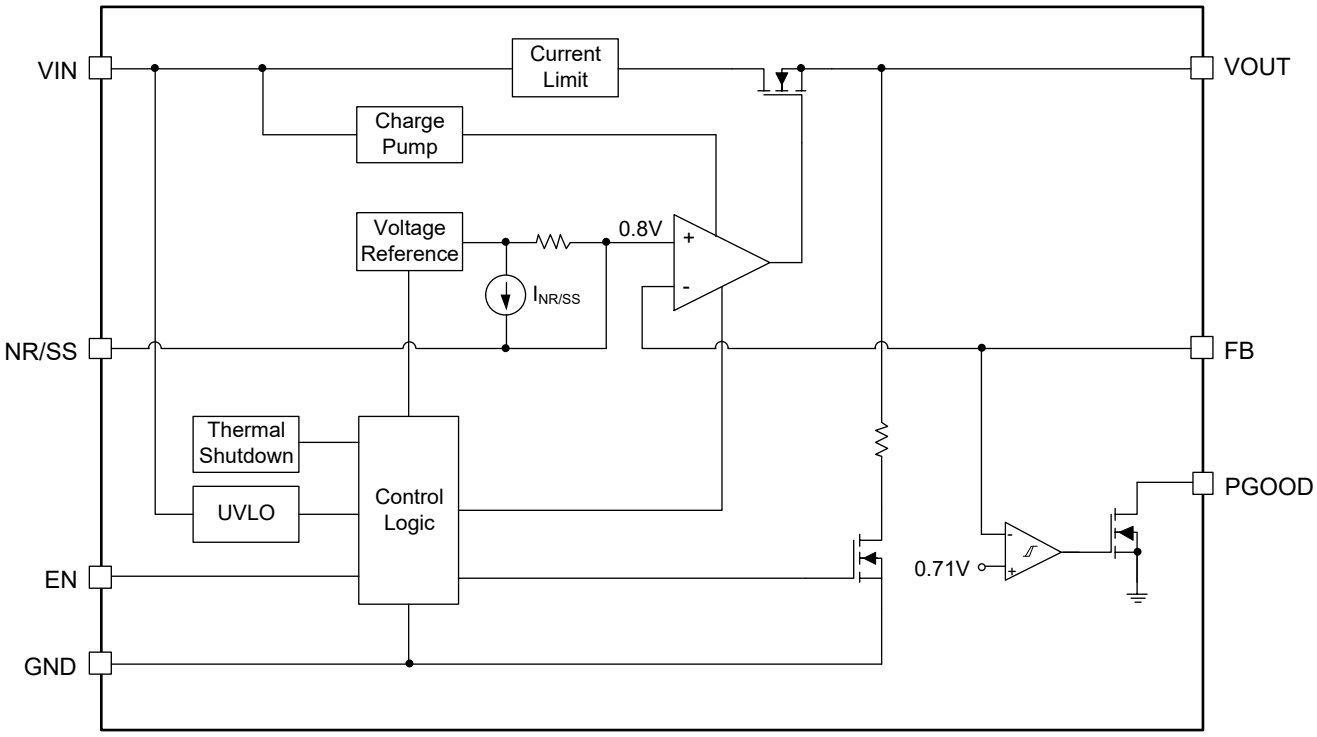


Figure 2. Block Diagram

ELECTRICAL CHARACTERISTICS

(V_{IN} = 1.1V, $V_{OUT(NOM)}$ = 0.8V (1), V_{EN} = 1.1V, C_{IN} = 10μF, C_{OUT} = 10μF, $C_{NR/SS}$ = 0nF, C_{FF} = 0nF, and PGOOD pin pulled up to V_{IN} with 100kΩ, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Operating Input Voltage Range	V_{IN}			1.1		7	V
Output Voltage Range	V_{OUT}			0.8		5.5	V
Output Voltage Accuracy	V_{OUT}	V_{IN} = ($V_{OUT(NOM)}$ + 0.3V), V_{OUT} = 0.8V to 5.5V, I_{OUT} = 5mA to 1.2A	T_J = +25℃	-1		1	%
			T_J = -40℃ to +125℃	-1.8		1.8	
Feedback Reference Voltage	V_{FB}	V_{IN} = ($V_{OUT(NOM)}$ + 0.3V) to 7V	T_J = +25℃	0.792	0.8	0.808	V
			T_J = -40℃ to +125℃	0.7856		0.8144	
FB Pin Leakage Current	I_{FB}	V_{IN} = 7V, V_{FB} = 0.85V				±50	nA
Under-Voltage Lockout Threshold	V_{UVLO}	V_{IN} increasing			1	1.1	V
	ΔV_{UVLO}	Hysteresis			95		mV
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	I_{OUT} = 5mA, V_{IN} = 1.1V to 7V			0.003	0.04	%/V
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = 5mA to 1.2A			0.06	1	%/A
Dropout Voltage	V_{DROP}	V_{IN} = 1.2V, I_{OUT} = 1.2A, V_{FB} = 0.776V			85	130	mV
Output Current Limit	I_{LIMIT}	V_{OUT} = 90% × $V_{OUT(NOM)}$, V_{IN} = ($V_{OUT(NOM)}$ + 0.4V)		1.7	2.3	3	A
Ground Pin Current	I_{GND}	V_{IN} = 7V, I_{OUT} = 0mA			2.7	4	mA
		V_{IN} = 1.4V, I_{OUT} = 1.2A			2.6	4	
Shutdown Current	I_{SHDN}	PGOOD = Open, V_{IN} = 7V, V_{EN} = 0.5V			1	20	μA
EN Pin Threshold Voltage	V_{EN_H}	EN input voltage "H", V_{IN} = 1.1V to 7V		1		7	V
	V_{EN_L}	EN input voltage "L", V_{IN} = 1.1V to 7V		0		0.5	
EN Pin Current	I_{EN}	V_{IN} = 7V, V_{EN} = 0V and 7V				±0.5	μA
Output Discharge Resistance	R_{DIS}	V_{EN} = 0.5V, V_{OUT} = 0.5V			90	130	Ω
Turn-On Time	t_{ON}	From assertion of V_{EN} to V_{OUT} = 90% × $V_{OUT(NOM)}$			320		μs
PGOOD Pin Threshold	V_{IT_PGOOD}	For the direction PGOOD signal falling with decreasing V_{OUT}		0.8 × V_{OUT}	0.867 × V_{OUT}	0.94 × V_{OUT}	V
PGOOD Pin Hysteresis	V_{PGOOD_HYS}	For PGOOD signal rising			0.024 × V_{OUT}		V
PGOOD Pin Low-Level Output Voltage	V_{PGOOD_L}	V_{OUT} < V_{IT_PGOOD}, I_{PGOOD} = -1mA (current into device)				0.2	V
PGOOD Pin Leakage Current	I_{PGOOD_LK}	V_{OUT} > V_{IT_PGOOD} , V_{PGOOD} = 7V				0.5	μA
NR/SS Pin Charging Current	$I_{NR/SS}$	$V_{NR/SS}$ = GND, V_{IN} = 7V		4.5	6.5	8.5	μA
NR/SS Pin Voltage	$V_{NR/SS}$				0.8		V
Power Supply Rejection Ratio	PSRR	V_{IN} = 4.3V, V_{OUT} = 3.3V, I_{OUT} = 750mA, $C_{NR/SS}$ = C_{FF} = 10nF, C_{OUT} = 22μF	f = 10kHz		60		dB
			f = 500kHz		50		
Output Voltage Noise	e_n	f = 10Hz to 100kHz, V_{IN} = 1.4V, V_{OUT} = 0.8V, I_{OUT} = 1A, $C_{NR/SS}$ = 10nF, C_{FF} = 10nF			6.5		μV_{RMS}
Thermal Shutdown Temperature	T_{SHDN}				150		℃
Thermal Shutdown Hysteresis	ΔT_{SHDN}				20		℃

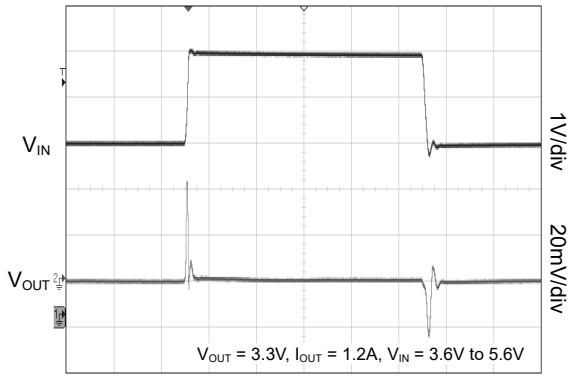
NOTE:

1. $V_{OUT(NOM)}$ is defined as the expected V_{OUT} value, which is set by the external feedback resistance.

TYPICAL PERFORMANCE CHARACTERISTICS

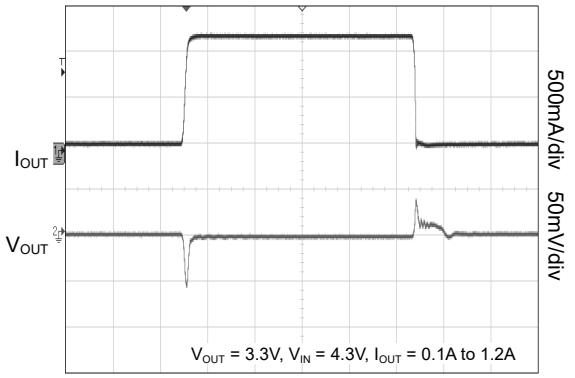
T_J = +25℃, V_{EN} = 1.1V, C_{IN} = C_{OUT} = 10μF, $C_{NR/SS}$ = C_{FF} = 10nF, and PGOOD pin pulled up to V_{IN} with 100kΩ, unless otherwise noted.

Line Transient Response



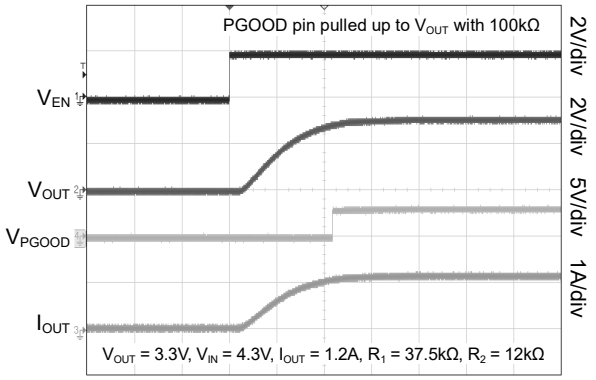
Time (20μs/div)

Load Transient Response



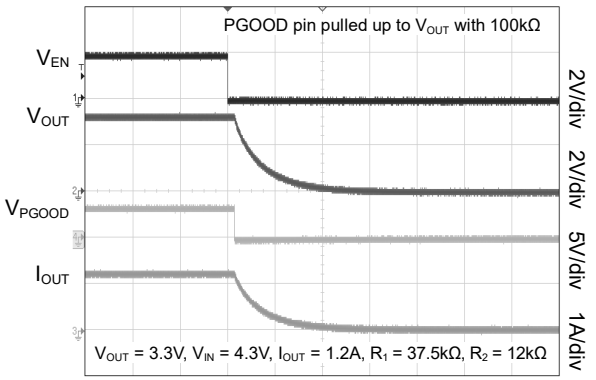
Time (20μs/div)

Turn-On Speed with EN Pin



Time (1ms/div)

Turn-Off Speed with EN Pin

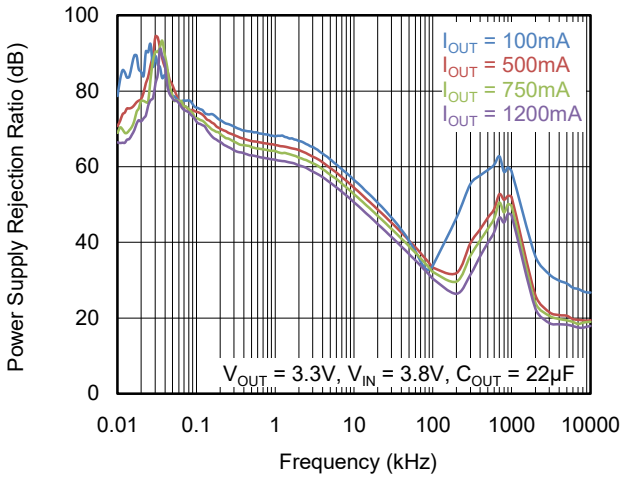


Time (50μs/div)

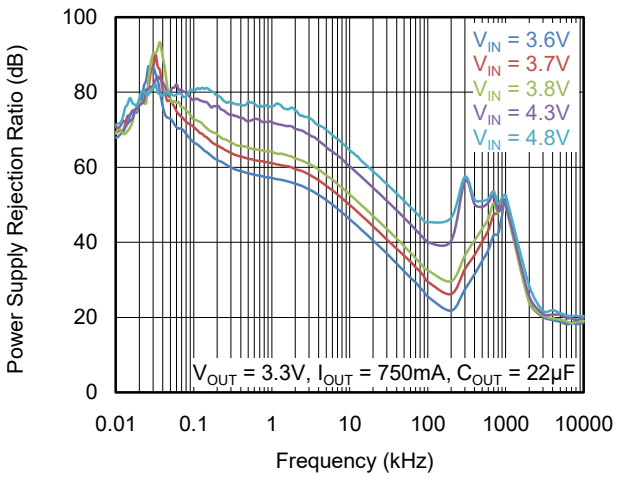
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, V_{EN} = 1.1V, C_{IN} = C_{OUT} = 10μF, $C_{NR/SS}$ = C_{FF} = 10nF, and PGOOD pin pulled up to V_{IN} with 100kΩ, unless otherwise noted.

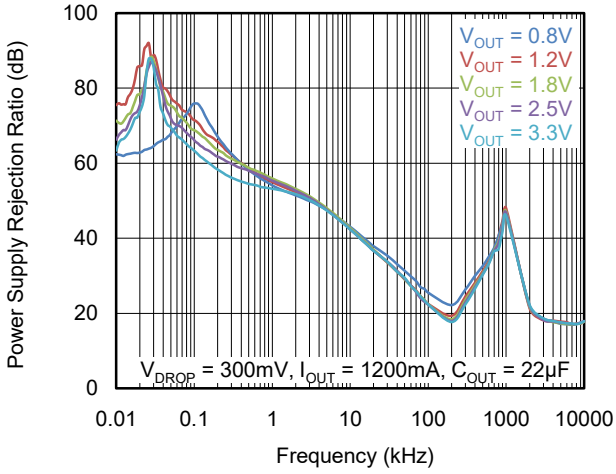
Power Supply Rejection Ratio vs. Frequency



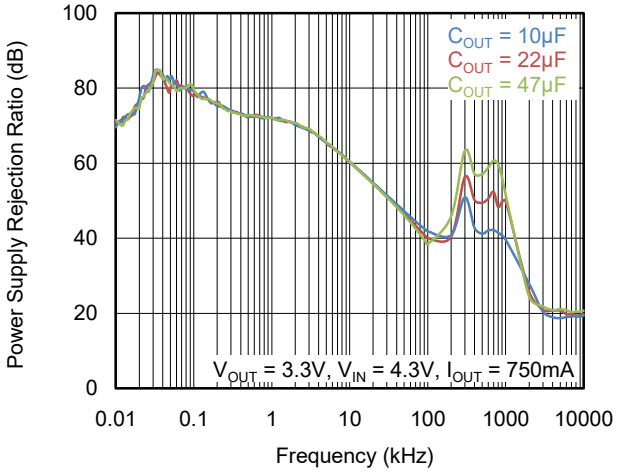
Power Supply Rejection Ratio vs. Frequency



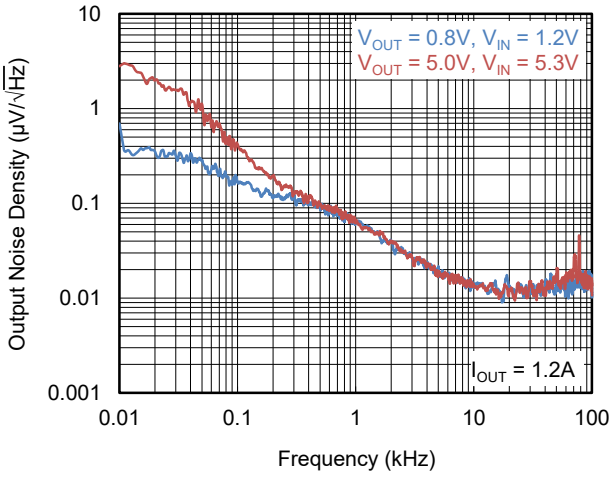
Power Supply Rejection Ratio vs. Frequency



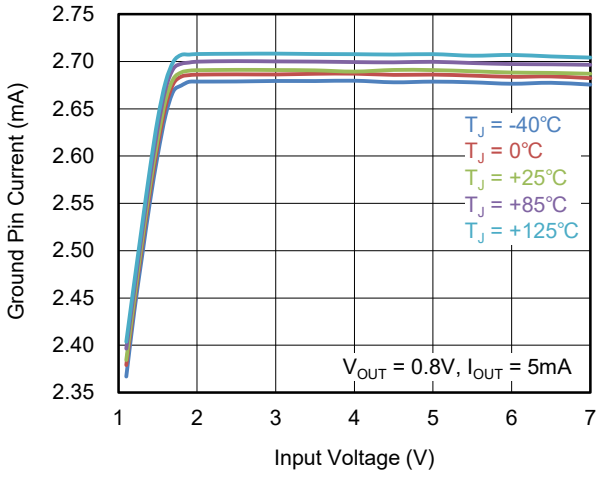
Power Supply Rejection Ratio vs. Frequency



Output Noise Density vs. Frequency



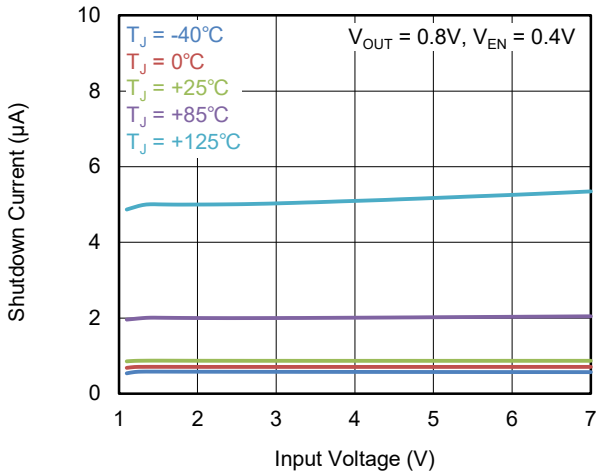
Ground Pin Current vs. Input Voltage



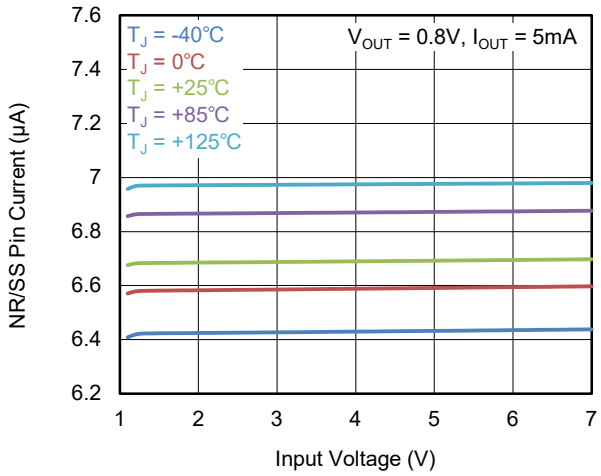
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, V_{EN} = 1.1V, C_{IN} = C_{OUT} = 10μF, $C_{NR/SS}$ = C_{FF} = 10nF, and PGOOD pin pulled up to V_{IN} with 100kΩ, unless otherwise noted.

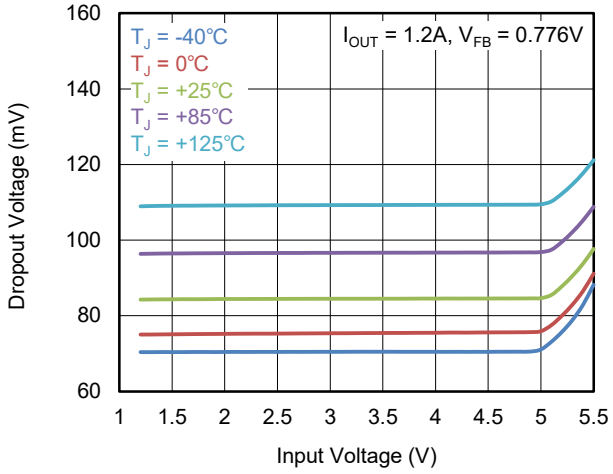
Shutdown Current vs. Input Voltage



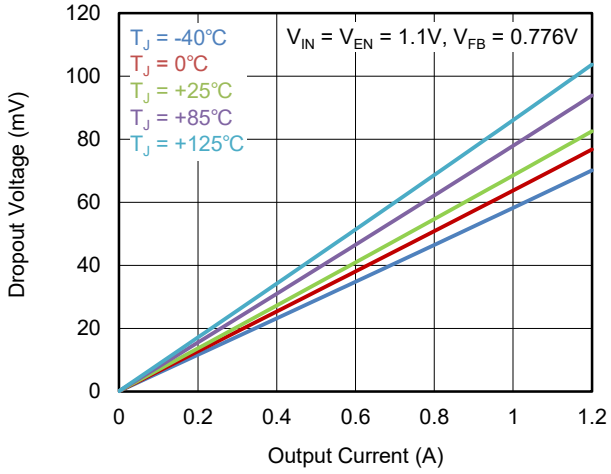
NR/SS Pin Current vs. Input Voltage



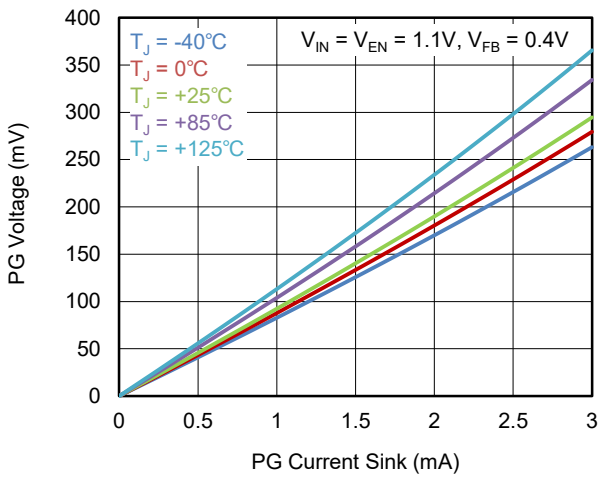
Dropout Voltage vs. Input Voltage



Dropout Voltage vs. Output Current



PG Voltage vs. PG Current Sink



APPLICATION INFORMATION

The SGM2056 is a high current, high PSRR, ultra-low noise and ultra-low dropout voltage linear regulator and provides 1.2A output current. These features make the device a reliable solution to solve many challenging problems in the generation of clean and accurate power supply. The high performance also makes the SGM2056 useful in a variety of applications. The SGM2056 provides the protection functions for output overload, output short-circuit condition and overheating.

The SGM2056 provides an EN pin as an external chip enable control to enable/disable the device. When the regulator is in shutdown state, the shutdown current consumes as low as 1μA (TYP).

Input Capacitor Selection (C_{IN})

The input decoupling capacitor should be placed as close as possible to the VIN pin to ensure the device stability. A 10μF or larger X7R or X5R ceramic capacitor is selected to get good dynamic performance.

When V_{IN} is required to provide large current instantaneously, a large effective input capacitor is required. Multiple input capacitors can limit the input tracking inductance. Adding more input capacitors is available to restrict the ringing and to keep it below the device absolute maximum ratings.

Output Capacitor Selection (C_{OUT})

The output capacitor should be placed as close as possible to the VOUT pin. A 10μF or larger X7R or X5R ceramic capacitor is selected to get good dynamic performance. The minimum effective capacitance of C_{OUT} that SGM2056 can remain stable is 9μF. For ceramic capacitor, temperature, DC bias and package size will change the effective capacitance, so enough margin of C_{OUT} must be considered in design. Additionally, C_{OUT} with larger capacitance and lower ESR will help increase the high frequency PSRR and improve the load transient response.

Noise-Reduction and Soft-Start Capacitor Selection ($C_{NR/SS}$)

The SGM2056 provides a programmable soft-start output function. It is generally recommended to connect an external capacitor ($C_{NR/SS}$) between the NR/SS pin and GND. It can not only slow down the V_{OUT} rise so as to achieve soft starting, but also reduce the output noise effectively.

Dropout Voltage

The SGM2056 features low dropout voltage due to low $R_{DS(ON)}$ NMOSFET power transistor. For Linear regulator, when (V_{IN} - V_{OUT}) < dropout voltage (V_{DROP}), the NMOSFET power transistor will be turned on like a switch and the parameter of linear regulator, such as PSRR, load and input transient responses, will be degraded so much. To get good performance in application, the V_{IN} must be larger than (V_{OUT} + V_{DROP}).

Adjustable Regulator

The output voltage of the SGM2056 can be adjusted from 0.8V to 5.5V. The FB pin will be connected to two external resistors as shown in Figure 3. The output voltage is determined by the following equation:

$$V_{OUT} = 0.8V \times \frac{R_1 + R_2}{R_2} \quad (1)$$

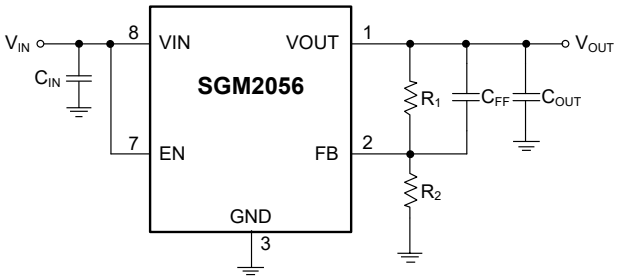


Figure 3. Adjustable Output Voltage Application

One parallel capacitor (C_{FF}) with R_1 can be used to improve the feedback loop stability and PSRR, increase the transient response and reduce the output noise. Use R_2 = 80kΩ to maintain a 10μA minimum load.

APPLICATION INFORMATION (continued)

Enable Operation

The EN pin of the SGM2056 is used to enable/disable its device and to deactivate/activate the output automatic discharge function.

When the EN pin voltage is lower than 0.5V, the device is in shutdown state. There is no current flowing from VIN to VOUT pins. In this state, the automatic discharge transistor is active to discharge the output voltage through a 90Ω (TYP) resistor.

When the EN pin voltage is higher than 1V, the device is in active state. The output voltage is regulated to the expected value and the automatic discharge transistor is turned off.

Under-Voltage Lockout (UVLO)

To protect the device from malfunctioning when the input voltage is insufficient, under-voltage lockout (UVLO) protection is included. The device will not operate until the input voltage exceeds UVLO rising threshold, and will lockout if the input voltage falls below the UVLO falling threshold. The local input capacitance prevents severe brownouts in most applications.

Reverse Current Protection

The pass transistor has an inherent body diode which will be forward biased in the case when V_{OUT} > (V_{IN} + 0.3V). If extended reverse voltage operation is anticipated, external limiting might be appropriate.

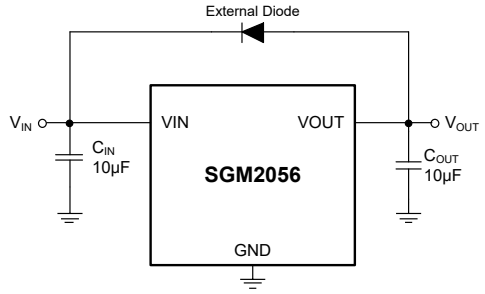


Figure 4. Reverse Protection Reference Design

Output Current Limit

When overload events happen, the output current is internally limited to 2.3A (TYP).

Thermal Shutdown

The SGM2056 can detect the temperature of die. When the die temperature exceeds the threshold value of thermal shutdown, the SGM2056 will be in shutdown state and it will remain in this state until the die temperature decreases to +130℃.

Power Dissipation (P_D)

Power dissipation (P_D) of the SGM2056 can be calculated by the equation $P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$. Thermal shutdown protection starts when the power dissipation of the device is too high and the operating junction temperature exceeds +150℃.

The maximum allowable power dissipation ($P_{D(MAX)}$) of the SGM2056 is affected by many factors, including the difference between junction temperature and ambient temperature ($T_{J(MAX)} - T_A$), package thermal resistance from the junction to the ambient environment (θ_{JA}), the rate of ambient airflow and PCB layout. $P_{D(MAX)}$ can be approximated by the following equation:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA} \quad (2)$$

Layout Guidelines

To get good PSRR, low output noise and high transient response performance, the input and output bypass capacitors must be placed as close as possible to the VIN pin and VOUT pin separately. It is recommended to use separate ground planes for V_{IN}/V_{BIAS} and V_{OUT} and these ground planes are single point connected to the GND pin.

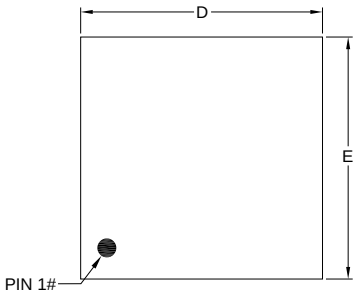
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

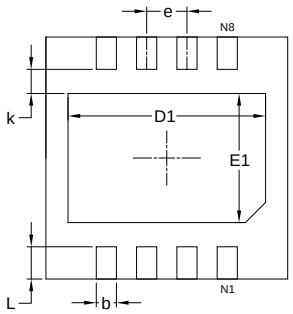
Changes from Original (NOVEMBER 2022) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

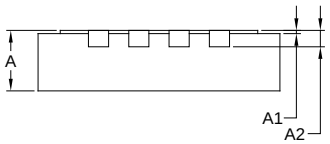
TDFN-3×3-8DL



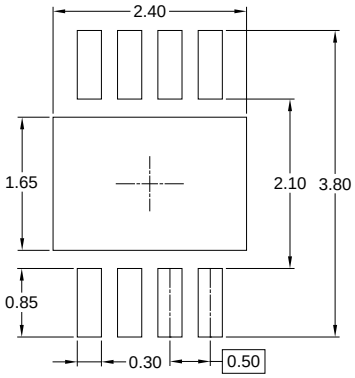
TOP VIEW



BOTTOM VIEW



SIDE VIEW



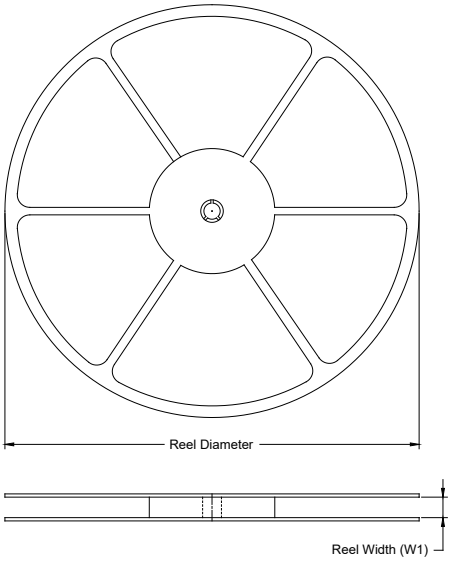
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.700	0.750	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.200	0.250	0.300
D	2.900	3.000	3.100
D1	2.350	2.450	2.550
E	2.900	3.000	3.100
E1	1.500	1.600	1.700
e	0.500 BSC		
k	0.300 REF		
L	0.350	0.400	0.450

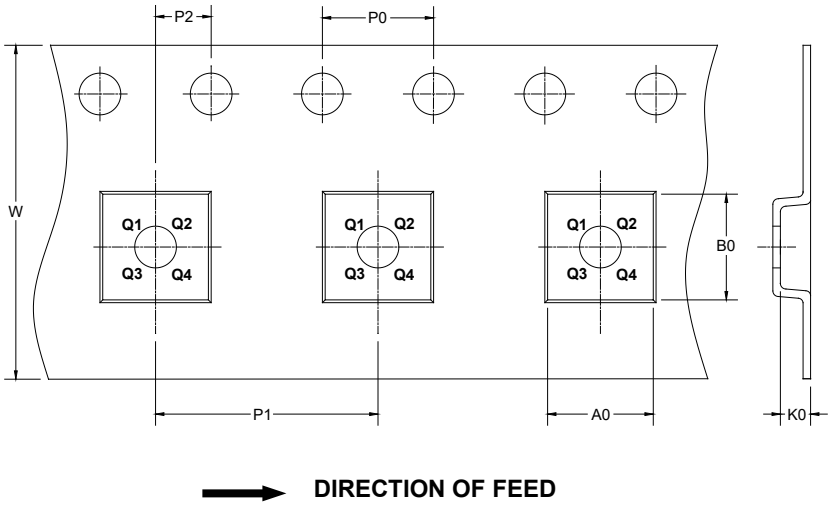
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



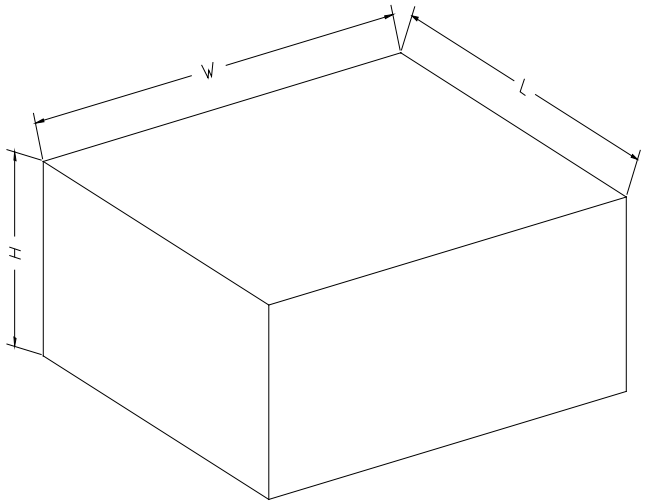
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TDFN-3×3-8DL	13″	12.4	3.30	3.30	1.10	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002