5W *Dual-Pump*™ Class-AB/D/G Audio Power Amplifier

GENERAL DESCRIPTION

The ft2850 is a 5W ***Dual-Pump***™ Class-AB/D/G audio power amplifier with automatic level control (ALC) for portable audio applications. It integrates Class-AB and Class-D audio power amplifiers with a Class-G charge pump regulator based upon proprietary ***Dual-Pump***™ topology. It operates from 3.3V to 5.25V supply. With a supply voltage at 4.2V, it can deliver an output power of 5.5W with 10% THD+N, or 4.5W with 1% THD+N, into a 4Ω speaker load.

In ft2850, the power supply rail of the audio amplifier's output stage is adaptively boosted and regulated by a Class-G charge pump regulator, allowing much higher audio loudness than a stand-alone one directly connected to the battery. The adaptive nature of the Class-G charge pump regulator, whose output voltage varies dynamically in response to the level of the audio output, improves overall power efficiency and extends battery life when playing music. The higher output power and greater power efficiency resulted from the Class-G charge pump regulator make ft2850 an ideal audio solution for battery-powered electronic devices.

To facilitate various applications, the ft2850 provides three types of audio amplifier outputs, i.e., Class-AB, Class-D, and Class-G. For typical applications, the Class-G/D audio output is preferred for its high efficiency. The Class-AB audio output can be chosen to alleviate design complexities for applications where minimum FM radio interference is required.

The ft2850 features ALC that constantly monitors and safeguards the audio output against the boosted supply voltage, preventing output clipping distortion, excessive power dissipation, or speaker over-load. Once an over-level condition is detected, the ALC lowers the voltage gain of the audio amplifier proportionally to limit the peak audio output voltage.

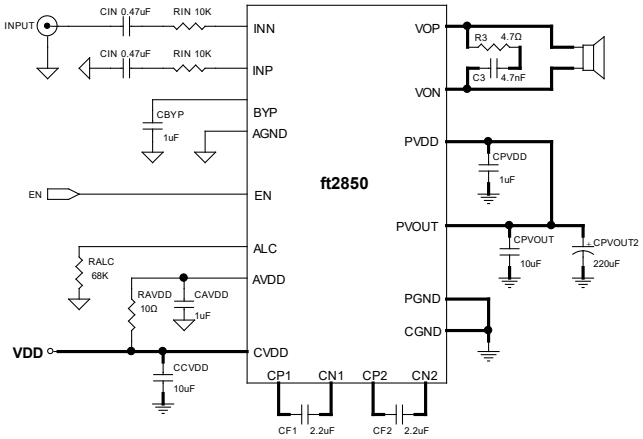
FEATURES

- Wide range of supply voltages from 3.3V to 5.25V
- Proprietary ***Dual-Pump***™ topology
- Selectable types of audio outputs: Class-AB/D/G
- Filterless Class-D audio amplifier integrated with a Class-G charge pump regulator
- Automatic level control to eliminate output clipping
- Selectable ALC dynamic characteristics
- Selectable fade-in time
- Maximum output power (Non-ALC Mode)
  - 6.3W (V_{DD}=4.2V, THD+N=10%, R_L=3Ω+33μH)
  - 5.5W (V_{DD}=4.2V, THD+N=10%, R_L=4Ω+33μH)
  - 3.2W (V_{DD}=4.2V, THD+N=10%, R_L=8Ω+33μH)
- ALC output power (ALC Mode)
  - 5.0W (V_{DD}=4.2V, THD+N=0.5%, R_L=3Ω+33μH)
  - 4.3W (V_{DD}=4.2V, THD+N=0.5%, R_L=4Ω+33μH)
  - 2.4W (V_{DD}=4.2V, THD+N=0.5%, R_L=8Ω+33μH)
- High Efficiency: 75%
  (V_{DD}=3.7V, R_L=4Ω+33μH, Po=4W)
- Low THD+N: 0.04%
  (V_{DD}=3.7V, R_L=4Ω+33μH, Po=2W)
- High PSRR: 70dB at 1kHz
- Maximum Voltage Gain: 28dB
- ALC dynamic range: 9dB
- Low quiescent current: 4.5mA @ V_{DD}=3.7V
- Auto-recovering over-current and thermal-overload protection
- Available in TSSOP-20L & QFN4X4-20L packages

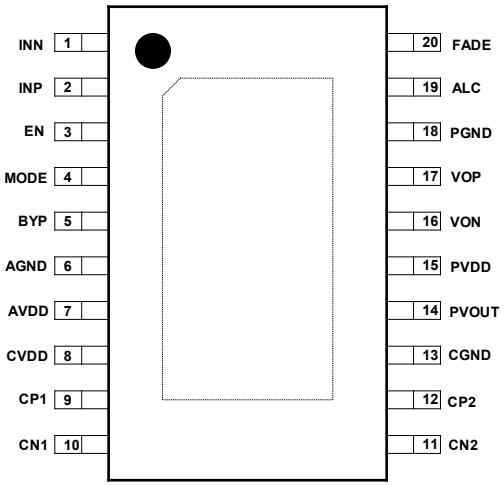
APPLICATIONS

- Blue Tooth Speakers
- Smart Speakers
- Portable Consumer Electronic Devices

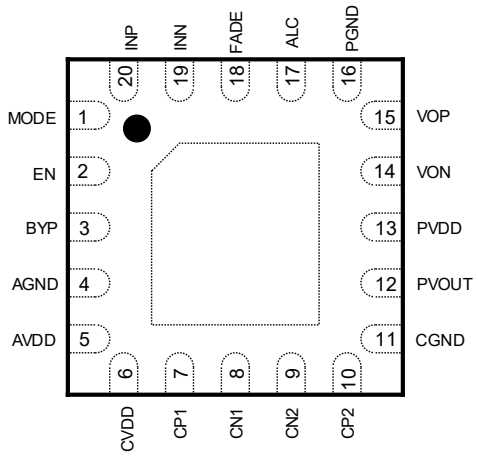
TYPICAL APPLICATION CIRCUIT



PIN ASSIGNMENT AND DESCRIPTION



ft2850P (TOP VIEW)



ft2850Q (TOP VIEW)

NAME	PIN #		PIN TYPE	DESCRIPTION
	TSSOP	QFN		
INN	1	19	AI	Inverting audio input.
INP	2	20	AI	Non-inverting audio input.
EN	3	2	DI	**Chip Enable** with an on-chip 300kΩ pulldown resistor to ground.
MODE	4	1	AI	**Operating Mode Control** with an on-chip 300kΩ pulldown resistor to ground.
BYP	5	3	AO	Common-mode voltage bias for the audio inputs. Connect to a 1μF capacitor for decoupling.
AGND	6	4	G	Analog ground. Connect to the system ground plane GND.
AVDD	7	5	P	Power supply input for analog circuitry. Connect to a 1μF capacitor for decoupling.
CVDD	8	6	P	Power supply input for the charge pump regulator. Connect to a 10μF capacitor for decoupling.
CP1	9	7	AO	Positive connection to the flying capacitor C_{F1} of the charge pump regulator.
CN1	10	8	AO	Negative connection to the flying capacitor C_{F1} of the charge pump regulator.
CN2	11	9	AO	Negative connection to the flying capacitor C_{F2} of the charge pump regulator.
CP2	12	10	AO	Positive connection to the flying capacitor C_{F2} of the charge pump regulator.
CGND	13	11	G	Power ground for the charge pump regulator. Connect to the system ground GND.
PVOUT	14	12	AO	Boosted voltage output of the charge pump regulator. Connect to a 10μF capacitor for decoupling. It must be externally shorted to PVDD on the system board.
PVDD	15	13	P	Power supply input for audio amplifier's output stage. Connect to a 1μF capacitor for decoupling. It must be externally shorted to PVOUT on the system board.
VON	16	14	AO	Inverting BTL audio output.
VOP	17	15	AO	Non-inverting BTL audio output.
PGND	18	16	G	Power ground for audio amplifier's output stage. Connect to the system ground GND.
ALC	19	17	AI	**ALC Mode Select** to set the ALC dynamic characteristic.
FADE	20	18	AI	**Fade-In Time Select** to set the fade-in time during startup.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKING OPTION	PACKAGE
ft2850P	-40°C to +85°C	Tape and Reel, 4000	TSSOP-20L
ft2850Q			QFN4X4-20L

REVISION HISTORY

Initial Release (December 2016)

Changed from Initial 1.0 (December 2016) to Revision 1.1 (March 2017)

1. Changed the PVDD specification from 6.6V±0.1V to 6.7V±0.2V.
2. Moved the ALC section in front of the Voltage Gain section for easy reference.

Changed from Revision 1.1 (March 2017) to Revision 1.2 (April 2017)

1. Revised the PVDD specification from 6.7V±0.2V to 6.65V±0.15V.
2. Corrected Figure 28 - Output Power vs. Input Frequencies.
3. Added the Output RC Snubber Circuit section on Page 23.
4. Added Figure 37 - Class-D Output RC Snubber Circuit.
5. Updated Figure 38, 39, and 40 with Class-D Output RC Snubber Circuits.
6. Updated Typical Application Circuit Diagram on the top page.

Changed from Revision 1.2 (April 2017) to Revision 1.3 (October 2017)

1. Added a new part number ft2850Q in QFN4X4-20L package.
2. Added Typical Application Diagram of ft2850Q in Figure 41.
3. Added Package Outline Dimensions of QFN4X4-20L.
4. Changed the PVDD specification from 6.65V±0.15V to 6.5V±0.15V.
5. Changed the recommended supply voltage range from (3.2V ~ 4.6V) to (3.3V ~ 5.25V).
6. Updated audio output power specifications in accordance with PVDD=6.5V.
7. Updated Figure 3, 4, 5, 6 in accordance with PVDD=6.5V.

Changed from Revision 1.3 (October 2017) to Revision 1.4 (January 2018)

1. Updated Figure 16, 17, and 18 (Efficiency vs. Output Power).

Changed from Revision 1.4 (January 2018) to Revision 1.5 (November 2018)

1. Changed Operating Junction Temperature Range from (0°C ~ 150°C) to (-40°C ~ 150°C).

Changed from Revision 1.5 (November 2018) to Revision 1.6 (September 2022)

1. Added PACKING OPTION.

ABSOLUTE MAXIMUM RATINGS (Note 1)

PARAMETER	VALUE
Supply Voltage, AVDD	-0.3V to 6V
PVOUT, PVDD, VOP, VON, CP1, CP2	-0.3V to 7.5V (Note 2)
All Other Pins	-0.3V to AVDD+0.3V
CVDD to AVDD, CGND to AGND, PGND to AGND	-0.3V to 0.3V
ESD Ratings - Human Body Model (HBM)	1500V
Operating Junction Temperature	-40°C to +150°C
Storage Temperature	-40°C to +125°C
Maximum Soldering Temperature (@10 sec. duration)	260°C

Note 1: Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

POWER DISSIPATION RATINGS (Note 3, 4)

PACKAGE	TA ≤ +25°C	TA = +70°C	TA = +85°C	Θ_{JA}
TSSOP-20L	4.2W	2.7W	2.2W	30°C/W
QFN4X4-20L	3.0W	1.9W	1.5W	42°C/W

Note 3: The thermal pad of the package must be directly soldered onto a grounded metal island as a thermal sink on the system board.
Note 4: The power dissipation ratings are for a two-side, two-plane printed circuit board (PCB).

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{DD}	AVDD, CVDD (Note 5)	3.3		5.25	V
Operating Ambient Temperature	T_A		-40		85	°C
Minimum Load Resistance	R_L	across VOP and VON	2.6	4		Ω
Digital “High” Input Voltage	V_{IH}	EN	1.2			V
Digital “Low” Input Voltage	V_{IL}	EN			0.4	V
Operating Mode Control Input Voltage	V_{MODE}	Class-G Audio Output			0.4	V
		Class-D Audio Output	0.6	0.8	1.0	V
		Class-AB Audio Output	1.4			V
Audio Input Capacitor	C_{IN}	@ INP, INN	0.1	0.47	1.0	μF
Audio Input Resistor	R_{IN}	@ INP, INN	0		39	kΩ
Charge Pump Input Capacitor	C_{CVDD}	@ CVDD		10		μF
Charge Pump Flying Capacitor	C_{F1}, C_{F2}	across CP1/2 and CN1/2	1.0	2.2		μF
Charge Pump Output Capacitor	C_{PVOUT}	Ceramic		10		μF
		Electrolytic or Tantalum (Note 6)	47	220	470	μF
ALC Mode Select Resistor	R_{ALC}	ALC-4 Mode	Short to GND			
		ALC-3 Mode	27kΩ to GND			
		ALC-2 Mode	68kΩ to GND			
		ALC-1 Mode	Unconnected			
		Non-ALC Mode	10kΩ to AVDD			
Fade-In Time Select Resistor	R_{FADE}	Fade-In Time=10ms	Short to GND			
		Fade-In Time=40ms	27kΩ to GND			
		Fade-In Time=160ms	68kΩ to GND			
		Fade-In Time=320ms	Unconnected			
		Fade-In Time=640ms	10kΩ to AVDD			

Note 5: The maximally allowed supply voltage will be also affected by the thermal dissipation capabilities of the package and system board. Since the power efficiency of the charge pump regulator is inversely proportional to the supply voltage, a thermal shutdown might occur occasionally for applications where the supply voltage is higher than 4.5V or the speaker load is less than 2.5Ω.

Note 6: An output buck capacitor is not required for proper operation of the charge pump regulator. However, additional bulk electrolytic or tantalum capacitors in tandem with ceramic capacitors facilitates higher voltage margin for higher output power at low frequencies, particularly for applications where the speaker load is 4Ω or less.

IMPORTANT APPLICATION NOTES

1. It is crucial to place the ft2850 in close proximity to the flying capacitors and input/output capacitors of the charge pump regulator on the system board, minimizing parasitic impedance of high current traces. Furthermore, place these capacitors on the same layer with ft2850. High-current traces are connected with short and wide metal lines and with no vias. Failure to do a proper layout of the system board can result in significant degradation of maximum output power, efficiency, and EMI performance.
2. The ft2850 is a high performance audio amplifier with an exposed thermal pad underneath the package. The thermal pad must be directly soldered onto a grounded metal island as a thermal sink on the system board for proper power dissipation. Failure to do so might result in the device entering into thermal shutdown prematurely.
3. The ft2850 requires adequate power supply decoupling to ensure its optimal performance in output power, efficiency, EMI emission, and THD+N. Place each decoupling capacitors as individually close as possible to AVDD, CVDD, BYP, PVOUT, and PVDD pins.
4. Place charge pump flying capacitors C_{F1} and C_{F2} close to their respective pins, CP1/2 and CN1/2.
5. It is recommended to employ a ground plane GND on the system board for ft2850. The AGND, CGND and PGND pins must be directly shorted to the ground plane.
6. Place a small decoupling resistor (10Ω) between AVDD and CVDD to prevent high frequency charge pump regulator's transient spikes from interfering with the on-chip linear circuitry.
7. For a stable operation, consider adding a small low-ESR ceramic capacitor of 0.1μF to the MODE pin for applications where the MODE pin is set by an external resistor divider or a GPIO port.
8. For best noise performance, use differential inputs from the audio source for ft2850. In single-ended input applications, the unused input of ft2850 should be AC-grounded at the audio source.
9. Use a simple ferrite bead filter comprising a ferrite bead and a capacitor, as shown in Figure 36, for further EMI suppression. Choose a ferrite bead with low DC resistance (DCR) and high impedance (220Ω ~ 470Ω) at high frequencies (>100MHz). Ensure that its rated current is no less than 3A for applications where the speaker load is 4Ω or less. Place each ferrite beard filter tightly together and individually close to VOP and VON pins.
10. For applications where speaker load resistances are 4Ω or less with long speaker wires, add an RC snubber circuit across two audio outputs, VOP and VON, as shown in Figure 37, to prevent the device from accelerated deterioration or abrupt destruction due to excessive inductive flybacks that are induced on fast output switching or by an over-current condition.
11. Do not connect either audio output pin VOP or VON directly to GND, AVDD, CVDD, PVOUT, or PVDD as this might damage the device permanently.
12. Do not connect CP1/2 directly to CN1/2 as this might damage the device permanently.

FUNCTIONAL BLOCK DIAGRAM

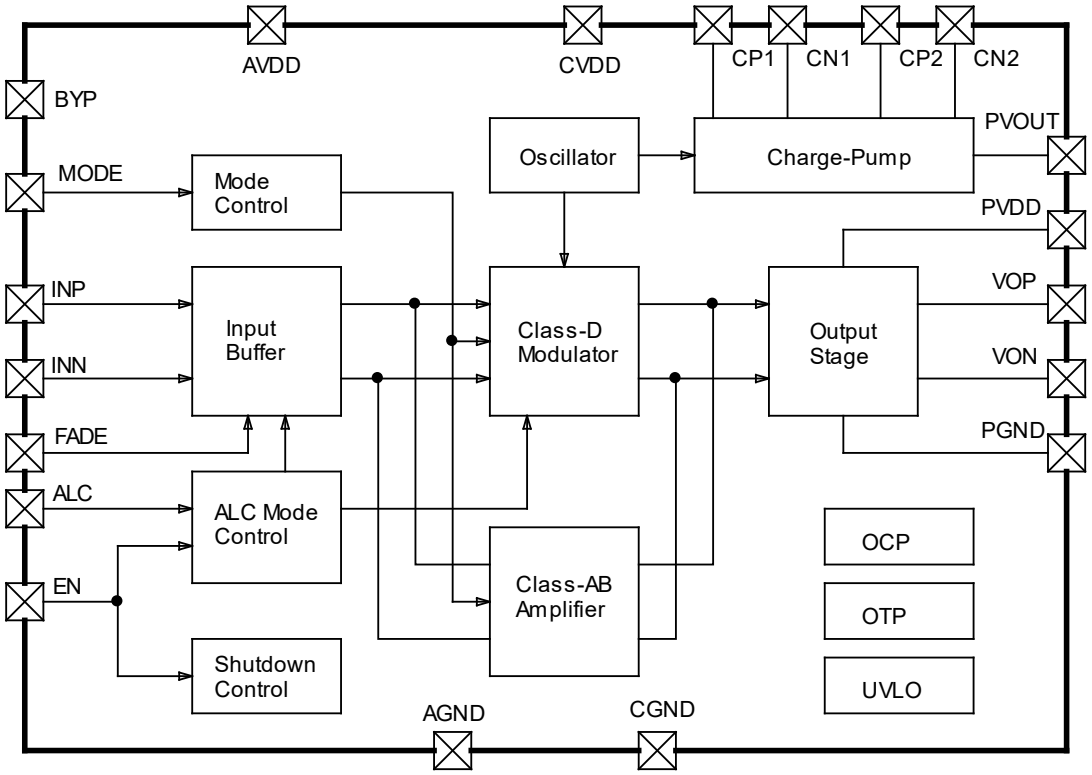


Figure 1: Simplified Functional Block Diagram of ft2850

TEST SETUP FOR ELECTRICAL & PERFORMANCE CHARACTERISTICS

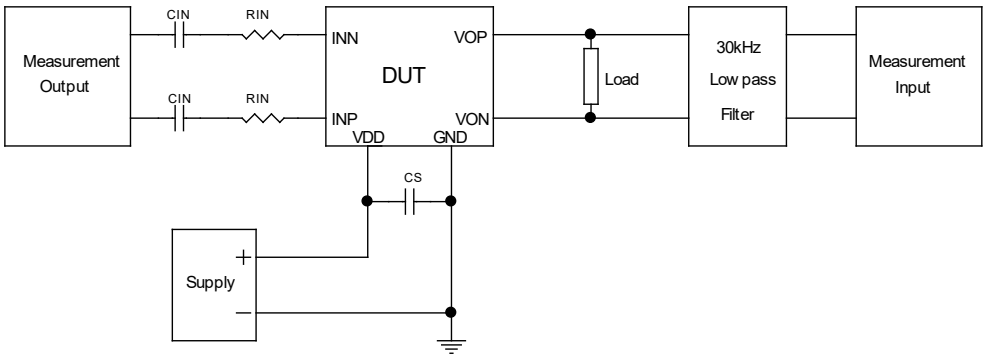


Figure 2: Test Setup Diagram for ft2850

All parameters specified in Electrical and Typical Performance Characteristics sections are measured according to the conditions:

1. The two differential inputs are shorted for common-mode input voltage measurement. All other parameters are taken with input resistors R_{IN}=10kΩ and input capacitors C_{IN}=0.47μF, unless otherwise specified.
2. The supply decoupling capacitor C_S=10μF is placed close to the CVDD pin.
3. The charge pump output capacitors C_{PVOUT}=0.1μF//10μF//220μF are placed close to the PVOUT pin.
4. The supply decoupling capacitor C_{PVDD}=0.01μF//1μF is placed close to the PVDD pin.
5. An output inductor of 33μH inductor is placed in series with the load resistor to emulate a speaker load for all AC and dynamic parameters.
6. The 33kHz lowpass filter is added even if the analyzer has an internal lowpass filter. An RC lowpass filter (1kΩ, 4.7nF) is used on each output for the datasheet graphs.

ELECTRICAL CHARACTERISTICS

V_{DD}=3.7V, f=1kHz, Load=4Ω+33μH, C_{IN}=0.47μF, R_{IN}=10kΩ (A_V=24dB), MODE=Low, ALC=Unconnected, FADE=GND, C_{CVDD}=10μF, C_{F1}=2.2μF, C_{F2}=2.2μF, C_{PVOUT}=0.1μF//10μF//220μF, R_{AVDD}=10Ω, C_{AVDD}=1μF, C_{PVDD}=0.01μF//1μF, C_{BYP}=1μF, TSSOP-20L package, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{DD}	Supply Voltage	AVDD, CVDD		3.3		5.25	V
V_{UVLOUP}	Power-On Threshold Voltage	V_{DD} from Low to High			2.2		V
V_{UVLODN}	Power-Off Threshold Voltage	V_{DD} from High to Low			2.0		V
I_{DD}	Supply Quiescent Current Inputs AC-Grounded, No Load	Class-G Configuration		3.0	4.5	6.0	mA
		Class-D Configuration		15	30	45	mA
		Class-AB Configuration		30	45	60	mA
I_{SD}	Shutdown Current	EN=Low				1	μA
V_{BYP}	Bypass Voltage	V_{DD}=3.7V		1.7	1.85	2.0	V
V_{ALC}	ALC Mode Select Voltage	ALC=Unconnected		2.1	2.4	2.7	V
		R_{ALC}=68kΩ to GND		1.0	1.36	1.72	V
V_{FADE}	Fade-In Time Select Voltage	FADE=Unconnected		2.1	2.4	2.7	V
		R_{FADE}=68kΩ to GND		1.0	1.36	1.72	V
V_H	Digital High Input Voltage	EN		1.2			V
V_L	Digital Low Input Voltage	EN				0.4	V
V_{MODE}	Operating Mode Control Input Voltage	Class-G Audio Output				0.4	V
		Class-D Audio Output		0.6	0.8	1.0	V
		Class-AB Audio Output		1.4			V
V_{ALC}	ALC Mode Control Input Voltage	Non-ALC Mode		V_{DD}-0.		V_{DD}	V
		ALC-1 Mode		2.05	2.4	2.75	V
		ALC-2 Mode		0.85	1.4	1.95	V
		ALC-3 Mode		0.35	0.55	0.75	V
		ALC-4 Mode				0.20	V
V_{FADE}	Fade-In Time Control Input Voltage	Fade-In Time=640ms		V_{DD}-0.		V_{DD}	V
		Fade-In Time=320ms		2.05	2.4	2.75	V
		Fade-In Time=160ms		0.85	1.4	1.95	V
		Fade-In Time=40ms		0.35	0.55	0.75	V
		Fade-In Time=10ms				0.20	V
T_{MODE}	Operating Mode Settling Time				120		ms
T_{OTSD}	Over-Temperature Threshold				160		°C
T_{HYS}	Over-Temperature Hysteresis				20		°C
CLASS-G CHARGE PUMP REGULATOR (MODE=Low or Unconnected)							
PVOUT	Charge Pump Output Voltage	I_{OUT}=100mA		6.35	6.5	6.65	V
f_{CP}	PWM Switching Frequency				1000		kHz
CLASS-D AUDIO AMPLIFIER (MODE=Low or Unconnected)							
$P_{O, MAX}$	Maximum Output Power Load=3Ω+33μH Non-ALC Mode	V_{DD}=4.2V	THD+N=10%		6.6		W
			THD+N=1%		5.3		W
		V_{DD}=3.7V	THD+N=10%		5.4		W
			THD+N=1%		4.7		W

ELECTRICAL CHARACTERISTICS (Cont'd)

V_{DD}=3.7V, f=1kHz, Load=4Ω+33μH, C_{IN}=0.47μF, R_{IN}=10kΩ (A_V=24dB), MODE=Low, ALC=Unconnected, FADE=GND, C_{CVDD}=10μF, C_{F1}=2.2μF, C_{F2}=2.2μF, C_{PVOUT}=0.1μF//10μF//220μF, R_{AVDD}=10Ω, C_{AVDD}=1μF, C_{PVDD}=0.01μF//1μF, C_{BYP}=1μF, TSSOP-20L package, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
CLASS-D AUDIO AMPLIFIER (MODE=Low or Unconnected) (Cont'd)							
$P_{O, MAX}$	Maximum Output Power Load=4Ω+33μH Non-ALC Mode	V_{DD}=4.2V	THD+N=10%		5.5		W
			THD+N=1%		4.5		W
		V_{DD}=3.7V	THD+N=10%		5.0		W
			THD+N=1%		4.2		W
	Maximum Output Power Load=8Ω+33μH Non-ALC Mode	V_{DD}=4.2V	THD+N=10%		3.2		W
			THD+N=1%		2.6		W
		V_{DD}=3.7V	THD+N=10%		3.1		W
			THD+N=1%		2.5		W
$P_{O, ALC}$	ALC Output Power Load=3Ω+33μH, ALC Mode	V_{DD}=4.2V, V_{IN}=0.40V_{RMS}			5.0		W
		V_{DD}=3.7V, V_{IN}=0.40V_{RMS}			4.5		W
	ALC Output Power Load=4Ω+33μH, ALC Mode	V_{DD}=4.2V, V_{IN}=0.40V_{RMS}			4.3		W
		V_{DD}=3.7V, V_{IN}=0.40V_{RMS}			4.0		W
	ALC Output Power Load=8Ω+33μH, ALC Mode	V_{DD}=4.2V, V_{IN}=0.40V_{RMS}			2.4		W
		V_{DD}=3.7V, V_{IN}=0.40V_{RMS}			2.4		W
THD+N	Total Harmonic Distortion + Noise	Load=4Ω+33μH, P_O=1.0W			0.05		%
		Load=4Ω+33μH, P_O=2.0W			0.04		%
		Load=4Ω+33μH, V_{DD}=3.7V ALC Mode, V_{IN}=0.40V_{RMS}			0.5		%
η	Overall Power Efficiency	Load=4Ω+33μH, P_O=0.7W			83		%
		Load=4Ω+33μH, P_O=2.0W			73		%
		Load=4Ω+33μH, V_{DD}=3.7V ALC Mode, V_{IN}=0.40V_{RMS}			75		%
A_V	Overall Voltage Gain	R_{IN}=0kΩ			28		dB
		R_{IN}=10kΩ			24		dB
A_{MAX}	Maximum ALC Attenuation				9		dB
V_{COMM}	Input Common-Mode Bias	@ INP, INN			1.7		V
R_{IN}	Input Resistance	@ INP, INN			18		kΩ
R_O	Output Resistance in Shutdown	EN=Low @ VOP, VON			2		kΩ
V_{OS}	Output Offset Voltage	Inputs AC-Grounded, No Load			±10		mV
V_N	Output Voltage Noise	Inputs AC-Grounded A_V=24dB, A-weighted			130		μV_{RMS}
SNR	Signal-To-Noise Ratio	Maximum Output (4.0V_{RMS}) A_V=24dB, A-weighted			90		dB
PSRR	Power Supply Rejection Ratio	200mV_{PP}, f=217Hz			72		dB
		200mV_{PP}, f=1kHz			70		dB
CMRR	Common Mode Rejection Ratio	V_{IN}=0.20V_{RMS}			70		dB
f_{PWM}	PWM Switching Frequency				500		kHz
$T_{STARTUP}$	Startup Time				40		ms
$T_{FADEOUT}$	Fade-Out Time				2		ms
T_{SD}	Shutdown Settling Time				10		ms

ELECTRICAL CHARACTERISTICS (Cont'd)

V_{DD}=3.7V, f=1kHz, Load=4Ω+33μH, C_{IN}=0.47μF, R_{IN}=10kΩ (A_V=24dB), MODE=Low, ALC=Unconnected, FADE=GND, C_{CVDD}=10μF, C_{F1}=2.2μF, C_{F2}=2.2μF, C_{PVOUT}=0.1μF//10μF//220μF, R_{AVDD}=10Ω, C_{AVDD}=1μF, C_{PVDD}=0.01μF//1μF, C_{BYP}=1μF, TSSOP-20L package, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
FADE-IN TIME SELECT							
$T_{FADE-IN}$	Fade-In Time	10kΩ to AVDD			640		ms
		Unconnected			320		ms
		68kΩ to GND			160		ms
		27kΩ to GND			40		ms
		Short to GND			10		ms
CLASS-AB AUDIO AMPLIFIER (MODE=High)							
$P_{O, MAX}$	Maximum Output Power Load=3Ω+33μH	V_{DD}=4.2V	THD+N=10%		2.5		W
			THD+N=1%		1.9		W
		V_{DD}=3.7V	THD+N=10%		1.9		W
			THD+N=1%		1.4		W
	Maximum Output Power Load=4Ω+33μH	V_{DD}=4.2V	THD+N=10%		2.1		W
			THD+N=1%		1.6		W
		V_{DD}=3.7V	THD+N=10%		1.6		W
			THD+N=1%		1.2		W
	Maximum Output Power Load=8Ω+33μH	V_{DD}=4.2V	THD+N=10%		1.2		W
			THD+N=1%		0.96		W
		V_{DD}=3.7V	THD+N=10%		0.95		W
			THD+N=1%		0.75		W
THD+N	Total Harmonic Distortion + Noise	Load=4Ω+33μH, P_O=0.5W			0.05		%
		Load=4Ω+33μH, P_O=1.0W			0.2		%
η	Overall Power Efficiency	Load=4Ω+33μH, P_O=1.0W			60		%
A_V	Overall Voltage Gain	R_{IN}=0kΩ			24		dB
		R_{IN}=10kΩ			20		dB
V_{COMM}	Input Common-Mode Bias	@ INP, INN, V_{DD}=3.7V			1.85		V
V_N	Output Voltage Noise	A_V=20dB, A-weighted Inputs AC-Grounded			80		μV_{RMS}
SNR	Signal-To-Noise Ratio	Maximum Output ($2.0V_{RMS}$) A_V=20dB, A-weighted			88		dB
PSRR	Power Supply Rejection Ratio	$200mV_{PP}$, f=217Hz			70		dB
		$200mV_{PP}$, f=1kHz			68		dB

TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD}=3.7V, f=1kHz, Load=4Ω+33μH, C_{IN}=0.47μF, R_{IN}=10kΩ (A_V=24dB), MODE=Low, ALC=Unconnected, FADE=GND, C_{CVDD}=10μF, C_{F1}=2.2μF, C_{F2}=2.2μF, C_{PVOUT}=0.1μF//10μF//220μF, R_{AVDD}=10Ω, C_{AVDD}=1μF, C_{PVDD}=0.01μF//1μF, C_{BYP}=1μF, TSSOP-20L package, unless otherwise specified.

List of Performance Characteristic Plots

DESCRIPTION	CONDITIONS	FIGURE #
ALC Output Power vs. Supply Voltage	R_L=8Ω+33μH/4Ω+33μH/3Ω+33μH, ALC-1 Mode	3
Output Power vs. Supply Voltage	R_L=8Ω+33μH, Non-ALC Mode, THD+N=1%, 10%	4
	R_L=4Ω+33μH, Non-ALC Mode, THD+N=1%, 10%	5
	R_L=3Ω+33μH, Non-ALC Mode, THD+N=1%, 10%	6
Output Power vs. Supply Voltage (Class-AB Output)	R_L=8Ω+33μH, THD+N=1%, 10%	7
	R_L=4Ω+33μH, THD+N=1%, 10%	8
	R_L=3Ω+33μH, THD+N=1%, 10%	9
Output Power vs. Input Voltage	R_L=8Ω+33μH, V_{DD}=3.7V, ALC-1, Non-ALC Modes	10
	R_L=8Ω+33μH, V_{DD}=4.2V, ALC-1, Non-ALC Modes	11
	R_L=4Ω+33μH, V_{DD}=3.7V, ALC-1, Non-ALC Modes	12
	R_L=4Ω+33μH, V_{DD}=4.2V, ALC-1, Non-ALC Modes	13
	R_L=3Ω+33μH, V_{DD}=3.7V, ALC-1, Non-ALC Modes	14
	R_L=3Ω+33μH, V_{DD}=4.2V, ALC-1, Non-ALC Modes	15
Efficiency vs. Output Power	R_L=8Ω+33μH, Non-ALC Mode, V_{DD}=3.7V, 4.2V	16
	R_L=4Ω+33μH, Non-ALC Mode, V_{DD}=3.7V, 4.2V	17
	R_L=3Ω+33μH, Non-ALC Mode, V_{DD}=3.7V, 4.2V	18
Power Dissipation vs. Output Power	R_L=8Ω+33μH, Non-ALC Mode, V_{DD}=3.7V, 4.2V	19
	R_L=4Ω+33μH, Non-ALC Mode, V_{DD}=3.7V, 4.2V	20
	R_L=3Ω+33μH, Non-ALC Mode, V_{DD}=3.7V, 4.2V	21
THD+N vs. Output Power	R_L=8Ω+33μH/4Ω+33μH/3Ω+33μH, Non-ALC Mode	22
THD+N vs. Output Power (Class-AB Output)	R_L=8Ω+33μH/4Ω+33μH/3Ω+33μH	23
THD+N vs. Input Voltage	R_L=8Ω+33μH/4Ω+33μH/3Ω+33μH, ALC-1 Mode	24
THD+N vs. Input Frequency	R_L=8Ω+33μH, P_O=0.5W	25
	R_L=4Ω+33μH, P_O=1W	
	R_L=3Ω+33μH, P_O=1.2W	
PSRR vs. Input Frequency	R_L=4Ω+33μH, Input AC-Grounded	26
Quiescent Current vs. Supply Voltage	Input AC-Grounded, No Load, Class-AB/D/G Output	27
Output Power vs. Input Frequency	V_{IN}=0.20V_{RMS}, R_L=4Ω+33μH, f=20Hz ~ 20kHz with 33kHz Lowpass Filter	28
Output Waveforms on ALC Attack	V_{IN}=0.23V_{RMS} → 0.70V_{RMS}, ALC Mode	29
Output Waveforms on ALC Release	V_{IN}=0.70V_{RMS} → 0.23V_{RMS}, ALC Mode	30
Output Waveforms during Startup	V_{IN}=0.10V_{RMS}, ALC Mode	31
Output Waveforms during Shutdown	V_{IN}=0.10V_{RMS}, ALC Mode	32

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

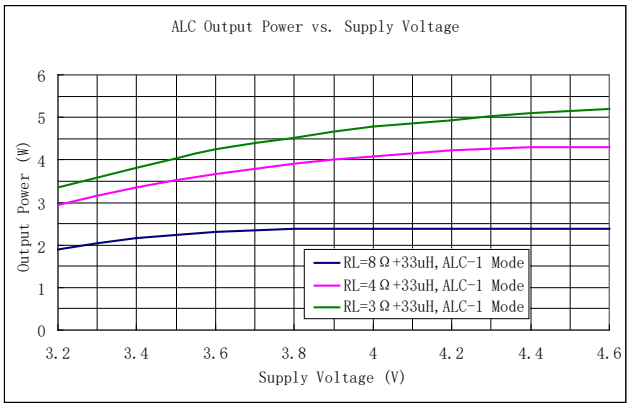


Figure 3: ALC Output Power vs. Supply Voltage

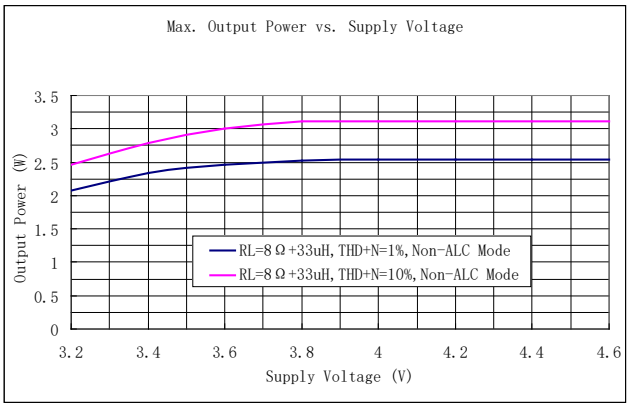


Figure 4: Output Power vs. Supply Voltage

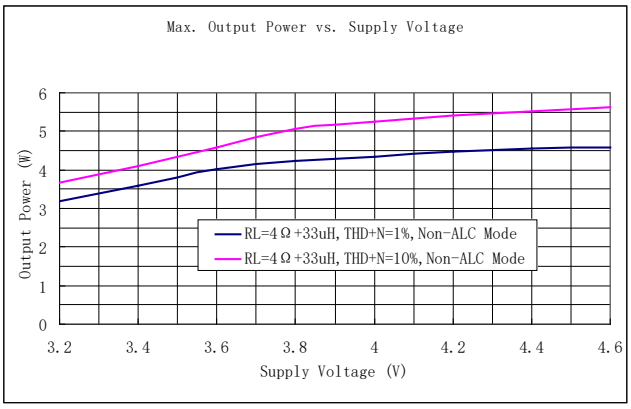


Figure 5: Output Power vs. Supply Voltage

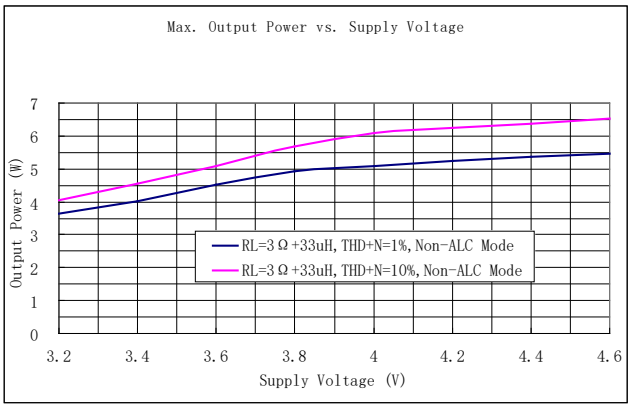


Figure 6: Output Power vs. Supply Voltage

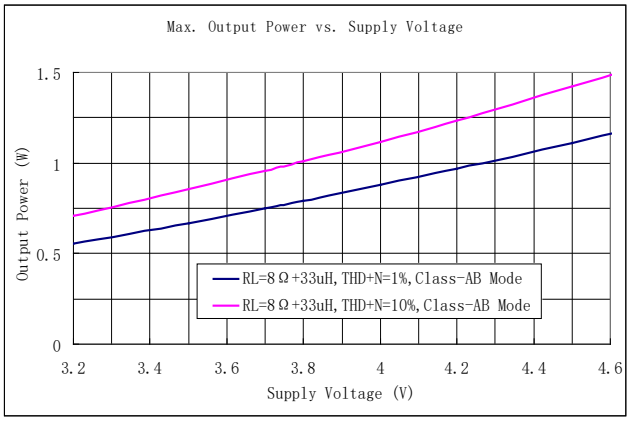


Figure 7: Output Power vs. Supply Voltage (Class-AB Output)

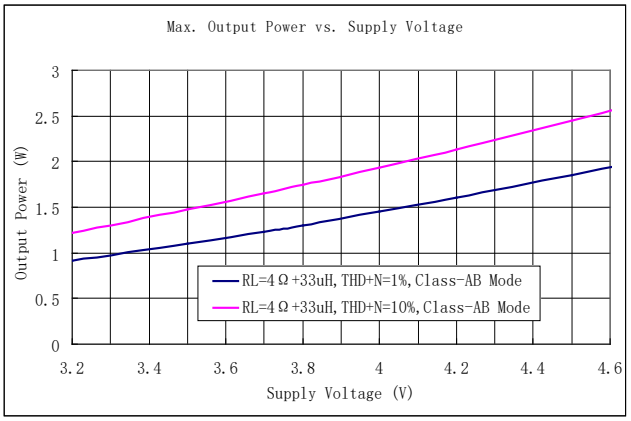


Figure 8: Output Power vs. Supply Voltage (Class-AB Output)

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

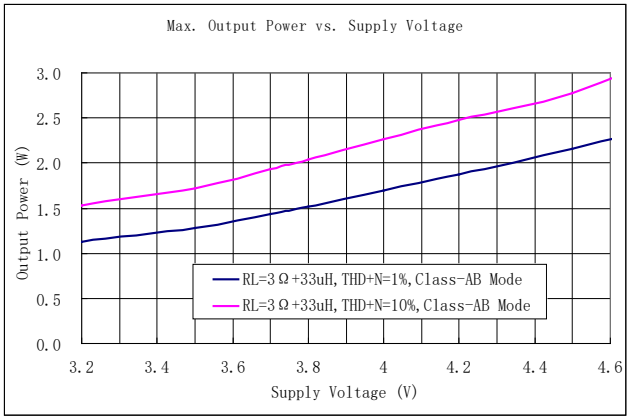


Figure 9: Output Power vs. Supply Voltage (Class-AB Output)

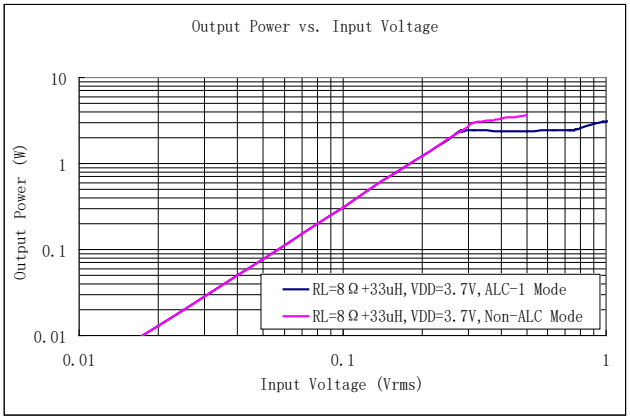


Figure 10: Output Power vs. Input Voltage

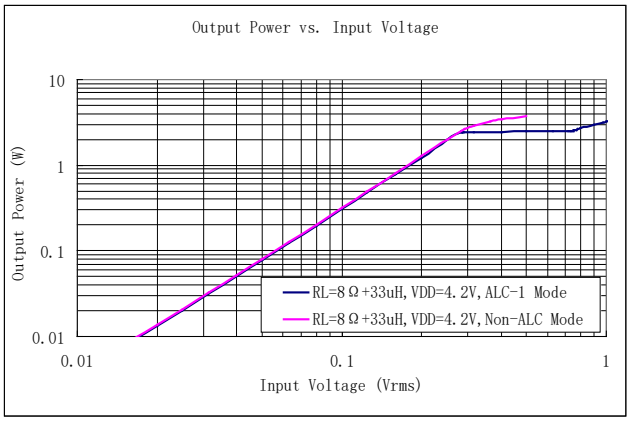


Figure 11: Output Power vs. Input Voltage

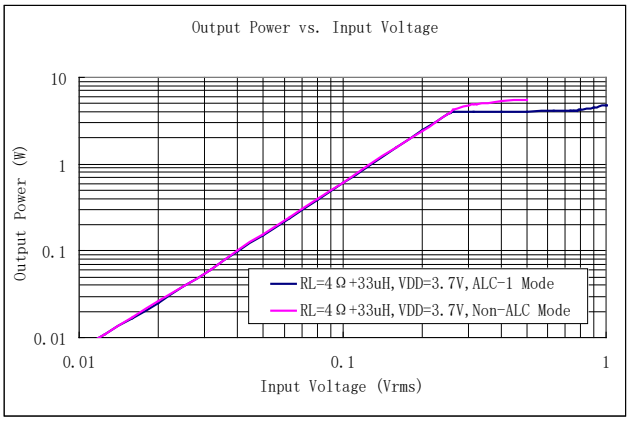


Figure 12: Output Power vs. Input Voltage

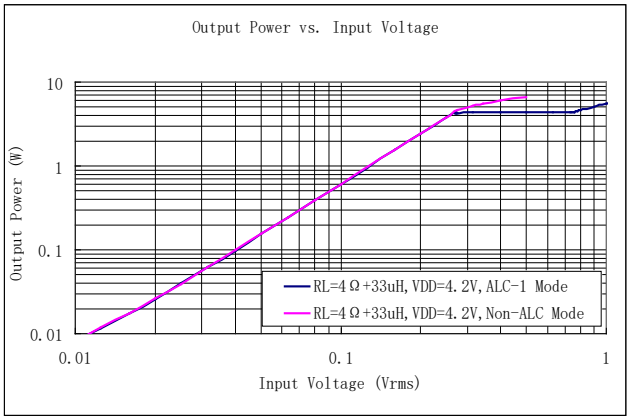


Figure 13: Output Power vs. Input Voltage

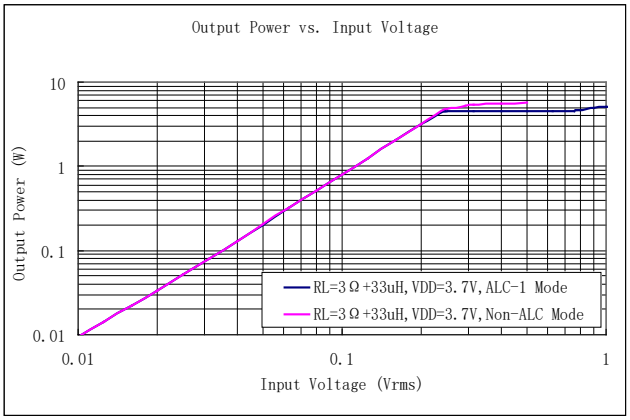


Figure 14: Output Power vs. Input Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

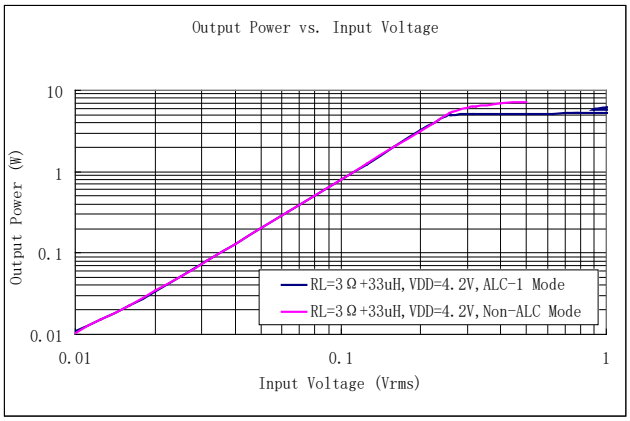


Figure 15: Output Power vs. Input Voltage

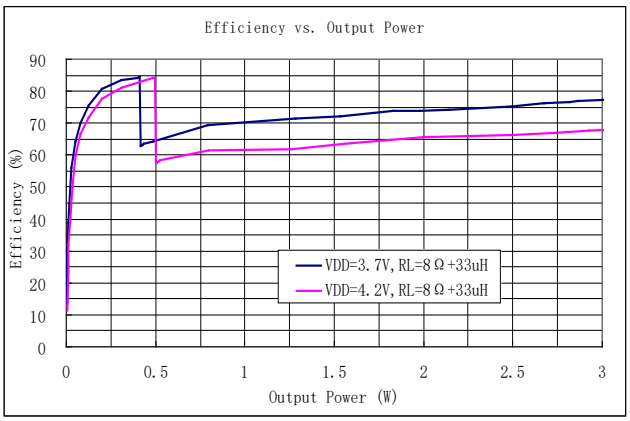


Figure 16: Efficiency vs. Output Power

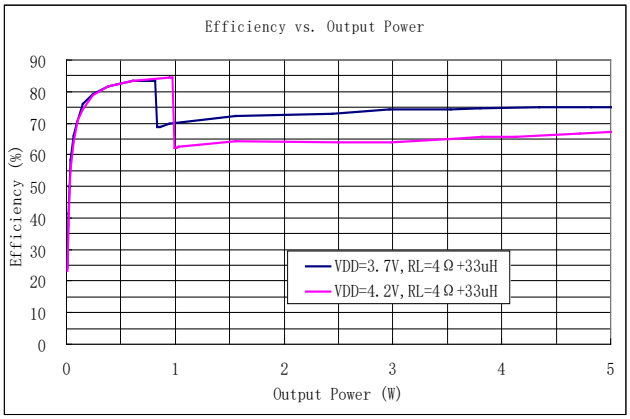


Figure 17: Efficiency vs. Output Power

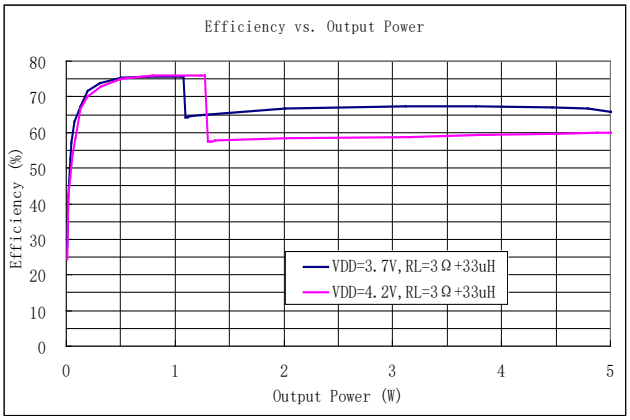


Figure 18: Efficiency vs. Output Power

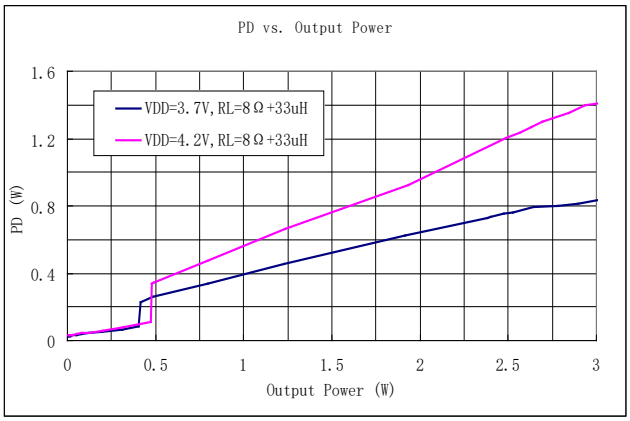


Figure 19: Power Dissipation vs. Output Power

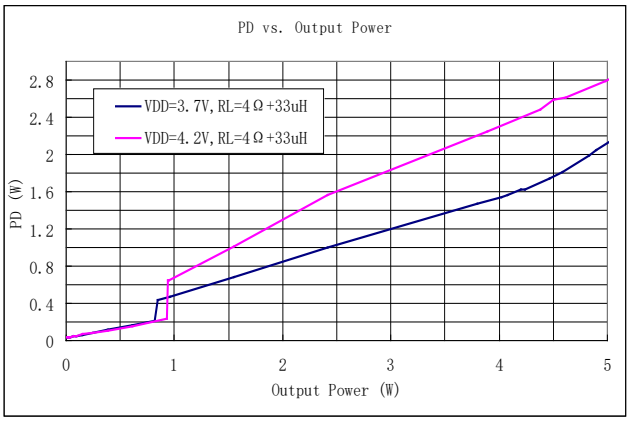


Figure 20: Power Dissipation vs. Output Power

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

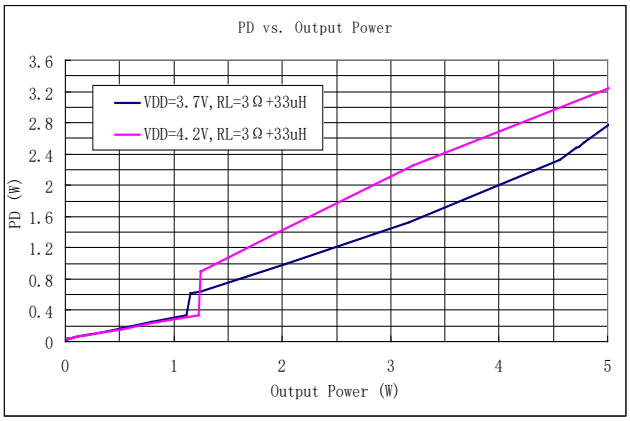


Figure 21: Power Dissipation vs. Output Power

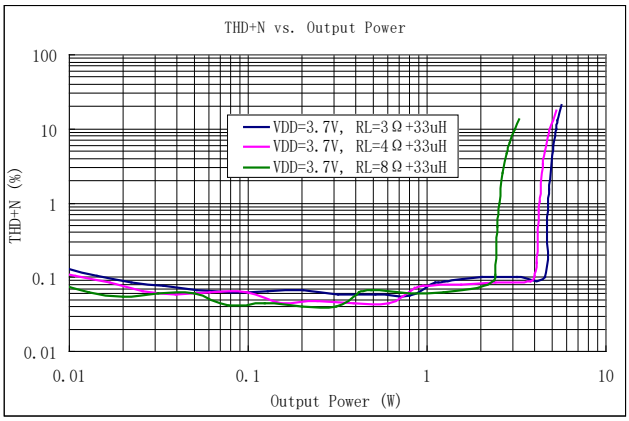


Figure 22: THD+N vs. Output Power

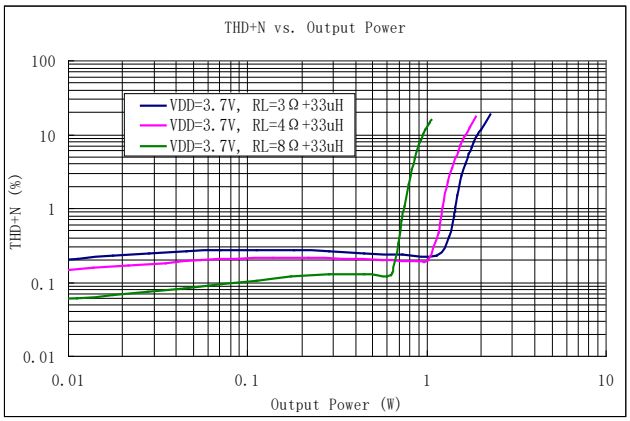


Figure 23: THD+N vs. Output Power (Class-AB Output)

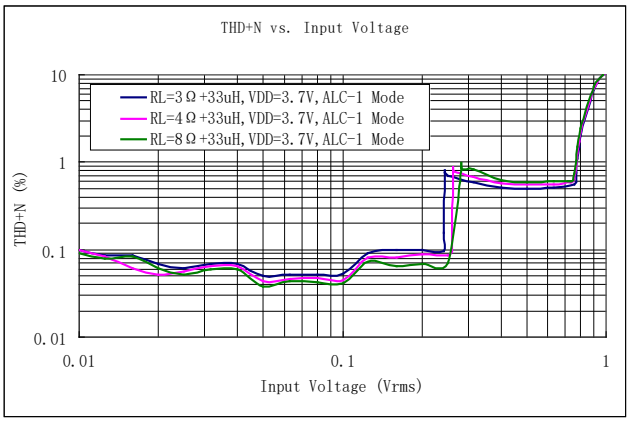


Figure 24: THD+N vs. Input Voltage

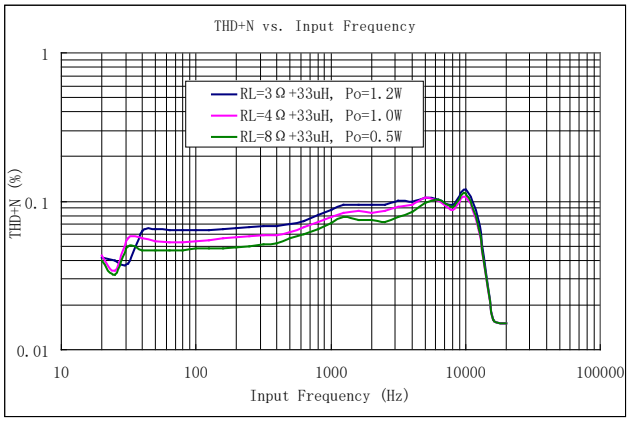


Figure 25: THD+N vs. Input Frequency

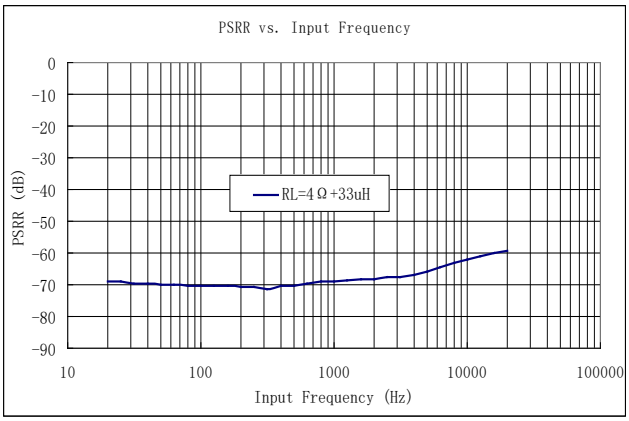


Figure 26: PSRR vs. Input Frequency

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

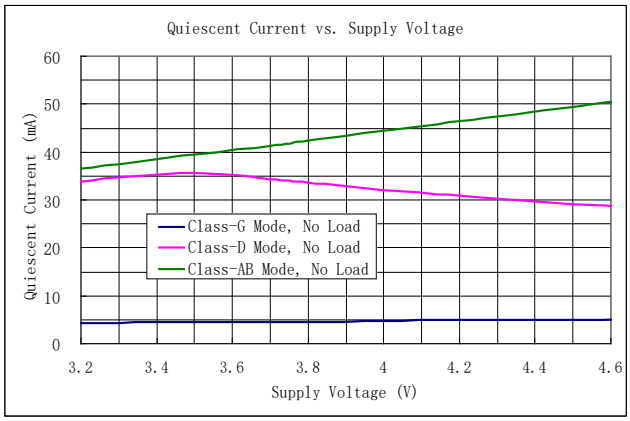


Figure 27: Quiescent Current vs. Supply Voltage

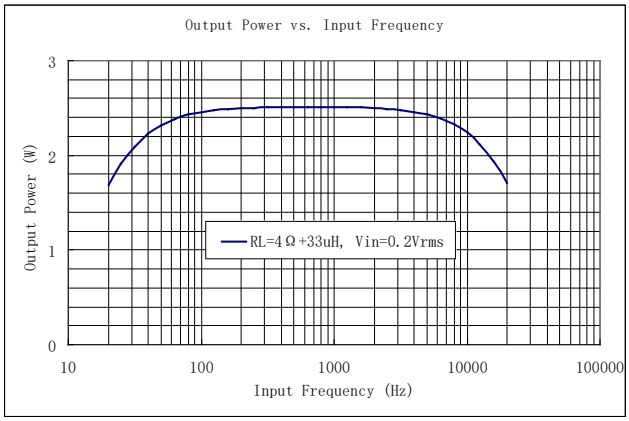


Figure 28: Output Power vs. Input Frequency (with 33kHz Lowpass Filter)

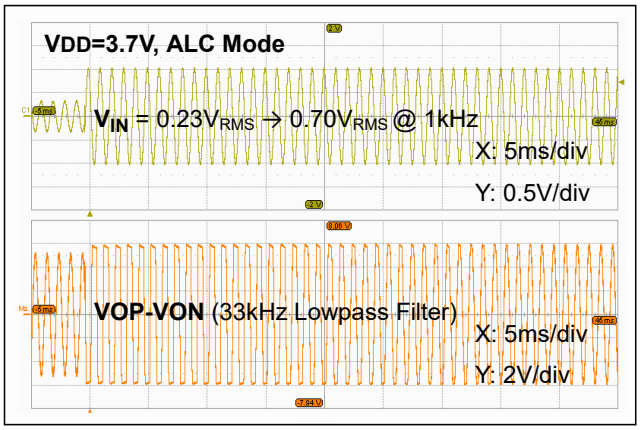


Figure 29: Output Waveforms on ALC Attack

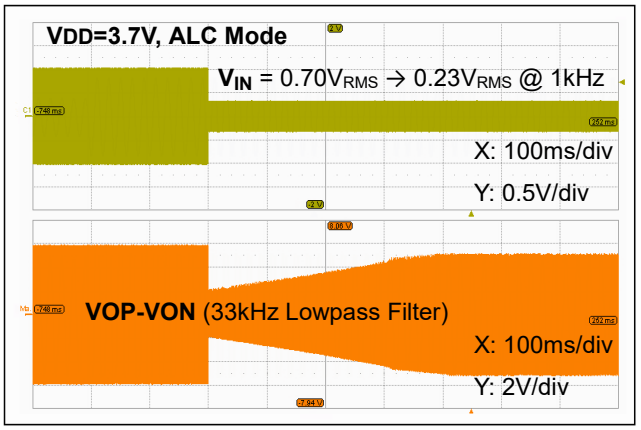


Figure 30: Output Waveforms on ALC Release

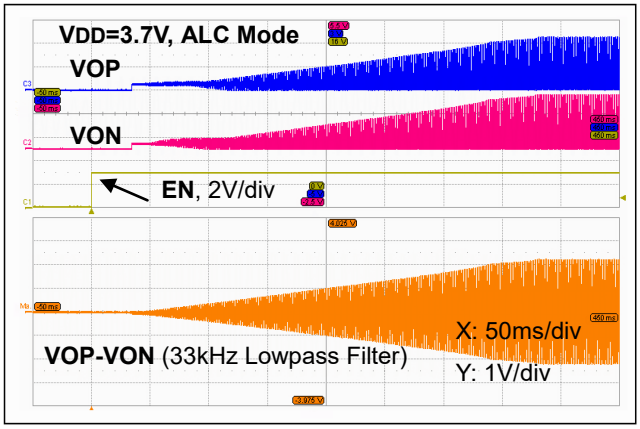


Figure 31: Output Waveforms during Startup

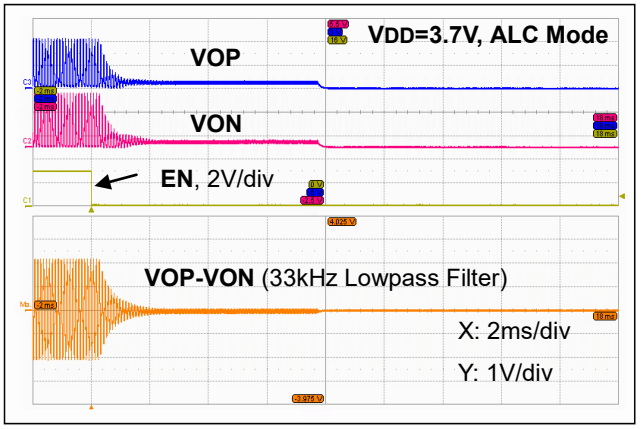


Figure 32: Output Waveforms during Shutdown

APPLICATION INFORMATION

The ft2850 is a 5W ***Dual-Pump***^{TM} Class-AB/D/G audio power amplifier with automatic level control (ALC) for portable audio applications. It integrates Class-AB and Class-D audio power amplifiers with a Class-G charge pump regulator based upon proprietary ***Dual-Pump***^{TM} topology. It operates from a range of supply voltages from 3.3V to 5.25V. With a supply voltage at 4.2V, it can deliver an output power of 5.5W with 10% THD+N, or 4.5W with 1% THD+N, into a 4Ω speaker load.

In ft2850, the power supply rail of the audio amplifier's output stage is adaptively boosted and regulated by a Class-G charge pump regulator, allowing much higher audio loudness than a stand-alone one directly connected to the battery. The adaptive nature of the Class-G charge pump regulator, whose output voltage varies dynamically in response to the level of the audio output, improves overall power efficiency and extends battery life when playing music. The higher output power and greater power efficiency resulted from the Class-G charge pump regulator make ft2850 an ideal audio solution for battery-powered electronic devices.

To facilitate various applications, the ft2850 provides three types of audio amplifier outputs, i.e., Class-AB, Class-D, and Class-G. For typical applications, the Class-G/D audio output is preferred for its high efficiency. The Class-AB audio output can be chosen to alleviate design complexities for applications where minimum FM radio interference is required.

The ft2850 features ALC that constantly monitors and safeguards the audio output against the boosted supply voltage, preventing output clipping distortion, excessive power dissipation, or speaker over-load. Once an over-level condition is detected, the ALC lowers the voltage gain of the audio amplifier proportionally to eliminate output clipping distortion while maintaining a maximum dynamic range of the audio output allowed by the boosted supply voltage. In ALC mode, with a 4.2V supply voltage, the ft2850 can deliver an ALC output power of 4.3W with 0.5% THD+N, into a 4Ω speaker load.

As specifically designed for portable device applications, the ft2850 incorporates shutdown mode to minimize the power consumption by holding the EN pin to ground. It also includes comprehensive protection features against various operating faults such as over-current, short-circuit, over-temperature, and under-voltage for a safe and reliable operation.

ADAPTIVE CHARGE PUMP REGULATOR

To allow for higher audio loudness, an on-chip Class-G charge pump regulator is employed to boost PVDD, the power supply rail of the audio amplifier's output stage, from the supply voltage AVDD to a higher value. It is thus required to connect PVDD directly to PVOUT, the output voltage of the charge pump regulator, on the system board via sufficiently wide metal trace. Whenever the audio output is higher than a prescribed level for an extended period of time, the charge pump regulator is activated to boost and regulate PVOUT at 6.5V, typically. In this manner, the charge pump regulator operates in the regulation mode.

On the other hand, when the audio output is less than a prescribed level for an extended period of time, the charge pump regulator is de-biased and forced into the standby mode. In the standby mode, the amplifier output stage is powered directly from the battery voltage through CVDD. The adaptive nature of the charge pump regulator can greatly improve the power efficiency of ft2850 when playing audio and extends battery life.

DUAL-PUMP^{TM} TECHNOLOGY

In order to maximize the output power, the ft2850 employs a proprietary ***Dual-Pump***^{TM} topology for the on-chip charge pump regulator using two flying capacitors to boost the supply voltage to a higher value. To limit the battery inrush current to an acceptable value when the supply voltage is first applied to the device, the charge pump regulator features soft-start during startup. Furthermore, when a short-circuit condition at the boosted voltage is detected, the ft2850 limits the input current to about 100mA for a safe operation.

Compared with a conventional charge pump topology using a single flying capacitor, the output current capability of the ***Dual-Pump***^{TM} can be significantly improved and the output voltage ripples minimized. In this manner, the output power of the Class-D audio amplifier is largely increased, particularly for low-impedance (4Ω or less)

speakers. With the ***Dual-Pump***^{TM} topology, the ft2850 can deliver an output power at 6.3W with 10% THD+N, or 5.3W with 1% THD+N, into a 3Ω speaker load when powered by a single-cell lithium battery at 4.2V.

DESIGN GUIDELINES OF *DUAL-PUMP*^{TM} REGULATOR

Selection of Flying Capacitors (C_{F1} & C_{F2})

A nominal value of 2.2μF is recommended for the flying capacitors (C_{F1} and C_{F2}) of the charge pump, but higher values can be used for applications to improve its dynamic response to load transients. A low equivalent-series-resistance (ESR) ceramic capacitor, such as X7R or X5R, is recommended.

Selection of Output Capacitor (C_{PVOUT})

The output capacitor of the charge pump regulator is required to keep output voltage ripples small and ensure maximum output power capability. Make sure that the output capacitor maintains its capacitance over the full range of DC bias and the desired operating temperature.

The low-frequency output power of the audio amplifier will be affected, to large extent, by the charge pump regulator's output capacitance, particularly for low-impedance (4Ω or less) speakers. Thus, for best audio quality, add a bulk tantalum or electrolytic capacitor in tandem with a 10μF low-ESR ceramic capacitor for the output capacitor (C_{PVOUT}). The value of the tantalum or electrolytic capacitor is application-specific. For 4Ω speaker loads, a bulk capacitor of 220μF should be sufficient.

It is highly recommended to add a small, good quality, low-ESR ceramic capacitor of 0.1μF in close proximity to the PVOUT pins for high-frequency filtering.

Speaker Load Impedance	C_{F1} & C_{F2} (Ceramic)	C_{PVOUT1} (Ceramic)	C_{PVOUT2} (Bulk Tantalum or electrolytic)
4Ω	1.5μF ~ 4.7μF	0.1μF//10μF	220μF ~ 470μF
8Ω	1.0μF ~ 3.3μF	0.1μF//10μF	100μF ~ 220μF

Table 1: Recommended Flying & Output Capacitors of *Dual-Pump*^{TM} Regulator

Selection of Supply Decoupling Capacitor (C_{CVDD})

For best power supply coupling, place a low-ESR ceramic capacitor (X7R or X5R), 10μF or greater, close to the CVDD pin. It is important to place the decoupling capacitor C_{CVDD} close to ft2850 since any parasitic resistances between ft2850 and C_{CVDD} cause efficiency loss. The decoupling capacitor serves as a charge reservoir for the input current that flows onto the flying capacitors C_{F1} and C_{F2}, thus reducing the amount of voltage ripples seen at the CVDD pin.

The decoupling capacitor C_{CVDD} must have an RMS current rating greater than 3A. Also the rated voltage of the input capacitor must be higher than the supply input voltage with sufficient voltage margin to minimize the effect of dc bias. For most applications, 15V with 10mΩ ESR is can be used. Also, consider adding a small, good quality, 0.1μF low-ESR ceramic capacitor to the CVDD pin for high-frequency supply coupling.

For applications where additional input capacitance is required to meet the requirement of the input current ripple or transient response, place an electrolytic or tantalum bulk capacitor in close proximity to ft2850. The bulk capacitor acts as a charge reservoir for the flying capacitor current, providing energy faster than the system power supply, mitigating current surges and/or voltage droops of the supply voltage. An electrolytic or tantalum bulk capacitor of 100μF should be sufficient for ft2850.

OPERATING MODE CONTROL

Three operating modes are available in ft2850 and can be selected via the MODE pin, as described in Table 2. For typical applications, the charge pump regulator is activated either adaptively (in response to the level of the audio output) or continually. With the charge pump regulator being activated adaptively where $V_{MODE} \leq 0.4V$, the Class-G audio output offers best power efficiency. On the other hand, the charge pump regulator can be activated at all times where $0.6V \leq V_{MODE} \leq 1.0V$. In this mode, the boosted voltage PVOUT of the charge pump can be used as a regulated supply voltage for other on-board devices such as LEDs. The total RMS current drawn from PVOUT by these external devices should be limited to less than 50mA. An excessive load current at

PVOUT will affect, to large extent, maximum output power and efficiency of ft2850.

For applications where FM interference must be minimized, the ft2850 can be configured into a traditional Class-AB audio amplifier where the charge pump regulator is disabled continually with $V_{MODE} \geq 1.4V$.

For a stable operation, add a small low-ESR ceramic capacitor of 0.1μF to the MODE pin for applications where the MODE pin is set by an external resistor divider or a GPIO port.

V_{MODE}	ALC Function	Charge Pump Regulator	Audio Output
$V_{MODE} \leq 0.4V$	Enabled	Enabled Adaptively	Class-G
$0.6V \leq V_{MODE} \leq 1.0V$	Enabled	Enabled Continually	Class-D
$V_{MODE} \geq 1.4V$	Disabled	Disabled Continually	Class-AB

Table 2: Operating Mode Control

AUTOMATIC LEVEL CONTROL (ALC)

The automatic level control is to maintain the audio output for a maximum voltage swing without clipping distortion when an excessive input that may cause output clipping is applied. With ALC, the ft2850 lowers the voltage gain of the amplifier to an appropriate value such that output clipping is substantially suppressed.

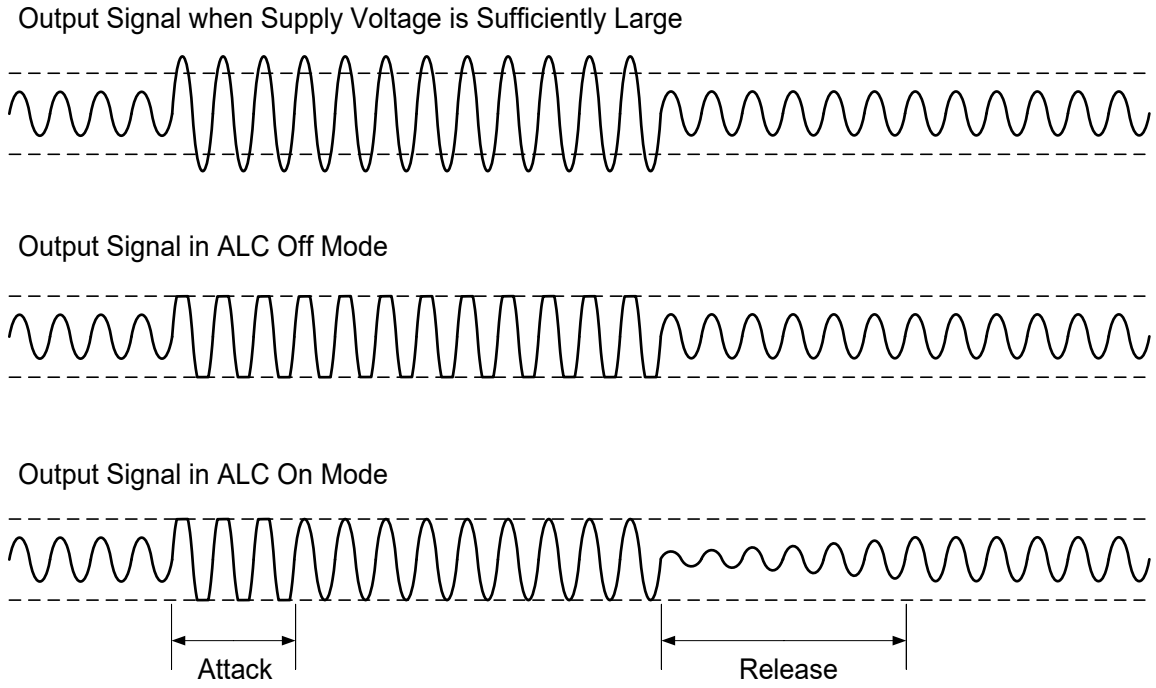


Figure 33: Automatic Level Control (ALC) Function Diagram

Attack is where the voltage gain of the audio amplifier decreases until output clipping is substantially eliminated. Release is where the voltage gain of the audio amplifier recovers (increases) until it reaches to a value that is maximally allowed without output clipping.

ALC MODE CONTROL

The ft2850 can be configured in ALC or Non-ALC mode via the ALC pin, as described in Table 5. When the ALC pin is shorted to AVDD through a 10kΩ resistor, the ft2850 operates in Non-ALC mode. The Non-ALC operation is typically chosen for applications where maximum audio loudness is much desired and the amount of output clipping distortions can be measurably controlled at the audio source. In other pin configurations, the ft2850 operates in ALC mode with four specific audio dynamic characteristics. For most applications, the ALC mode of operation is much preferred for its capability to substantially eliminate output clipping distortion, excessive power dissipation, and speaker over-load.

Four sets of ALC dynamic characteristics can be selected for specific sound effects, as described in Table 5. The ALC-1 mode (the ALC pin unconnected) tends to play music in a most dynamic manner with some extent of

clipping distortion and higher average output power (loudness). On the other hand, the ALC-4 mode (the ALC pin shorted to GND) tends to play music in a most mellow manner with negligible amount of clipping distortion and lower average output power.

Note that the ALC function can be activated only when the audio amplifier operates in Class-G/D configuration. The ALC function is deactivated when the audio amplifier operates in Class-AB configuration.

ALC Pin Configuration	ALC Mode	Sound Effects	
		Loudness	Output Clipping Distortion
10kΩ to AVDD	Non-ALC	Potentially highest loudness	No control on output clipping
Unconnected	ALC-1	Most dynamic sound (Highest loudness under ALC)	Acceptable output clipping
68kΩ to GND	ALC-2	Slightly lower loudness	Medium output clipping
27kΩ to GND	ALC-3	Medium loudness	Slight output clipping
Short to GND	ALC-4	Most mellow sound (Lowest loudness under ALC)	Negligible output clipping

Table 5: ALC Mode Control

VOLTAGE GAIN SETTING

The voltage gain of the audio amplifier can be adjusted by inserting an external input resistor in series with an input capacitor to both differential inputs (INN and INP) individually. The value of R_{IN} in kΩ for a given voltage gain can be calculated by Equation 1, where A_V is the voltage gain of the audio amplifier. Table 3 shows suitable resistor values of R_{IN} that can be used for specific voltage gains.

$$A_V = \frac{450}{R_{IN} + 18} \qquad (1)$$

R_{IN} (kΩ)	0	2.2	4.7	7.5	10	14	18	22	27	33	39
A_V (V/V)	25	22	20	17.6	16	14	12.5	11	10	9	8
A_V (dB)	28	27	26	25	24	23	22	21	20	19	18

Table 3: External Input Resistors Required for Specific Voltage Gains

The choice of the voltage gain will highly influence the loudness and quality of audio sounds. In general, the higher the voltage gain is, the louder the sound is perceived. However an excessive voltage gain may cause the audio output to be severely compressed or clipped for high-level (loud) audio sounds. On the other hand, an unusually low gain may cause relatively low-level (quiet) sounds soft or inaudible. Thus it is crucial to choose a proper voltage gain for high audio quality.

The voltage gain is chosen based upon various system-level considerations including the boosted supply voltage, maximum input level of the audio source, output power rating, and desired sound effect. As an example, Table 4 shows the voltage gains for various audio input levels. In the table, R_{IN} is the external input resistor in series with the input capacitor. Typically, the voltage gain of audio amplifiers is set between 25X (28dB) and 8X (18dB), which corresponds to an external input resistor between 0Ω and 39kΩ, respectively.

$V_{IN, MAX}$ (V_{RMS})	R_{IN} (kΩ)	Class-G/D Output		Class-AB Output	
		A_V (V/V)	A_V (dB)	A_V (V/V)	A_V (dB)
0.30	0	25	28	15	24
0.50	10	16	24	10	20
0.70	22	11	21	7	17
1.0	39	8	18	5	14

Table 4: Typical Voltage Gain Settings for Various Audio Input Levels

In Class-AB configuration where the charge pump regulator is disabled, the voltage gain is internally lowered to 60% (-4dB) of the value defined in Class-G/D operation where the charge pump regulator is enabled.

The voltage gain can be also expressed in Equation 2. In the equation, $V_{IN, MAX}$ (in V_{RMS}) is the maximum input level of the audio source, PVDD (in volts) is the boosted supply voltage, and α is a design parameter that determines the ALC dynamic range (maximum attention) and typically ranges from 0.65 to 1.2. Higher α results in higher ALC range (maximum attenuation) and higher average output power (loudness) with some degree of compression for high-level audio sounds. Conversely, lower α results in lower ALC range and lower average output power (loudness) with minimum or no compression for high-level audio sounds.

$$A_V = \frac{\alpha \times PVDD}{V_{IN, MAX}} \qquad (2)$$

VOLUME FADE-IN & FADE-OUT

The ft2850 features volume fade-in and fade-out to reduce intermittent sound and eliminate uncomfortable hearing experience during the transitions when the device enters into or exits out of normal operation. Figure 34 and Figure 35 show the audio output waveforms during fade-in and fade-out respectively.

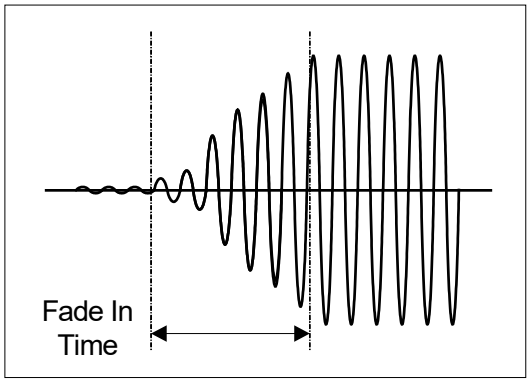


Figure 34: Fade-In Output Waveform

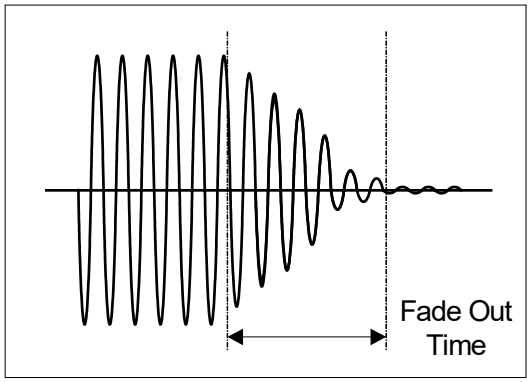


Figure 35: Fade-Out Output Waveform

For specific sound effects during startup, there are five fade-in times that can be selected by use of different pin configurations at the FADE pin. Table 6 describes the corresponding pin configuration for each individual fade-in time ranging from 10 milliseconds to 640 milliseconds. When the FADE pin is left unconnected, the fade-in time is set at its default value at 320 milliseconds.

FADE Pin Configuration	Fade-In Time (ms)
10kΩ to AVDD	640
Unconnected	320
68kΩ to GND	160
27kΩ to GND	40
Short to GND	10

Table 6: Fade-In Time Settings

SHUTDOWN AND STARTUP

The ft2850 employs EN pin to minimize power consumption while it is not in use. When the EN pin is pulled to ground, the ft2850 is forced into shutdown mode, where all the analog circuitry is de-biased and the supply current is reduced to be less than 1μA, and the differential outputs are individually shorted to ground through an internal resistor (2kΩ). Once in shutdown mode, the EN pin must remains low for at least 10 milliseconds (T_{SD}), the shutdown settling time, before it can be brought high again. When the EN pin is asserted high, the device exits out of shutdown mode and resumes normal operation after the startup time (T_{STUP}) of 40 milliseconds.

Note that an internal pulldown resistor of 300kΩ is included onto the EN pin. Furthermore, shutdown mode is the state when the power supply is first applied to the device. Whenever possible, it is recommended to assert EN high to exit the device out of shutdown mode only after the device is properly started up. Also, place the amplifier in shutdown mode prior to removing the power supply voltage.

CLICK-AND-POP SUPPRESSION

The audio power amplifier in ft2850 features comprehensive click-and-pop suppression. During startup, the click-and-pop suppression circuitry reduces audible transients internal to the device. When entering into shutdown mode, the differential audio outputs ramp down to ground quickly and simultaneously.

BYPASS PIN

A voltage at $V_{DD}/2$ is internally generated and provided to the BYP pin. Add a 1μF low-ESR ceramic capacitor to the pin for a high PSRR.

PSRR ENHANCEMENT

With a dedicated pin for the common-mode voltage bias and an external holding capacitor onto the pin, the ft2850 achieves a high PSRR, 70dB at 1kHz.

PROTECTION MODES

Against various operating faults for a safe and reliable operation, the ft2850 features comprehensive protection modes including Under-Voltage Lockout (UVLO), Over-Current Protection (OCP), and Over-Temperature Shutdown (OTSD).

Under-Voltage Lockout (UVLO)

The ft2850 incorporates circuitry to detect a low supply voltage. When the supply voltage is first applied, the ft2850 remains inactive until the supply voltage exceeds 2.2V (V_{UVLU}). When the supply voltage is removed and drops below 2.0V (V_{UVLD}), the ft2850 enters into shutdown mode immediately.

Over-Temperature Shutdown (OTSD)

When the die temperature exceeds a preset threshold (160°C), the device enters into over-temperature shutdown mode, where two differential outputs are pulled to ground through an internal resistor (2kΩ) individually. The device will resume a normal operation once the die temperature returns to a lower temperature, which is about 20°C lower than the threshold.

Over-Current Protection (OCP)

During operation, the ft2850 constantly monitors the output of Class-D audio amplifier for any over-current or short-circuit conditions. When a short-circuit condition between two differential outputs, differential output to PVDD or ground is detected, the output stage of the amplifier is immediately forced into high impedance state. Once the fault condition persists over a prescribed period, the ft2850 then enters into shutdown mode and remains in this mode for about 120 milliseconds. During shutdown, the power switches of the charge pump regulator are also turned off, and the PVDD is discharged through an internal resistor to ground.

When shutdown mode times out, the ft2850 will initiate another startup sequence and then check if the short-circuit condition has been removed. Meanwhile, the charge pump regulator tries to bring PVDD up to the preset voltage again. If the fault condition is still present, the ft2850 will repeat itself for the process of a startup followed by detection, qualification, and shutdown. It is the so-called hiccup mode of operation. Once the fault condition is removed, the ft2850 automatically restores to its normal mode of operation.

Although the output stage of the Class-D audio amplifier can withstand a short between VOP and VON, do not connect either output directly to GND, AVDD, CVDD, PVOUT, PVDD as this might damage the device permanently.

CLASS-D AUDIO AMPLIFIER

The Class-D audio amplifier in the ft2850 operates in much the same way as traditional Class-D amplifiers and similarly offers much higher power efficiency than Class-AB amplifiers. The high efficiency of Class-D operation is achieved by the switching operation of the output stage of the amplifier. The power loss associated with the output stage is limited to the conduction and switching loss of the power switches, which are much less than the power loss associated with a linear output stage in Class-AB amplifiers.

Fully Differential Amplifier

The ft2850 includes a fully differential amplifier with differential inputs and outputs. The fully differential amplifier ensures that the differential output voltage is equal to the differential input voltage times the amplifier gain. Although the ft2850 supports for a single-ended input, differential inputs are much preferred for applications where the environment can be noisy in order to ensure maximum SNR.

Low-EMI Filterless Output Stage

Traditional Class-D audio amplifiers require for the use of external LC filters, or shielding, to meet EN55022B electromagnetic-interference (EMI) regulation standards. The ft2850 applies an edge-rate control circuitry to reduce EMI emission, while maintaining high power efficiency.

Filterless Design

Traditional Class-D amplifiers require an output filter to recover the audio signal from the amplifier's output. The filter adds cost, increases the solution size of the amplifier, and can adversely affect efficiency and THD+N performance. The traditional PWM scheme uses large differential output swings (twice of the supply voltage) and causes large ripple currents. Any parasitic resistance in the filter components results in loss of power and lowers the efficiency.

The ft2850 does not require an output filter. The device relies on the inherent inductance of the speaker coil and the natural filtering of both the speaker and the human ear to recover the audio component of the square-wave output. By eliminating the output filter, a smaller, less costly, and more efficient solution can be accomplished.

Because the frequency of the ft2850 output is well beyond the bandwidth of most speakers, voice coil movement due to the square-wave frequency is very small. Although this movement is small, a speaker not designed to handle the additional power can be damaged. For optimal performance, use a speaker with a series inductance greater than 10μH. Typical 4Ω speakers exhibit series inductances in the range from 10μH to 47μH.

Ferrite Bead EMI Filter

The ft2850 does not require an LC output filter for short connections from the amplifier to the speaker. However, additional EMI suppression can be made by use of a simple ferrite bead filter comprising a ferrite bead and a capacitor, as shown in Figure 36. Choose a ferrite bead with low DC resistance (DCR) and high impedance (220Ω ~ 470Ω) at high frequencies (>100MHz). The current flowing through the ferrite bead must be also taken into consideration. The effectiveness of ferrites can be greatly aggravated at much lower than the rated current values. Choose a ferrite bead with a rated current value no less than 3A. The capacitor value varies based on the ferrite bead chosen and the actual speaker lead length. Choose a capacitor less than 1nF based on EMI performance. Place each ferrite bead filter tightly together and individually close to VOP and VON pins respectively.

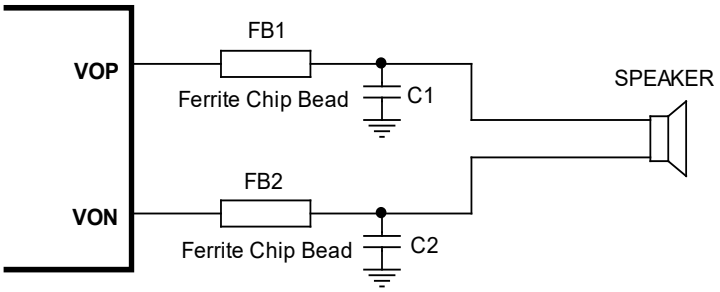


Figure 36: Ferrite Bead Filter to Reduce EMI

Class-D Output RC Snubber Circuit

For applications where speaker load resistances are 4Ω or less with long speaker wires, it may become necessary to add a snubber circuit across the two output pins, VOP and VON, to prevent the device from accelerated deterioration or abrupt destruction due to excessive inductive flybacks that are induced on fast output switching or by an over-current or short-circuit condition. The snubber circuit can also lower EMI emission of Class-D outputs.

Figure 37 shows a simple RC snubber circuit with suggested values of R_3=4.7Ω in series with C_3=4.7nF. Note that the design of the RC snubber circuit is specific to each design and must take into account the parasitic reactance of the system board to reach proper values of R_3 and C_3. Evaluate and ensure that the voltage spikes (overshoots and undershoots) at VOP and VON on the actual system board are within their absolute maximum ratings. Pay close attention to the layout of the RC snubber circuit to be tight and close to VOP and VON pins.

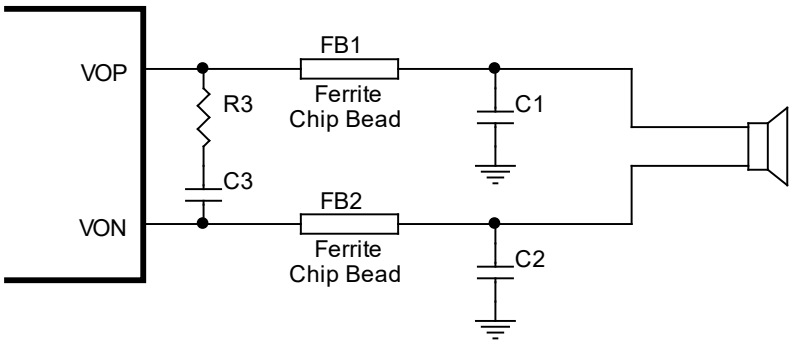


Figure 37: Class-D Output RC Snubber Circuit

Input Resistors (R_{IN})

In ft2850, a pair of 18kΩ input resistors is internally integrated onto INP and INN pins respectively. Internal input resistors bring such benefits as fewer variations on PSRR and minimum turn-on pop noise since on-chip resistors tend to match well. Additional input resistors can be externally added onto INP and INN pins respectively for specific voltage gains. The value of external input resistors must be included for the calculation of overall voltage gain, as described in Equation 3, as well as the selection of proper input capacitors, as described in Equation 4. As shown in Equation 3, the external input resistors attenuate the original voltage gain by the ratio of $R_{INTERNAL}$ / (R_{IN}+$R_{INTERNAL}$).

$$A_V = A_{V0} \times [R_{INTERNAL} / (R_{IN}+R_{INTERNAL})] \quad (3)$$

where A_{V0} = 25 (28dB) and $R_{INTERNAL}$ = 18kΩ

Input Capacitors (C_{IN})

Input DC decoupling capacitors for audio inputs are recommended. The input DC decoupling capacitors will remove the DC bias from audio inputs. The input capacitor C_{IN} and input resistors (R_{IN} plus $R_{INTERNAL}$) form a highpass filter with the corner frequency, f_C, defined in Equation 4.

$$f_C = 1 / [2 \times \pi \times (R_{IN} + 18k\Omega) \times C_{IN}] \quad (4)$$

R_{IN} is the external input resistance for a specific voltage gain. Note that the variation of the actual input resistance will affect the voltage gain proportionally. Choose R_{IN} with a tolerance of 2% or better.

Choose C_{IN} such that the f_C is well below the lowest frequency of interest. Setting f_C too high affects the low frequency response of the amplifier. Consider an example where the specification calls for A_V=24dB and a flat frequency response down to 20Hz. In this example, R_{IN}=10kΩ and C_{IN} is calculated to be 0.28μF; thus either 0.33μF or 0.47μF, as a common choice of capacitances, can be chosen for C_{IN}.

Note that any mismatch in resistance or capacitance between two audio inputs will cause a mismatch in the corner frequencies. Severe mismatch may also cause turn-on pop noise, PSRR, CMRR performance. Choose C_{IN} with a tolerance of ±2% or better.

Furthermore, the type of the input capacitors is crucial to audio quality. For best audio quality, use capacitors whose dielectrics have low voltage coefficients, such as tantalum or aluminum electrolytic. Capacitors with high-voltage coefficients, such as ceramics, may result in increased distortion at low frequencies.

Supply Decoupling Capacitors (C_{AVDD}, C_{PVDD})

Sufficient decoupling of the power supplies is crucial for the audio amplifier in ft2850 to ensure high efficiency, low distortion, and low EMI.

Place a 1μF low-ESR ceramic capacitor (C_{AVDD}) in close proximity to the AVDD pin. Furthermore, add a small decoupling resistor (R_{AVDD}) of 10Ω between the system power supply and the AVDD pin, minimizing the detrimental effect of high battery current ripples on on-chip linear circuitry.

Place a 1μF low-ESR ceramic capacitor of (C_{PVDD}) in close proximity to the PVDD pin. In tandem with C_{PVDD}, add a small, good quality, low-ESR ceramic capacitor of 0.1μF for high-frequency supply coupling.

PRINTED CIRCUIT BOARD (PCB) LAYOUT CONSIDERATIONS

Ground Plane - It is required to use a solid metal plane with sufficiently wide area as a central ground connection (GND) for ft2850. All ground pins (AGND, CGND, and PGND) should be directly connected to the ground plane.

Supply Decoupling capacitors – The supply decoupling capacitors (C_{AVDD} and C_{PVDD}) should be placed as individually close as possible to AVDD and PVDD pins. Also, in tandem with C_{PVDD}, add a small, good quality, low-ESR ceramic capacitor of 0.1μF to PVDD pin for high-frequency supply coupling.

Charge Pump Input Capacitor - Place a 10μF ceramic capacitor C_{CVDD} as close to CVDD pins as possible. In tandem with C_{CVDD}, consider adding a small, good quality, high-frequency, low-ESR ceramic capacitor of 0.1μF.

Charge Pump Flying Capacitors – Place C_{F1} flying capacitor as close as possible to CP1 and CN1 pins and C_{F2} flying capacitor as close as possible to CP2 and CN2 pins.

Charge Pump Output Capacitor - Place a 10μF ceramic capacitor C_{PVOUT} as close to PVOUT pin as possible. In tandem, it is highly recommended to add a small, good quality, high-frequency, low-ESR ceramic capacitor of 0.1μF. The PVDD pin must be directly shorted to the PVOUT pin with wide and short metal trace on the system board. For higher audio output power (3W or greater) applications, place additional bulk electrolytic or tantalum capacitor (100μF or greater) in tandem with C_{PVOUT}.

Ferrite Bead EMI Filter – The ferrite bead EMI filters should be placed tightly together and individually close to the audio output pins, VOP and VON respectively, for the best EMI performance. Keep the current loop, traversing from each of the audio outputs through the ferrite bead the small filter capacitors and back to PGND, as short as possible.

Class-D Output RC Snubber – Place the RC snubber circuit tightly together and as close as possible to the audio output pins, VOP and VON.

Power Dissipation - The maximum output power of ft2850 can be severely limited by its thermal dissipation capability. To ensure the device operating properly and reliably at its maximum output power without incurring over-temperature shutdown, the following guidelines are given for optimum thermal dissipation capability:

- Fill both top and bottom layers of the system board with solid GND metal traces.
- Solder the thermal pad directly onto a grounded metal plane.
- Place lots of equally-spaced vias underneath the thermal pad connecting the top and bottom layers of GND. The vias are connected to a solid metal plane on the bottom layer of the board.
- Reserve wide and uninterrupted areas along the thermal flow on the top layer, i.e., no wires cutting through the GND layer and obstructing the thermal flow.
- Place the Input/output capacitors of the charge pump regulator tightly together and on the same layer of the board with ft2850.
- Avoid using vias for traces carrying high current.

TYPICAL APPLICATION CIRCUITS

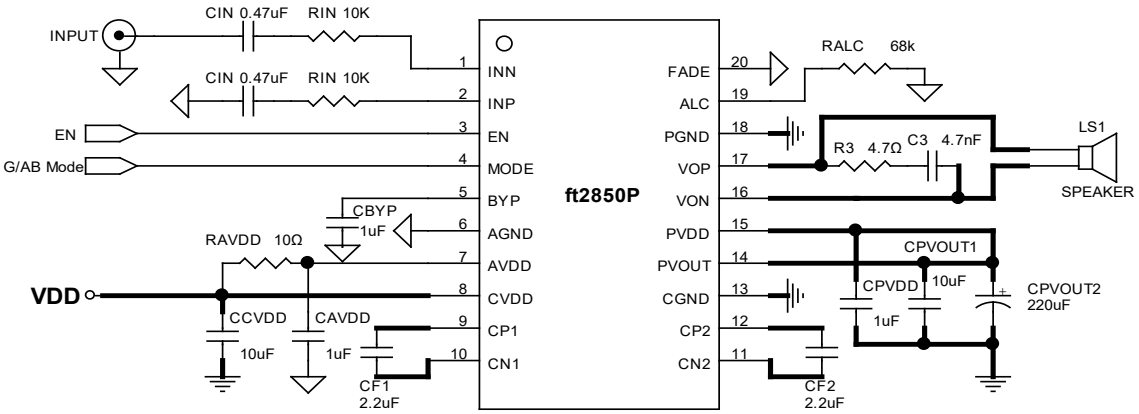


Figure 38: Single-Ended Audio Input in ALC-2 Mode with Selectable Class-G/AB Operation

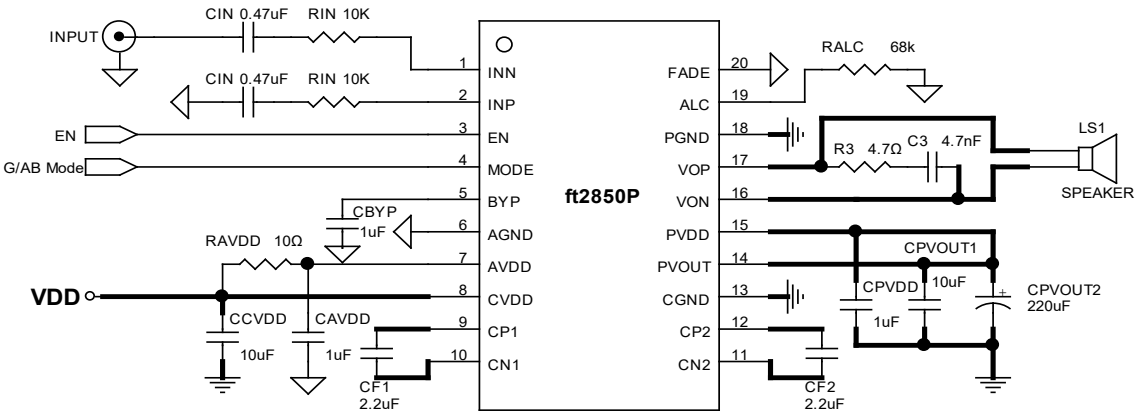


Figure 39: Differential Audio Inputs in ALC-1 Mode with Selectable Class-G/D Operation

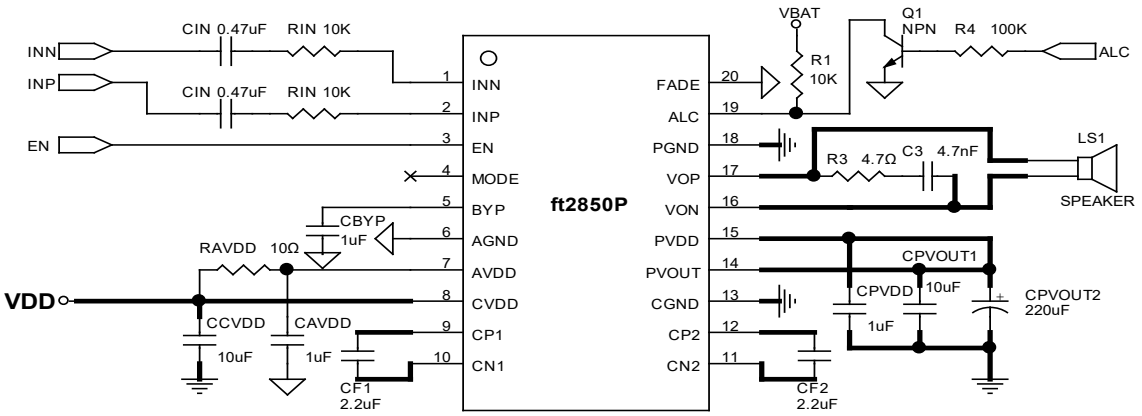


Figure 40: Selectable Non-ALC/ALC-4 Mode with Class-G Operation

Note: The bold lines indicate high current paths and their respective traces are required to be as wide and short as possible on the system board for high power applications.

TYPICAL APPLICATION CIRCUITS (Cont'd)

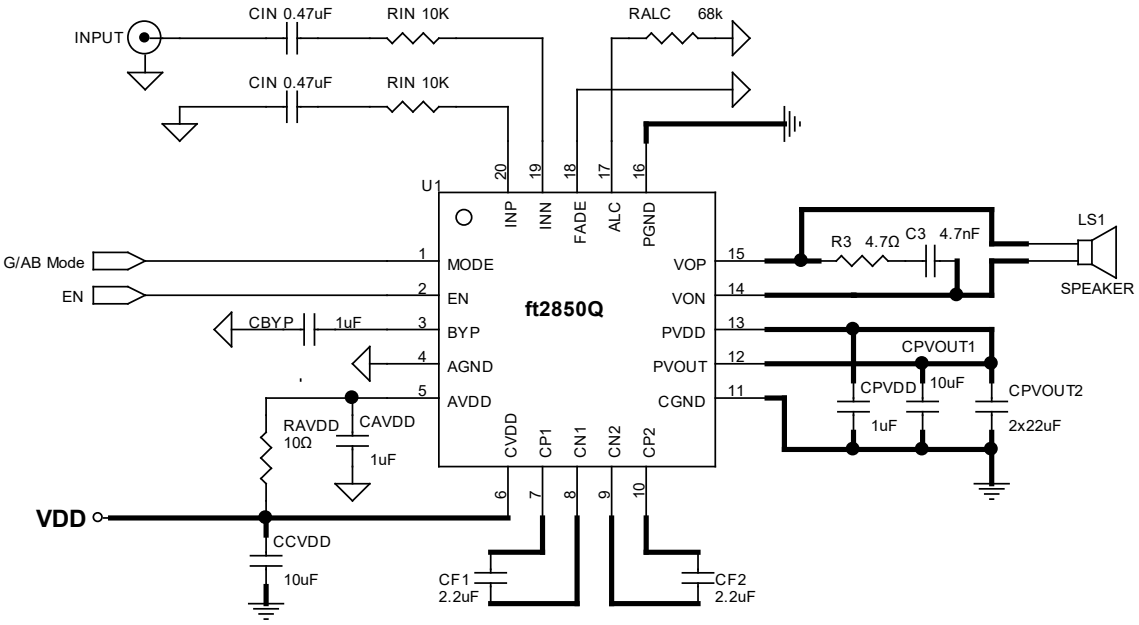
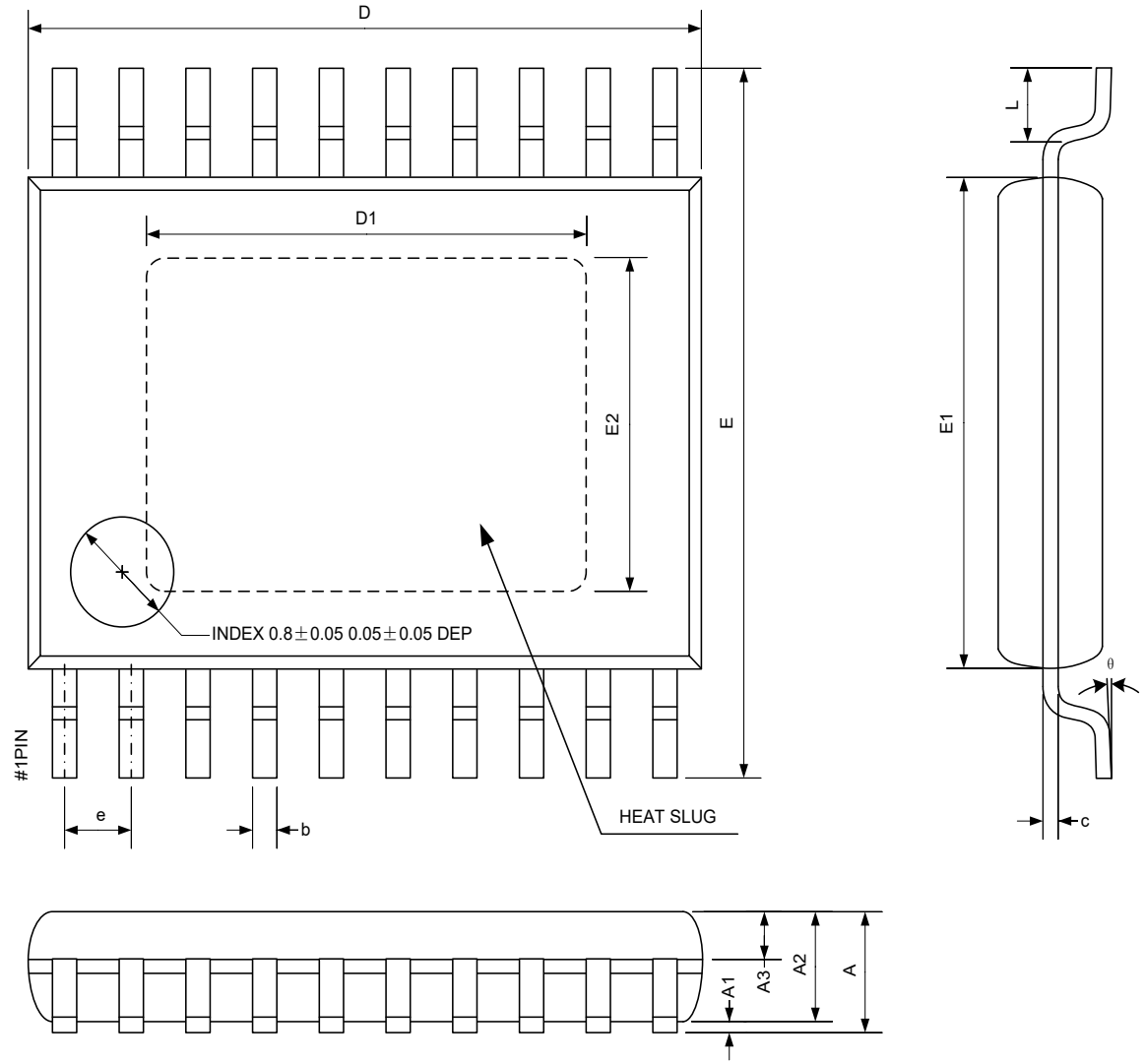


Figure 41: ALC-2 Mode with Selectable Class-G/AB Operation

PHYSICAL DIMENSIONS

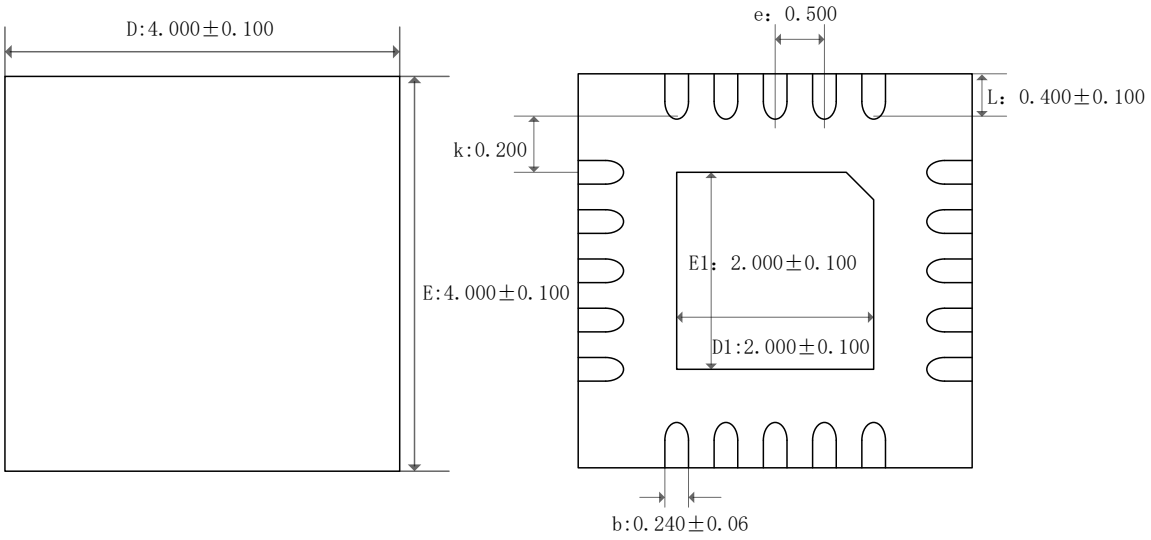
TSSOP-20L PACKAGE OUTLINE DIMENSIONS



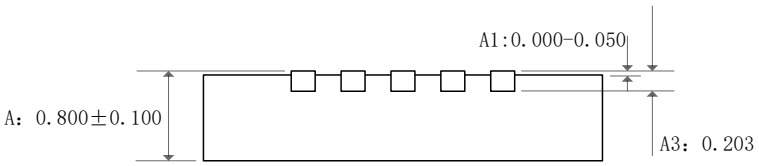
SYMBOL	MIN	NOM	MAX	UNIT
A	-	-	1.20	mm
A1	0.05	-	0.15	mm
A2	0.90	1.00	1.05	mm
A3	0.34	0.44	0.54	mm
b	0.20	-	0.28	mm
c	0.10	-	0.19	mm
D	6.40	6.50	6.60	mm
D1	4.00	4.20	4.40	mm
E	6.20	6.40	6.60	mm
E1	4.30	4.40	4.50	mm
E2	2.80	3.00	3.20	mm
e	0.65BSC			mm
L	0.45	0.60	0.75	mm
θ	0	-	8	°

PHYSICAL DIMENSIONS (Cont'd)

QFN4X4-20L PACKAGE OUTLINE DIMENSIONS



Top View Bottom View



Side View

All dimensions are in millimeters

Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	3.900	4.100	0.154	0.161
E	3.900	4.100	0.154	0.161
D1	1.900	2.100	0.075	0.083
E1	1.900	2.100	0.075	0.083
k	0.200MIN.		0.008MIN.	
b	0.180	0.300	0.007	0.012
e	0.500TYP.		0.020TYP.	
L	0.300	0.500	0.012	0.020

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