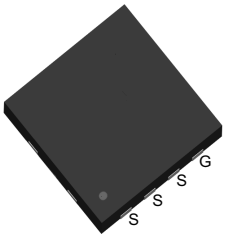
WPM3028

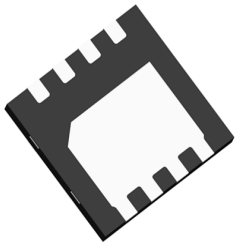
Single P-Channel, -30V, -22A, Power MOSFET

Http://www.sh-willsemi.com

V_{DS} (V)	Typical $R_{DS(on)}$ (mΩ)
-30	11 @ V_{GS}=-10V
	15 @ V_{GS}=-5V



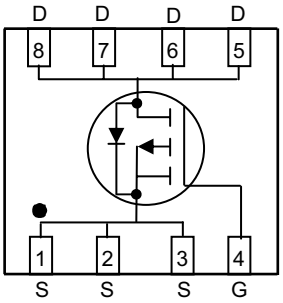
Top View



Bottom View

Description

The WPM3028 is P-Channel enhancement MOS Field Effect Transistor. Uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in DC-DC conversion, power switch and charging circuit. Standard Product WPM3028 is Pb-free.



Pin configuration (Top view)

Features

- Trench Technology
- Supper high density cell design
- Excellent ON resistance
- Extremely Low Threshold Voltage
- Small package DFN3X3-8L

3028 = Device Code
PS = Special Code
Y = Year
W = Week(A~z)

Marking

Applications

- DC/DC converters
- Power supply converters circuit
- Load/Power Switching for portable device

Order information

Device	Package	Shipping
WPM3028-8/TR	DFN3X3-8L	3000/Tape&Reel

Absolute Maximum ratings

Parameter		Symbol	Maximum	Unit
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±25	
Continuous Drain Current [d]	T_C=25°C	I_D	-22	A
	T_C=70°C		-22	A
Pulsed Drain Current [c]		I_{DM}	-88	A
Continuous Drain Current	T_A=25°C	I_{DSM}	-14	A
	T_A=70°C		-11	
Avalanche Energy L=0.3mH		E_{AS}	97	mJ
Power Dissipation [b]	T_C=25°C	P_D	43	W
	T_C=70°C		27	
Power Dissipation [a]	T_A=25°C	P_{DSM}	4.5	W
	T_A=70°C		2.8	
Operating Junction Temperature		T_J	-55 to 150	°C
Storage Temperature Range		T_{STG}	-55 to 150	°C

Thermal resistance ratings

Single Operation					
Parameter		Symbol	Typical	Maximum	Unit
Junction-to-Ambient Thermal Resistance [a]	t ≤ 10 s	$R_{\theta JA}$	21	28	°C/W
	Steady State		46	58	
Junction-to-Case Thermal Resistance	Steady State	$R_{\theta JC}$	2.1	3	

Note:

a The value of $R_{\theta JA}$ is measured with the device mounted on 1-inch^2 (6.45cm^2) with 2oz.(0.071mm thick) Copper pad on a 1.5*1.5 inch^2, 0.06-inch thick FR4 PCB, in a still air environment with T_A =25°C. The power dissipation P_{DSM} is based on $R_{\theta JA}$ t≤10s value and the $T_{J(MAX)}$=150°C. The value in any given application is determined by the user's specific board design.

b The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

c Repetitive rating, ~10us pulse width, duty cycle ~1%, keep initial T_J =25°C, the maximum allowed junction temperature of 150°C.

d The maximum current rating by source bonding technology.

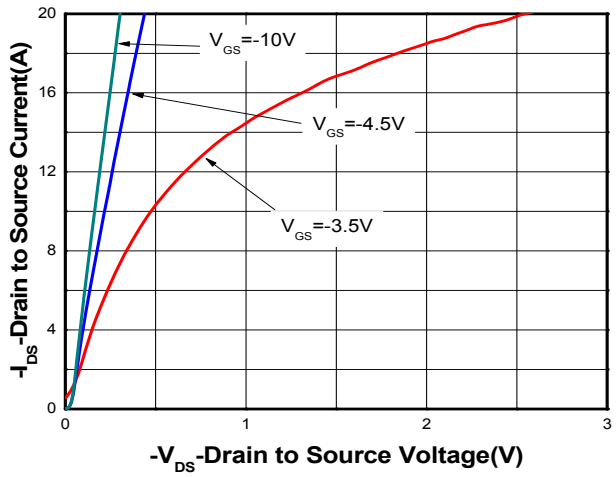
e The static characteristics are obtained using ~380us pulses, duty cycle ~1%.

f Guaranteed by design

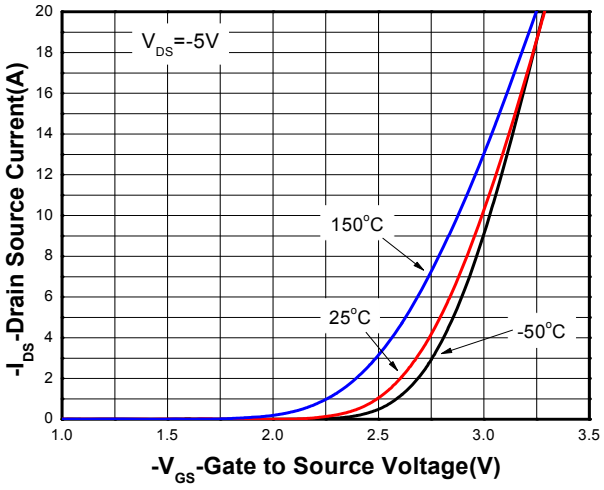
Electronics Characteristics (Ta=25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = -250uA	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} =-24V, V_{GS} = 0V			-1	uA
Gate-to-source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±25V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = -250uA	-1.0	-1.8	-3.0	V
Drain-to-source On-resistance	$R_{DS(on)}$	V_{GS} = -10V, I_D = -10A		11	15	mΩ
		V_{GS} =-5V, I_D = -7A		15	20	
Forward Transconductance	g_{FS}	V_{DS} = -5 V, I_D = -8A		7	16	S
Maximum Body-Diode Continuous Current [f]	Is				-22	A
CHARGES, CAPACITANCES AND GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1.0MHz, V_{DS} = -15 V		2106		pF
Output Capacitance	C_{OSS}			353		
Reverse Transfer Capacitance	C_{RSS}			274		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = -10 V, V_{DS} = -15 V, I_D =-10 A		38		nC
Threshold Gate Charge	$Q_{G(TH)}$			4		
Gate-to-Source Charge	Q_{GS}			7.7		
Gate-to-Drain Charge	Q_{GD}			6.5		
Gate Resistance	R_g	V_{GS} = 0 V, V_{DS} = 0 V, f=1MHz		10		Ω
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	td(ON)	V_{GS} = -10 V, V_{DS} =-15 V, I_D=-5A, R_G=6Ω		18		ns
Rise Time	tr			24		
Turn-Off Delay Time	td(OFF)			114		
Fall Time	tf			47		
BODY DIODE CHARACTERISTICS						
Forward Voltage	V_{SD}	V_{GS} = 0 V, I_S = -1A		-0.8	-1.2	V

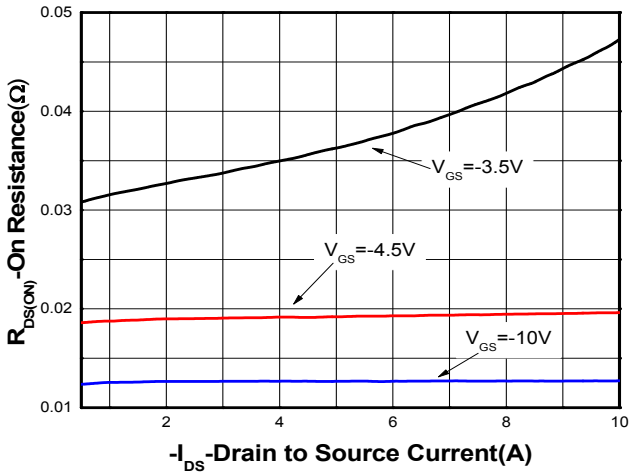
Typical Characteristics (Ta=25°C, unless otherwise noted)



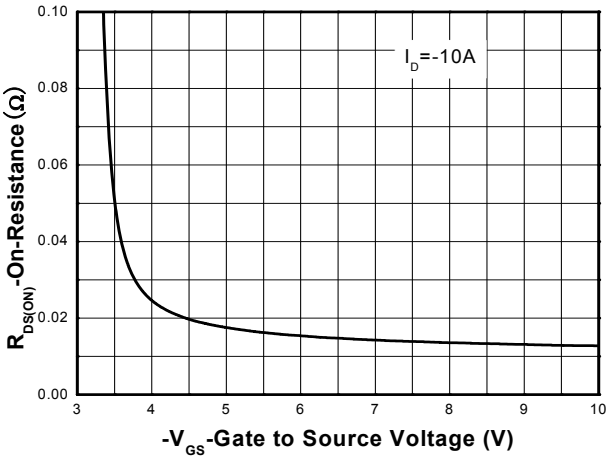
Output Characteristics [e]



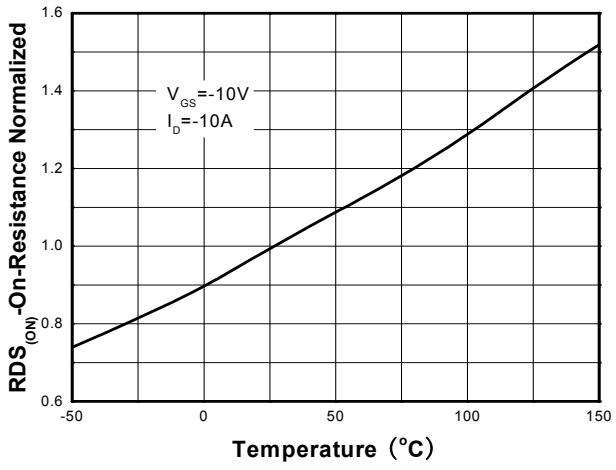
Transfer Characteristics [e]



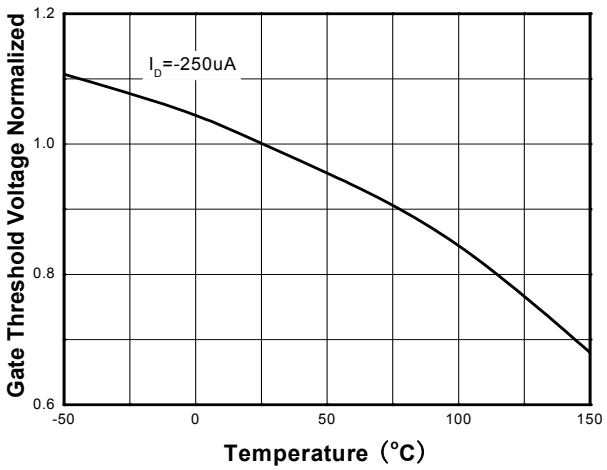
On-Resistance vs. Drain Current [e]



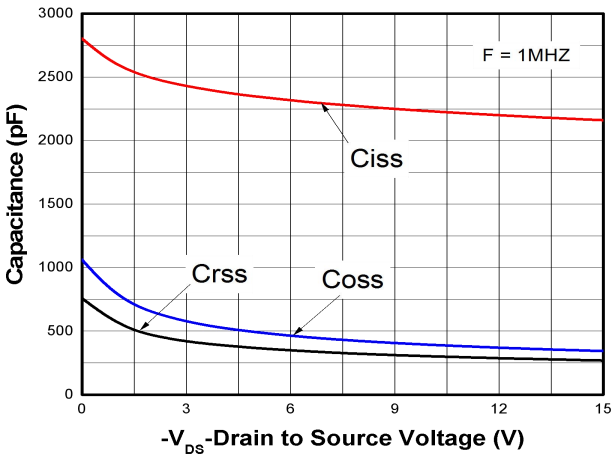
On-Resistance vs. Gate-to-Source Voltage [e]



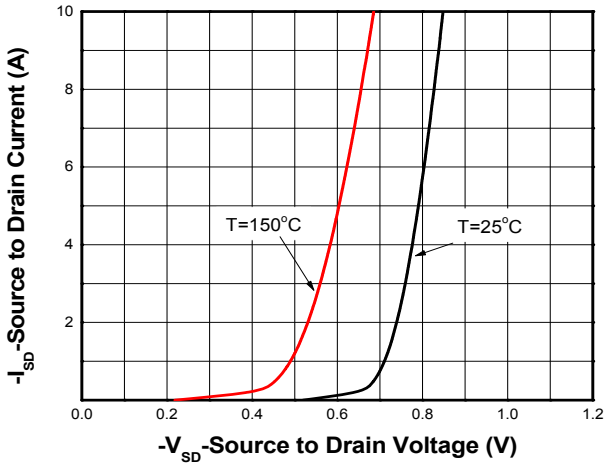
On-Resistance vs. Junction Temperature [e]



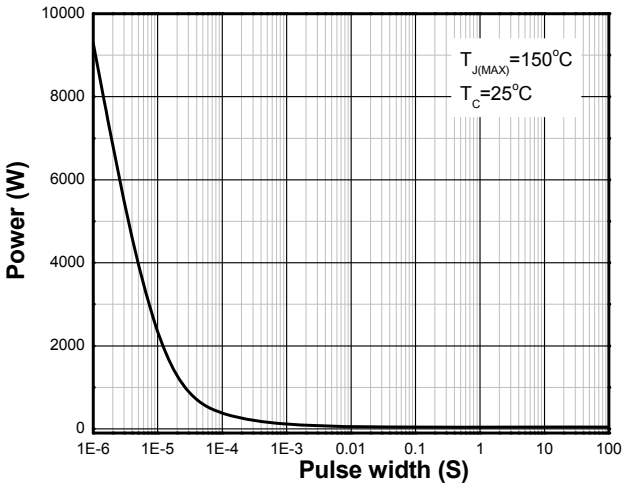
Threshold Voltage vs. Temperature



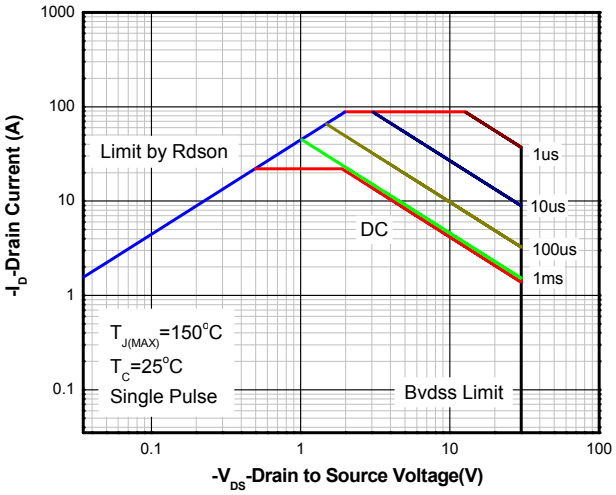
Capacitance



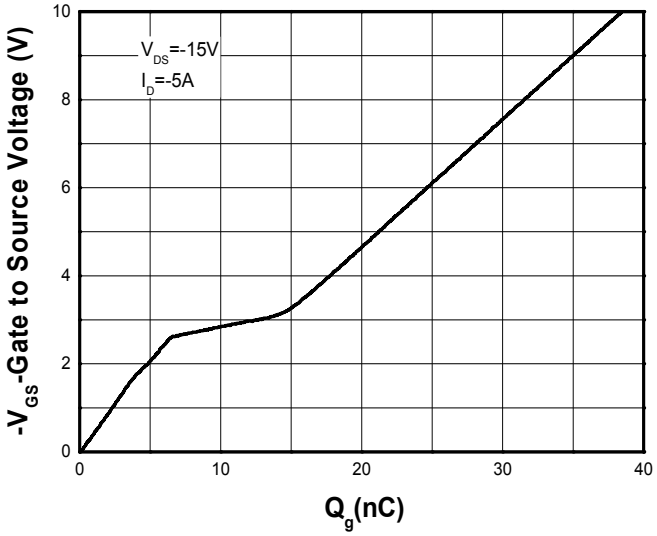
Body Diode Forward Voltage [e]



Single Pulse power

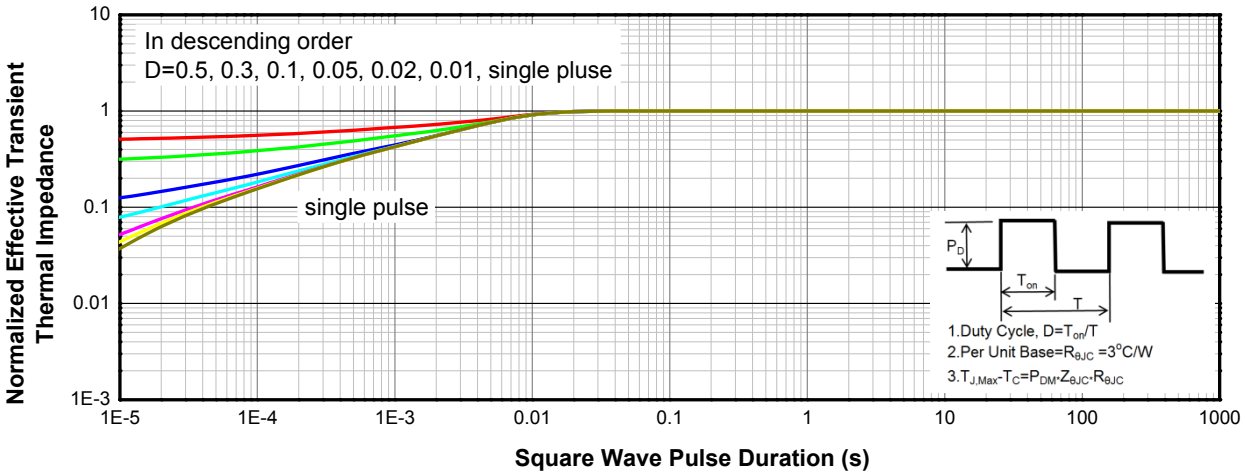


Safe Operating Power

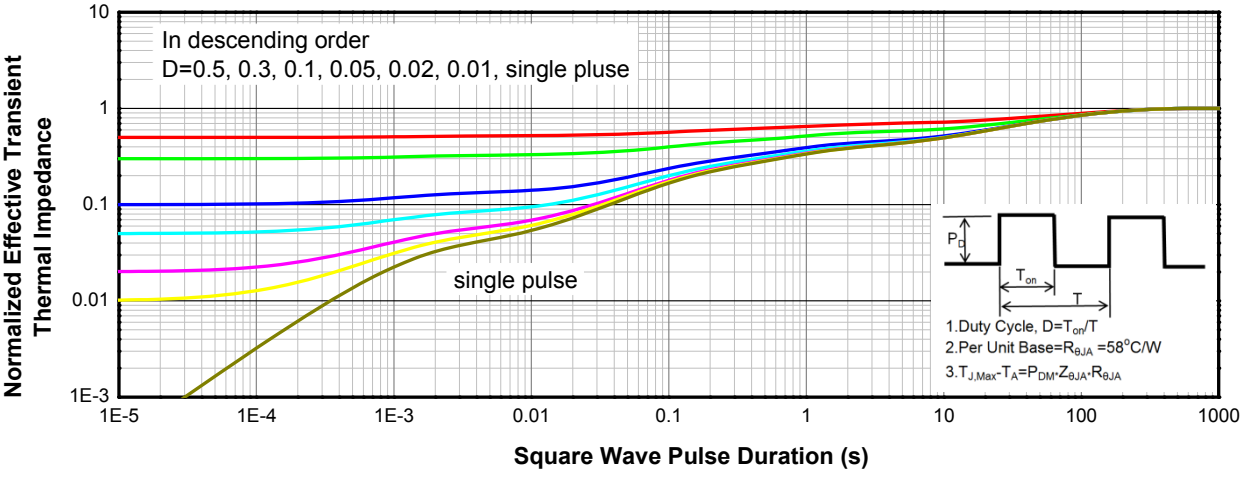


Gate Charge Characteristics

Transient Thermal Response (Junction-to-Case)

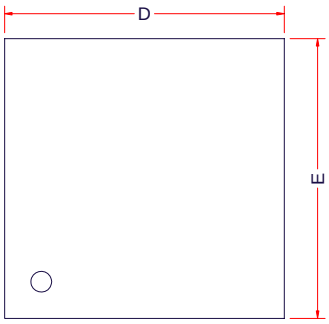


Transient Thermal Response (Junction-to-Ambient)

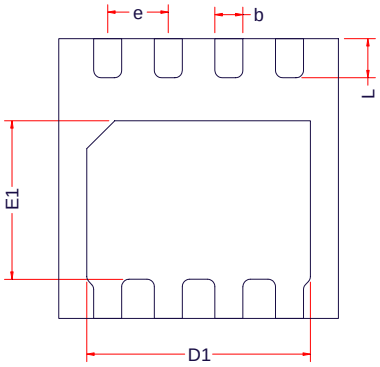


PACKAGE OUTLINE DIMENSIONS

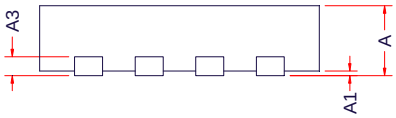
DFN3x3-8L



TOP VIEW



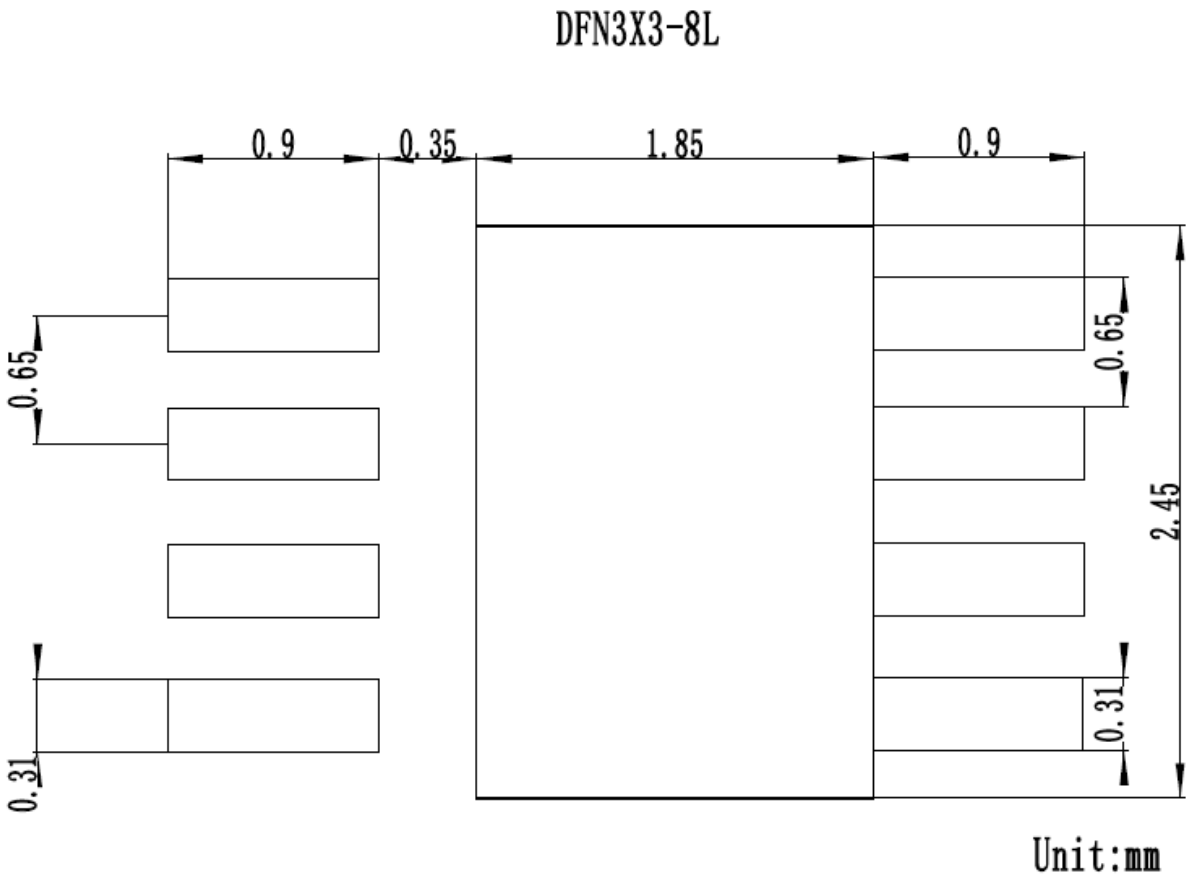
BOTTOM VIEW



SIDE VIEW

Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2		0.20Ref	
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D1	2.35	2.40	2.45
E1	1.65	1.70	1.75
b	0.25	0.30	0.35
e		0.65BSC	
L	0.37	0.42	0.47

RECOMMENDED LAND PATTERN (Unit: mm)

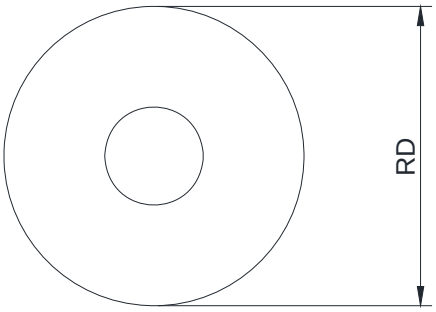


Notes:

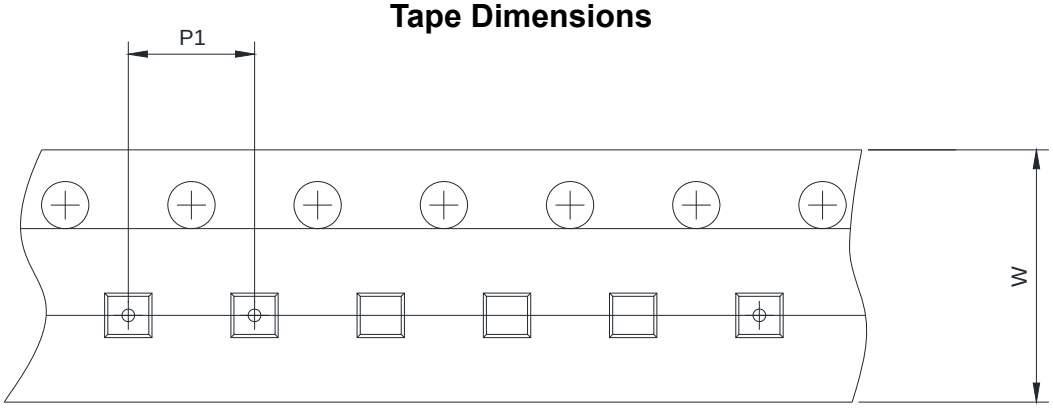
This recommended land pattern is for reference purposes only. Please consult your manufacturing group to ensure your PCB design guidelines are met.

TAPE AND REEL INFORMATION

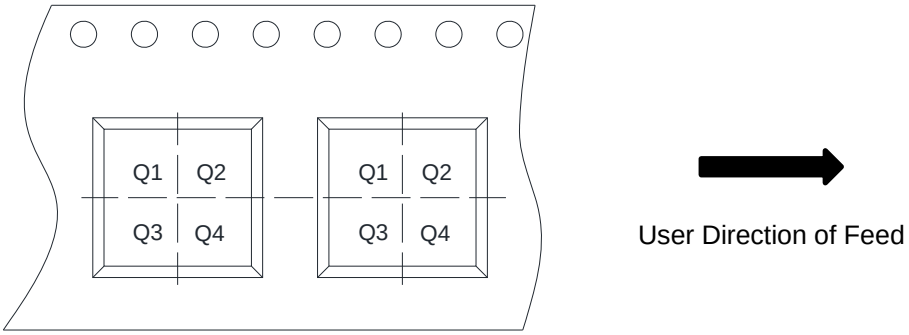
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimension	☐ 7inch ☑ 13inch
W	Overall width of the carrier tape	☐ 8mm ☑ 12mm ☐ 16mm
P1	Pitch between successive cavity centers	☐ 2mm ☐ 4mm ☑ 8mm
Pin1	Pin1 Quadrant	☑ Q1 ☐ Q2 ☐ Q3 ☐ Q4