General description

The MX1025D is a single channel low-side enhancement-mode GaN FET and logic-level MOSFET driver for high switching frequency applications. Narrow pulse width capability, fast switching specification, and small pulse distortion combine to significantly enhance LiDAR, ToF, and Power Converter performance. 1.25ns output pulse width enables more powerful, eye-safe diode pulses. This, combined with 300ns distortion, leads to longer-range, precise LiDAR/ToF systems. 2.9ns propagation delay significantly improves the control loop response time and thus overall performance of the power converters. Split output allows the drive strength and timing to be independently adjusted through external resistors between OUTH, OUTL, and the FET gate.

The driver features undervoltage lockout (UVLO) and over-temperature protection (OTP) to ensure the device is not damaged in overload or fault conditions.

Features

- ♦ 1.25ns typical minimum input pulse width
- ♦ 2.5ns typical rising propagation delay
- ♦ 2.7ns typical falling propagation delay
- ♦ 300ps typical pulse distortion
- ♦ Independent 7A pull-up and 5A pull-down current
- ♦ 950ps typical rise time 100pF load)
- ♦ 1150ps typical fall time (100pF load)
- ♦ 2mm×2mm DFN package
- ♦ Inverting and non-inverting inputs
- ♦ UVLO and over-temperature protection
- ♦ Single 5V supply voltage

Applications

- ♦ LiDAR
- ♦ Driver Monitoring
- ♦ Vehicle Occupant Detection Sensor
- ♦ DC/DC Converters

General information

Ordering information

Part Number	Description
MX1025D	DFN2*2-6L
MPQ	3000pcs

Package dissipation rating

Package	RθJA（℃/W）
DFN2*2-6L	83

Absolute maximum ratings

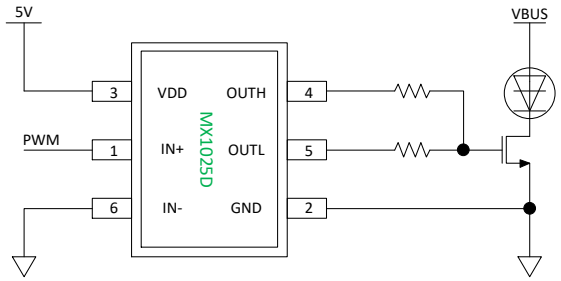
Parameter	Value
VDD Pin to GND	0 to 5.75V
IN+, IN- Pins to GND	-0.3 to VDD + 0.3V
OUTH, OUTL Pins to GND	-0.3 to 5.75V
Junction temperature	150℃
Storage temperature, Tstg	-50 to 150℃
Leading temperature （soldering,10secs）	260℃
ESD Susceptibility HBM	±2000V

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

Recommended operating condition

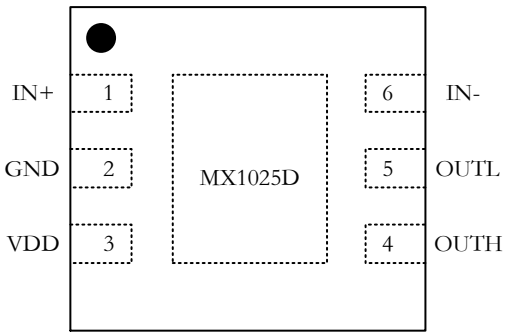
Symbol	Range
VDD Pin	4.75~5.25V
IN+, IN- Pins	0~VDD
OUTH, OUTL Pins	0~5.25V
Operating temperature	-40~125℃

TYPICAL APPLICATION



Typical Application

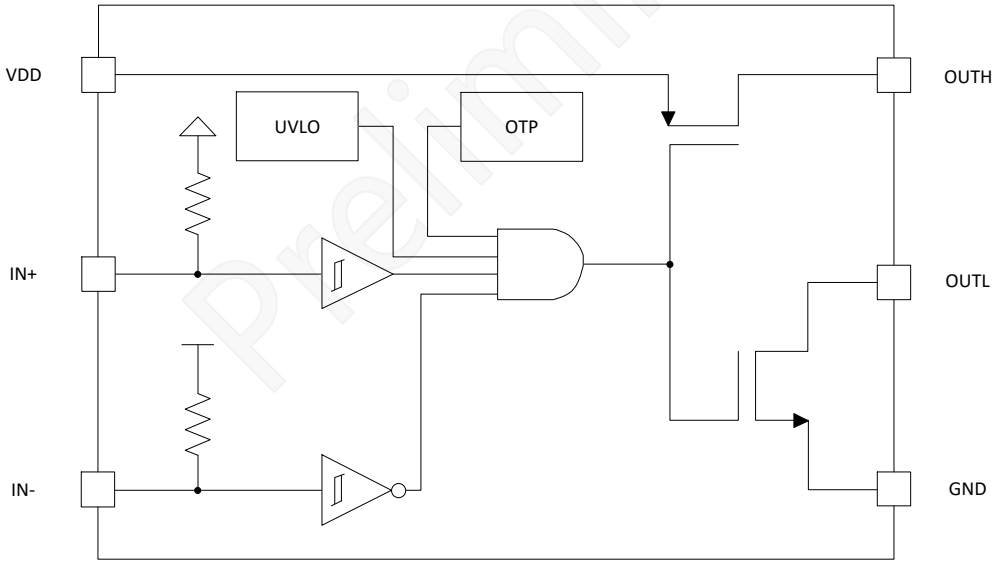
TERMINAL ASSIGNMENTS



Pin information

PIN NO.	PIN name	Description
1	**IN+**	Positive logic-level input.
2	**GND**	Power supply and source return. Connect with a direct path to the transistor's source.
3	**VDD**	Input voltage supply. Decouple through a compact capacitor to GND.
4	**OUTH**	Pull-up gate drive output. Connect through a resistor to the target transistor's gate.
5	**OUTL**	Pull-down gate drive output. Connect through an optional resistor to the target transistor's gate.
6	**IN–**	Negative logic-level input.
	Thermal Pad	Internally connected to GND through substrate. Connect this pad to large copper area, generally a ground plane.

BLOCK DIAGRAM



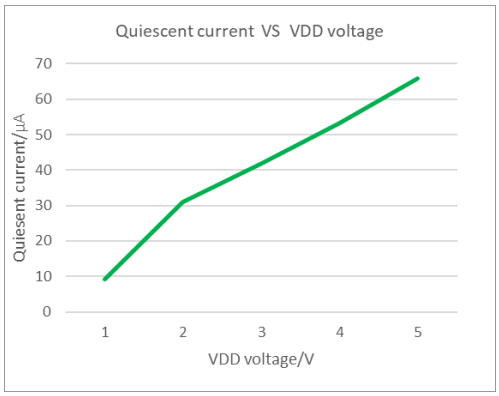
Electrical characteristics

（V_{DD} = 5V, TA = 25℃, unless otherwise noted）

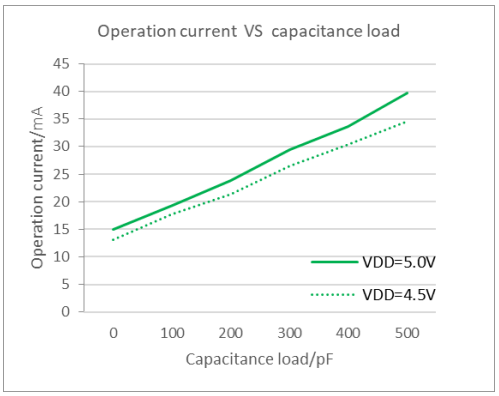
Symbol	Parameter	Test condition	Min	Typ.	Max	Unit
VDD PIN						
I_Q	VDD Quiescent Current	IN+ = IN- = 0V			75	uA
I_{VDD}	Operating Supply Current	f_{sw} = 100kHz, no load, 2Ω as R_{OUTH} and R_{OUTL}		0.25		mA
		f_{sw} = 10MHz, 100pF load, 2Ω as R_{OUTH} and R_{OUTL}		18		
UVLO	Under-voltage Lockout	VDD rising	4.0		4.35	V
$UVLO_{HYST}$	UVLO Hysteresis			90		mV
IN PINS						
V_{IH}	IN+, IN- high threshold		1.9		2.5	V
V_{IL}	IN+, IN- low threshold		1.1		1.8	V
V_{HYST}	IN+, IN- hysteresis		0.38		1	V
R_{IN+}	Positive input pull-down resistance	to GND	100	150	250	kΩ
R_{IN-}	Negative input pull-up resistance	to VDD	100	150	250	kΩ
C_{IN+}	Positive input pin capacitance	to GND		1.45		pF
C_{IN-}	Negative input pin capacitance	to GND		1.45		pF
OUT PINS						
V_{OL}	OUTL voltage	I_{OUTL} = 100mA, IN+ = IN- = 0V			30	mV
VDD - V_{OH}	OUTH voltage	I_{OUTH} = 100mA, IN+ = 5V, IN- = 0V, VDD = 5V			50	mV
I_{OH}	Peak source current	V_{OUTH} = 0V, IN+ = 5V, IN- = 0V, VDD = 5V		7		A
I_{OL}	Peak sink current	VOUTL = 5V, IN+ = IN- = 0V, VDD = 5V		5		A
OTP						
T_{OTP}	Over temperature shutdown, turn-off threshold			170		℃
ΔT_{OTP}	Over temperature hysteresis			20		℃
Symbol	Parameter	Test condition	Min	Typ.	Max	Unit
Switching Characteristics						
t_{start}	Startup time, VDD rising above UVLO	IN- = GND, IN+ = VDD, VDD rising above		40	78	μs
$t_{shut-off}$	ULVO falling	4.4V to OUTH rising	0.7	2.5	3.5	μs
t_{pdr}	Propagation delay, turn on	IN- = GND, IN+ = VDD, VDD falling	1.5	2.6	4.1	ns
t_{pdf}	Propagation delay, turn off	below 3.9V to OUTH falling	1.8	2.9	4.4	ns
Δt_{pd}	Pulse positive distortion, (t_{pdf} - t_{pdr})		0	300	610	ps
t_{rise}	Output rise time	0Ω series 220pF load		1.2		ns
t_{fall}	Output fall time	0Ω series 220pF load		1.1		ns
t_{min}	Minimum input pulse width that changes output state	0Ω series 220pF load		1.5		ns

Characteristic plots

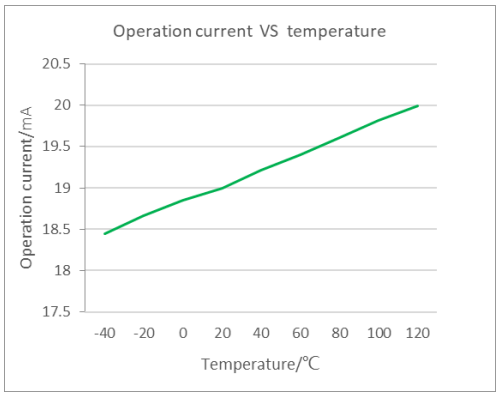
（VDD = 5V, TA = 25℃, unless otherwise noted）



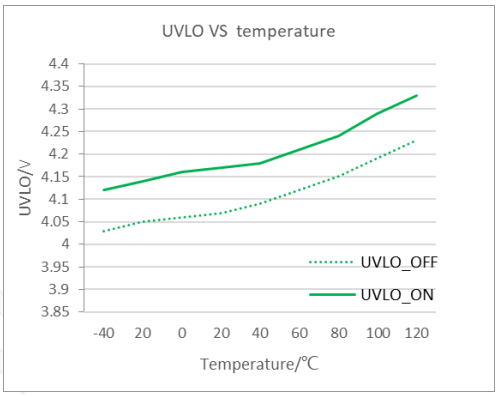
Quiescent current



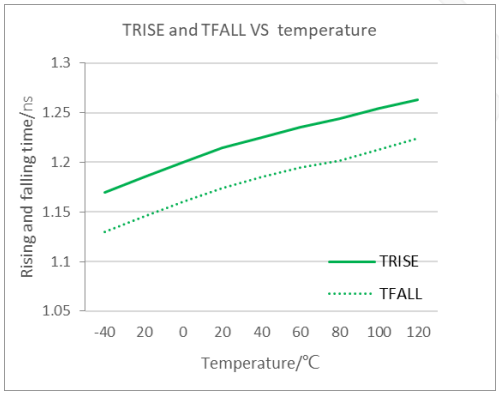
Operation current with different capacitance load



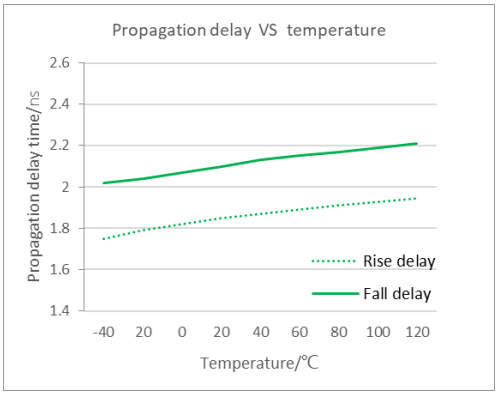
Operation current with 100pF load



Under voltage



Rising and falling time with 100pF load



Propagation delay time

Operation description

MX1025D is a high-performance low-side 5V gate driver for GaN and logic-level MOSFETs. While it is designed to function well in high-speed applications, such as wireless power transmission and LiDAR/ToF and quick charger in small volume, it can be used in any application where a low-side gate driver is required. The MX1025D is optimized to provide the lowest propagation delay through the driver to the power transistor. MX1025D is in a small 2mm×2mm DFN package with wettable flanks, to minimize its parasitic inductance. This low inductance design is necessary to achieve high current, low ringing performance in very high frequency operation when driving power FETs. The same holds true for when designing with MX1025D. DFN package with wettable flanks is also needed to improve system robustness in many applications.

Input Stage

The input stage features two Schmitt-triggers at the pins IN+ and IN– to reduce sensitivity to noise on the inputs. IN+ signal and the inverted IN– signal are both sent to an AND gate. IN+ relates to a pull-down resistor while IN– is connected with a pull-up resistor to prevent unintended turn-on. The output of the driver will be high when input voltage goes above input thresholds and output goes low when input voltage is below input threshold mentioned in the electrical characteristics table. Both IN+ and IN– are single ended inputs, and these two pins cannot be used as a differential input pair. Parasitic elements become extremely important in high frequency designs and extreme care should be taken while laying out the printed circuit board to minimize these parasitic elements. The performance of MX1025D and the performance of the overall system gets affected by the layout and components being selected.

Output Stage

MX1025D provides 7A source, 5A sink (asymmetrical drive) peak-drive current capability and features a split output configuration. The OUTH and OUTL outputs of MX1025D allow the user to use independent resistors connecting to the gate. The two resistors allow the user to independently adjust the turn-on and turn-off drive strengths to control slew rate and EMI, and to control ringing on the gate signal. For GaN FETs, controlling ringing is important to reduce stress on the GaN FET and driver. The output stage OUTL is also pulled down in undervoltage condition, which prevents the unintended charge accumulation of device Ciss, and thus preventing false turn-on. This ringing heavily depends on the layout as switching frequency increases and as rise and fall time gets shorter. The distance between the gate driver and power device needs to be as minimum as possible. Gate loop should be as minimum as possible. If ringing is un-avoidable, then the gate resistor should be selected in such a way that the ringing is minimized. Bypass capacitor type, value, and position also significantly affects this ringing.

Bias Supply and Under Voltage Lockout

MX1025D features nominal 5V and maximum 5.25V of supply voltage, and its absolute maximum supply voltage is 5.75V. In the design, it is recommended to limit the variability of the power supply to be within 5% (0.25V), and the overshoot voltage during switching transient not to exceed the absolute maximum voltage. MX1025D also features internal undervoltage lockout (UVLO) to protect the driver and circuit in case of fault conditions. The UVLO point is setup between 4.0V and 4.35V with a hysteresis of 90mV. This UVLO level is specifically designed to guarantee that GaN power devices can be switched at a low $R_{DS(ON)}$ region. During UVLO condition, the OUTL pin is pulled down to ground.

Overtemperature Protection (OTP)

MX1025D features overtemperature protection (OTP) function by having a rising edge trigger point at around 170°C of junction temperature. With a hysteresis of 20°C, the device can restart to operate when junction temperature is below 150°C.

Device Functional Modes

The device will operate in following mode when not in UVLO state.

IN-	IN+	OUTH	OUTL
L	L	Open	L
L	H	H	Open
H	L	Open	L
H	H	Open	L

Application and Implementation

Application Information

To operate GaN FET or MOSFET at very high switching frequencies and to reduce associated switching losses, a powerful gate driver is employed between the PWM output of controller and the gate of the GaN transistor. Also, gate drivers are indispensable when the outputs of the PWM controller do

not meet the voltage or current levels needed to directly drive the gates of the switching devices. With the advent of digital power, this situation is often encountered because the PWM signal from the digital controller is often a 3.3V logic signal, which cannot effectively turn on a power switch. A level-shift circuit is needed to boost the 3.3V signal to the gate-drive voltage (such as 5V) to fully turn on the power device and minimize conduction losses.

Gate drivers effectively provide the buffer-drive functions. Gate drivers also address other needs such as minimizing the effect of high-frequency switching noise (by placing the high-current driver MX1025D physically close to the power switch), reducing power dissipation and thermal stress in controllers by moving gate charge power losses from the controller into the driver.

The MX1025D is a high frequency low-side gate driver for enhancement mode GaN FETs and Si FETs in a single ended configuration. The split-gate outputs with strong source and sink capability provides flexibility to adjust the turn-on and turn-off strength independently. As a low side driver, MX1025D can be used in a variety of applications, including different power converters, LiDAR, time-of-flight (ToF) laser drivers, class-E wireless chargers, synchronous rectifiers, and augmented reality devices. MX1025D can also be used as a high frequency low current laser diode driver, or as a signal buffer with very fast rise/fall time.

Typical Application

The MX1025D is designed to be used with a single low-side, ground-referenced GaN or logic-level FET. Independent gate drive resistors, R1 and R2, are used to independently control the turn-on and turnoff drive strengths, respectively. For fast and strong turnoff, R2 can be shorted and OUTL directly connected to the transistor's gate. For symmetric drive strengths, it is acceptable to short OUTH and OUTL and use a single gate-drive resistor. The care should be taken that the ringing on the gate of the power device or ringing on any of the gate driver pin does not exceed the recommended rating. Resistors play an important role in damping these ringing. The layout and type of gate resistor with respect to gate driver and power device is also very important.

It is strongly recommended to use at least a 2Ω resistor at each OUTH and OUTL to avoid voltage overstress due to inductive ringing. Ringing must be ensured to be below VDD + 0.3V.

Design Requirements

When designing a multi-MHz (or nano-second pulse) application that incorporates MX1025D gate driver and GaN power FETs, some design considerations must be evaluated first to make the most appropriate selection. Among these considerations are layout optimization, circuit voltages, passive components, operating frequency, and controller selection.

Detailed Design Procedure

Handling Ground Bounce

For the best switching performance and gate loop with lowest parasitic, it is recommended to connect the ground return pin of MX1025D as close as possible to the source of the low-side FET in a low inductance manner. However, doing so can cause the ground of MX1025D to bounce relative to the system or controller ground and lead to erroneous switching logic on the input so as mis-turn on/off on the output.

First, MX1025D has input hysteresis built into the input buffers to help counteract this effect. The maximum di/dt allowed to prevent the input voltage transient from exceeding the input hysteresis is given by the following Equation:

$$\frac{di_S}{dt} = \frac{V_{HYST}}{L_{RS}}$$

where

L_{RS} is the inductance of the sense resistor,

V_{HYST} is the hysteresis of the input pin,

di_s/dt is the maximum allowed current slew rate.

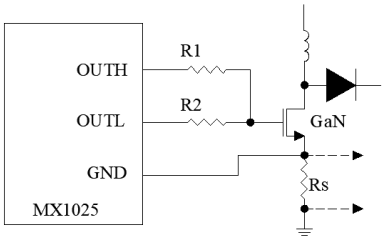
For an assumed shunt resistor parasitic inductance of 0.5nH and a minimum hysteresis of 0.5V, the maximum slew rate is 1A/ns. Many applications would exhibit higher current slew rates, up to the 10A/ns range, which would make this approach impractical. The stability of this approach can be improved by using the IN– input for the PWM signal and locally tying IN+ to VDD. By using the inverting input, the transient voltage applied to the input pin reinforces the PWM signal in a positive feedback loop. While this approach would reduce the probability of false pulses or oscillation, the transient spikes due to high di/dt may overly stress the inputs to MX1025D. A current-limiting, 100Ω resistor can be placed right before the IN– input to limit excessive current spikes in the device.

Secondly, for moderate ground-bounce cases, a simple RC filter can be built with a simple resistor in series with the inputs. By utilizing the input capacitance of MX1025D, the resistor could be close to its input pin. The addition of a small capacitor on the input as supplement can also be helpful. A small time

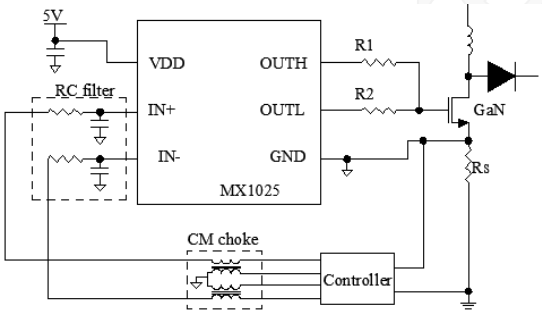
constant of the RC filter may be enough to filter out high frequency noise. This solution is acceptable for moderate cases in applications where extra delay is acceptable and the pulse width is not extremely short such as in 1ns range.

For more extreme cases, or where no delay is tolerable while pulse width is extremely short, using a common mode choke provides the best results.

One example application where ground-bounce is particularly challenging is when using a current sense resistor. In the following figure MX1025D ground is connected to the source of GaN FET, while the controller ground is connected to the other side of the current sense resistor. Due to the fast switching and very fast current slew rates, the high ground potential bounce induced by inductance of the sense resistor can disrupt the operation of the circuit or even damage the part.

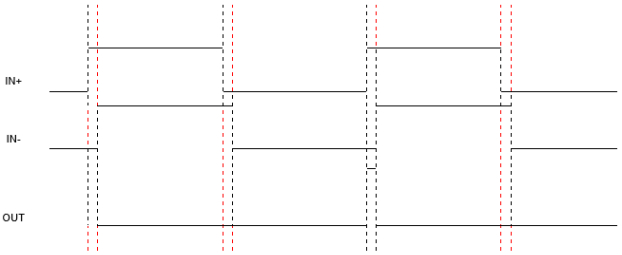


To prevent this, a common-mode choke can be used for IN+ and IN–, respectively. Resistors can also add to the signal output line before MX1025D depending on the input signal pulse width to provide additional RC filtering as shown in the following figure.



Creating Nanosecond Pulse

MX1025D can be used to drive pulses of nano seconds duration on to a capacitive load. MX1025D can be driven with a equivalently short pulse on one input pin. However, this takes a sufficiently strong digital driver and careful consideration of the routing parasitics from digital output to input of MX1025D. Two inputs and included AND gate in MX1025D provide an alternate method to create a short pulse at MX1025D output. Starting with both IN+ and IN– at low, taking IN+ high will cause the output to go high. Now if IN– is taken high as well, output will be pulled low. So a digital signal and its delayed version can be applied to IN+ and IN– respectively to create a pulse at the output with width corresponding to the delay between the signals, as shown in Figure 10. The delay can be digitally controlled in the nanosecond range. This method alleviates the requirements for driving the input of MX1025D. If a separate delayed version of the digital signal is not available, an RC delay followed by a buffer can be used to derive the second signal. Optionally, if MX1025D must be driven with a single short duration pulse, that pulse can itself be generated using another MX1025D by the above method to meet drive requirements.



VDD and Overshoot

Fast switching with high current is prone to ringing with parasitic inductances, including those on PCB traces. Overshoot associated with such ringing transients need to be evaluated and controlled as a part of the PCB design process to limit device stress. The parameters affecting stress are how high the overshoot is above the absolute maximum specification and the ratio of overshoot duration to the switching time period. Recommended design practice is to limit the overshoots to the absolute maximum pin voltages. This is accomplished with carful PCB layout to minimize parasitic inductances, choice of components with low ESL and addition of series resistance to limit rise times. For large overshoots, limiting the variability of the power supply may be required. For example, 0.5V of overshoot will be permissible with a maximum recommended supply of 5.25V (5% variability); however, for larger overshoots, a supply with lower variability will be preferred.

Operating at Higher Frequency

With fast rise/fall time, and capability of achieving nano-second pulse width, depending on the capacitive load condition, the operating frequency of MX1025D can be increased in a burst manner. In conditions which requires very high frequency pulsing, a pulse train with certain period of

pause between each burst can be adopted to avoid overheat of the device. This will help maintain the RMS output current similar as lower frequency operation but boost the transient frequency to very high. In addition, higher decoupling capacitance will be needed to supply high frequency charging of the capacitive load.

Power Supply Recommendations

A low ESR/ESL ceramic capacitor must be connected close to MX1025D, between VDD and GND pins to support the high peak current being drawn from VDD during turn-on of the FETs. It is most desirable to place the VDD decoupling capacitor on the same side of the PC board as the driver. The inductance of via holes can impose excessive ringing on MX1025D pins.

Maxin micro recommends the use of a three-terminal capacitor connecting in shunt-through manner to achieve the lowest ESL and best transient performance. This capacitor can be placed as close as possible to MX1025D, while another capacitor in larger capacitance can be placed closely to the three-terminal cap to supply enough charge but with slightly lower bandwidth. As a general practice, the combination of a 0.1μF of 0402 or feed-through capacitor (closest to MX1025D) and a 1μF 0603 capacitor is recommended.

Layout Guidelines

The layout of MX1025D is critical to its performance and functionality. The MX1025D is available in a 2x2 DFN, which allows a low inductance connection to a FET.

A four-layer or higher layer count board is required to reduce the parasitic inductances of the layout to achieve suitable performance. To minimize inductance and board space, resistors, and capacitors in the 0201 package should be used here. The gate drive power loss must be calculated to ensure an 0201 resistor will be able to handle the power level.

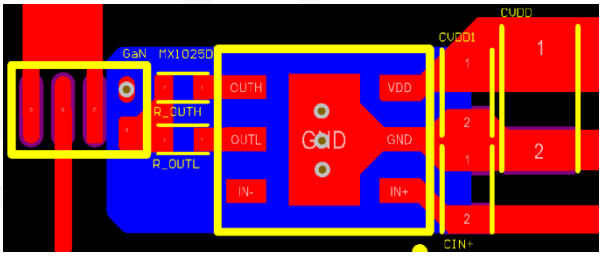
Gate Drive Loop Inductance and Ground Connection

A compact, low-inductance gate-drive loop is essential to achieving fast switching frequencies with MX1025D. The MX1025D should be placed as close to the GaN FET as possible, with gate drive resistors immediately connecting OUTH and OUTL to the FET gate. Large traces need to be used to minimize resistance and parasitic inductance.

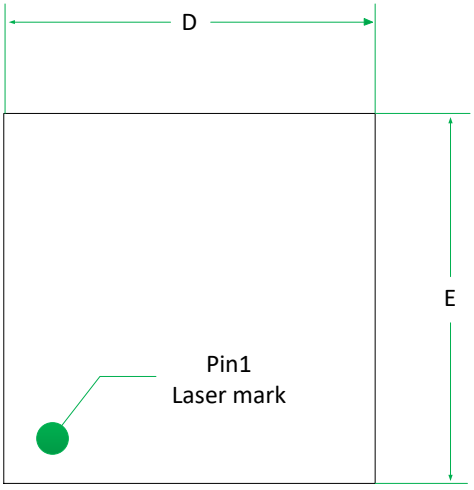
To minimize gate drive loop inductance, the source return should be on layer 2 of the PCB, immediately under the component (top) layer. Vias immediately adjacent to both the FET source and MX1025D GND pin connect to this plane with minimal impedance. Finally, care must be taken to connect the GND plane to the source power plane only at the FET to minimize common-source inductance and to reduce coupling to the ground plane.

Bypass Capacitor

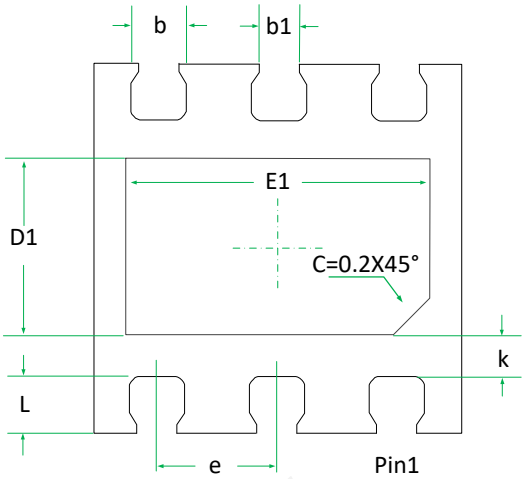
The VDD power terminal of MX1025D must by bypassed to ground immediately adjacent to MX1025D. The placement and value of the bypass capacitor is very critical because of the fast gate drive of MX1025D. The bypass capacitor must be located on the top layer, as close as possible to MX1025D, and connected to both VDD and GND using large power planes. This bypass capacitor must be at least a 0.1μF, up to 1μF, with temperature coefficient X7R or better. Recommended body types are LICC, IDC, Feed-though, and LGA. Finally, an additional 1μF capacitor should be placed as close to MX1025D as practical.



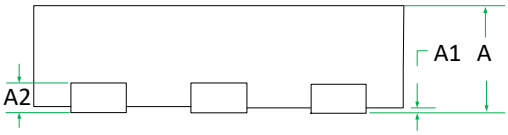
Package information



Top View



Bottom View



Side View

SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.02	0.022	0.024
A1	0	0.025	0.050	0	0.001	0.002
A2		0.152BSC			0.006BSC	
D	1.900	2.000	2.100	0.075	0.078	0.083
E	1.900	2.000	2.100	0.075	0.078	0.083
D1	0.860	0.960	1.060	0.034	0.038	0.042
E1	1.550	1.650	1.750	0.061	0.065	0.069
k		0.220BSC			0.008BSC	
b	0.250	0.300	0.350	0.010	0.012	0.014
b1		0.220BSC			0.008BSC	
e		0.650BSC			0.026BSC	
L	0.224	0.300	0.376	0.009	0.012	0.015

DFN2*2-6L for MX1025D

Restrictions on Product Use

◆ MAXIN micro is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing MAXIN products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such MAXIN products could cause loss of human life, bodily injury or damage to property.

◆ In developing your designs, please ensure that MAXIN products are used within specified operating ranges as set forth in the most recent MAXIN products specifications.

◆ The information contained herein is subject to change without notice.

Version update record:

V10 The original version （preliminary）