General Description

UCC27524 is a dual-channel, high-speed, low-side gate driver device capable of effectively driving MOSFET and IGBT power switches.

UCC27524 can deliver high peak current pulses of up to 5A source and 5A sink with extremely small propagation delay from inputs to outputs (typically 22ns). In addition, the delay matching between two channels of UCC27524 is less than 2ns and the two channels can connect in parallel with a single input signal.

The input pins are compatible with 5V and 3.3V, which offer excellent noise immunity.

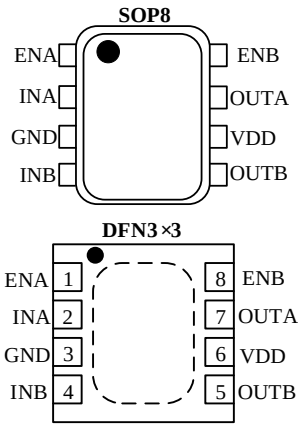
Features

- Wide Supply Voltage Range: 4.5V~30V
- Two Independent Gate Drive Channels
- 5A Peak Source and Sink Drive Current
- Fast Propagation Delays (22ns Typical)
- Fast Rise and Fall Times (7ns Typical)
- 1ns Typical Delay Matching Between Two Channels
- Two Inputs are in Parallel for Higher Driving Current
- Outputs Held Low when Inputs Floating
- DFN3×3 and SOP8 Package Options

Applications

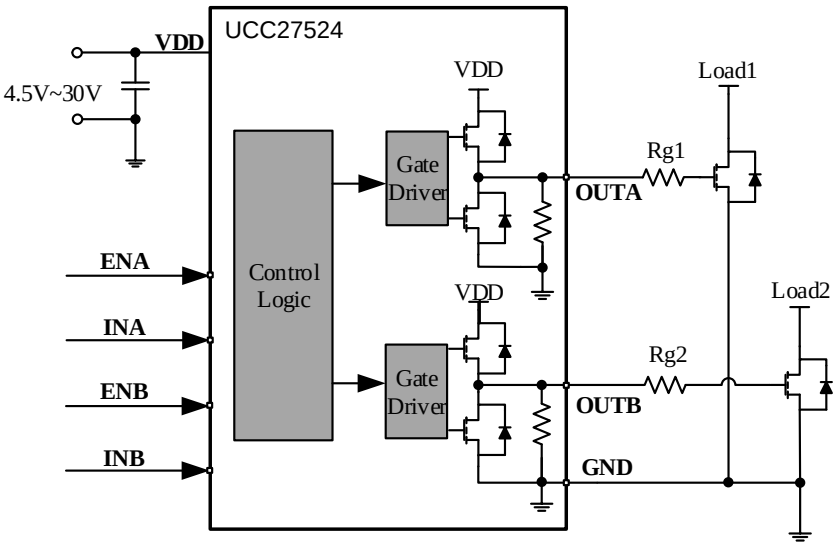
- Switched-Mode Power Supplies
- Motor Control
- Power MOSFET and IGBT Gate Driver

Package/Order Information



Order Code	Package
UCC27524DR	SOP8
UCC27523DR	SOP8
UCC27525DR	SOP8
UCC27524ADR	DFN3×3
UCC27524ADR	DFN3×3
UCC27524ADR	DFN3×3

Typical Application



Pin Definitions

Pin Name	Pin Number	Pin Function Description
ENA	1	Channel A enable signal, ENA="L", Channel A output is Low; ENA="H", see the truth table for channel A output.
INA	2	Channel A input signal, control OUTA.
GND	3	GND
INB	4	Channel B input signal, control OUTB.
OUTB	5	Channel B drive output.
VDD	6	Power Supply
OUTA	7	Channel A drive output.
ENB	8	Channel B enable signal, ENB="L", Channel B output is Low; ENB="H", see the truth table for channel B output.

Truth Table

Input				Output					
				UCC27524		UCC27523		UCC27525	
ENA	ENB	INA	INB	OUTA	OUTB	OUTA	OUTB	OUTA	OUTB
H/F	H/F	L	L	L	L	H	H	H	L
H/F	H/F	L	H	L	H	H	L	H	H
H/F	H/F	H	L	H	L	L	H	L	L
H/F	H/F	H	H	H	H	L	L	L	H
L	L	×	×	L	L	L	L	L	L
×(2)	×	F(1)	F	L	L	L	L	L	L

Note: (1) Floating state. (2) Any state.

Block Diagram

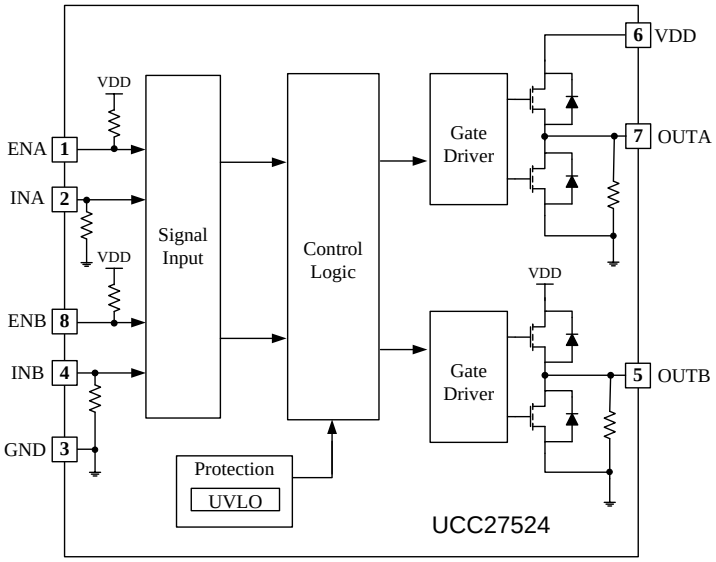


Fig. 1 UCC27524

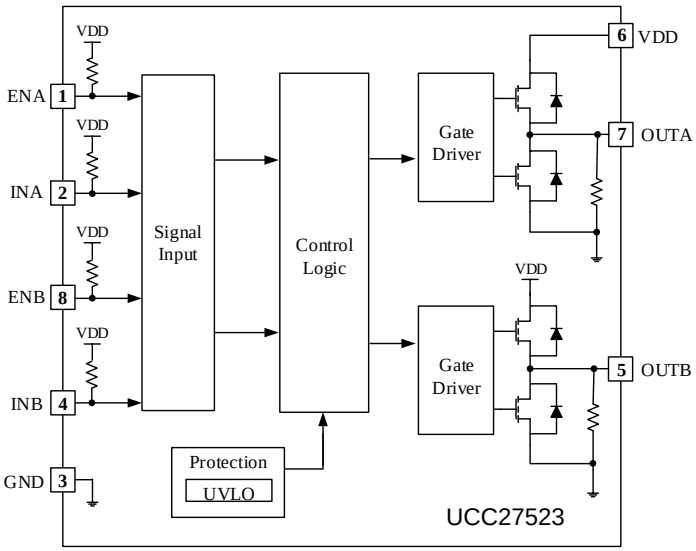


Fig. 2 UCC27523

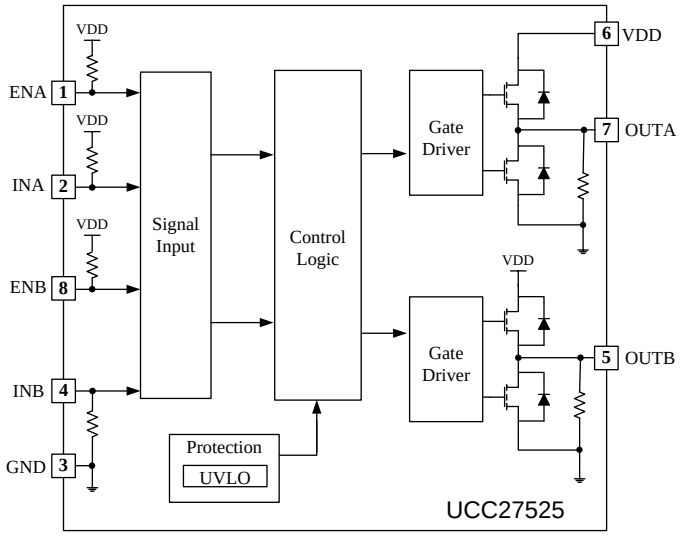


Fig. 3 UCC27525

Absolute Maximum Ratings

Supply Voltage VDD……-0.3~32V
Pin ENA, ENB, INA, INB……-0.3~32V
Pin OUTA, OUTB……-0.3~32V
Storage Temperature Range……-55~150 °C
Lead Temperature (Soldering, 10Secs)……260 °C

Package Thermal Resistance θ_{JC} (DFN3×3)……45 °C /W
Package Thermal Resistance θ_{JC} (1) (SOP8)……40 °C /W
HBM ESD Protection (2)…… ±3kV
CDM ESD Protection (3)…… ±2kV

Note：(1) Thermal resistance from chip to top surface of plastic sealant.
(2) Test standard: ESDA/JEDEC JS-001-2017.
(3) Test standard: ESDA/JEDEC JS-002-2018.

Recommended Operating Range

Supply Voltage, VDD……4.5~30V
Pin OUTA, OUTB……0~30V

Pin ENA, ENB, INA, INB……0~30V
Operating Junction Temperature……-40~150 °C

Electrical Characteristics

(T_J= 25°C, VDD=12V, C_{OUT} =1.8nF, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power Supply (VDD)						
VDD voltage	VDD_{ON}		4.1	4.5	4.9	V
VDD start-up threshold	VDD_{OFF}		3.8	4.2	4.6	V
VDD under voltage hysteresis	V_{HYS}	VDD_{ON}-VDD_{OFF}		0.3		V
VDD quiescent current	I_{VDDQ1}	VDD=12V, OUT=High	0.4	0.6	1	mA
	I_{VDDQ2}	VDD=12V, OUT=Low	0.15	0.3	0.45	mA
Input Pin（ENA, ENB, INA, INB）						
Input logic high voltage	V_{IH}		1.9	2.1	2.3	V
Input logic low voltage	V_{IL}		0.9	1.1	1.3	V
Pull down to ground resistance	R_{IPD}		80	100	130	kΩ
Pull up the power resistance	R_{IPU}		320	400	480	kΩ
Output Pin（OUTA, OUTB）						
High-side on resistance (1)	R_{ONSRC}	I_{SRC}=50mA	0.35	0.7	1.2	Ω
High-side peak current of power tube(1)	I_{SRC}	C_{LOAD}=0.22uF, F_{SW}=1kHz		5		A
Low-side on resistance (1)	R_{ONSNK}	I_{SNK}=-50mA	0.2	0.4	0.8	Ω
Low-side peak current of power tube(1)	I_{SNK}	C_{LOAD}=0.22uF, F_{SW}=1kHz		-5		A
Output pull-down resistance to ground(1)	R_{OPD}		60	80	100	kΩ
Output rise time (2)	T_r	10% to 90%VDD		6	10	ns
Output fall time (2)	T_f	90% to 10%VDD		6	10	ns
Input signal to output flip to high level transmission delay(2)	T_{PLH1}		15	22	30	ns
Input signal to output flip to low level transmission delay(2)	T_{PHL1}		15	22	30	ns
Enable signal to output flip to high level transmission delay(2)	T_{PLH2}		15	22	30	ns
Enable signal to output flip to low level transmission delay(2)	T_{PHL2}		15	22	30	ns
Dual-channel matching delay(2)	T_M			1	2	ns

Parameter Definition

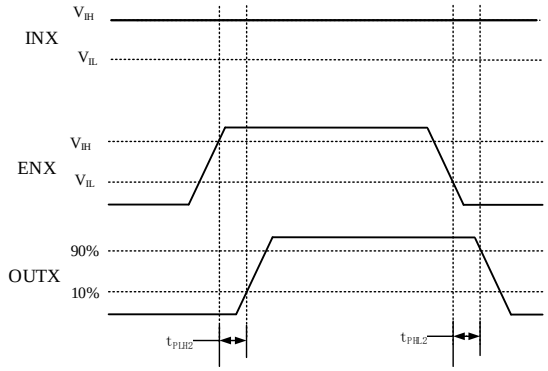


Fig. 4 Enable pin and output waveform diagram (Input and output in phase)

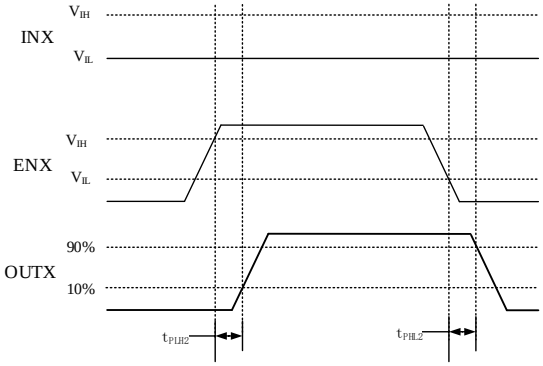


Fig. 5 Enable pin and output waveform diagram (Input and output reversed phase)

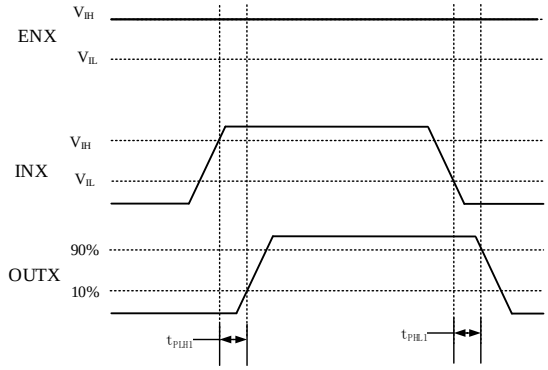


Fig. 6 Input and output waveform diagram (Input and output in phase)

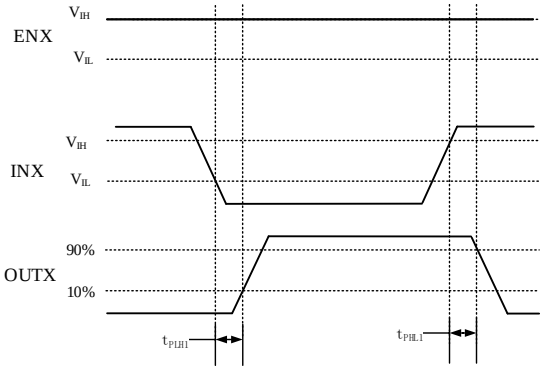


Fig. 7 Input and output waveform diagram (Input and output reversed phase)

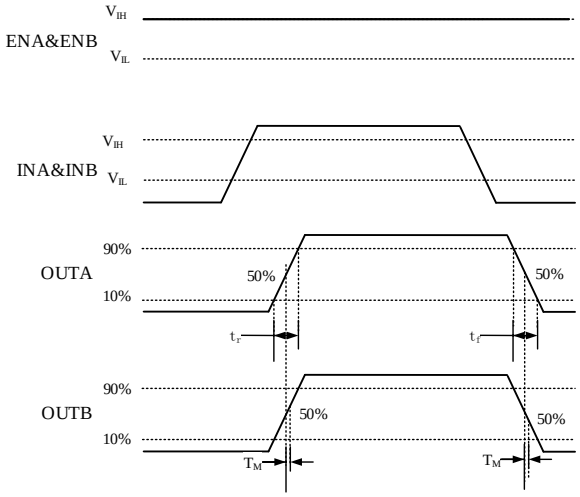
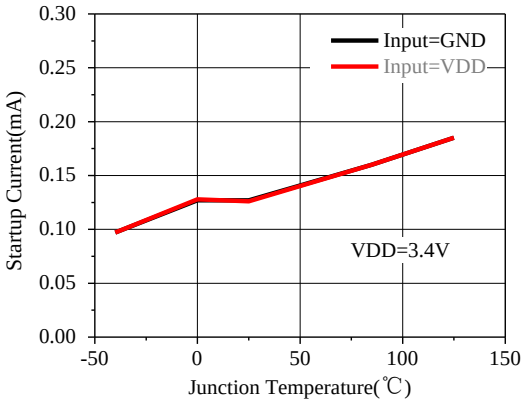
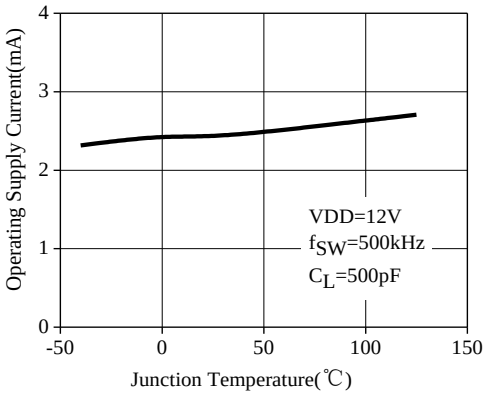


Fig. 8 Output waveform diagram (Input and output in phase)

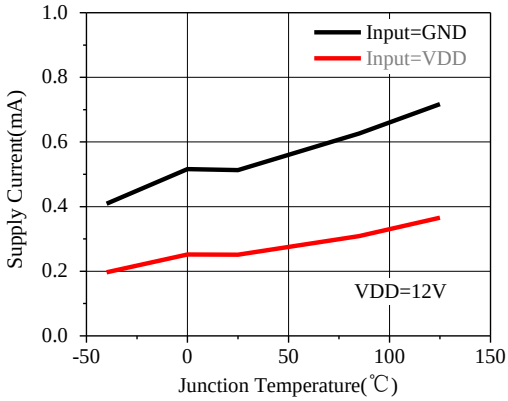
Typical Characteristics Plots



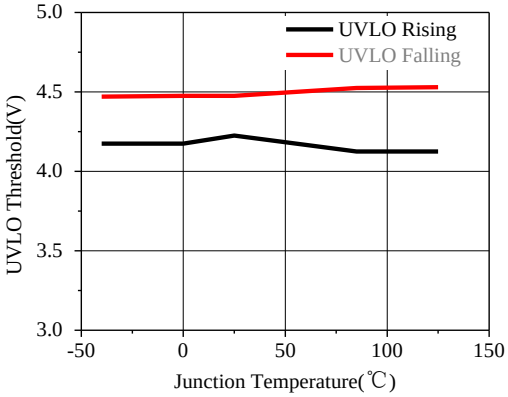
(a) Startup current VS T_J



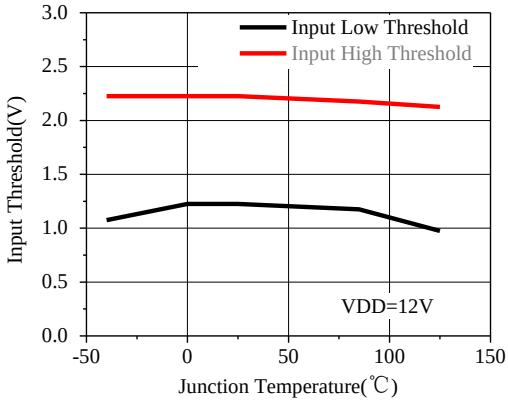
(b) Operating supply current VS T_J



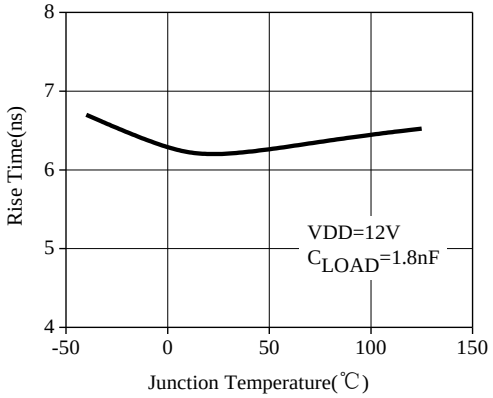
(c) Supply current VS T_J



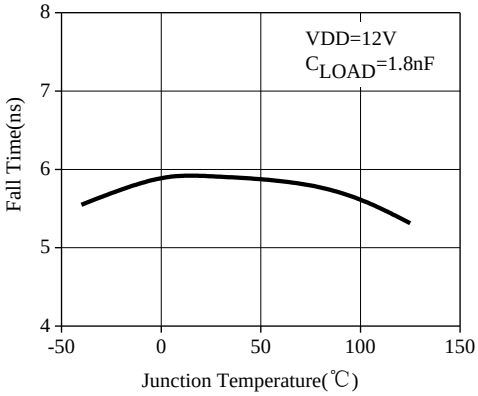
(d) UVLO threshold VS T_J



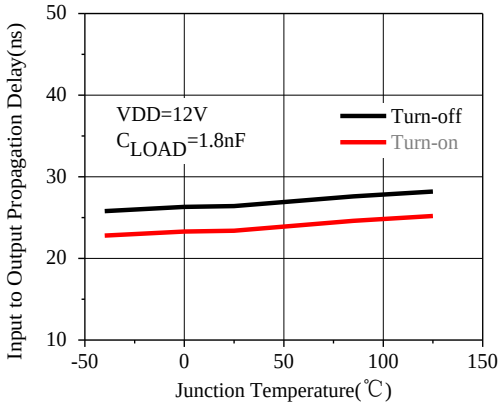
(e) Input threshold VS T_J



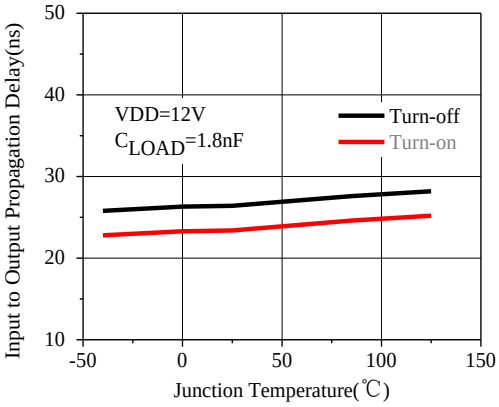
(f) Rise time VS T_J



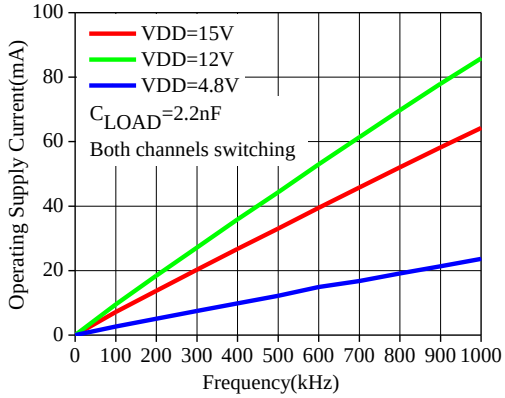
(g) Fall time VS T_J



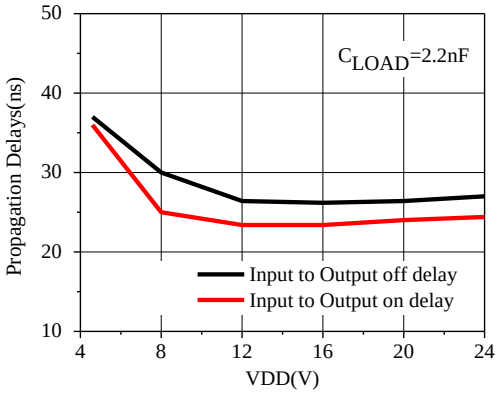
(h) Input to output propagation VS T_J



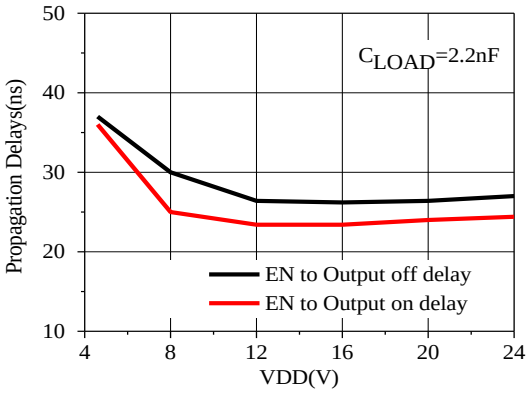
(i) EN to output propagation VS T_J



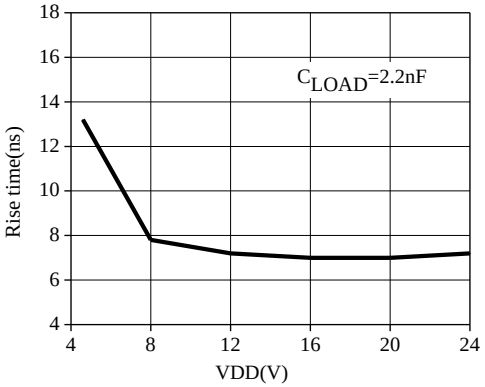
(j) Operating supply current VS Frequency



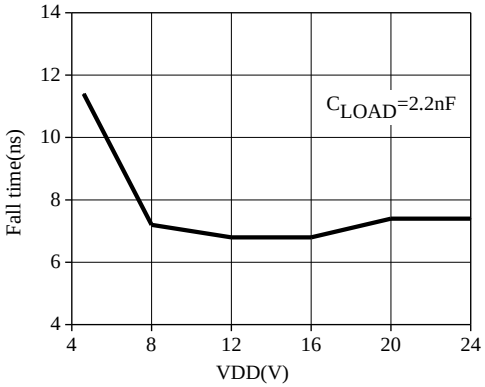
(k) Input to output propagation VS VDD



(l) EN to output propagation VS VDD



(m) Rise time VS VDD



(n) Fall time VS VDD

Test Waveform

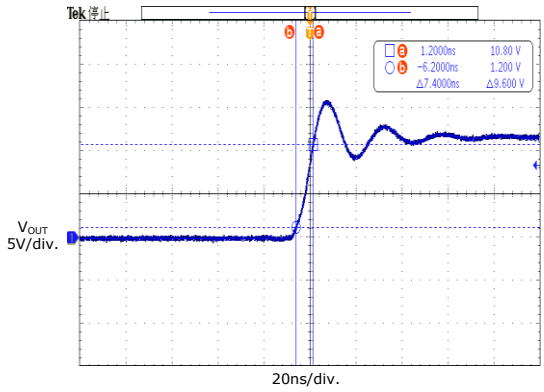


Fig. 10 Output rise time (C_L=1.8nF, VDD=12V)

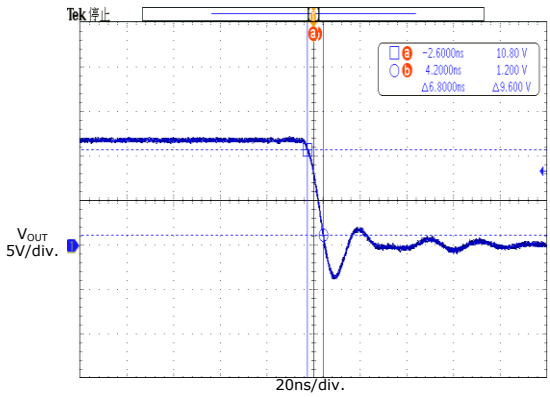


Fig. 11 Output falling time (C_L=1.8nF, VDD=12V)

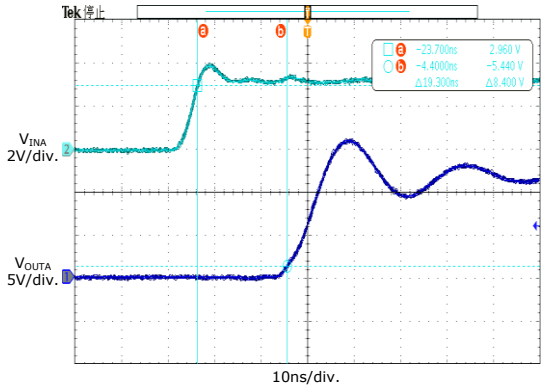


Fig. 12 Input to output flip to high propagation delay (C_L=1.8nF, VDD=12V)

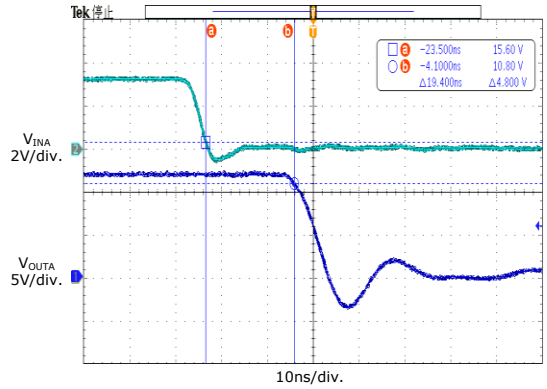
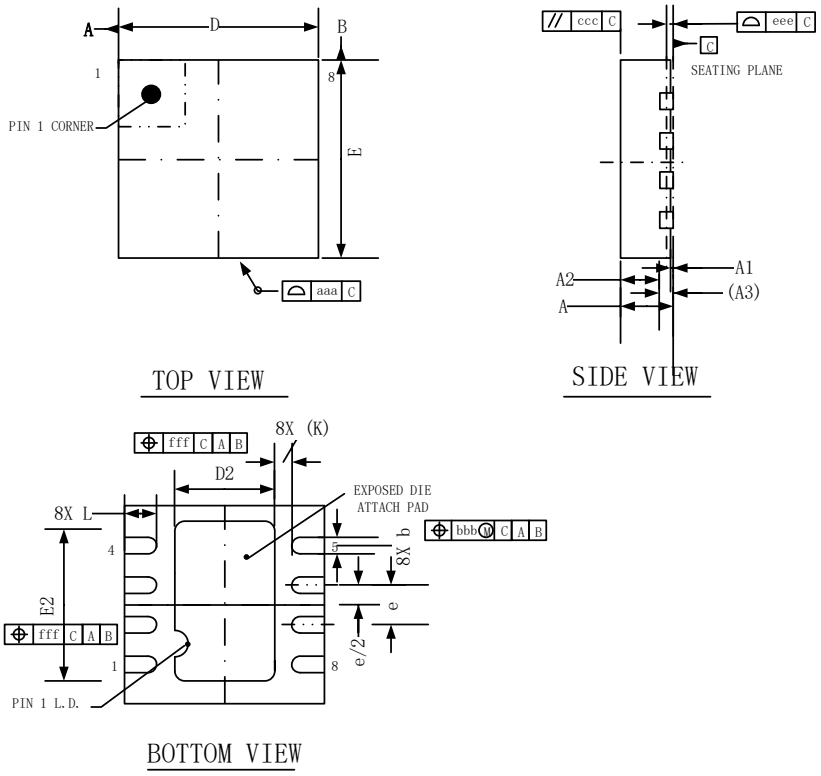


Fig. 13 Input to output flip to low propagation delay (C_L=1.8nF, VDD=12V)

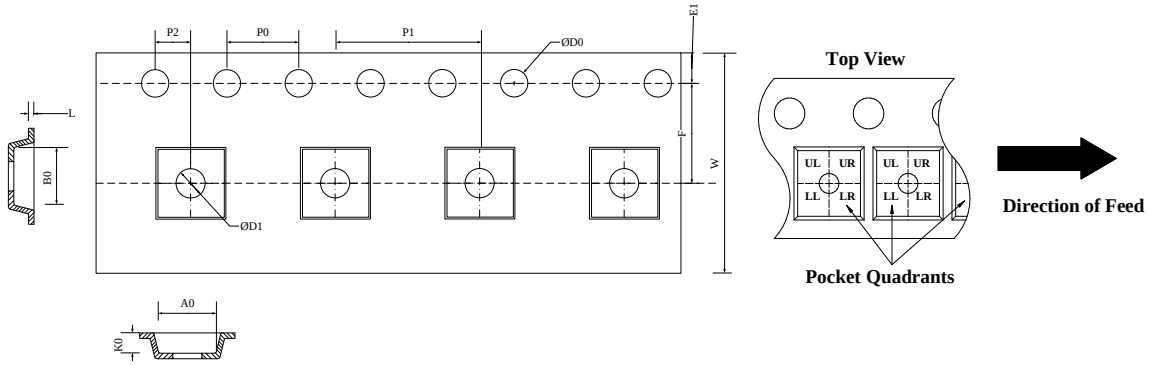
Package Information

Package Information DFN3×3



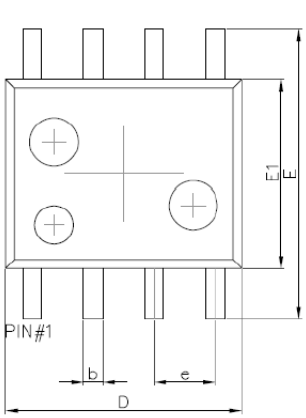
Size / Symbol	Min. (mm)	Typ. (mm)	Max. (mm)	Size / Symbol	Min. (mm)	Typ. (mm)	Max. (mm)
A	0.7	0.75	0.8	E2	2.25	2.3	2.35
A1	0	0.02	0.05	L	0.375	0.475	0.575
A2	---	0.55	---	K	0.275 REF		
A3	0.203 REF			aaa	0.05		
b	0.2	0.25	0.3	ccc	0.1		
D	3 BSC			eee	0.08		
E	3 BSC			bbb	0.1		
e	0.65 BSC			fff	0.1		
D2	1.45	1.5	1.55				

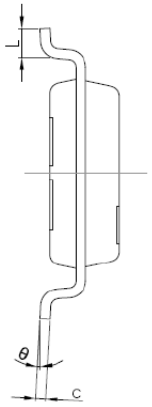
Tape and Reel Information

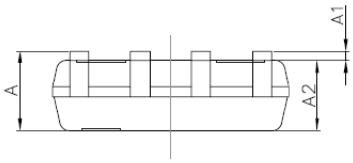


DFN3×3	
Symbol	**Size(mm)**
A0	3.2+/-0.05
B0	3.2+/-0.05
L	0.25+/-0.05
K0	1.1+/-0.05
E1	1.75+/-0.1
F	5.5+/-0.1
W	12+/-0.3
P0	4+/-0.1
P1	8+/-0.1
P2	2+/-0.05
D0	1.5+/-0.15
Pin 1 Quadrant	UL

Package Information SOP8

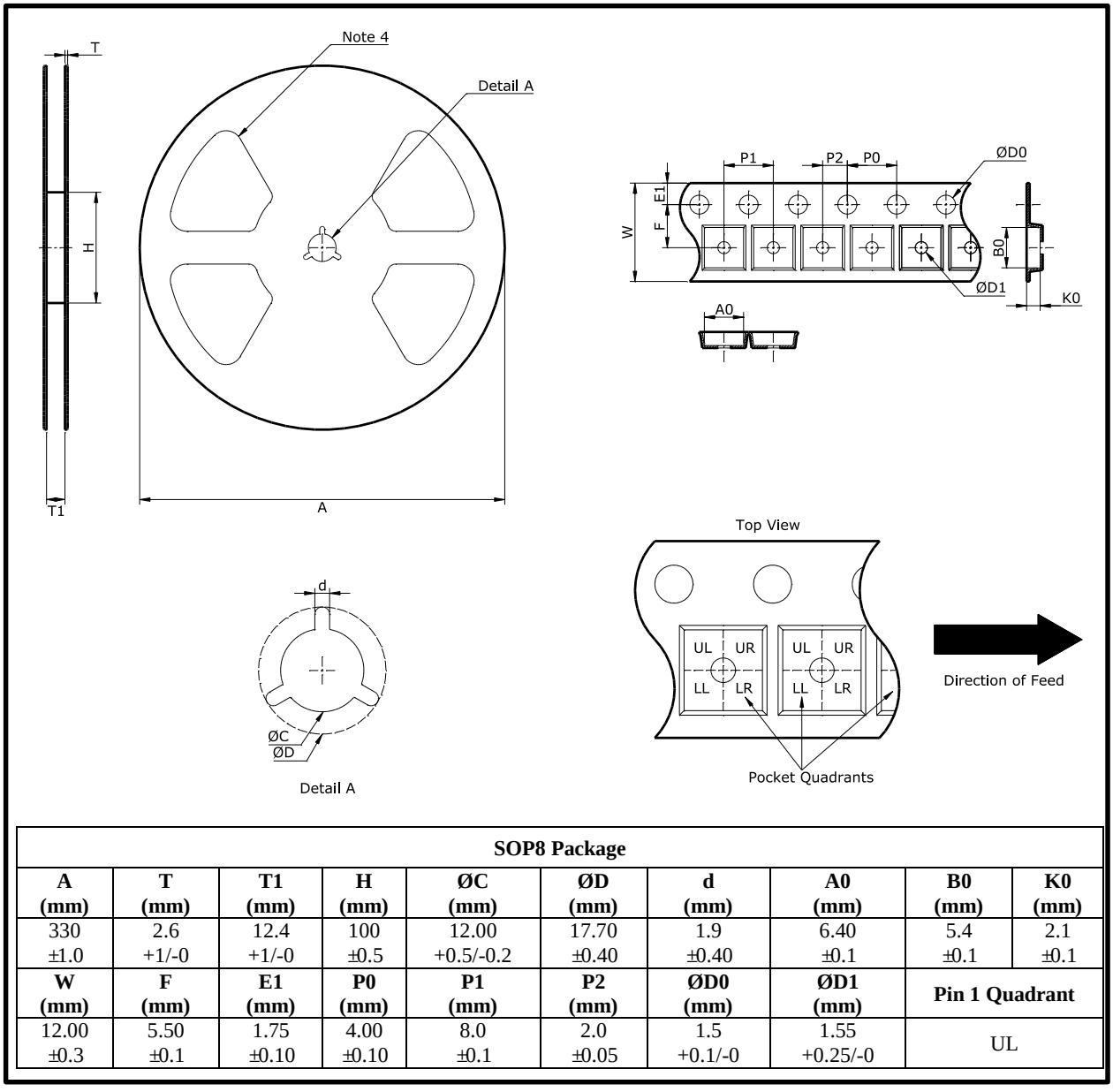






Size / Symbol	Min.（mm）	Max.（mm）
A	1.450	1.750
A1	0.100	0.250
A2	1.350	1.550
b	0.330	0.510
c	0.170	0.250
D	4.700	5.100
E	5.800	6.200
E1	3.800	4.000
e	1.270（BSC）	
L	0.400	1.270
θ	0°	8°

Tape and Reel Information



SOP8 Package									
A (mm)	**T (mm)**	**T1 (mm)**	**H (mm)**	**ØC (mm)**	**ØD (mm)**	**d (mm)**	**A0 (mm)**	**B0 (mm)**	**K0 (mm)**
330 ±1.0	2.6 +1/-0	12.4 +1/-0	100 ±0.5	12.00 +0.5/-0.2	17.70 ±0.40	1.9 ±0.40	6.40 ±0.1	5.4 ±0.1	2.1 ±0.1
W (mm)	**F (mm)**	**E1 (mm)**	**P0 (mm)**	**P1 (mm)**	**P2 (mm)**	**ØD0 (mm)**	**ØD1 (mm)**	**Pin 1 Quadrant**	
12.00 ±0.3	5.50 ±0.1	1.75 ±0.10	4.00 ±0.10	8.0 ±0.1	2.0 ±0.05	1.5 +0.1/-0	1.55 +0.25/-0	UL	