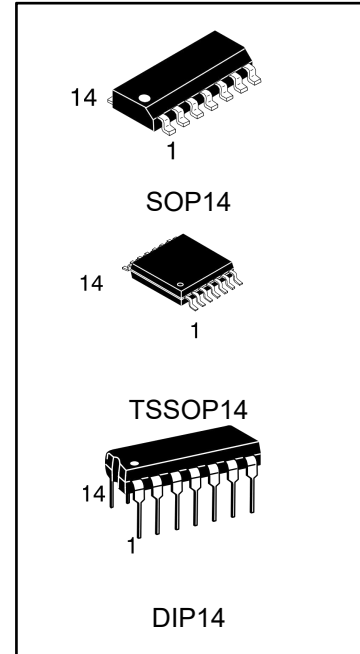


## CMOS AND Gate High-Voltage Types

### Features

CD4073B and CD4082B AND Gates provide the system ed Inner with direct implementation of the AND function and supplement the existing family of CMOS gates.

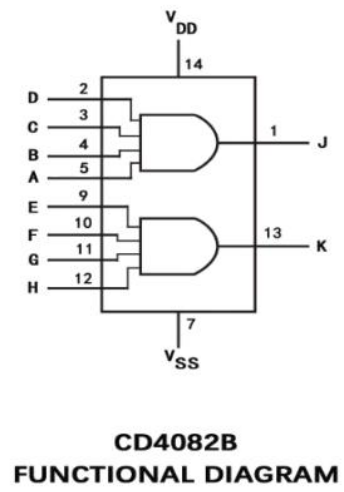
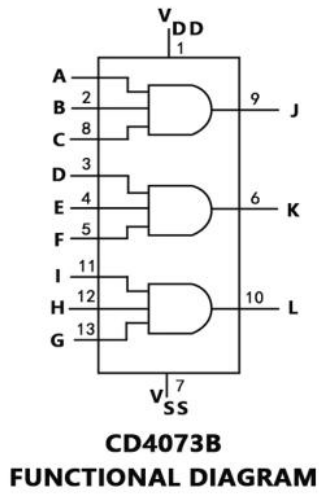
- Medium-Speed Operation - $T_{PLH}$ ,  $T_{PHL}$ =60ns (tsp.) at  $V_{DD} = 10 V$
- 100% tested for quiescent current at 20V Maximum input current of 1 $\mu$ A at 18 V over full pack-temperature range, 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range)
  - 1V at  $V_{DD}$ =5V
  - 2V at  $V_{DD}$ =10V
  - 2.5V at  $V_{DD}$ =15V
- Standardized, symmetrical ou taut characteristics
- 5V、10V and 15V parametric ratings
- Meets all requirements of JEDEC Tentative Tankard No.13B, Standard Specifications



### Ordering Information

DEVICE	Package Type	MARKING	Packing	Packing Qty
CD4073BE	DIP14	CD4073BE	TUBE	1000pcs/box
CD4073BM/TR	SOP14	CD4073B	REEL	2500pcs/reel
CD4073BMT/TR	TSSOP14	CD4073B	REEL	2500pcs/reel
CD4082BE	DIP14	CD4082BE	TUBE	1000pcs/box
CD4082BM/TR	SOP14	CD4082B	REEL	2500pcs/reel
CD4082BMT/TR	TSSOP14	CD4082B	REEL	2500pcs/reel

Logic Diagram



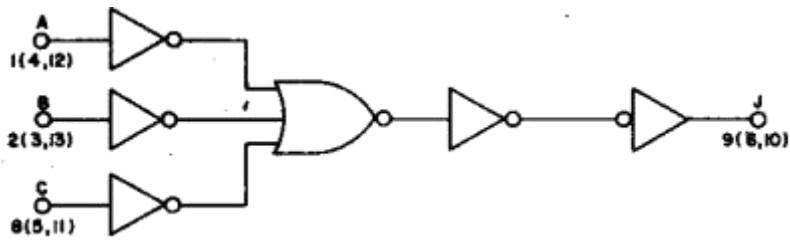
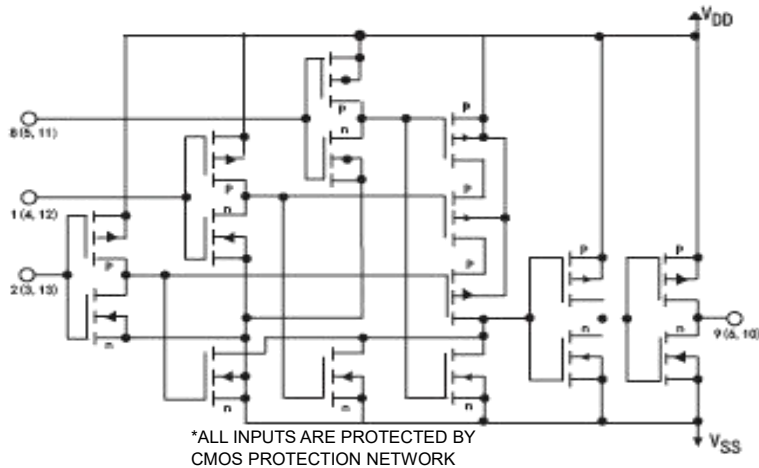


Fig.1 - Logic diagram for CD4073B(1 of 3 identical Gates).

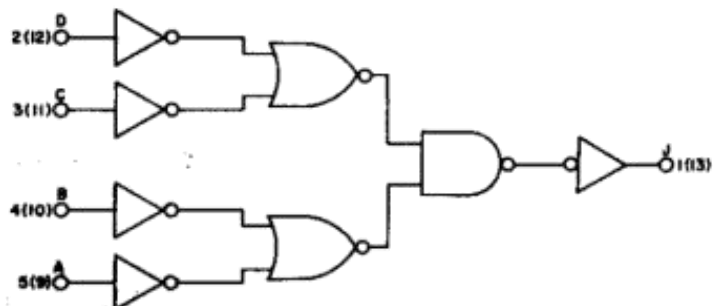
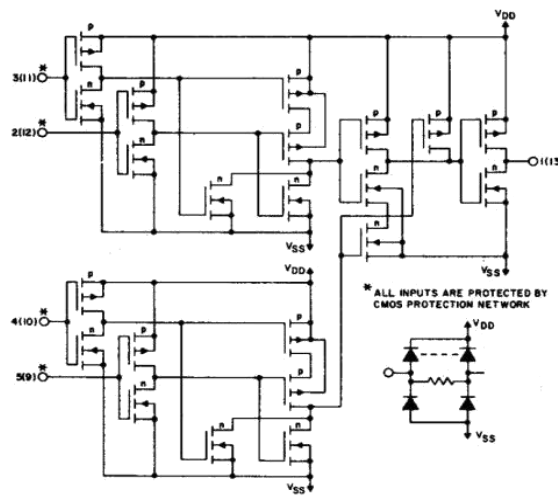
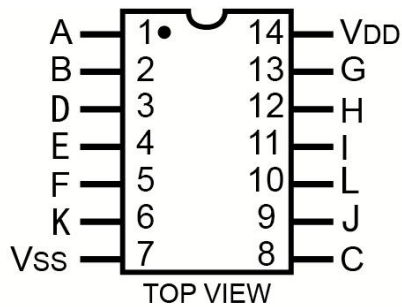
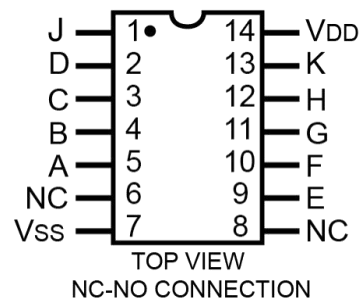


Fig.2 - Logic diagram for CD4082B (1 of 2 identical gates).

## Pin Configuration


 DIP/SOP/TSSOP  
 CB4073B

 DIP/SOP/TSSOP  
 CB4082B

## MAXIMUM RATINGS, Absolute-Maximum Values:

Condition	Min	Max	Units
<b>DC SUPPLY-VOLTAGE RANGE, (VDD):</b>			
Voltages reference to VSS Terminal)	-0.5	+20	V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5	+0.5	V
DC INPUT CURRENT ANY ONE INPUT	-	+10	mA
<b>POWER DISSIPATION PER PACKAG-(PD):</b>			
For TA=55°C to +100°C	-	500	mA
For TA=+100°C to +125°C (Derate Linearity at)	12	200	mW
<b>DEVICE DISSIPATION PER OUTPUT TRANSISTOR:</b>			
FOR TA-FULL PACKAGE=TEMPERATURE RANGE(All Package Types)	-	100	mW
OPERATING-TEMPERATURE RANGE(TA)	-40	+85	°C
STORAGE TEMPERATURE RANGE(stag)	-65	+150	°C
At distance 1/16±1/32inch(1.59+0.79mm)from case for 10s max	-	+265	°C

## Recommended operating conditions

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (for T=Full Package Temperature Range)	5	15	V

## DYNAIC ELECTRICAL CHARACTERISTICS

at TA=25°C, Input tr, ft=20ns, and CL=50 pf, RL=200KΩ

CHARACTERISTIC	TEST CONDITIOS		ALL TYPES LIMITS		UNITS
		VDD Volts	TYP.	MAX.	
Propagation Delay Time, T <sub>PHL</sub> , T <sub>PLH</sub>		5	125	250	NS
		10	60	120	
		15	40	90	
Transition Time, T <sub>PHL</sub> , T <sub>PLH</sub>		5	100	200	NS
		10	50	100	
		15	40	80	
Input Capacitance, C <sub>IN</sub>	Any Input	-	5	7.5	Pf

**STATIC ELECTRICAL CHARACTERISTICS**

CHARACTER. ISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES(°C)					UNITS
	VO (V)	VIN (V)	VDD (V)				+25		
				-40	+85	Min	TYP	MAX	
Quiescent Device Current, IDD Max.	-	0.5	5	0.25	7.5	-	0.01	0.25	μA
	-	0.10	10	0.5	15	-	0.01	0.5	
	-	0.15	15	1	30	-	0.01	1	
	-	0.20	20	5	150	-	0.02	5	
Output Low (Sink)Current IOL Min.	0.4	0.5	5	0.61	0.42	0.51	1	-	mA
	0.5	0.10	10	1.5	1.1	1.3	2.6	-	
	1.5	0.15	15	4	2.8	3.4	6.8	-	
Output High (Source) Current, IOH Min.	4.6	0.5	5	-0.61	-0.42	-0.51	-1	-	mA
	2.5	0.5	5	-1.8	-1.3	-1.6	-3.2	-	
	9.5	0.10	10	-1.5	-1.1	-1.3	-2.6	-	
	13.5	0.15	10	-4	-2.8	-3.4	-6.8	-	
Output Voltage Low-Level, VOL Max.	-	0.5	5	0.05		-	0	0.05	V
	-	0.10	10	0.05		-	0	0.05	
	-	0.15	15	0.05		-	0	0.05	
Output Voltage High-Level, VOH Min.	-	0.5	5	1.95		4.95	5	-	V
	-	0.10	10	9.95		9.95	10	-	
	-	0.15	15	14.95		14.95	15	-	
Input Low Voltage, VIL Max.	0.5	-	5	1.5		-	-	1.5	V
	1	-	10	3		-	-	3	
	1.5	-	15	4		-	-	4	
Input High Voltage, VIH Min.	0.5.4.5	-	5	3.5		3.5	-	-	V
	1.9	-	10	7		7	-	-	
	1.5.13.5	-	15	11		11	-	-	
Input Current VIN Max.		0.18	18	±0.1	±1	-	±10 <sup>-5</sup>	±0.1	μA

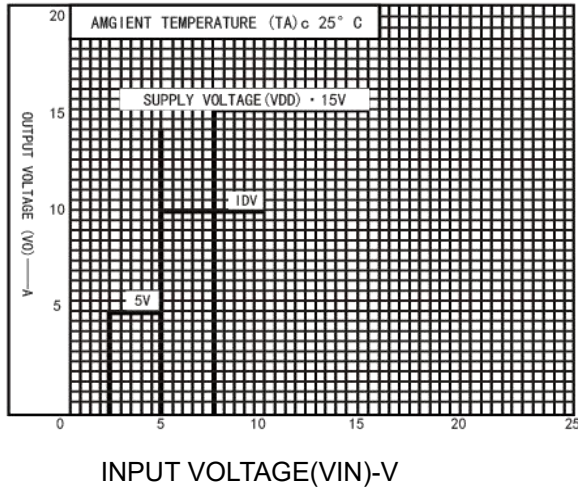


Fig.3-Typical voltage transfer characteristic.

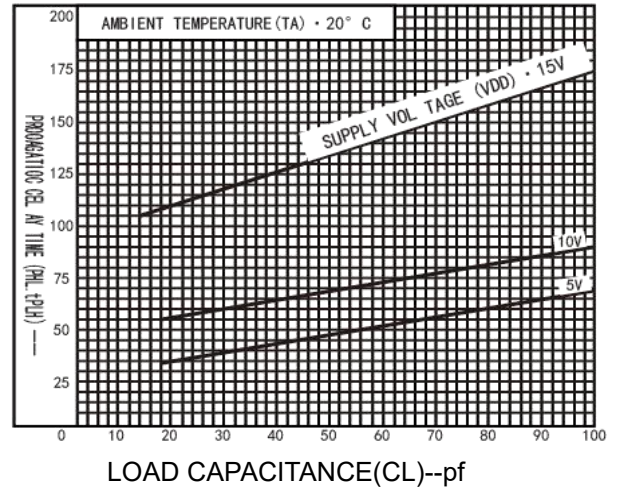


Fig.4 - Typical propagation delay time as a function of load capacitance.

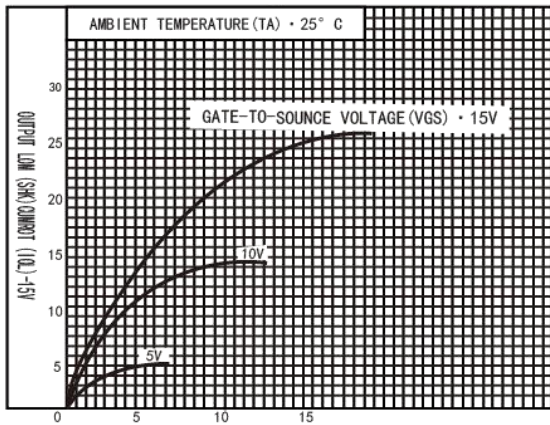


Fig.5 - Typical output low (sink) Current characteristics.

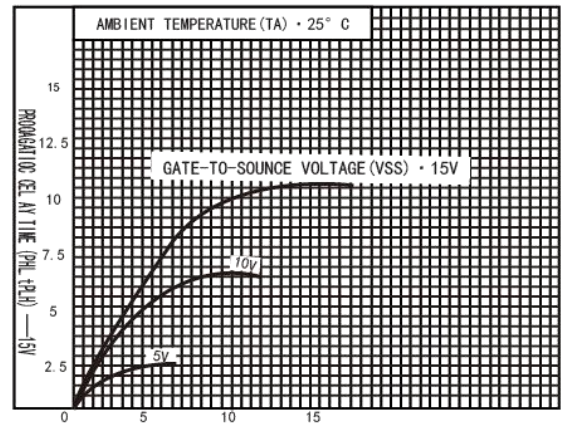


Fig.6 - Minimum output low (sink) Current characteristics.

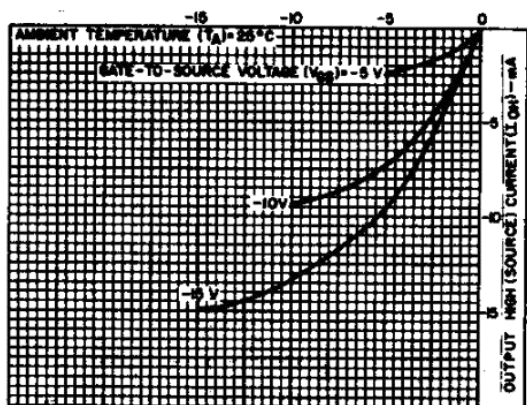


Fig.7 - Minimum output high (source) current characteristics

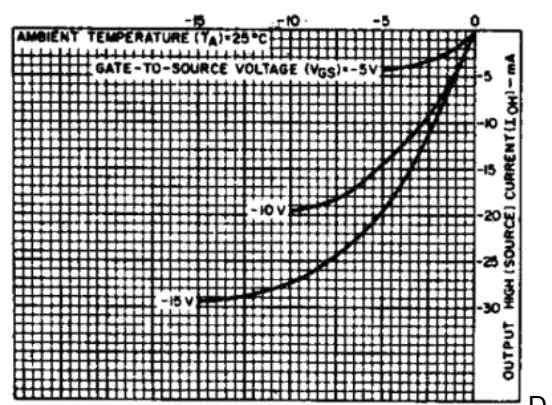


Fig.8 - Typical output high (source) current characteristics.

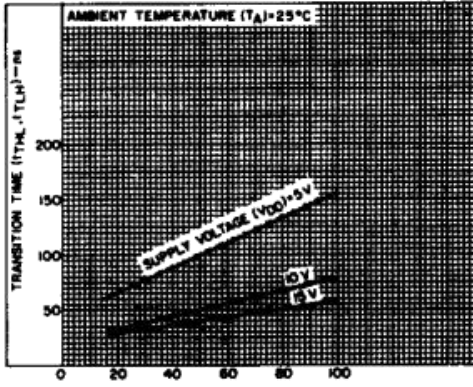


Fig.9 -Typical transition time as a function of load capacitance

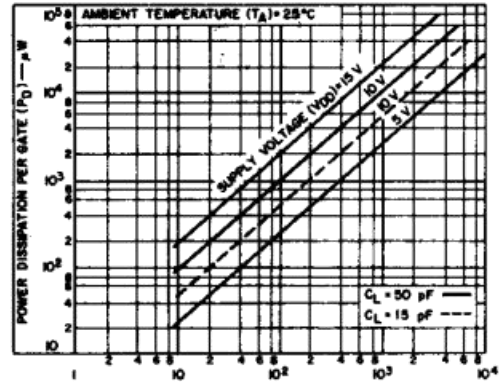


Fig.10 -Typical dynamic power dissipation per gate as a function of load capacitance

**TERMINAL ASSIGNMENTS**

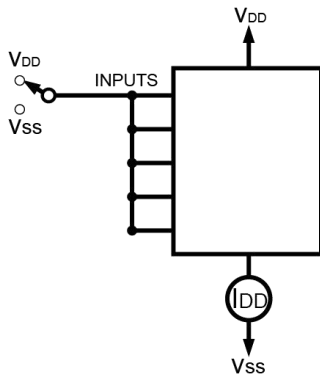


Fig.11 - Quiescent device current test circuit.

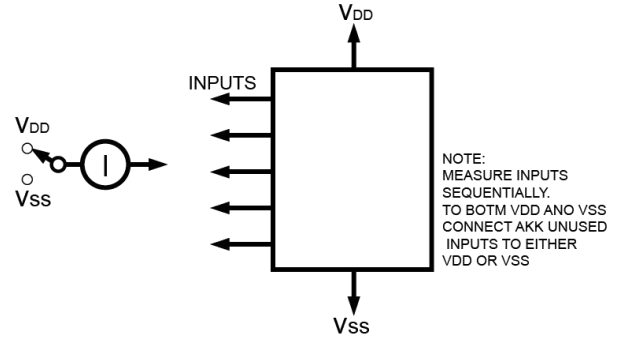


Fig.12 - Input current test circuit.

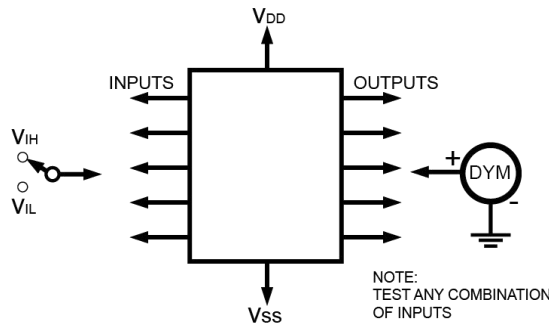
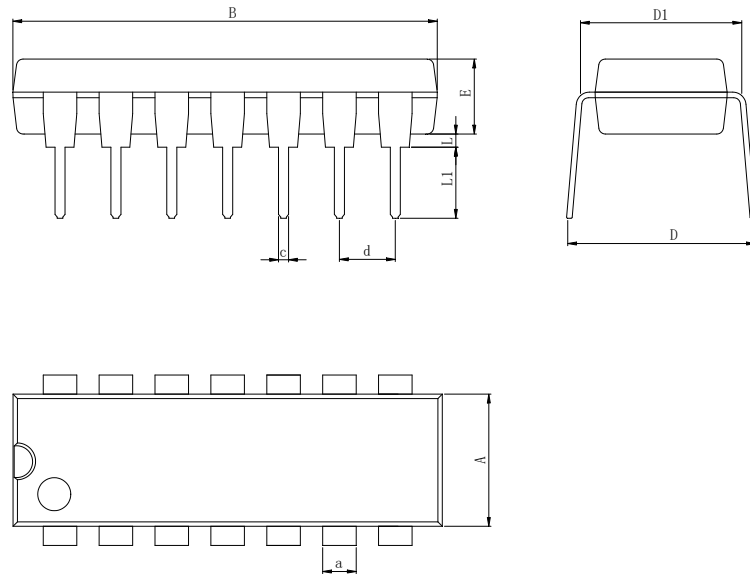


Fig.13 - Input-voltage test circuit.

## Physical Dimensions

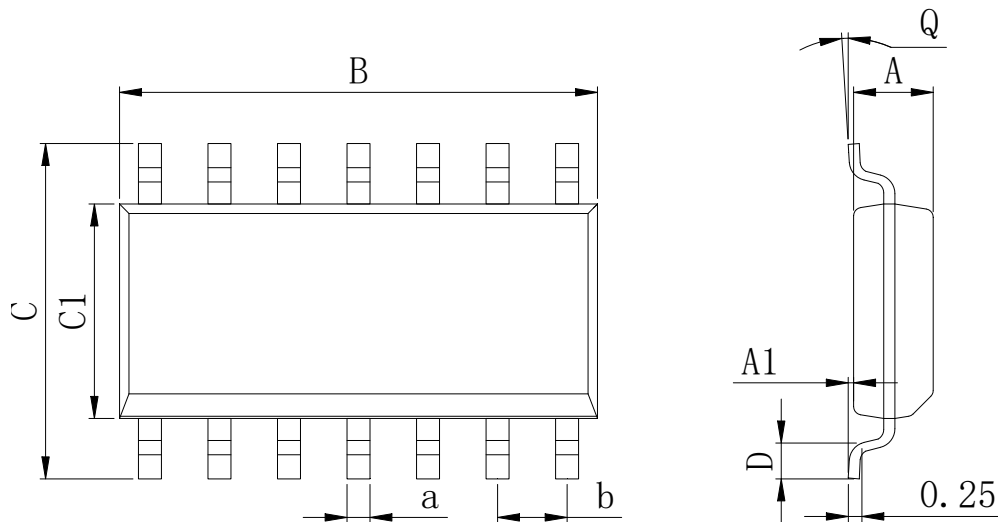
### DIP14



Dimensions In Millimeters(DIP14)

Symbol:	A	B	D	D1	E	L	L1	a	c	d
Min:	6.10	18.94	8.40	7.42	3.10	0.50	3.00	1.50	0.40	2.54 BSC
Max:	6.68	19.56	9.00	7.82	3.55	0.70	3.60	1.55	0.50	

### SOP14



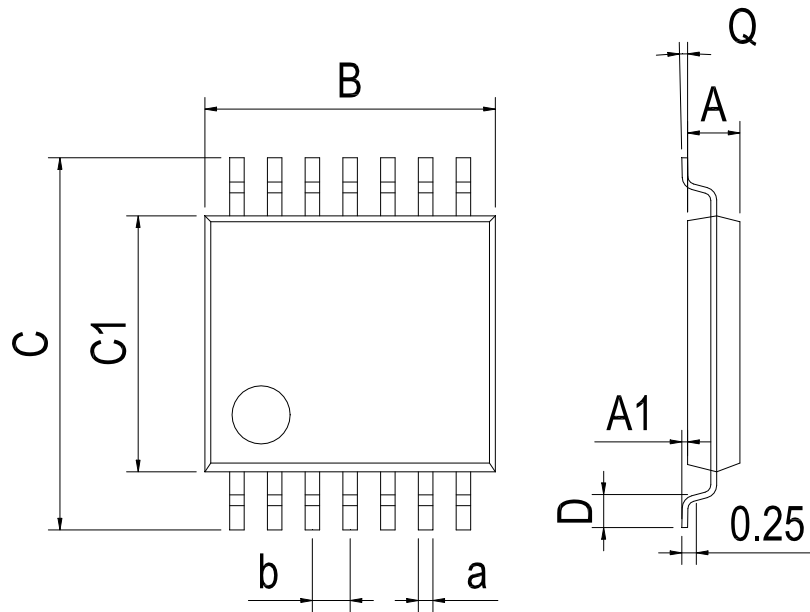
Dimensions In Millimeters(SOP14)

Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	8.55	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	8.75	6.20	4.00	0.80	8°	0.45	



## Physical Dimensions

TSSOP14



Dimensions In Millimeters(TSSOP14)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.85	0.05	4.90	6.20	4.30	0.40	0°	0.20	0.65 BSC
Max:	0.95	0.20	5.10	6.60	4.50	0.80	8°	0.25	

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