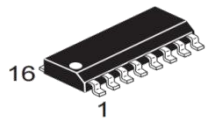
4-BIT SYNCHRONOUS UP/DPWN COUNTERS

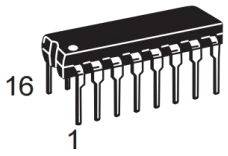
(DUAL CLOCK WITH CLEAR)

FEATURES

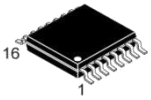
- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80-μA Max ICC
- Typical tpd = 20 ns
- ±4-mA Output Drive at 5 V
- Low Input Current of 1 μA Max
- Look-Ahead Circuitry Enhances Cascaded Counters
- Fully Synchronous in Count Modes
- Parallel Asynchronous Load for Modulo-N Count Lengths
- Asynchronous Clear



SOP16



DIP16



TSSOP16

ORDERING INFORMATION

DEVICE	Package Type	MARKING	Packing	Packing Qty
74HC193N	DIP16	74HC193	TUBE	1000pcs/Box
74HC193M/TR	SOP16	74HC193	REEL	2500pcs/Reel
74HC193MT/TR	TSSOP16	HC193	REEL	2500pcs/Reel

Description

The 74HC193 devices are 4-bit synchronous, reversible, up/down binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

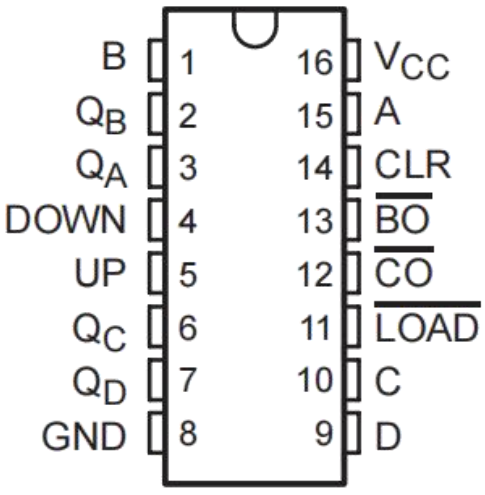
The outputs of the four flip-flops are triggered on a low-to-high-level transition of either count (clock) input (UP or DOWN). The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load ($\overline{LOAD}$) input and entering the desired data at the data inputs. The output changes to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers simply by modifying the count length with the preset inputs.

A clear (CLR) input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and $\overline{LOAD}$ inputs.

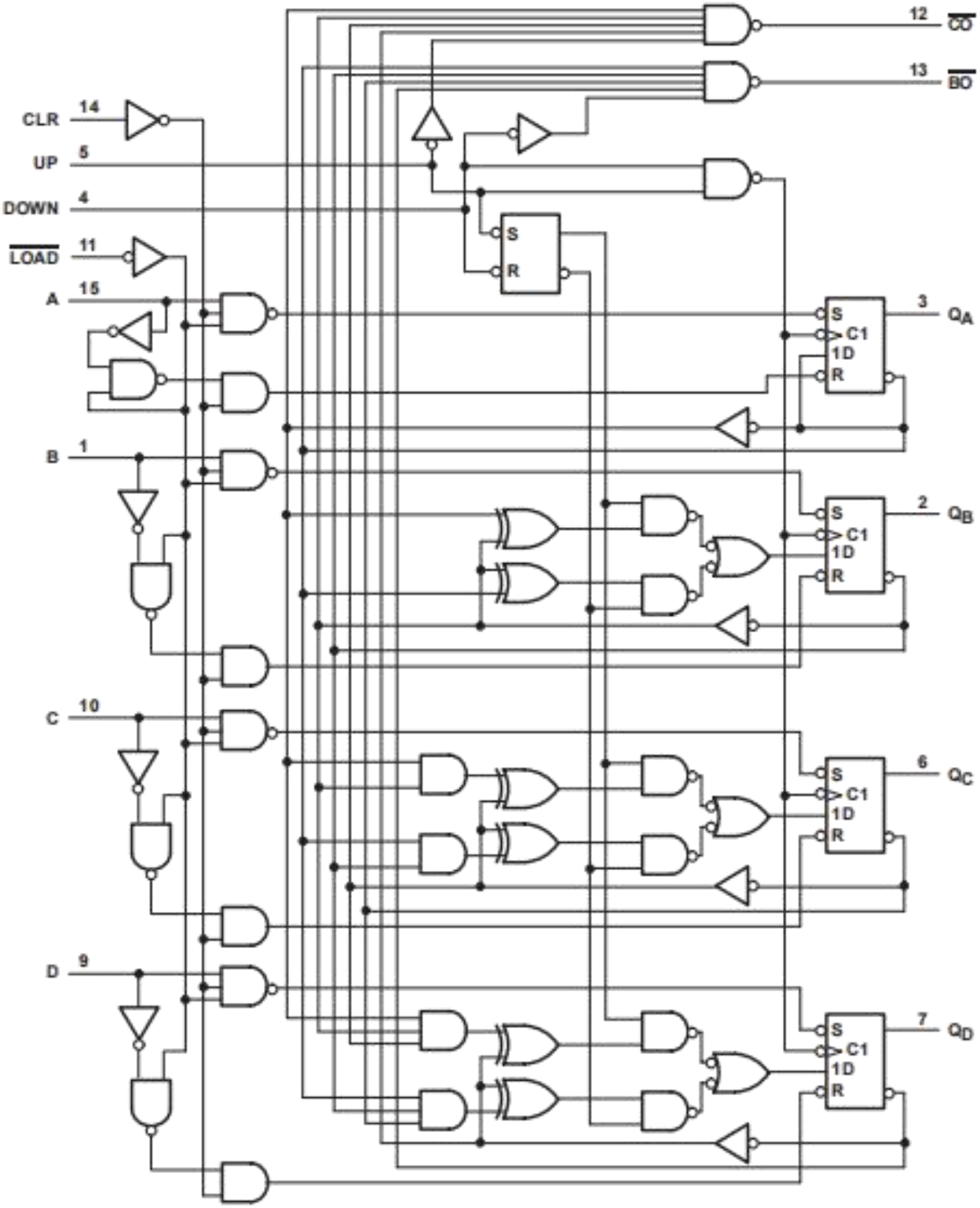
These counters were designed to be cascaded without the need for external circuitry. The borrow ($\overline{BO}$) output produces a low-level pulse while the count is zero (all outputs low) and DOWN is low. Similarly, the carry ($\overline{CO}$) output produces a low-level pulse while the count is maximum (9 or 15), and UP is low. The counters then can be cascaded easily by feeding $\overline{BO}$ and $\overline{CO}$ to DOWN and UP, respectively, of the succeeding counter.

Pin Configuration



DIP16/SOP16/TSSOP16

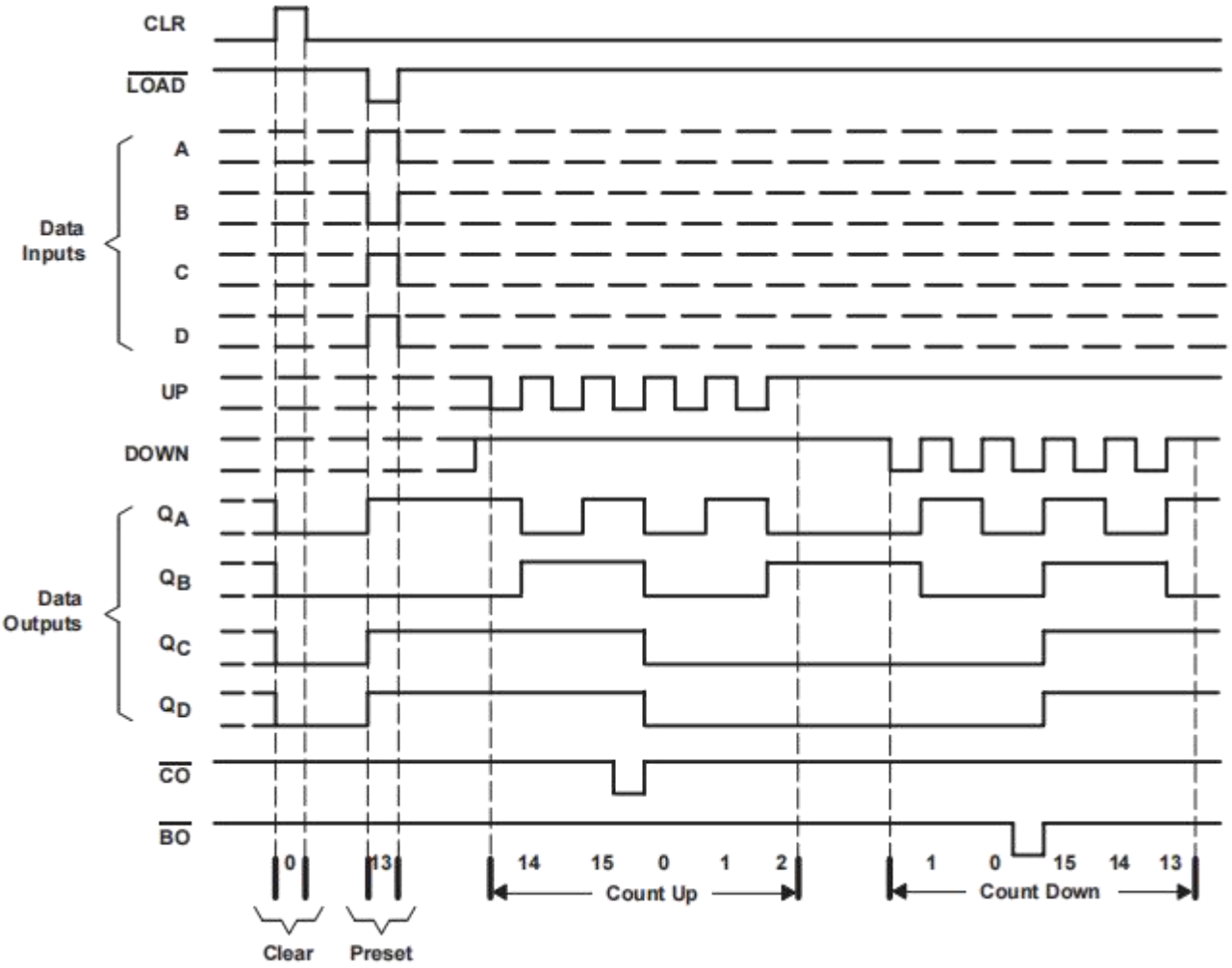
logic diagram (positive logic)



typical clear, load, and count sequence

The following sequence is illustrated below:

1. Clear outputs to 0
2. Load (preset) to binary 13
3. Count up to 14, 15, carry, 0, 1, and 2
4. Count down to 1, 0, borrow, 15, 14, and 13



NOTES: A. CLR overrides $\overline{\text{LOAD}}$, data, and count inputs.

B. When counting up, count-down input must be high; when counting down, count-up input must be high.

absolute maximum ratings over operating free-air temperature range

(unless otherwise noted)

Condition		Min	Max
Supply voltage range,VCC		-0.5V	7V
Input clamp current IIK(VI<0 or VI>VCC)(see Note 1)		-20mA	+20mA
Output clamp current,IO(Vo<0 or Vo>VCC)(see Note 1)		-20mA	+20mA
Continuous output current,IO(VO=0 to VCC)		-25mA	+25mA
Continuous current through VCC or GND		-50mA	+50mA
Package thermal impedance, θJA (see Note 2):	M package	-	73°C/W
	N package	-	67°C/W
	MT package	-	108°C/W
Storage temperature range,Tstg		-65°C	150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.
Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			74HC193			UNIT
			MIN	NOM	MAX	
VCC	Supply voltage		2	5	6	V
VIH	High-level input voltage	VCC = 2 V	1.5			V
		VCC = 4.5 V	3.15			
		VCC = 6 V	4.2			
VIL	Low-level input voltage	VCC = 2 V			0.5	V
		VCC = 4.5 V			1.35	
		VCC = 6 V			1.8	
VI	Input voltage		0		VCC	V
VO	Output voltage		0		VCC	V
t/△v‡	Input transition rise/fall time	VCC = 2 V			1000	ns
		VCC = 4.5 V			500	
		VCC = 6 V			400	
TA	Operating free-air temperature		−40		85	°C

NOTE 3: All unused inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.
‡ If this device is used in the threshold region (from VILmax = 0.5 V to VIHmin = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at tt = 1000 ns and VCC = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

electrical characteristics over recommended operating free-air temperature range

(unless otherwise noted)

PARAMETER	TEST CONDITIONS		VCC	TA = 25°C			74HC193		UNIT
				MIN	TYP	MAX	MIN	MAX	
VOH	VI = VIH or VIL	IOH = −20 A	2 V	1.9	1.998		1.9		V
			4.5 V	4.4	4.499		4.4		
			6 V	5.9	5.999		5.9		
		IOH = −4 mA	4.5 V	3.98	4.3		3.84		
		IOH = −5.2 mA	6 V	5.48	5.8		5.34		
VOL	VI = VIH or VIL	IOL = 20 A	2 V		0.002	0.1		0.1	V
			4.5 V		0.00	0.1		0.1	
			6 V		0.001	0.1		0.1	
		IOL = 4 mA	4.5 V		0.17	0.26		0.33	
		IOL = 5.2 mA	6 V		0.15	0.26		0.33	
II	VI = VCC or 0		6 V		±0.1	±100		±1000	nA
ICC	VI = VCC or 0,IO = 0		6 V			8		80	μA
Ci			2 V to 6 V		3	10		10	pF

timing requirements over recommended operating free-air temperature range

(unless otherwise noted)

		VCC	TA = 25°C		74HC193		UNIT
			MIN	MAX	MIN	MAX	
fclock Clock frequency		2 V		4.2		3.3	MHz
		4.5 V		21		17	
		6 V		24		19	
tw Pulse duration	CLR high	2 V	120		150		ns
		4.5 V	24		30		
		6 V	21		26		
	$\overline{LOAD}$ low	2 V	120		150		
		4.5 V	24		30		
		6 V	21		26		
	UP or DOWN high or low	2 V	120		150		
		4.5 V	24		30		
		6 V	21		26		
tsu Setup time	Data before $\overline{LOAD}$ inactive	2 V	110		140		ns
		4.5 V	22		28		
		6 V	19		24		
	CLR inactive before UP↑ or DOWN	2 V	110		140		
		4.5 V	22		28		
		6 V	19		24		
	$\overline{LOAD}$ inactive before UP↑ or DOWN	2 V	110		140		
		4.5 V	22		28		
		6 V	19		24		
th Hold time	Data after $\overline{LOAD}$ inactive	2 V	5		5		ns
		4.5 V	5		5		
		6 V	5		5		

switching characteristics over recommended operating free-air temperature range, CL = 50 pF

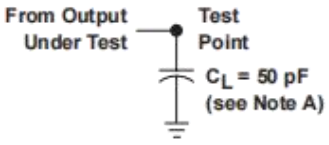
(unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC	TA = 25°C			74HC193		UNIT
				MIN	TYP	MAX	MIN	MAX	
fmax			2 V	4.2	8		3.3		MHz
			4.5 V	21	55		17		
			6 V	24	60		19		
tpd	UP	CO	2 V		75	165		205	ns
			4.5 V		24	33		41	
			6 V		20	28		35	
	DOWN	BO	2 V		75	165		205	
			4.5 V		24	33		41	
			6 V		20	28		35	
	UP or DOWN	Any Q	2 V		190	250		315	
			4.5 V		40	50		63	
			6 V		35	43		54	
	LOAD	Any Q	2 V		190	260		325	
			4.5 V		40	52		65	
			6 V		35	44		55	
tPHL	CLR	Any Q	2 V		170	240		300	ns
			4.5 V		36	48		60	
			6 V		31	41		51	
tt		Any	2 V		38	75		95	ns
			4.5 V		8	15		19	
			6 V		6	13		16	

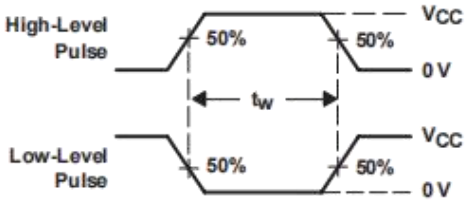
operating characteristics, TA = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
Cpd	Power dissipation capacitance	No load	50	pF

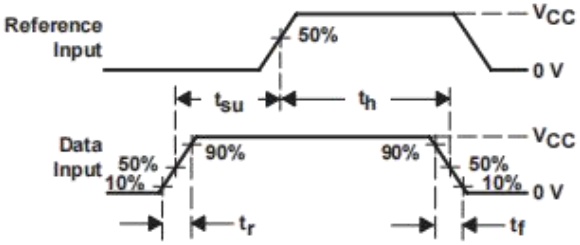
PARAMETER MEASUREMENT INFORMATION



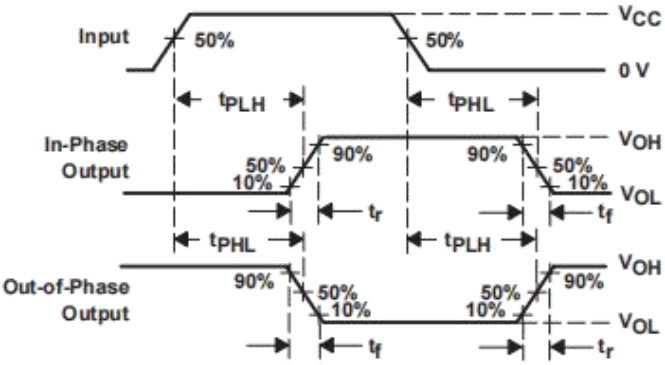
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES:

A. CL includes probe and test-fixture capacitance.

B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ⩽ 1 MHz, ZO = 50 Ω, tr = 6 ns, tf = 6 ns.

C. For clock inputs, fmax is measured when the input duty cycle is 50%.

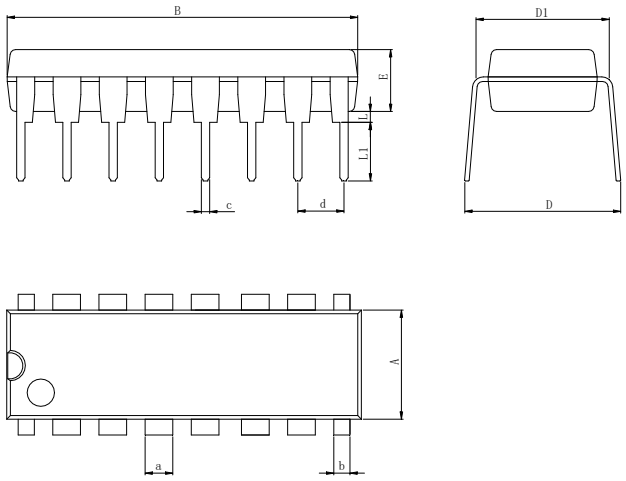
D. The outputs are measured one at a time with one input transition per measurement.

E. tPLH and tPHL are the same as tpd.

Figure 1. Load Circuit and Voltage Wave forms

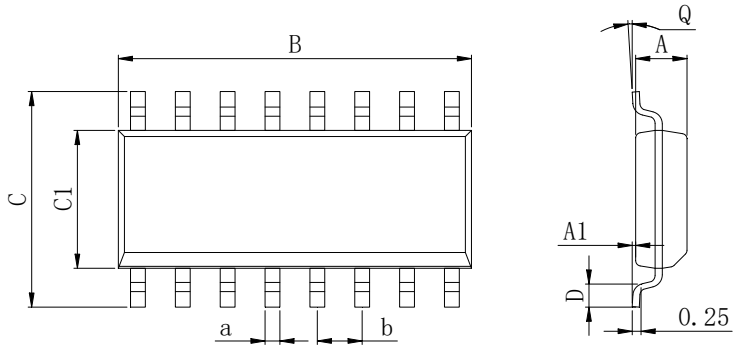
Physical Dimensions

DIP16



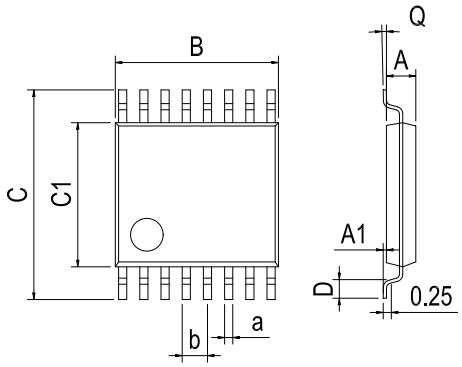
Dimensions In Millimeters(DIP16)											
Symbol:	A	B	D	D1	E	L	L1	a	b	c	d
Min:	6.10	18.94	8.40	7.42	3.10	0.50	300	1.50	0.85	0.40	2.54 BSC
Max:	6.68	19.56	9.00	7.82	3.55	0.70	3.60	1.55	0.90	0.50	

SOP16



Dimensions In Millimeters(SOP16)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	9.80	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	10.0	6.20	4.00	0.80	8°	0.45	

TSSOP16



Dimensions In Millimeters(TSSOP16)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.85	0.05	4.90	6.20	4.30	0.40	0°	0.20	0.65 BSC
Max:	0.95	0.20	5.10	6.60	4.50	0.80	8°	0.25	

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