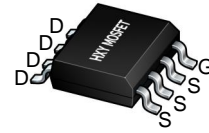




Description

The HXY4480S uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



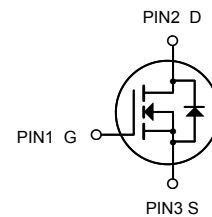
SOP-8

General Features

$V_{DS} = 40V$ $I_D = 14 A$
 $R_{DS(ON)} < 18m\Omega @ V_{GS}=10V$
 $R_{DS(ON)} < 24m\Omega @ V_{GS}=4.5V$

Application

Battery protection
 Load switch
 Uninterruptible power supply



N-Channel MOSFET

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
HXY4480S	SOP-8	4480 XXXX	3000

Absolute Maximum Ratings ($T_c=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Limit	Unit
V_{DS}	Drain-Source Voltage	40	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Drain Current-Continuous	14	A
$I_D(70^\circ C)$	Drain Current-Continuous($T_c=70^\circ C$)	10	A
I_{DM}	Pulsed Drain Current	70	A
P_D	Maximum Power Dissipation	3.1	W
EAS	Single pulse avalanche energy (Note 5)	135	mJ
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 To 150	$^\circ C$



Electrical Characteristics Ta = 25°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
Drain-Source Breakdown Voltage	V _{DSS}	I _D =250 μ A, V _{GS} =0V	40			V	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =32V, V _{GS} =0V			1	μA	
		V _{DS} =32V, V _{GS} =0V, T _J =55°C			5		
Gate-Body Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	μA	
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1		3	V	
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =14A		14	18	mΩ	
		V _{GS} =10V, I _D =14A T _J =125°C		18	24		
		V _{GS} =4.5V, I _D =5A			16.5		
On State Drain Current	I _{D(ON)}	V _{GS} =10V, V _{DS} =5V	70			A	
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =5A	50			S	
Input Capacitance	C _{iss}	V _{GS} =0V, V _{DS} =20V, f=1MHz		1600	1920	pF	
Output Capacitance	C _{oss}			320			
Reverse Transfer Capacitance	C _{rss}			100			
Gate Resistance	R _g	V _{GS} =0V, V _{DS} =0V, f=1MHz		3.4		Ω	
Total Gate Charge (10V)	Q _g	V _{GS} =10V, V _{DS} =20V, I _D =14A		22		nC	
Total Gate Charge (4.5V)				10.5			
Gate Source Charge			Q _{gs}		4.2		
Gate Drain Charge			Q _{gd}		4.8		
Turn-On DelayTime	t _{d(on)}	V _{GS} =10V, V _{DS} =20V, R _L =1.5Ω, R _{GEN} =3Ω		3.5		ns	
Turn-On Rise Time	t _r			6			
Turn-Off DelayTime	t _{d(off)}			13.2			
Turn-Off Fall Time	t _f			3.5			
Body Diode Reverse Recovery Time	t _{rr}	I _F = 14A, di/dt= 100A/us		31		nC	
Body Diode Reverse Recovery Charge	Q _{rr}			33			
Maximum Body-Diode Continuous Current	I _S				4	A	
Diode Forward Voltage	V _{SD}	I _S =1A, V _{GS} =0V			1	V	

Note : The static characteristics in Figures 1 to 6 are obtained using <300 us pulses, duty cycle 0.5% max.



Typical Characteristics

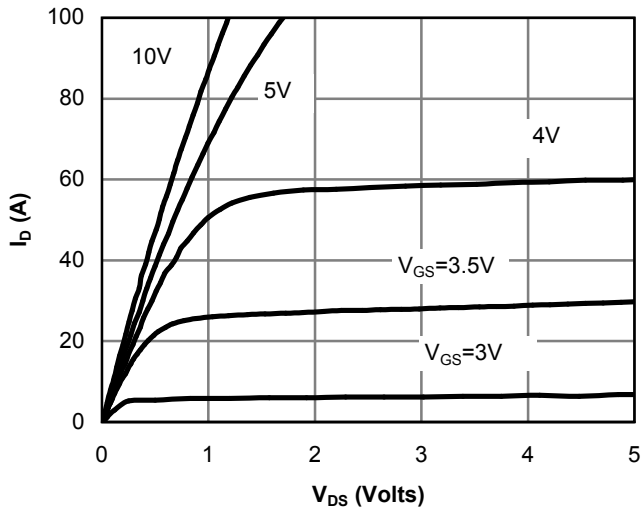


Figure 1: On-Region Characteristics

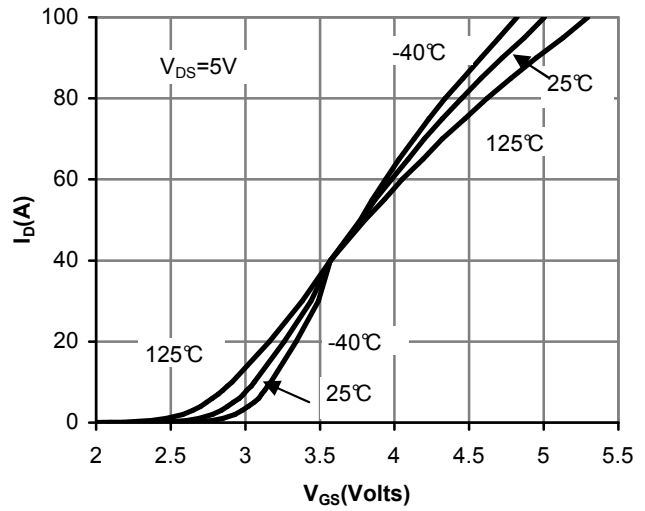


Figure 2: Transfer Characteristics

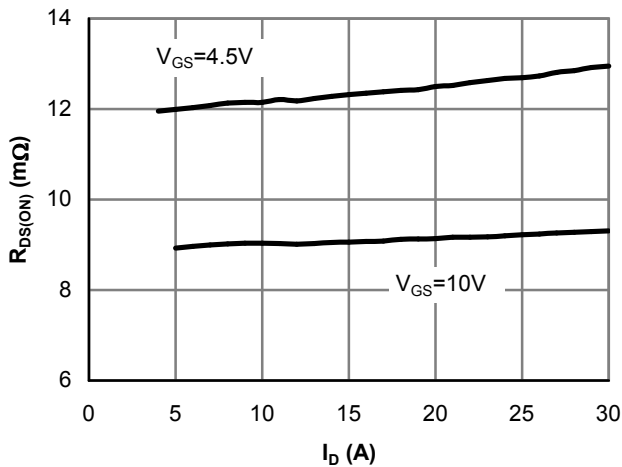


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

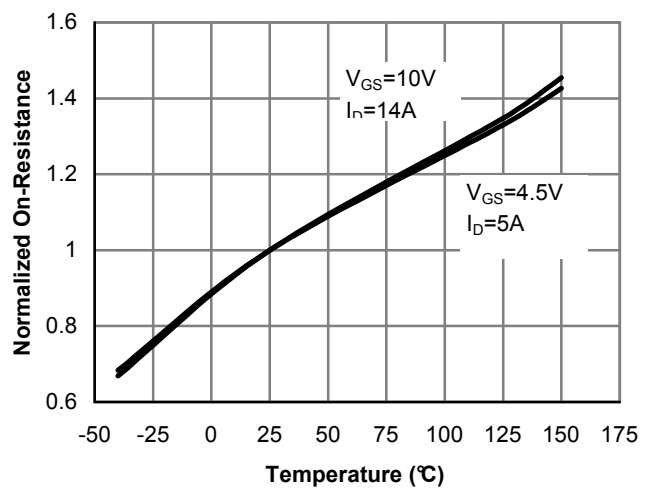


Figure 4: On-Resistance vs. Junction Temperature

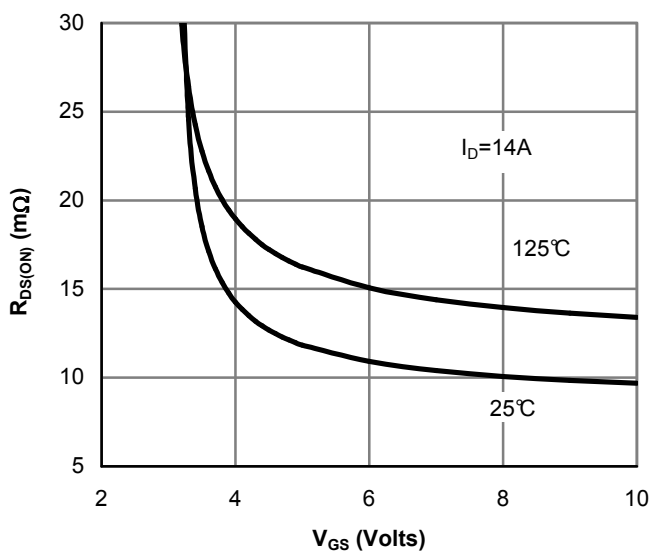


Figure 5: On-Resistance vs. Gate-Source Voltage

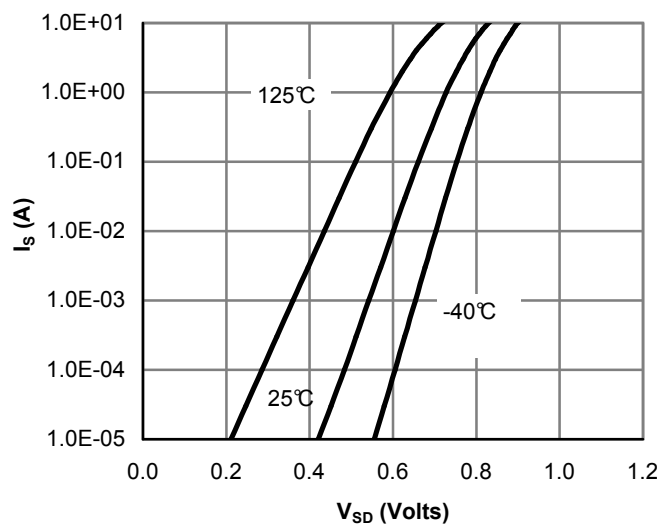


Figure 6: Body-Diode Characteristics



Typical Characteristics

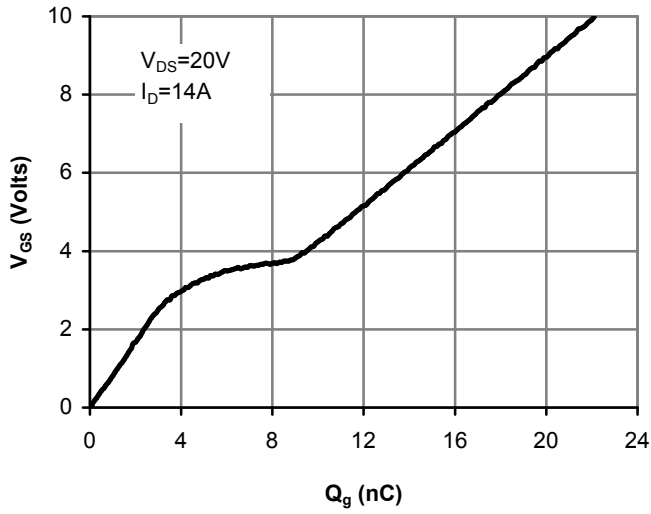


Figure 7: Gate-Charge Characteristics

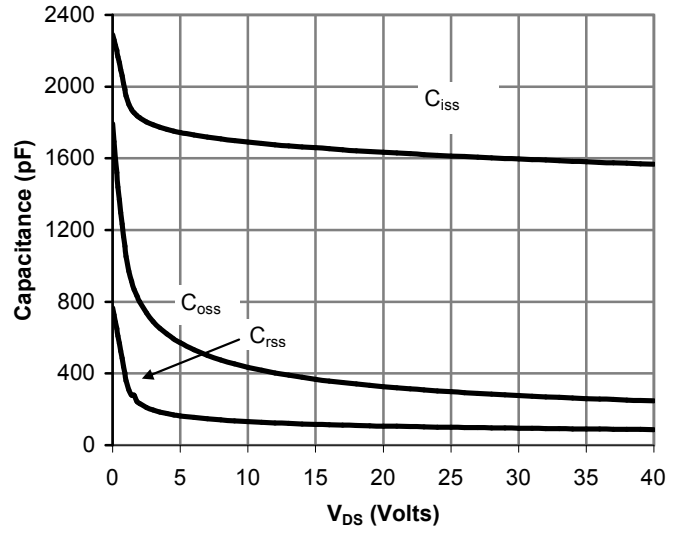


Figure 8: Capacitance Characteristics

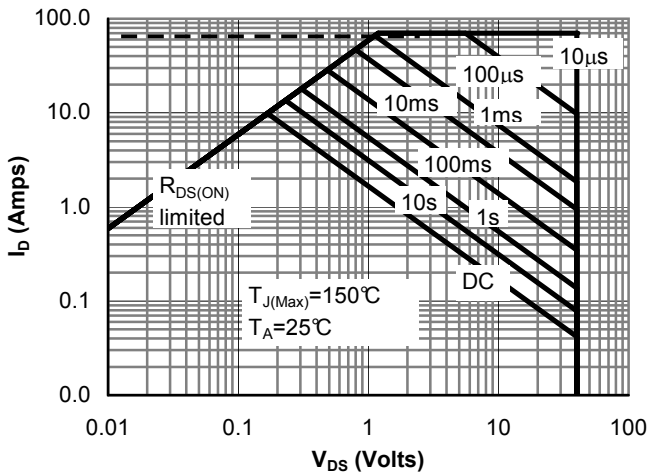


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

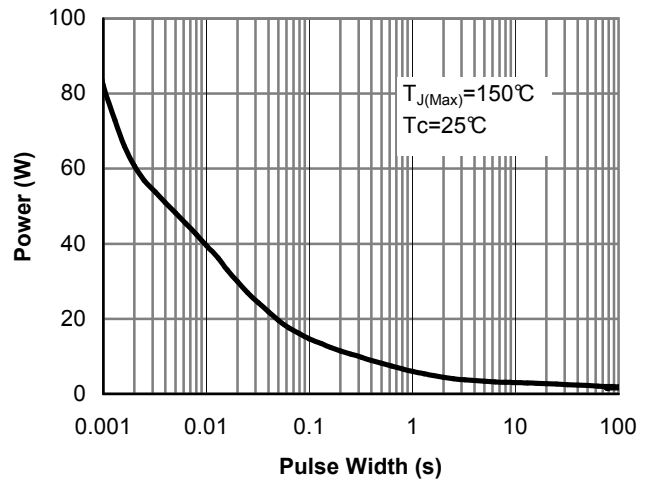


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

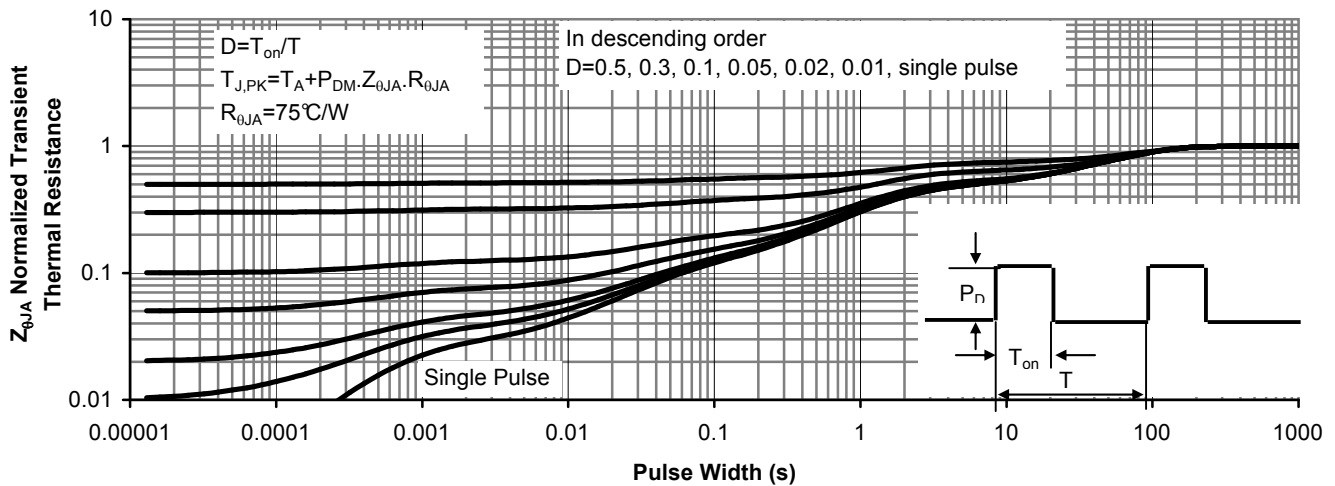
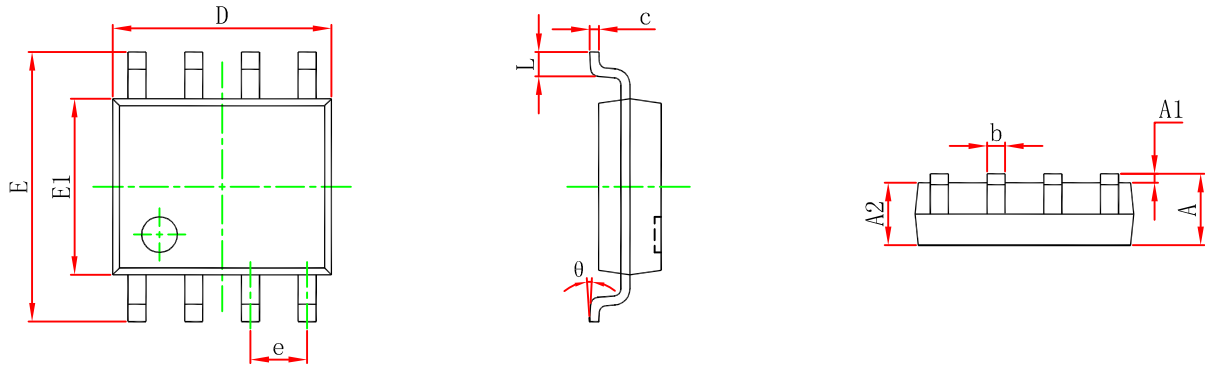


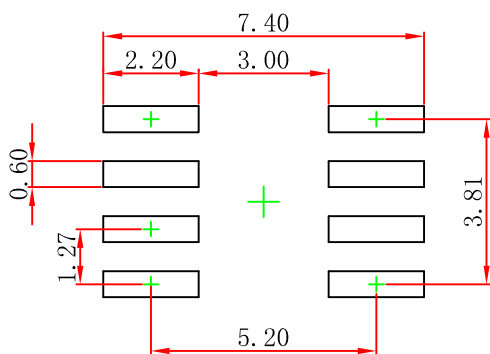
Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)



SOP-8 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



- Note:
1. Controlling dimension: in millimeters.
 2. General tolerance: $\pm 0.05\text{mm}$.
 3. The pad layout is for reference purposes only.



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