

**Description**

The 1216D2 uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages. This device is suitable for use as a load switching application and a wide variety of other applications.

**General Features**

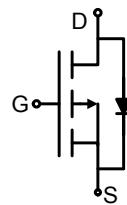
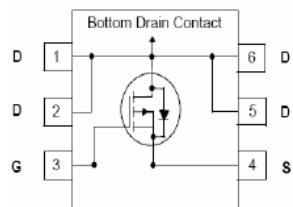
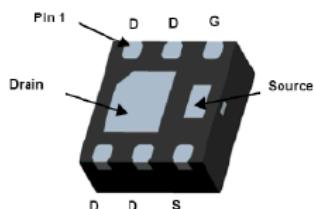
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$V_{DSS}$	$R_{DS(ON)}$ @ -4.5V(Typ)	$R_{DS(ON)}$ @ -2.5V(Typ)	$I_D$
-12V	12.7mΩ	19mΩ	-16A

- Advanced trench MOSFET process technology
- Ultra low on-resistance with low gate charge

**Application**

- PWM applications
- Load switch
- Battery charge in cellular handset

**Schematic diagram****Pin assignment****DFN2X2-6L****Ordering Information**

Part Number	Marking	Case	Packaging
1216D2	1216	DFN2*2-6L	3000pcs/Reel

**Absolute maximum ratings ( $T_c=25^\circ\text{C}$  unless otherwise noted)**

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	-12	V
Gate-Source Voltage	$V_{GS}$	$\pm 8$	V
Drain Current-Continuous	$I_D$	-16	A
Drain Current -Pulsed (Note 1)	$I_{DM}$	-65	A
Maximum Power Dissipation	$P_D$	18	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	°C

**Thermal Characteristic**

Thermal Resistance, Junction-to-Case (Note 2)	$R_{\theta JC}$	6.9	°C/W
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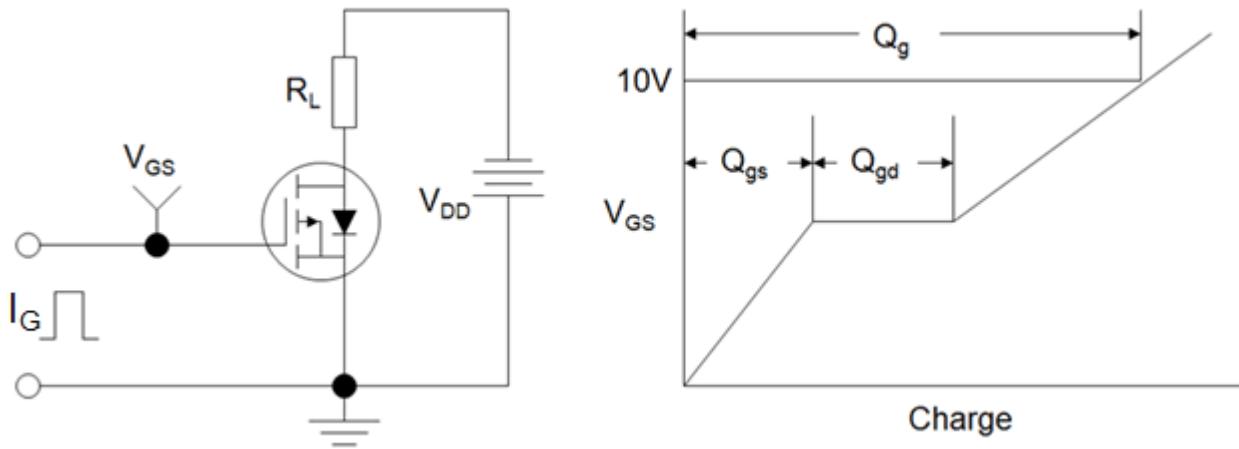
**Electrical characteristics ( $T_A=25^\circ\text{C}$  unless otherwise noted)**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{GS}=0\text{V}, I_D=-250\mu\text{A}$	-12	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=-12\text{V}, V_{GS}=0\text{V}$	-	-	-1	$\mu\text{A}$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 8\text{V}, V_{DS}=0\text{V}$	-	-	$\pm 100$	nA
<b>On Characteristics</b> <sup>(Note 3)</sup>						
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS}=V_{GS}, I_D=-250\mu\text{A}$	-0.6	-1	-1.2	V
Drain-Source On-State Resistance	$R_{DS(\text{ON})}$	$V_{GS}=-4.5\text{V}, I_D=-1\text{A}$	-	12.7	21	$\text{m}\Omega$
		$V_{GS}=-2.5\text{V}, I_D=-1\text{A}$	-	19	27	$\text{m}\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=-5\text{V}, I_D=6.7\text{A}$	20	-	-	S
<b>Dynamic Characteristics</b> <sup>(Note 4)</sup>						
Input Capacitance	$C_{iss}$	$V_{DS}=-10\text{V}, V_{GS}=0\text{V}, F=1.0\text{MHz}$	-	2700	-	PF
Output Capacitance	$C_{oss}$		-	680	-	PF
Reverse Transfer Capacitance	$C_{rss}$		-	590	-	PF
<b>Switching Characteristics</b> <sup>(Note 4)</sup>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-10\text{V}, I_D=-1\text{A}$ $V_{GS}=-4.5\text{V}, R_{GEN}=10\Omega$	-	11	-	nS
Turn-on Rise Time	$t_r$		-	35	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	30	-	nS
Turn-Off Fall Time	$t_f$		-	10	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=-6\text{V}, I_D=-10\text{A}, V_{GS}=-4.5\text{V}$	-	35	48	nC
Gate-Source Charge	$Q_{gs}$		-	5	-	nC
Gate-Drain Charge	$Q_{gd}$		-	10	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage <sup>(Note 3)</sup>	$V_{SD}$	$V_{GS}=0\text{V}, I_S=-8\text{A}$	-	-	-1	V
Diode Forward Current <sup>(Note 2)</sup>	$I_S$		-	-	-16	A

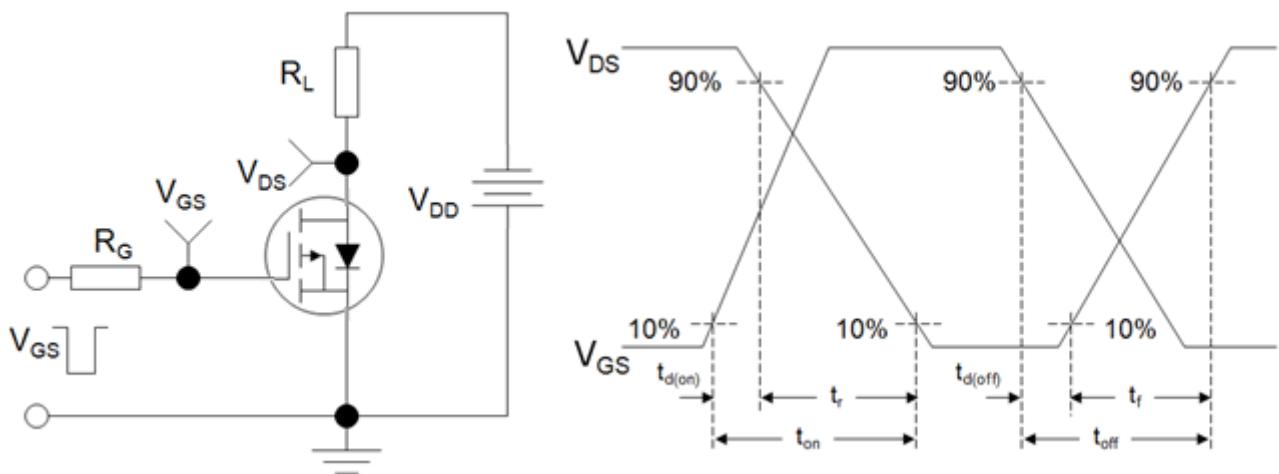
**Notes:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production

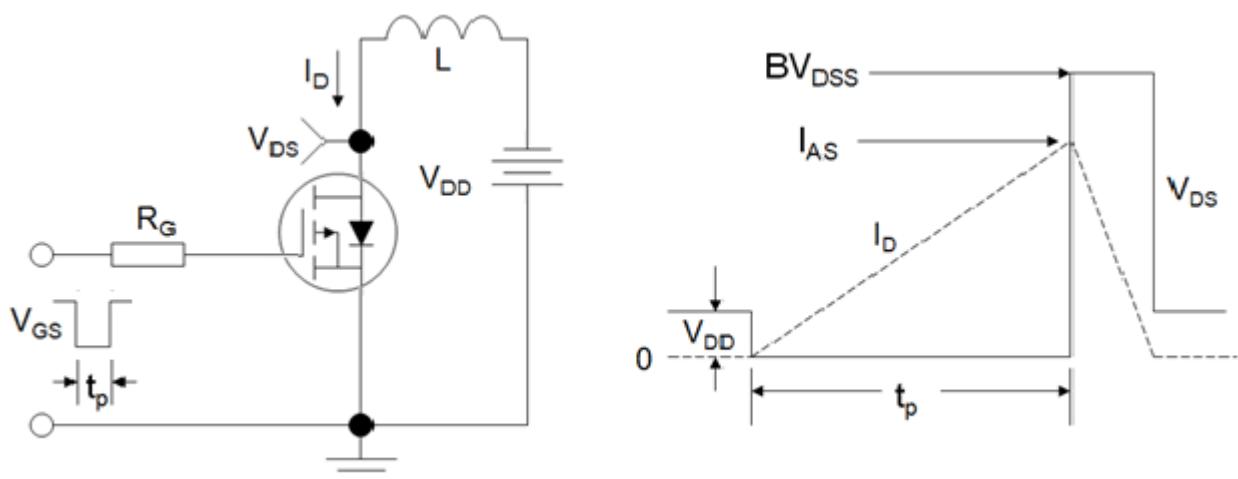
Gate Charge Test Circuit

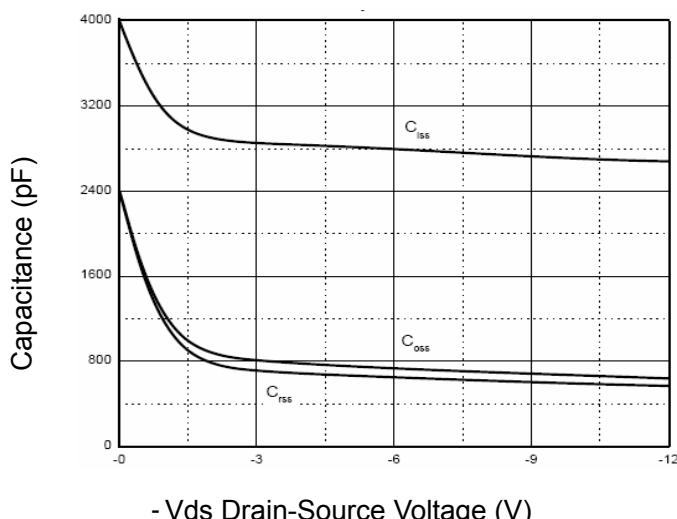


Switch Time Test Circuit



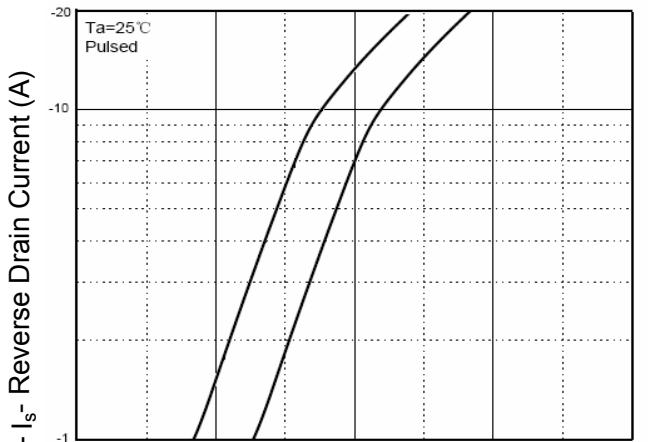
EAS Test Circuit





- Vds Drain-Source Voltage (V)

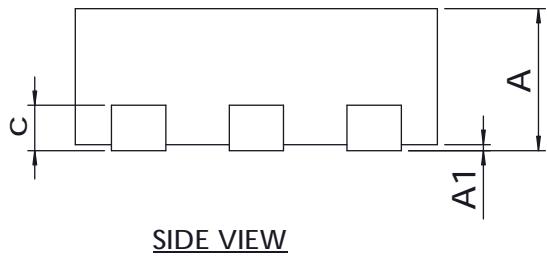
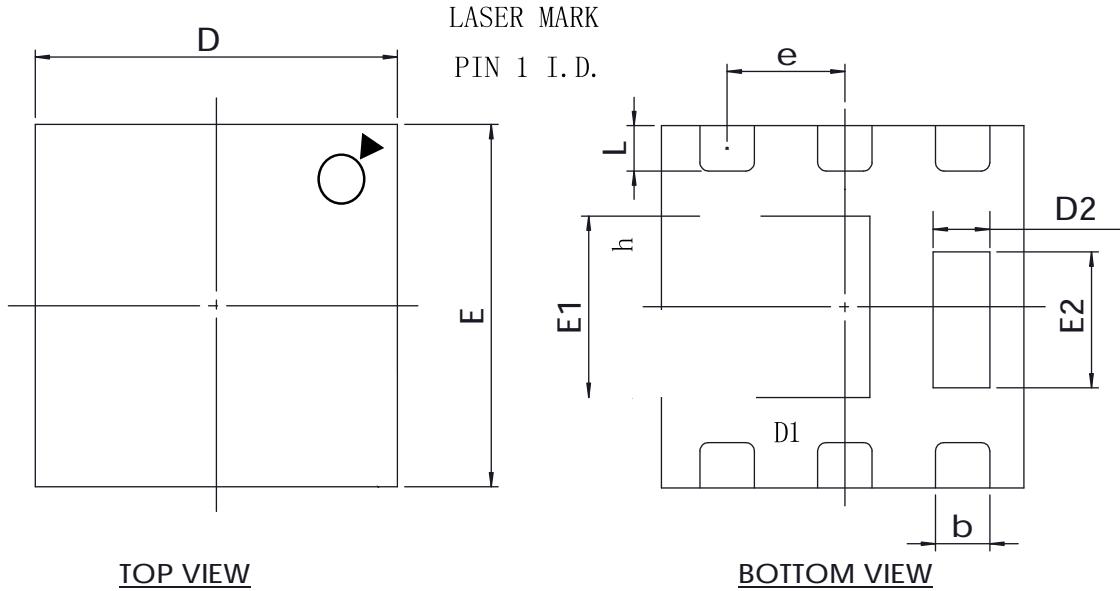
**Figure 7 Capacitance vs Vds**



-Vsd Source-Drain Voltage (V)

**Figure 8 Source- Drain Diode Forward**

## Package Information



COMMON DIMENSIONS  
(UNITS OF MEASURE=mm)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	NA	0.02	0.05
b	0.20	0.27	0.34
c	0.18	0.20	0.25
D	1.95	2.00	2.07
E	1.95	2.00	2.07
D1	0.80	0.90	1.00
E1	0.90	1.00	1.10
D2	0.20	0.30	0.40
E2	0.65	0.75	0.85
L	0.20	0.25	0.35
h	0.20	0.25	0.30
e	0.65BSC		