

# N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY						
V <sub>DS</sub> (V)	$R_{DS(on)}(\Omega)$	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)			
30	0.008 at V <sub>GS</sub> = 10 V	13	6.1 nC			
	0.011 at V <sub>GS</sub> = 4.5 V	11	0.1110			

**SO-8** 

Top View

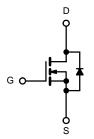
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#### **FEATURES**

- · Halogen-free
- TrenchFET® Power MOSFET
- Optimized for High-Side Synchronous Rectifier Operation
- 100 % R<sub>g</sub> Tested
- 100 % UIS Tested

#### **APPLICATIONS**

- Notebook CPU Core
  - High-Side Switch



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS	<b>S</b> T <sub>A</sub> = 25 °C, unles	s otherwise no	oted	
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	$V_{DS}$	30	V	
Gate-Source Voltage		$V_{GS}$	± 20	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
	T <sub>C</sub> = 25 °C		13	
Continuous Proin Current (T. – 150 °C)	T <sub>C</sub> = 70 °C	I <sub>D</sub>	10	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	T <sub>A</sub> = 25 °C		9 <sup>b, c</sup>	
	T <sub>A</sub> = 70 °C		7 <sup>b, c</sup>	٦ ,
Pulsed Drain Current		I <sub>DM</sub>	45	A
Cantinua Causa Daria Dia da Custant	T <sub>C</sub> = 25 °C	,	3.7	
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	I <sub>S</sub>	2.0 <sup>b, c</sup>	
Single Pulse Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	20	
Avalanche Energy	L = 0.1 mm	E <sub>AS</sub>	21	mJ
	T <sub>C</sub> = 25 °C		4.1	
Manianum Davier Disabation	T <sub>C</sub> = 70 °C	В	2.5	W
Maximum Power Dissipation	T <sub>A</sub> = 25 °C	$P_{D}$	2,2 <sup>b, c</sup>	¬
	T <sub>A</sub> = 70 °C		1.3 <sup>b, c</sup>	
Operating Junction and Storage Temperature Ra	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>b, d</sup>	t ≤ 10 s	R <sub>thJA</sub>	39	55	°C/W	
Maximum Junction-to-Foot (Drain)	Steady State	R <sub>thJF</sub>	25	29	C/VV	

#### Notes:

- a. Base on  $T_C = 25$  °C.
- b. Surface Mounted on 1" x 1" FR4 board.
- c. t = 10 s.
- d. Maximum under Steady State conditions is 85 °C/W.



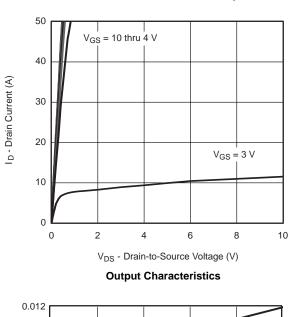
<b>SPECIFICATIONS</b> $T_J = 25  ^{\circ}\text{C}$ Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Static				.,,,,			
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$	30			V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$			26		mV/°C	
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA		- 6			
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1.0		3.0	V	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
		V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V			1		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C	10		μΑ		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	20			Α	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A		0.008		Ω	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 9 A		0.011			
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 10 A		50		S	
Dynamic <sup>b</sup>					I	1	
Input Capacitance	C <sub>iss</sub>			800		pF	
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		165			
Reverse Transfer Capacitance	C <sub>rss</sub>			73			
Total Cata Charms		V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A		15	23	nC	
Total Gate Charge	$Q_g$			6.8	10.2		
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS} = 15 \text{ V}, V_{GS} = 5 \text{ V}, I_{D} = 10 \text{ A}$		2.5			
Gate-Drain Charge	$Q_{gd}$			2.3			
Gate Resistance	$R_g$	f = 1 MHz	0.36	1.8	3.6	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			16	23		
Rise Time	t <sub>r</sub>	$V_{DD}$ = 15 V, $R_L$ = 1.4 $\Omega$		12	16		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 9 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		16	22		
Fall Time	t <sub>f</sub>			10	18	200	
Turn-On Delay Time	t <sub>d(on)</sub>			8	16	ns	
Rise Time	t <sub>r</sub>	$V_{DD}$ = 15 V, $R_L$ = 1.4 $\Omega$		10	20		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 9 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		16	22		
Fall Time	t <sub>f</sub>			8	15		
<b>Drain-Source Body Diode Characterist</b>	ics						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			10	Δ	
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>				50	A	
Body Diode Voltage	$V_{SD}$	I <sub>S</sub> = 9 A		0.8	1.2	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>			15	30	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> = 9 A, dI/dt = 100 A/μs, T <sub>J</sub> = 25 °C		6	12	nC	
Reverse Recovery Fall Time	t <sub>a</sub>	i <sub>F</sub> = θ A, αί/αι = 100 A/μs, 1 <sub>J</sub> = 25 °C		8		20	
everse Recovery Rise Time t <sub>b</sub>				7		ns	

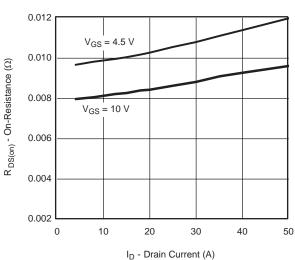
#### Notes:

- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

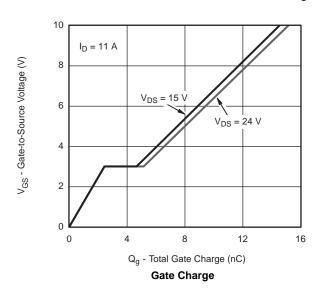
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

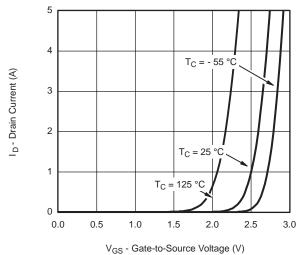




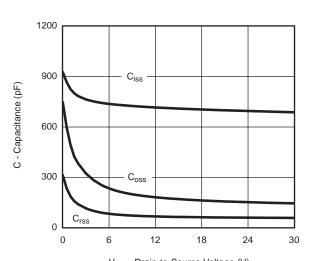




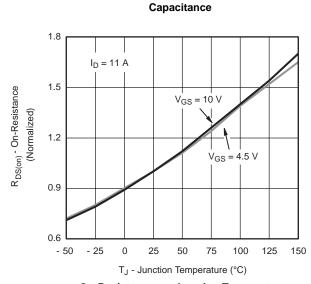




Transfer Characteristics

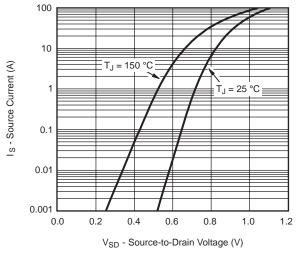


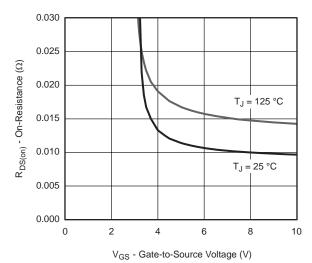
V<sub>DS</sub> - Drain-to-Source Voltage (V)



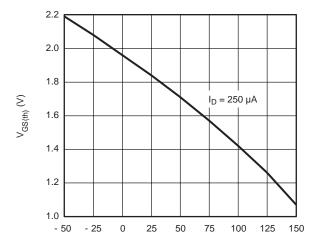
On-Resistance vs. Junction Temperature



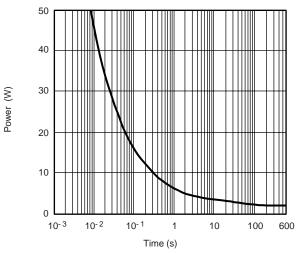




#### Source-Drain Diode Forward Voltage

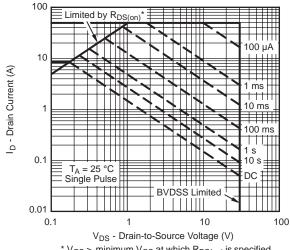


On-Resistance vs. Gate-to-Source Voltage



T<sub>J</sub> - Temperature (°C) **Threshold Voltage** 

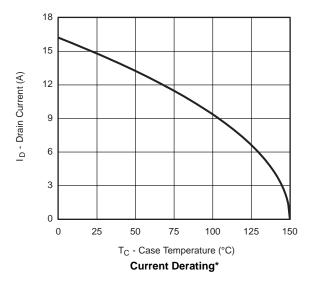
Single Pulse Power, Junction-to-Ambient

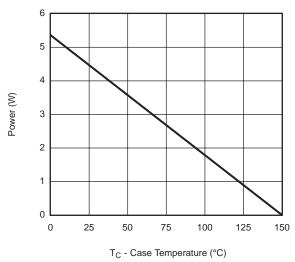


\*  $V_{GS} > \mbox{minimum } V_{GS}$  at which  $R_{DS(on)}$  is specified

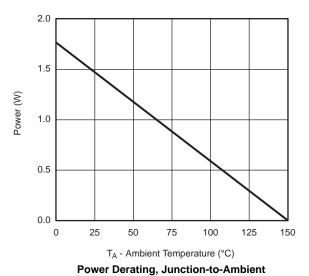
Safe Operating Area, Junction-to-Ambient





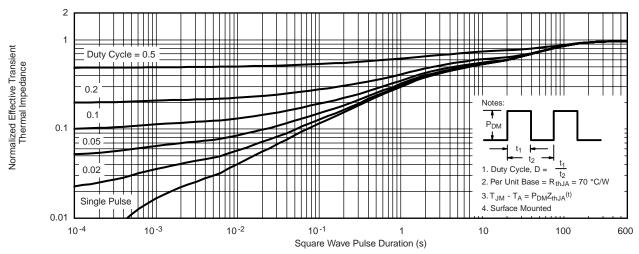


Power Derating, Junction-to-Foot

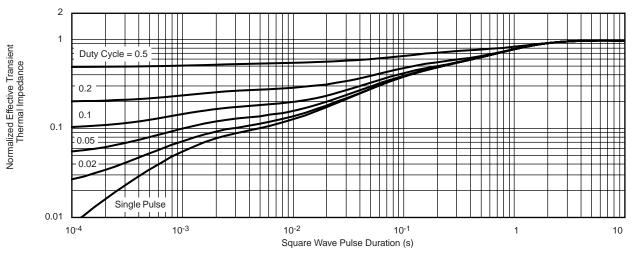


\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





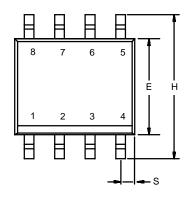
#### Normalized Thermal Transient Impedance, Junction-to-Ambient

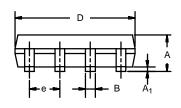


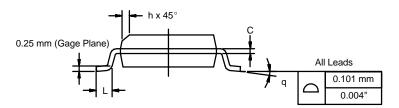
Normalized Thermal Transient Impedance, Junction-to-Foot



## SOIC (NARROW): 8-LEAD







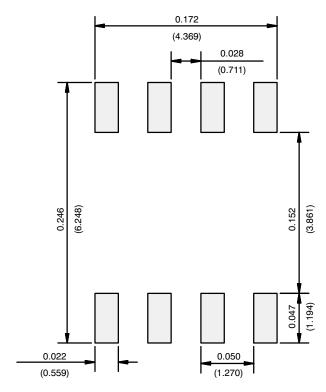
	MILLIM	IETERS	INCHES			
DIM	Min	Max	Min	Max		
Α	1.35	1.75	0.053	0.069		
A <sub>1</sub>	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
E	3.80	4.00	0.150	0.157		
е	1.27 BSC		0.050 BSC			
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
ECN: C-06527-Pey I 11-Sep-06						

ECN: C-06527-Rev. I, 11-Sep-06

DWG: 5498



### **RECOMMENDED MINIMUM PADS FOR SO-8**



Recommended Minimum Pads Dimensions in Inches/(mm)



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