



## N-channel Enhancement Mode Mosfet

## CX010N06

### DESCRIPTION

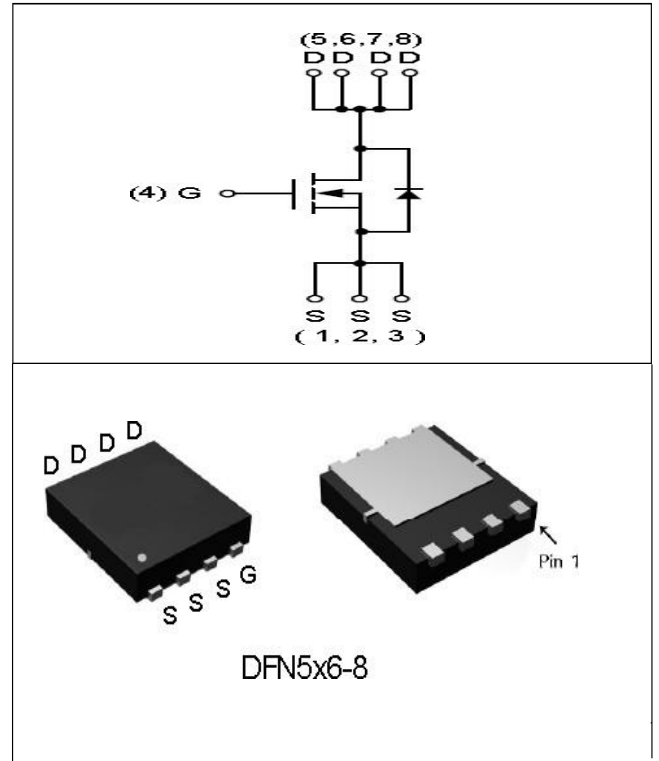
The CX010N06 is the high cell density trenched N-CH MOSFETs, which provide excellent  $R_{DS(on)}$  and GATE charge for most of the synchronous Rectification

### GENERAL FEATURES

- $V_{DS} = 95V$   
 $R_{DS(on)} = 6.1 m\Omega @ V_{GS} = 10V$
- Low  $R_{DS(on)}$  & FOM
- Extremely low switching loss
- Excellent reliability and uniformity
- Fast switching and soft recovery

### Application

- PD charger
- Switching voltage regulator
- DC-DC convertor
- Switched mode power supply



### ■ Absolute Maximum Ratings ( $T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit	
Drain-source Voltage	$V_{DS}$	95	V	
Gate-source Voltage	$V_{GS}$	$\pm 20$	V	
Drain Current	$I_D$	$T_C = 25^\circ C$	110	A
		$T_C = 100^\circ C$	80	
Pulsed Drain Current <sup>A</sup>	$I_{DM}$	280	A	
Total Power Dissipation	$P_D$	88	W	
Single Pulse Avalanche Energy <sup>B</sup>	EAS	78	mJ	
Thermal Resistance Junction-to-Case <sup>C</sup>	$R_{\theta JC}$	1.6	$^\circ C/W$	
Thermal resistance, junction-ambient <sup>4)</sup>	$R_{\theta JA}$	30	$^\circ C/W$	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55~+150	$^\circ C$	



### ELECTRICAL CHARACTERISTICS (T<sub>A</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =250μA	95	102		V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 95V V <sub>GS</sub> =0V	T <sub>J</sub> =25°C		1	μA
			T <sub>J</sub> =55°C		10	
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250μA	2	3	4	V
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> =40A		6.1	7.4	mΩ
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =50 A, V <sub>GS</sub> =0V		0.95	1.4	V
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =50V, V <sub>GS</sub> =0V, f=1MHZ		2270		pF
Output Capacitance	C <sub>oss</sub>			797		
Reverse Transfer Capacitance	C <sub>rss</sub>			36		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =50V, I <sub>b</sub> = 25A		32		nC
Gate-Source Charge	Q <sub>gs</sub>			11		
Gate-Drain Charge	Q <sub>gd</sub>			4.78		
Gate plateau voltage						
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =20A, V <sub>GS</sub> =0V, di <sub>S</sub> /dt=100A/uS		64		
Reverse Recovery Time	t <sub>rr</sub>			51.5		
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =50V, I <sub>b</sub> = 25A RG=2. 2 Ω		9.3		ns
Turn-on Rise Time	t <sub>r</sub>			34.8		
Turn-off Delay Time	t <sub>D(off)</sub>			24.6		
Turn-off fall Time	t <sub>f</sub>			71		

A. Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

B. T<sub>J</sub>=25°C, V<sub>DD</sub>=50V, L=0.5mH, R<sub>g</sub>=25 Ω I<sub>AS</sub>=20A.

C. R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJC</sub> is guaranteed by design, while R<sub>θJA</sub> is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



### Typical Performance Characteristics

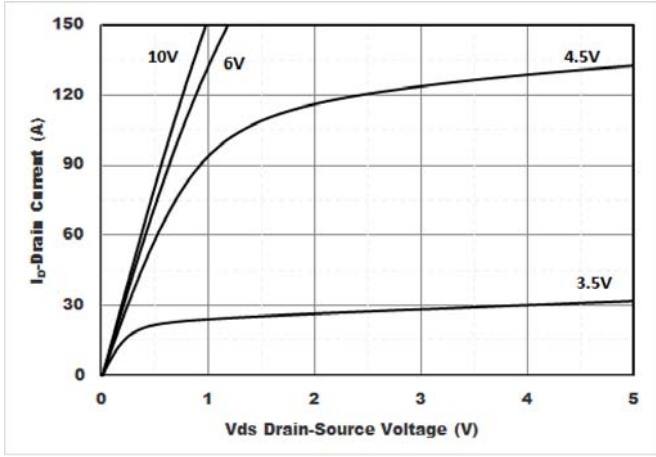


Figure1. Output Characteristics

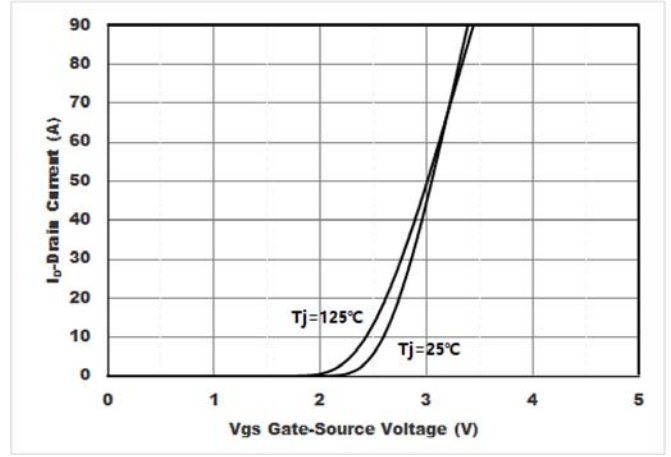


Figure2. Transfer Characteristics

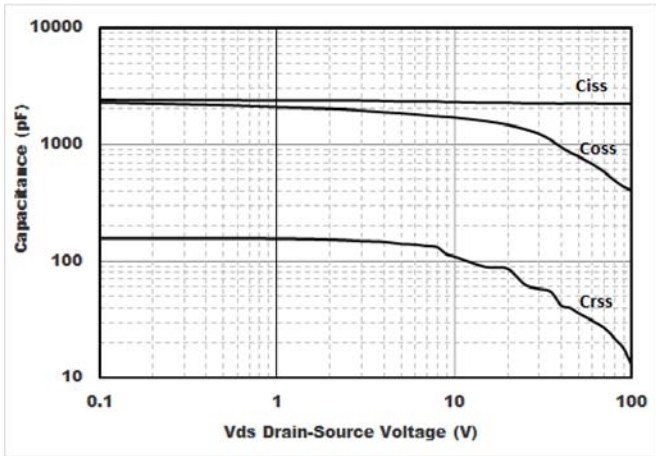


Figure3. Capacitance Characteristics

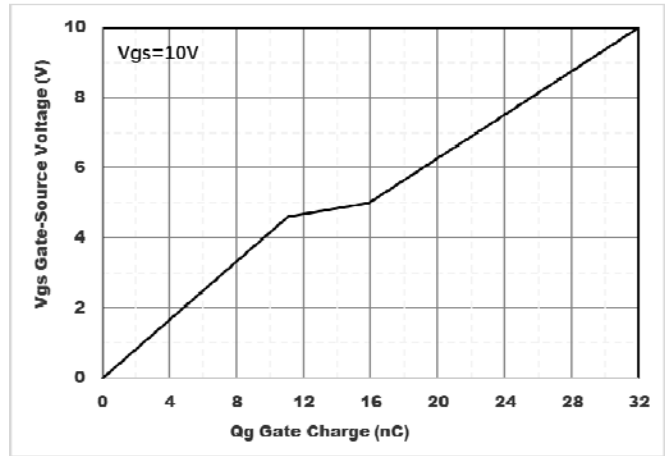


Figure4. Gate Charge

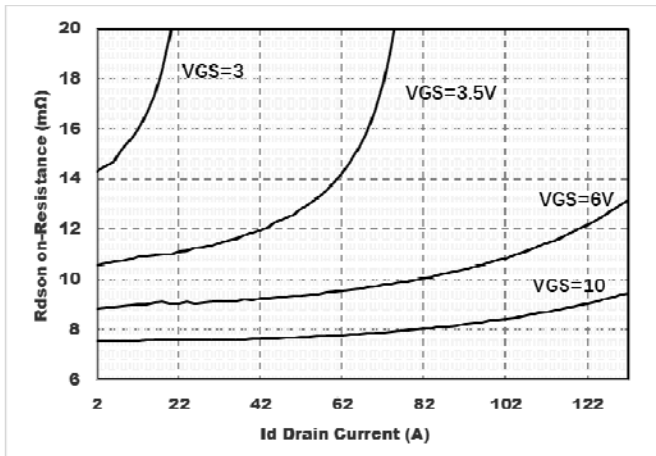


Figure5. : On-Resistance vs. Gate to Source Voltage

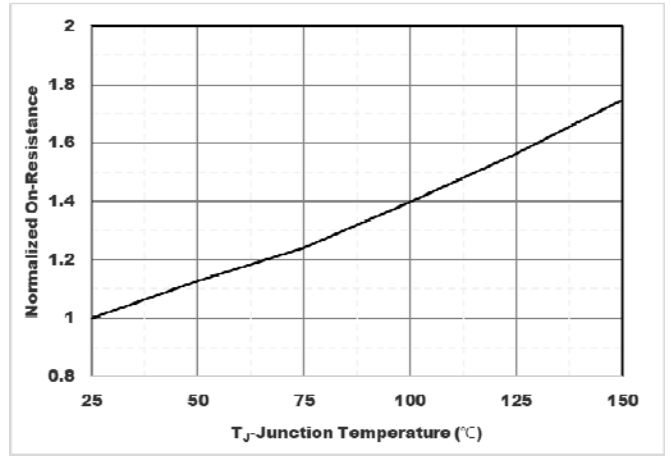


Figure6. Normalized On-Resistance

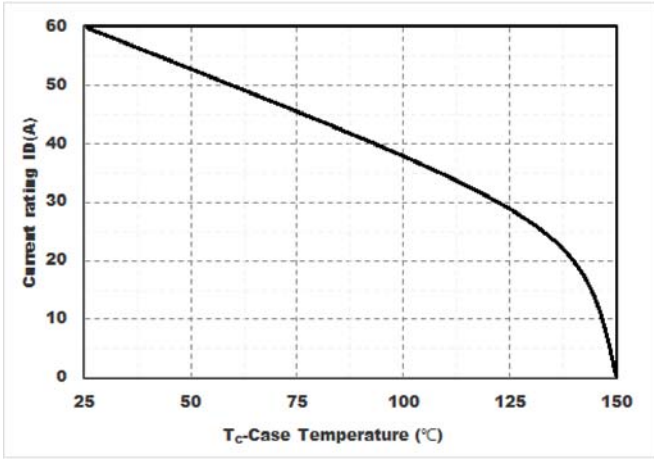


Figure7. Drain current

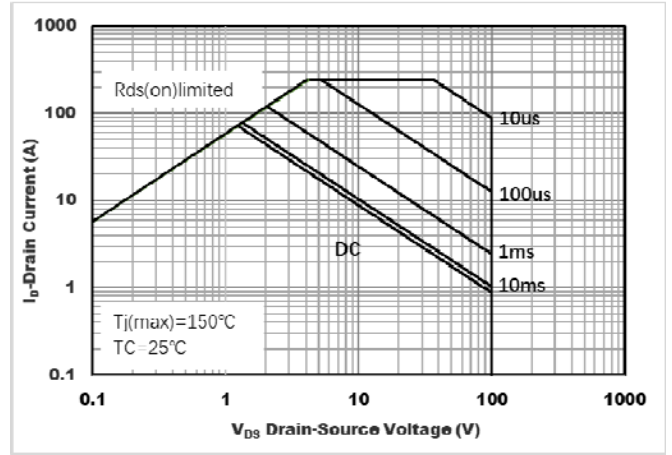


Figure8.Safe Operation Area

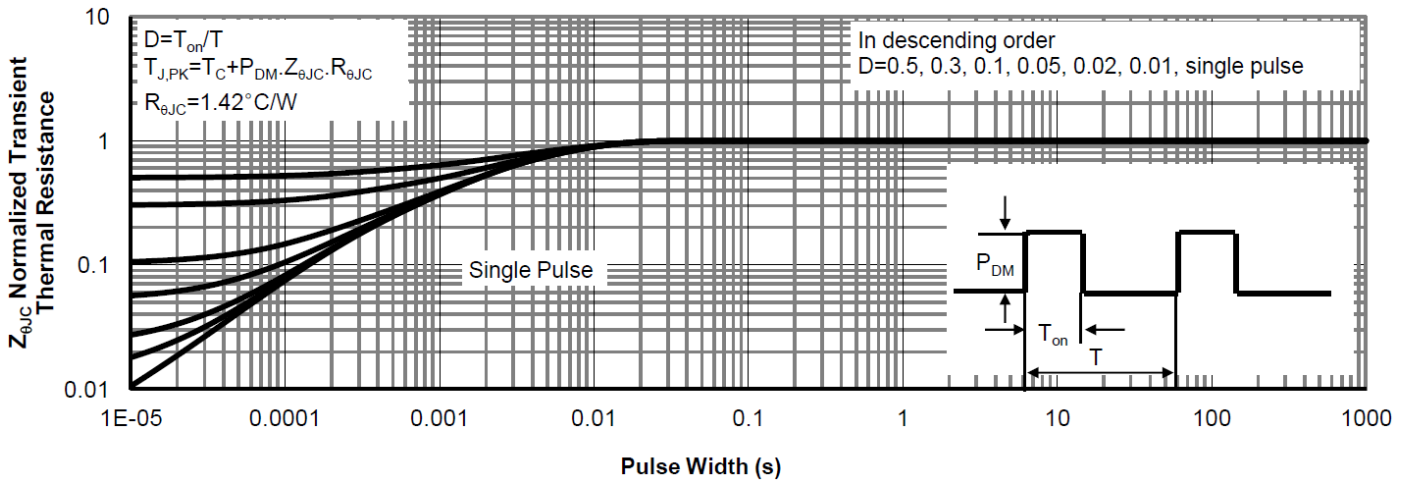


Figure9.Normalized Maximum Transient thermal impedance

### Test circuits and waveforms

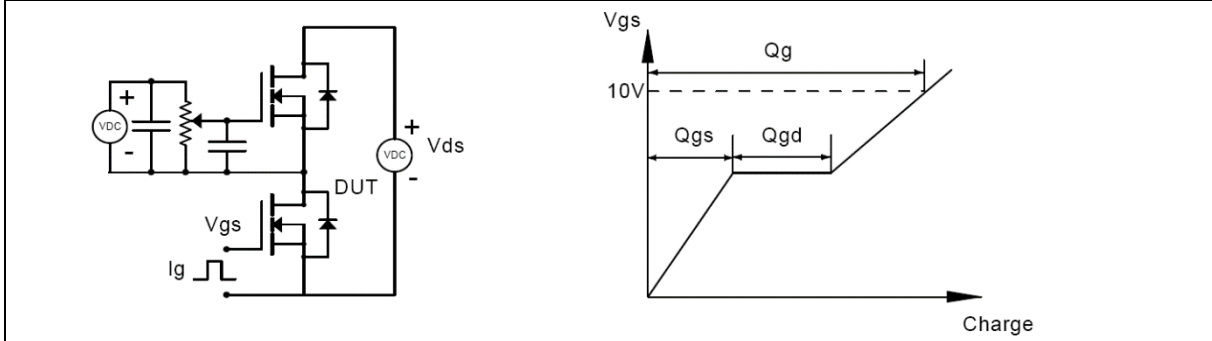


Figure 1. Gate charge test circuit & waveform

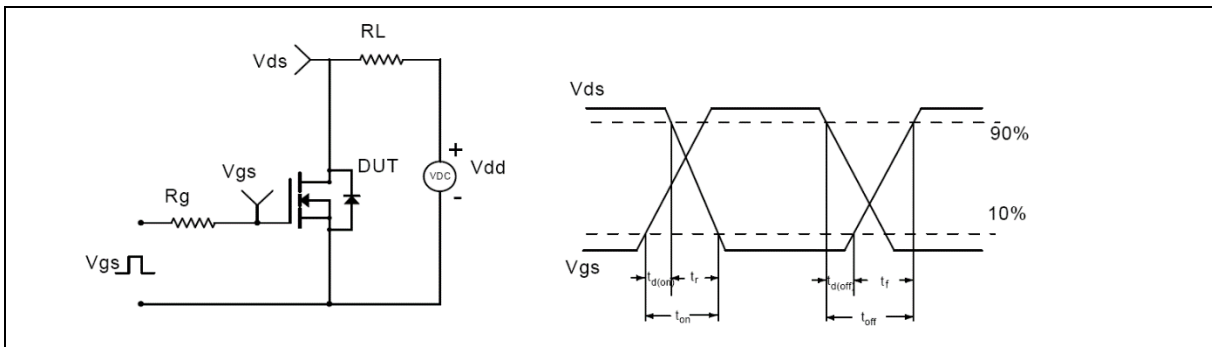


Figure 2. Switching time test circuit & waveforms

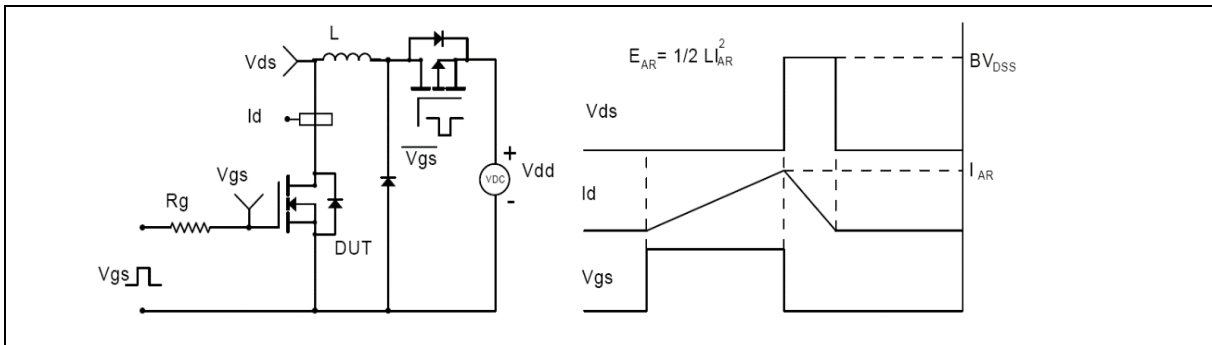


Figure 3. Unclamped inductive switching (UIS) test circuit & waveforms

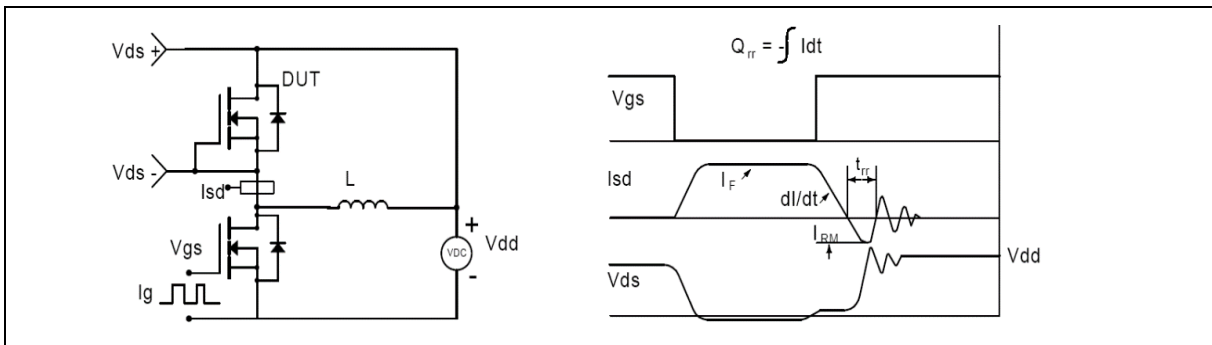
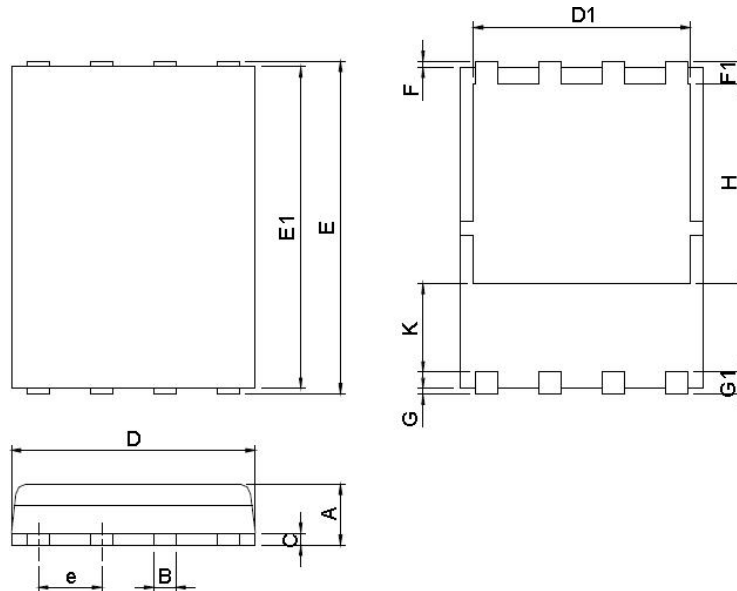


Figure 4. Diode reverse recovery test circuit & waveforms

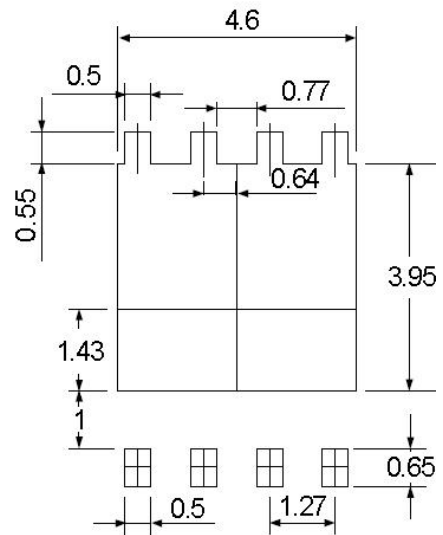
### Package Information

■ DFN5\*6-8 Package



DIMENSIONS	DFN5x6-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.90	1.20	0.035	0.047
B	0.3	0.51	0.012	0.020
C	0.19	0.25	0.007	0.010
D	4.80	5.30	0.189	0.209
D1	4.00	4.40	0.157	0.173
E	5.90	6.20	0.232	0.244
E1	5.50	5.80	0.217	0.228
e	1.27 BSC		0.050 BSC	
F	0.05	0.30	0.002	0.012
F1	0.35	0.75	0.014	0.030
G	0.05	0.30	0.002	0.012
G1	0.35	0.75	0.014	0.030
H	3.34	3.9	0.131	0.154
K	0.762	-	0.03	-

### RECOMMENDED LAND PATTERN



UNIT: mm

Note : 1.Dimension D, D1,D2 and E1 do not include mold flash or protrusions.  
Mold flash or protrusions shall not exceed 10 mil.