TVS0500 5V 平缓钳位浪涌保护器件

1 特性

- 保护特性符合针对工业信号线路的 2kV、42Ω IEC 61000-4-5 浪涌测试要求
- 43A、8/20μs 浪涌电流下的最大钳位电压为 9.2V
- 关断电压：5V
- 4mm^2 小型封装尺寸
- 在 125°C 时，可耐受超过 5,000 次的 35A 8/20μs 浪涌电流的重复冲击
- 强大的浪涌保护：
  - IEC61000-4-5 (8/20μs)：43A
  - IEC61643-321 (10/1000μs)：22A
- 低泄漏电流
  - 27°C 下为 70pA（典型值）
  - 85°C 下为 6.5nA（典型值）
- 低电容：155pF
- 集成 4 级 IEC 61000-4-2 ESD 保护

2 应用

- 工业传感器
- PLC I/O 模块
- 5V 电源线路
- 电器
- 医疗设备
- 智能仪表

3 说明

TVS0500 可将高达 43A 的 IEC 61000-4-5 故障电流进行可靠分流，以保护系统免受高功率瞬态冲击或雷击。该器件为满足常见的工业信号线路 EMC 要求提供了解决方案，可通过 42Ω 电阻进行耦合的方式承受最高 2kV IEC 61000-4-5 开路电压。TVS0500 使用独特的反馈机制确保在故障期间发挥精确的平缓钳位能力，保证系统接触电压低于 10V。精确的电压调节允许设计人员放心地选择具有较低电压容差的系统组件，不但减少了系统成本和复杂度，而且不损害可靠性。

此外，TVS0500 还采用 2mm × 2mm 小型 SON 封装，非常适用于空间受限 应用，与业内标准的 SMA 和 SMB 封装相比，尺寸减小了 70%。极低的器件泄露电流和电容确保最大限度地降低了对受保护线路的影响。为了确保在产品的整个寿命期间提供可靠保护，TI 在高温环境下对 TVS0500 进行了 5000 次重复浪涌冲击测试，但器件性能未发生任何变化。

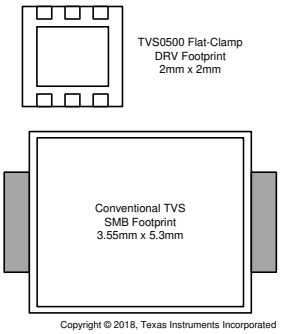
TVS0500 是 TI 的平缓钳位系列浪涌器件中的一款产品。有关该系列其他器件的更多信息，请参阅*器件比较表*

器件信息(1)

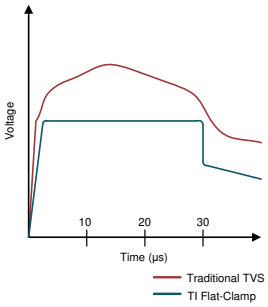
器件型号	封装	封装尺寸（标称值）
TVS0500	SON (6)	2.00mm × 2.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

封装比较



对 8/20μs 浪涌事件的电压钳位响应



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4 修订历史记录

Changes from Revision B (February 2018) to Revision C **Page**

- Fixed grammar error in the *Reliability Testing* section ... 9

Changes from Revision A (February 2018) to Revision B **Page**

- Changed DC Breakdown Current MAX from 100 to 50 in the Specifications *Absolute Maximum Ratings* table ... 5
- Changed Break-down Voltage MIN from 7.6 to 7.5 and MAX from 8.2 to 8.4 in the Specifications *Electrical Characteristics* table ... 5

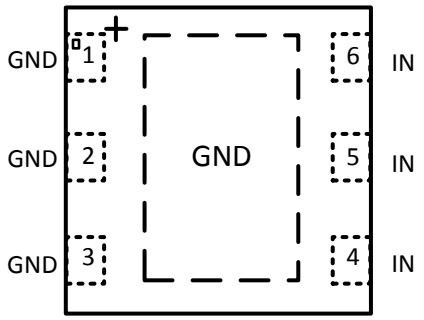
Changes from Original (December 2017) to Revision A **Page**

5 Device Comparison Table

Device	V_{rwm}	V_{clamp} at I_{pp}	I_{pp} (8/20 µs)	V_{rwm} leakage (nA)	Package Options	Polarity
TVS0500	5	9.2	43	0.07	SON	Unidirectional
TVS1400	14	18.4	43	2	SON	Unidirectional
TVS1800	18	22.8	40	0.5	SON	Unidirectional
TVS2200	22	27.7	40	3.2	SON	Unidirectional
TVS2700	27	32.5	40	1.7	SON	Unidirectional
TVS3300	33	38	35	19	WCSP, SON	Unidirectional

6 Pin Configuration and Functions

DRV Package
6-Pin SON
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	No.		
IN	4, 5, 6	I	ESD and surge protected channel
GND	1, 2, 3, exposed thermal pad	GND	Ground

7 Specifications

7.1 Absolute Maximum Ratings

T_A = 27℃ (unless otherwise noted)(1)

		MIN	MAX	UNIT
Maximum Surge	IEC 61000-4-5 Current (8/20 µs)		43	A
	IEC 61000-4-5 Power (8/20 µs)		400	W
	IEC 61643-321 Current (10/1000 µs)		20	A
	IEC 61643-321 Power (10/1000 µs)		180	W
Maximum Forward Surge	IEC 61000-4-5 Current (8/20 µs)		50	A
	IEC 61000-4-5 Power (8/20 µs)		80	W
	IEC 61643-321 Current (10/1000 µs)		23	A
	IEC 61643-321 Power (10/1000 µs)		60	W
EFT	IEC 61000-4-4 EFT Protection		80	A
I_{BR}	DC Breakdown Current		50	mA
I_F	DC Forward Current		500	mA
T_A	Ambient Operating Temperature	-40	125	°C
T_{stg}	Storage Temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings - JEDEC

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 ESD Ratings - IEC

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	±24	kV
		IEC 61000-4-2 air-gap discharge	±30	

7.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
V_{RWM}	Reverse Stand-off Voltage		5		V

7.5 Thermal Information

THERMAL METRIC(1)		TVS0500 DRV (SON) 6 PINS	UNIT
R_{qJA}	Junction-to-ambient thermal resistance	70.4	°C/W
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	73.7	°C/W
R_{qJB}	Junction-to-board thermal resistance	40	°C/W
Y_{JT}	Junction-to-top characterization parameter	2.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

Thermal Information (continued)

THERMAL METRIC(1)		TVS0500 DRV (SON) 6 PINS	UNIT
Y_{JB}	Junction-to-board characterization parameter	40.3	°C/W
$R_{qJC(bot)}$	Junction-to-case (bottom) thermal resistance	11	°C/W

7.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LEAK}	Leakage Current	Measured at $V_{IN} = V_{RWM}$, T_A = 27°C		0.07	5.5	nA
		Measured at $V_{IN} = V_{RWM}$, T_A = 85°C		6.5	220	nA
		Measured at $V_{IN} = V_{RWM}$, T_A = 105°C		38	755	nA
V_F	Forward Voltage	I_{IN} = 1 mA from GND to IO	0.25	0.5	0.65	V
V_{BR}	Break-down Voltage	I_{IN} = 1 mA from IO to GND	7.5	7.9	8.4	V
V_{FCLAMP}	Forward Clamp Voltage	35 A IEC 61000-4-5 Surge (8/20 µs) from GND to IO, 27°C		2	5	V
V_{CLAMP}	Clamp Voltage	24 A IEC 61000-4-5 Surge (8/20 µs) from IO to GND, V_{IN} = 0 V before surge, 27°C		8.6	8.8	V
		43 A IEC 61000-4-5 Surge (8/20 µs) from IO to GND, V_{IN} = 0 V before surge, 27°C		9.2	9.5	V
		35 A IEC 61000-4-5 Surge (8/20 µs) from IO to GND, $V_{IN} = V_{RWM}$ before surge, T_A = 125°C		9.2	9.5	V
R_{DYN}	8/20 µs surge dynamic resistance	Calculated from V_{CLAMP} at .5*I_{pp} and I_{pp} surge current levels, 27°C		30	50	mΩ
C_{IN}	Input pin capacitance	V_{IN} = 5 V, f = 1 MHz, 30 mV_{pp}, IO to GND		155		pF
SR	Maximum Slew Rate	0-V_{RWM} rising edge, sweep rise time and measure slew rate when I_{PEAK} = 1 mA, 27°C		2.5		V/µs
		0-V_{RWM} rising edge, sweep rise time and measure slew rate when I_{PEAK} = 1 mA, 105°C		0.7		V/µs

7.7 Typical Characteristics

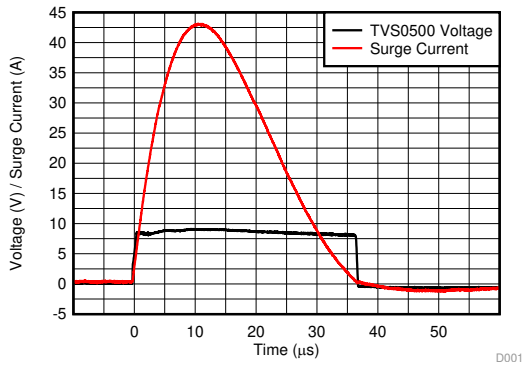


图 1. 8/20 µs Surge Response at 43 A

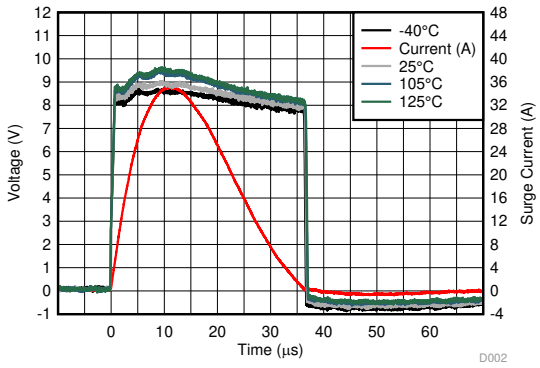
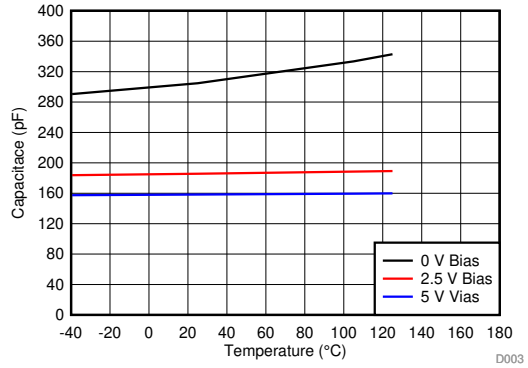


图 2. 8/20 µs Surge Response at 35 A Across Temperature



f = 1 MHz, 30 mVpp, IO to GND

图 3. Capacitance vs Temperature Across Bias

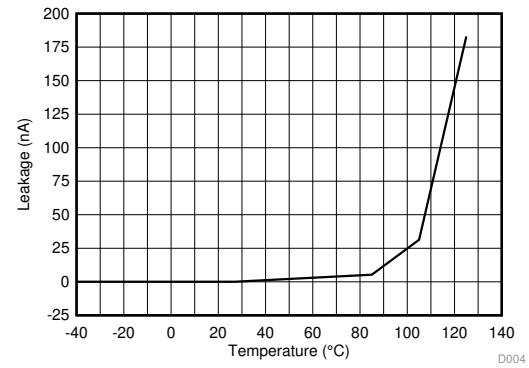


图 4. Leakage Current vs Temperature at 5 V

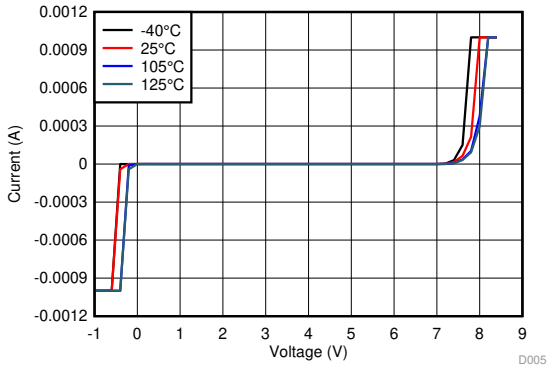


图 5. I/V Curve Across Temperature

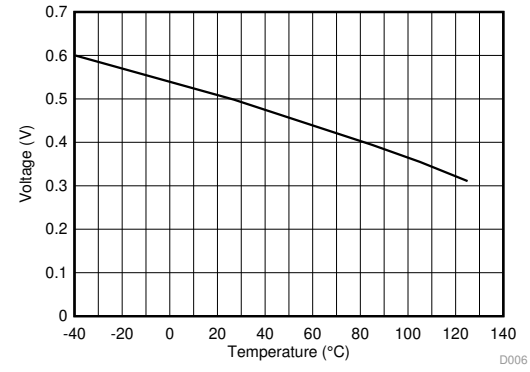


图 6. Forward Voltage vs Temperature

Typical Characteristics (接下页)

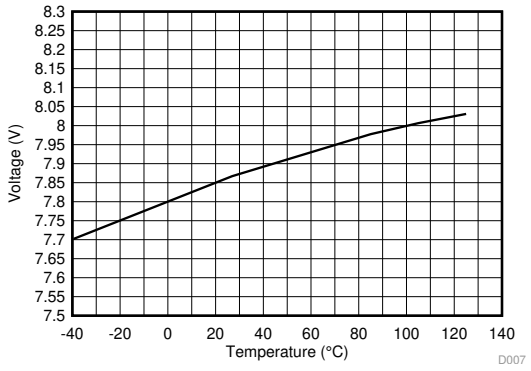


图 7. Breakdown Voltage (1 mA) vs Temperature

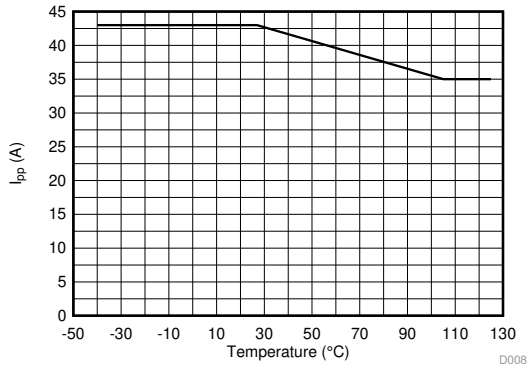


图 8. Max Surge Current (8/20 µs) vs Temperature

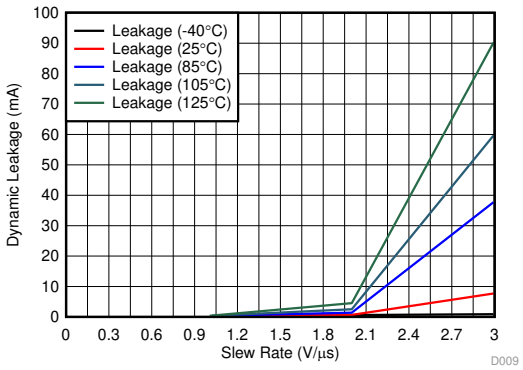


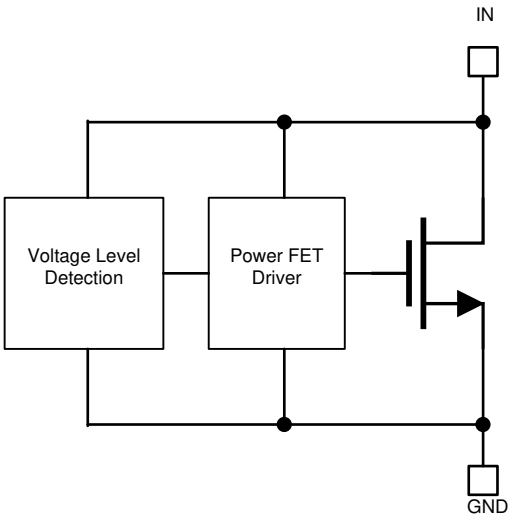
图 9. Dynamic Leakage vs Signal Slew Rate across Temperature

8 Detailed Description

8.1 Overview

The TVS0500 is a precision clamp with a low, flat clamping voltage during transient overvoltage events like surge and protecting the system with zero voltage overshoot.

8.2 Functional Block Diagram



8.3 Feature Description

The TVS0500 is a precision clamp that handles 43 A of IEC 61000-4-5 8/20 µs surge pulse. The flat clamping feature helps keep the clamping voltage very low to keep the downstream circuits from being stressed. The flat clamping feature can also help end-equipment designers save cost by opening up the possibility to use lower-cost, lower voltage tolerant downstream ICs. The TVS0500 has minimal leakage under the standoff voltage of 5 V, making it an ideal candidate for applications where low leakage and power dissipation is a necessity. IEC 61000-4-2 and IEC 61000-4-4 ratings make it a robust protection solution for ESD and EFT events. Wide ambient temperature range of –40°C to +125°C a good candidate for most applications. Compact packages enable it to be used in small devices and save board area.

8.4 Reliability Testing

To ensure device reliability, the TVS0500 is characterized against 5000 repetitive pulses of 35 A IEC 61000-4-5 8/20 µs surge pulses at 125°C. The test is performed with less than 10 seconds between each pulse at high temperature to simulate worst case scenarios for fault regulation. After each surge pulse, the TVS0500 clamping voltage, breakdown voltage, and leakage are recorded to ensure that there is no variation or performance degradation. By ensuring robust, reliable, high temperature protection, the TVS0500 enables fault protection in applications that must withstand years of continuous operation with no performance change.

8.5 Device Functional Modes

8.5.1 Protection Specifications

The TVS0500 is specified according to both the IEC 61000-4-5 and IEC 61643-321 standards. This enables usage in systems regardless of which standard is required in relevant product standards or best matches measured fault conditions. The IEC 61000-4-5 standards requires protection against a pulse with a rise time of 8 µs and a half length of 20 µs, while the IEC 61643-321 standard requires protection against a much longer pulse with a rise time of 10 µs and a half length of 1000 µs.

Device Functional Modes (接下页)

The positive and negative surges are imposed to the TVS0500 by a combinational waveform generator (CWG) with a 2-Ω coupling resistor at different peak voltage levels. For powered on transient tests that need power supply bias, inductances are usually used to decouple the transient stress and protect the power supply. The TVS0500 is post tested by assuring that there is no shift in device breakdown or leakage at V_{rwm}.

In addition, the TVS0500 has been tested according to IEC 61000-4-5 to pass a ±2 kV surge test through a 42-Ω coupling resistor and a 0.5 µF capacitor. This test is a common test requirement for industrial signal I/O lines and the TVS0500 will serve an ideal protection solution for applications with that requirement.

The TVS0500 allow integrates IEC 61000-4-2 level 4 ESD Protection and 80 A of IEC 61000-4-4 EFT Protection. These combine to ensure that the device can protect against most transient conditions regardless of length or type.

For more information on TI's test methods for Surge, ESD, and EFT testing, reference TI's IEC 61000-4-x Testing Application Note

8.5.2 Minimal Derating

Unlike traditional diodes the TVS0500 has very little derating of max power dissipation and ensures robust performance up to 125°C, shown in 图 8. Traditional TVS diodes lose up to 50% of their current carrying capability when at high temperatures, so a surge pulse above 85°C ambient can cause failures that are not seen at room temperature. The TVS0500 prevents this and ensures that you will see the same level of protection regardless of temperature.

8.5.3 Transient Performance

During large transient swings, the TVS0500 will begin clamping the input signal to protect downstream conditions. While this prevents damage during fault conditions, it can cause leakage when the intended input signal has a fast slew rate. In order to keep power dissipation low and remove the chance of signal distortion, it is recommended to keep the slew rate of any input signal on the TVS0500 below 2.5 V/µs at room temperature and below 0.7 V/µs at 125°C shown in 图 9. Faster slew rates will cause the device to clamp the input signal and draw current through the device for a few microseconds, increasing the rise time of the signal. This will not cause any harm to the system or to the device, however if the fast input voltage swings occur regularly it can cause device overheating.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TVS0500 can be used to protect any power, analog, or digital signal from transient fault conditions caused by the environment or other electrical components.

9.2 Typical Application

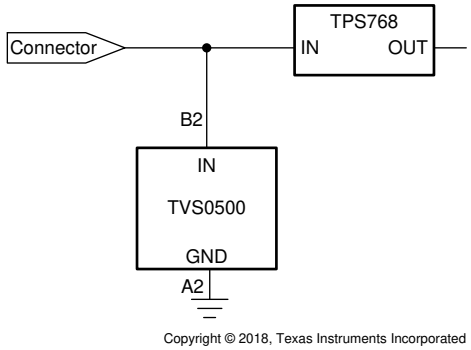


图 10. TVS0500 Application Schematic

9.2.1 Design Requirements

A typical operation for the TVS0500 would be protecting a nominal 5 V input to an LDO similar to 图 10. In this example, the TVS0500 is protecting the input to a TPS768, a standard 1 A LDO with an input voltage range of 2.7 V to 10 V. Without any input protection, if a surge event is caused by lightning, coupling, ringing, or any other fault condition this input voltage will rise to hundreds of volts for multiple microseconds, violating the absolute maximum input voltage and harming the device. An ideal surge protection diode will maximize the useable voltage range while still clamping at a safe level for the system, TI's Flat-Clamp technology provides the best protection solution.

9.2.2 Detailed Design Procedure

If the TVS0500 is in place to protect the device, during a surge event the voltage will rise to the breakdown of the diode at 7.9 V, and then the TVS0500 will turn on, shunting the surge current to ground. With the low dynamic resistance of the TVS0500, large amounts of surge current will have minimal impact on the clamping voltage. The dynamic resistance of the TVS0500 is around 30 mΩ, which means 30 A of surge current will cause a voltage raise of 30 A × 30 mΩ = 0.9 V. Because the device turns on at 7.9 V, this means the LDO input will be exposed to a maximum of 7.9 V + 0.9 V = 8.8 V during surge pulses, well within the absolute maximum input voltage. This ensures robust protection of your circuit.

The small size of the device also improves fault protection by lowering the effect of fault current coupling onto neighboring traces. The small form factor of the TVS0500 allows the device to be placed extremely close to the input connector, lowering the length of the path fault current will take through the system compared to larger protection solutions.

Finally, the low leakage of the TVS0500 will have low input power losses. At 5 V, the device will see typical 70 pA leakage for a constant power dissipation of less than 1 nW, a negligible quantity that will not effect overall efficiency metrics or add heating concerns.

Typical Application (接下页)

9.2.3 Configuration Options

The TVS0500 can be used in either unidirectional or bidirectional configuration. 图 10 shows unidirectional usage to protect an input. By placing two TVS0500's in series with reverse orientation, bidirectional operation can be used, allowing a working voltage of ±5 V. TVS0500 operation in bidirectional will be similar to unidirectional operation, with a minor increase in breakdown voltage and clamping voltage. The TVS3300 bidirectional performance has been characterized in the TVS3300 Configurations Characterization. While the TVS0500 in bidirectional configuration has not specifically been characterized, it will have similar relative changes to the TVS3300 in bidirectional configuration.

10 Power Supply Recommendations

The TVS0500 is a clamping device so there is no need to power it. To ensure the device functions properly do not violate the recommended V_{IN} voltage range (0 V to 5 V) .

11 Layout

11.1 Layout Guidelines

The optimum placement is close to the connector. EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures. The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.

Route the protected traces straight.

Eliminate any sharp corners on the protected traces between the TVS0500 and the connector by using rounded corners with the largest radii possible. Electric fields tend to build up on corners, increasing EMI coupling.

11.2 Layout Example

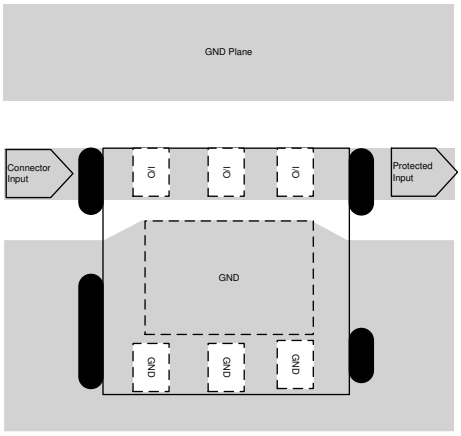


图 11. TVS0500 Layout

12 器件和文档支持

12.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com. 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 社区资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 商标

E2E is a trademark of Texas Instruments.

12.4 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TVS0500DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1HRH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

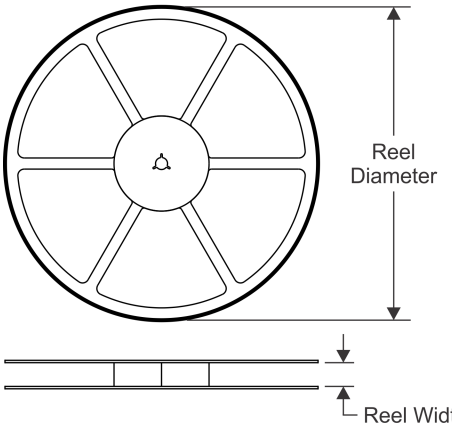
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

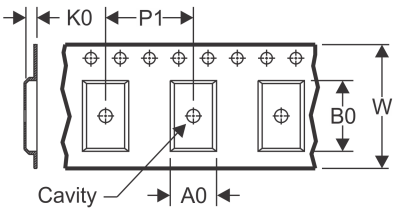
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

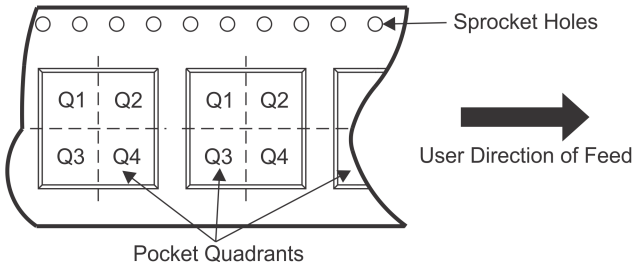


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

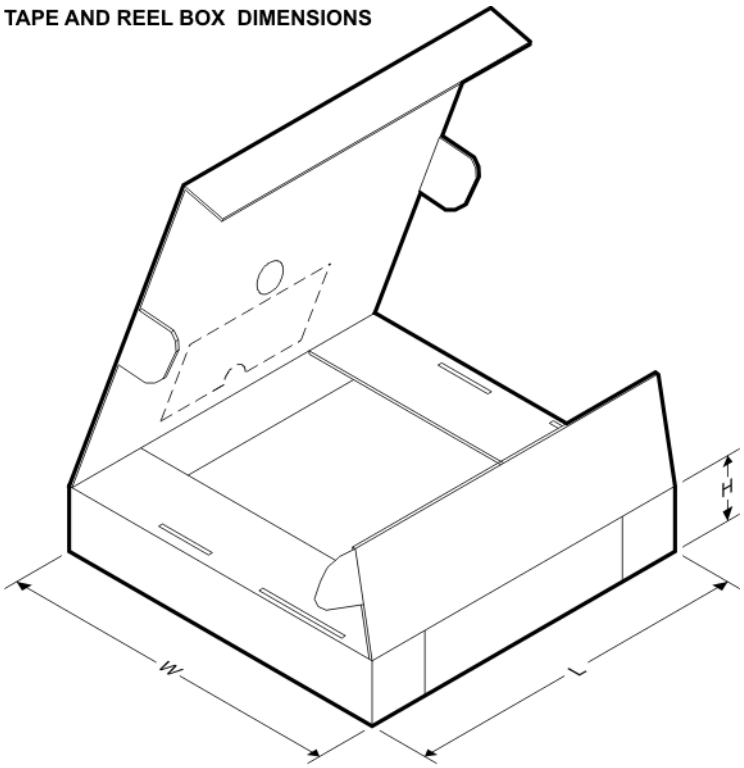
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TVS0500DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

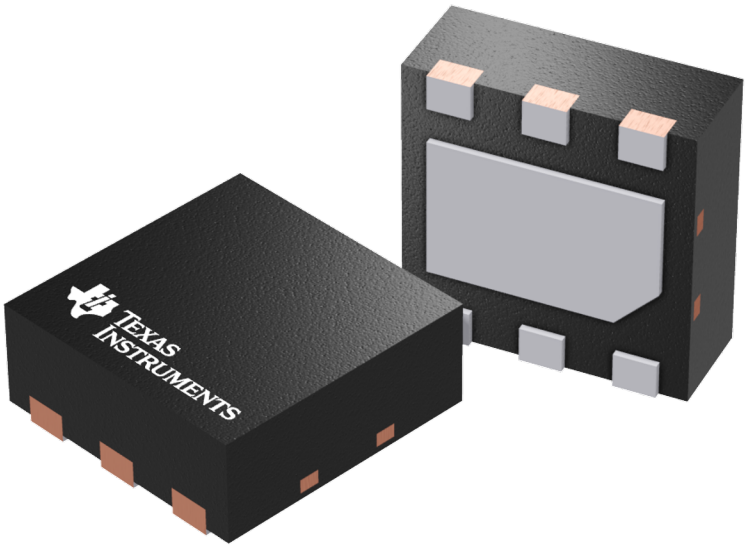


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TVS0500DRVR	WSON	DRV	6	3000	210.0	185.0	35.0

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



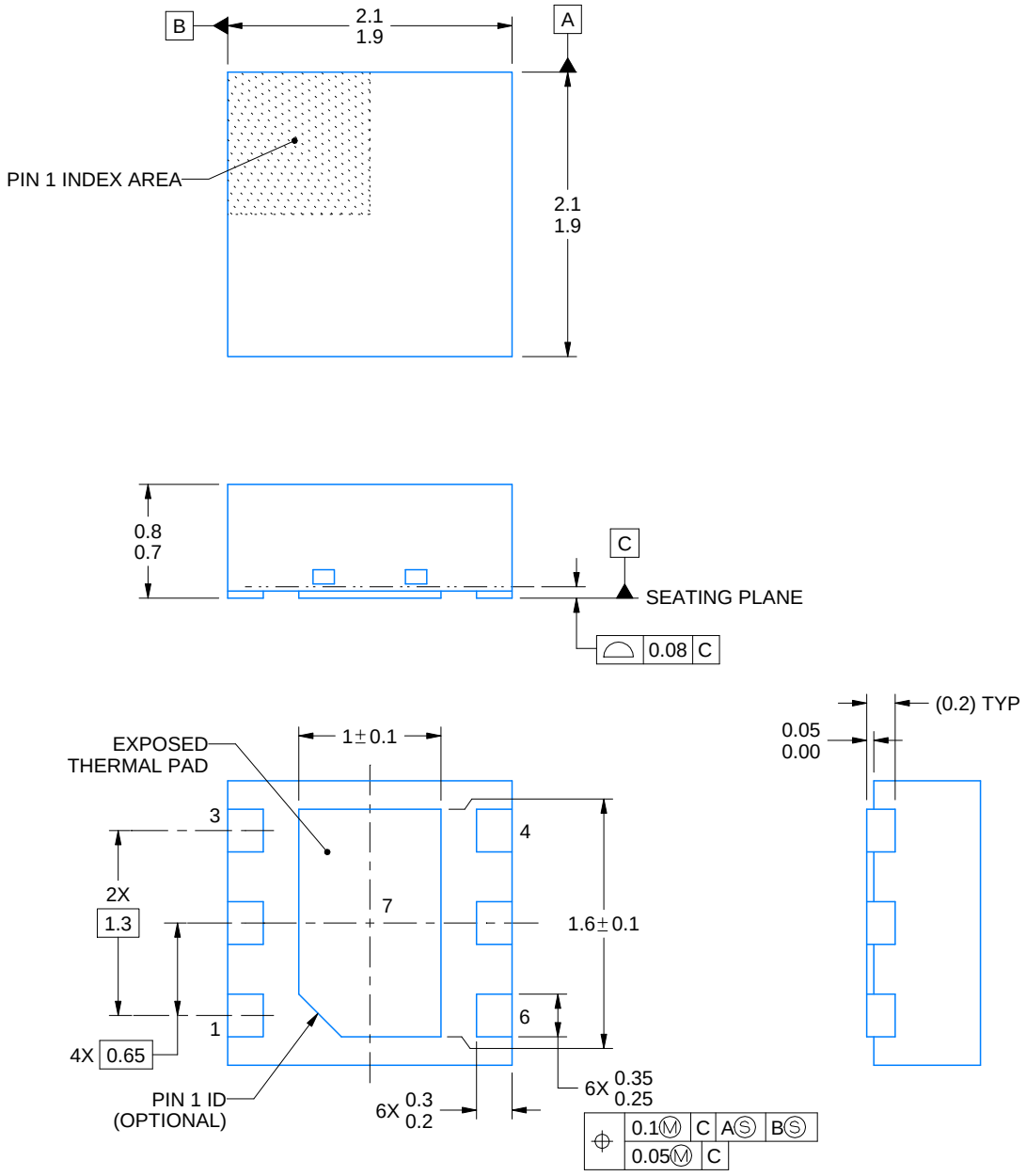
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DRV0006A

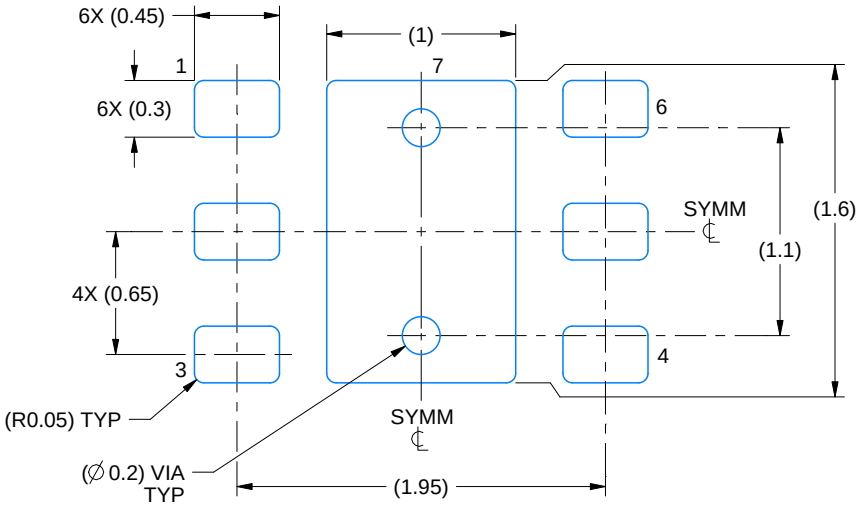
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

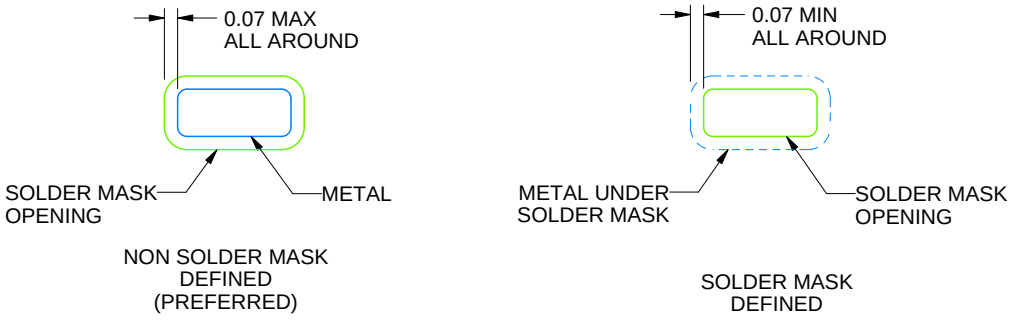


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS

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NOTES: (continued)

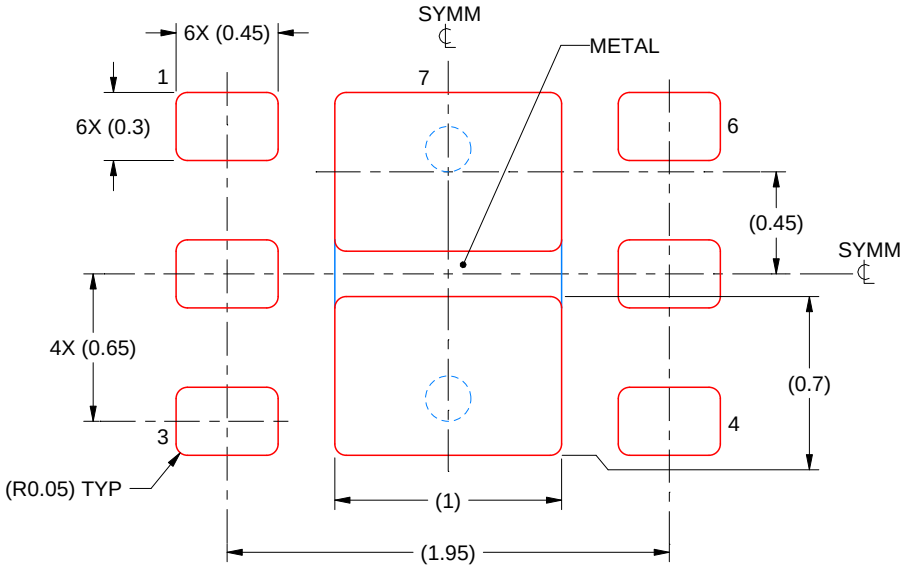
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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