Valens

VS100 Product Family Datasheet

VS100TX, VS100RX – HDBaseT™ Transmitter / Receiver

Ver 3.06

Valens First in HDBaseT

Valens Semiconductor Ltd.
8 Hanagar Street, POB 7152, Hod Hasharon 45240 Israel
Tel: +972-9-7626900, Fax: +972-9-7626901
www.valens-semi.com

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Revision History

Revision	Date	Author	Description
1.0	Oct, 2008	Micha Risling	First datasheet version.
1.1	July, 2009	Micha Risling	Updated datasheet.
1.2	Aug, 2009	Micha Risling	Minor fixes.
1.3 – 1.5	Dec, 2009	Ori Kaplan	Minor fixes.
1.6	Mar, 2010	Ori Kaplan	PDIF correction.
1.7	Apr, 2010	Ori Kaplan	Power consumption update.
1.8	Jun, 2010	Ori Kaplan	GPIO, PDIF and Power consumption corrections.
1.9	June 2011	Alon Benzaray	• Add IR and RS232. • Formatting, typos, mode of operations.
2.0	February, 2012	Nadav Banet Ariel Marcus	• Add “Operation Mode Status” and “Fast Active” option. • Operation Mode Change diagram. Update GPIO table. • GPIO selection method for Manual Operation Mode. • Add CIR and UART support in LPPF. • Add Marking Diagrams.
2.1	Apr 2012	Danny Raz	• Update electrical characteristics. • Update storage temperature. • Add chip marking diagrams.
2.2	Apr 2012	Danny Raz	• New and revised operational modes chapter. • New and revised PDIF chapter + Table 7. • Misc improvements (tech writing).
2.3	Aug 2012	Danny Raz	• Added setup/hold time for SPI input signal. • Reset activation diagram and hold time requirement.
2.4	Dec 2012	Danny Raz	• Technical writer revised • Range capability revised in feature section • Add Remark on PDIF 1,2 reserved in pin description table
2.5	Feb 2013	Danny Raz	• JTAG restricted for fab testing only
2.6	Aug 2013	Danny Raz	• Added LVDS HDBaseT max ratings (common mode and differential voltage)
2.7	Oct 2013	Danny Raz	• New section (previously in separate ANs): Clock oscillator
2.8	Mar 2014	Danny Raz	• Revised description of WAKEUP_IN behavior. • Table 3 correction. Partners in Long reach / ACTIVE causes link to follow long reach.

2.9	Apr 2014	Danny Raz	• Product ordering code changed to VS100RX-A1. Added power consumption at partner detect state. • Fixed tables 16,17 VL TMDS DC definition.
2.91	May 2014	Daniel Shwartzberg	• Added pull-down on MII_Tx_ERR_GPIO input when not in use • Added 4K2K power consumption
2.92	June 2014	Daniel Shwartzberg	• Updated current consumption tables
2.93	June 2014	Daniel Shwartzberg	• Updated TMDS DC specification tables
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2.95	November 2014	Daniel Shwartzberg	• Updated modulated / unmodulated CIR details in section 3.7.2 • Clarified CIR / RS232 Update Parameter configuration for both Active and Low Power modes in section 3.7.2
2.96	December 2014	Daniel Shwartzberg	• Fixed typo in first row of table 12 (changed 36bpp to 24bpp)
2.97	February 2015	Daniel Shwartzberg	• Clarifications in pin configurations (tables 8 and 9)
2.98	April 2015	Daniel Shwartzberg	• Updated Operating Temperature range (tables 10 and 11)
2.99	August 2015	Daniel Shwartzberg	• Updated RX package drawing (figure 21) – adds minimum value for dimension A
3.00	October 2015	Daniel Shwartzberg	• Added note that HDCP 2.2 is supported (section 3.2.2)
3.01	March 2016	Daniel Shwartzberg	• Added details on 4K/60/4:2:0 support from HDMI 2.0 specification • Updated $T_{rst\text{-}hd}$ in table 20 • Added wake-on-RS232 details
3.02	January 2017	Daniel Shwartzberg	• Do not use 25MHz MII clock outputs for system purposes (section 3.3.1)
3.03	May 2017	Daniel Shwartzberg	• Additional clarifications on MII and RMII clocking
3.04	June 2017	Daniel Shwartzberg	• Added ESD ratings
3.05	March 2018	Yaki Sfadya	• Additional clarification for fallback only in Automatic mode selection • VS100RX mechanical drawing updated for better visibility • Corrected RESET_IN hold time on TX to 1 us
3.06	August 2018	Yaki Sfadya	• Removed reference to AN1020

Contact Information

Valens Semiconductor Ltd.

8 Hanagar St. • POB 7152

Hod Hasharon 45240 • Israel

Tel: +972-9-762-6900 • Fax: +972-9-762-6901

info@valens-semi.com • www.valens-semi.com

Glossary

Term	Definition
AFE	Analog Front End
AV	Audio Video/Visual
BER	Bit Error Rate
CE	Consumer Electronic
CEC	Consumer Electronic Control
DDC	Display Data Channel
DVI	Digital Visual Interface
EEPROM	Electronically Erasable Programmable Read-only Memory
GPIO	General Purpose Input Output
HD	High Definition
HDMI	High Definition Multimedia Interface
HLIC	HDBaseT Link Internal Controls
HPD	Hot Plug Detect
I^2C	Inter IC
MAC	Media Access Control Layer
MII	Media Independent Interface
PD	Powered Device
PHY	Physical Layer
PoE	Power Over Ethernet
PRBS	Pseudo Random Bit Stream
PSE	Power Sourcing Equipment
RMII	Reduced Media Independent Interface
SERDES	Serializer DeSerializer
STB	Set-Top Box
SMI	Serial Management Interface
TMDS	Transition Minimized Differential Signaling
UART	Universal Asynchronous Receive Transmit
LPPF	Low Power Partial Functionality

Contents

1 Overview

This section includes the following topics:

- What is the VS100 Family?
- Technology Overview
- HDBaseT Channel Terminology

1.1 What is the VS100 Family?

Valens Semiconductor developed the VS100 product family to enable high quality, wired connectivity of uncompressed high-definition (HD), HDMI 1.4 compatible, multimedia content (audio and video) together with 100Mbps Ethernet data. The VS100 product family is based on the HDBaseT™ technology. This innovative patent-pending technology is the first to enable simplified, long-distance wired connectivity of uncompressed HD multimedia content over a single standard 100m/328ft LAN cable.

The VS100 product family consists of two devices:

- **VS100TX (HDBaseT Transmitter):** A source-side implementation designed for use inside DVDs, STBs, and other HD source equipment.
- **VS100RX (HDBaseT Receiver):** A sink-side implementation designed for use inside HDTVs, projectors, and other display equipment.

1.1.1 Features

The VS100 family features the following:

- Enables 10.2 Gbps of HDMI 1.4 traffic (including HDCP) and 100Mbps Ethernet in parallel over a single LAN cable according to the following specifications:

<table>
<tr><th>Cable Type</th><th>Range</th><th>Supported Video</th></tr>
<tr><td rowspan="2">CAT5e/CAT6</td><td>100 meters</td><td>Most common full HD formats:
Up to 1080, 60 Hz, 36 bpp
Data rates lower than 5.3 Gbps or below 225 MHz TMDS clock</td></tr>
<tr><td>70 meter</td><td rowspan="2">Ultra HD video formats:
Deep color: 1080p, 60 Hz, 48 bpp
4Kx2K
Data rates higher than 5.3 Gbps or above 225 MHz TMDS clock</td></tr>
<tr><td>CAT6a/CAT7</td><td>100 meter(*)</td></tr>
</table>

(*) please refer to application note 1002 for more details working with ultra HD video and 100 meter reach

- Full HD support: 1080p@60Hz@48 b/pixels, 3D, 4Kx2K(30Hz).

- Support for HDMI Spec 2.0 4K/60/4:2:0 formats with the following color spaces:
  - YCbCr, sYCC601, Adobe YCC-601
- General purpose bus for point-to-point transmission in parallel to AV (e.g., RS232, IR).
- Bi-directional delivery of power over cable.
- Optional HDMI Pass-through on the source side.
- Support of fallback to 100BaseTx according to IEEE 802.3u.
- Support auto resolve of twisted pair crossover and semi crossover (between different Rx and Tx pairs), in HDBaseT mode and Ethernet fallback mode.
- Maximum VS100TX to VS100RX (and vice versa) latency of 10usec over 100m LAN cable.
- CISPR/FCC Class B EMC/EMI compliance.
- ROHS and green compliant.

1.1.2 Applications

The following are typical HDBaseT applications:

- Blu-ray, DVD players and recorders
- Digital set-top boxes (STBs)
- AV receivers
- Game console
- PC Video output ports
- HDMI repeaters, splitters and switches
- DTVs, LCDs and plasma displays
- Rear and front projectors

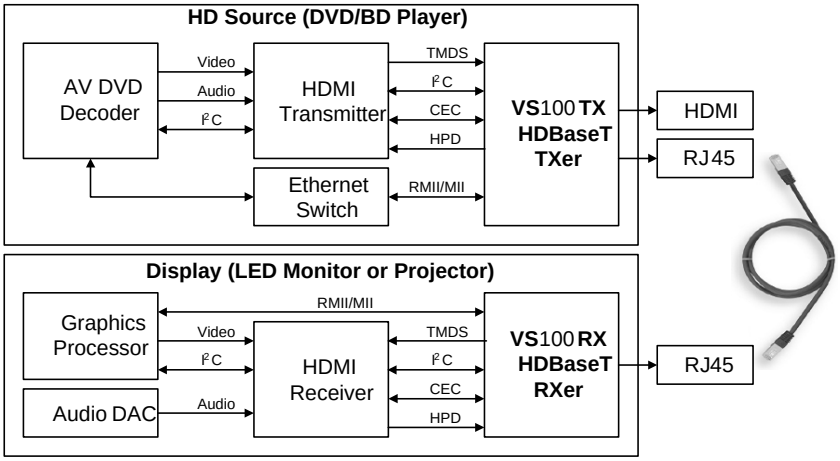


Figure 1: System Functional Diagram

1.2 Technology Overview

Valens' next-generation connectivity technology HDBaseT™ is designed to keep the HD market thriving for years to come. This innovative patent pending technology is the first to enable long-distance wired connectivity of uncompressed HD multimedia content over a single standard LAN cable.

HDBaseT transfers up to 10.2 Gbps of uncompressed HD all-digital video, audio, and Ethernet over long distances (up to 100 m / 328 ft). HDBaseT supports full HD applications of up to 1080p@60Hz@48 b/pixels, 3D and 4K x 2K. Consequently, HDBaseT is becoming the leading physical layer technology for last-leg wired connectivity between HD multimedia stream sources (e.g., set-top boxes (STBs), Blu-ray and DVD players, and PCs) and HD display monitors (e.g., flat-panel LCD and plasma HDTVs).

HDBaseT adds significant value to the entire home entertainment ecosystem, including:

- CE / PC equipment manufacturers
- Audio / Video connectivity product suppliers
- System integrators
- System retailers
- Installers
- Consumers

Unlike existing wired connectivity technologies, HDBaseT enables easy long-distance connectivity of high-performance HD devices over cost-efficient Cat5e/6 cables. Additionally, when compared to emerging wireless technologies, HDBaseT offers superior performance and robustness at minimal system costs.

Delivering improved quality, enhanced reliability, and future-proof interoperability, HDBaseT unleashes the full potential of uncompressed HD connectivity.

HDBaseT provides a channel that simultaneously delivers the following over a point-to-point single 4-pair 100 m / 328 ft UTP cable:

- Unidirectional uncompressed multimedia content from a source device to a sink device.
- Bidirectional multimedia controls between the source and sink devices.
- Bidirectional 100 Mbps Ethernet data between the source and sink devices.

HDBaseT can also incorporate power delivery over the same cable, including the support of Power over Ethernet (PoE, PoE+) technology. HDBaseT operates over CAT5e/6 UTP cables terminated by RJ45 connectors, with up to two intermediate passive RJ45 connectors.

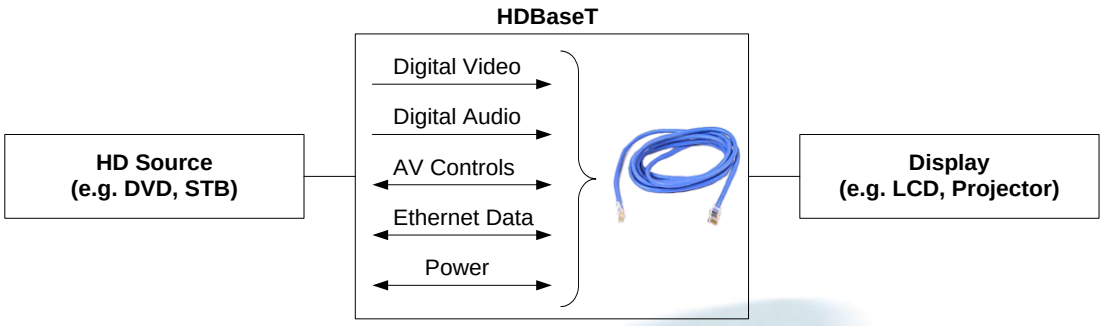


Figure 2: HDBaseT Technology

The HDBaseT channel consists of two distinct asymmetric unidirectional channels:

- **Main Channel** – Directed downstream from the HDBaseT transmitter to the HDBaseT receiver, carrying uncompressed multimedia content as well as the transmitter to receiver portion of the Ethernet data content and multimedia controls.
- **Auxiliary Return Channel** – Directed upstream from the HDBaseT receiver to the HDBaseT transmitter, carrying the receiver to transmitter portion of the data content and the return channel controls.

Both channels use all four twisted pairs of the UTP cable and transmit in full duplex, both downstream and upstream, at the same time.

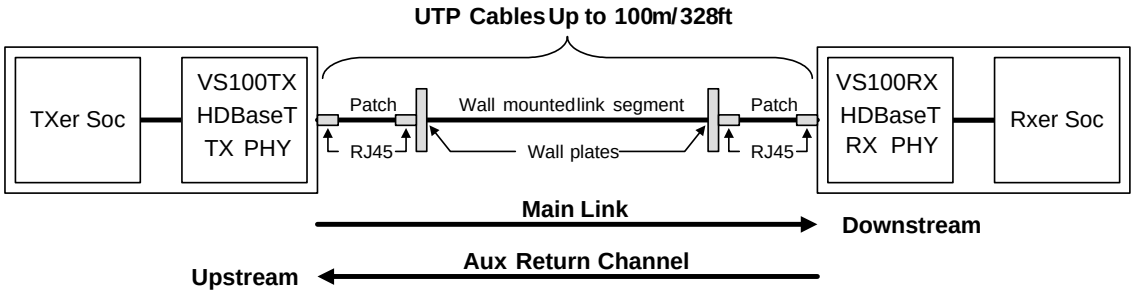


Figure 3: HDBaseT Link

1.3 HDBaseT Channel Terminology

The HDBaseT Transmitter and Receiver chips are labeled *VS100TX* and *VS100RX*, respectively. The HDBaseT transmitter is used to connect the HD source equipment (STBs, Blu-ray / DVD players, etc.) while the HDBaseT receiver is used to connect the sink equipment (monitors, TVs, projectors, etc.).

2 Functional Description

This section includes the following topics:

- Single Stream Source to Sink HDMI over HDBaseT
- HDMI Pass-through on VS100TX
- Ethernet Fallback
- Power Over Cable
- VS100 Main Functionality
- Block Diagrams
- Configuration and Operation Modes

2.1 Single Stream Source to Sink HDMI over HDBaseT

Valens' ground-breaking HDBaseT technology enables the consolidated transmission of uncompressed high definition multimedia (audio and video) content together with 100 Mb/s Ethernet, over a standard Cat5e/6 cable, while still providing quality, security, and high performance.

The VS100 family consists of two devices:

- **VS100TX (HDBaseT Transmitter)** – A source-side implementation, designed for use inside Blu-ray / DVD players, STBs, and other HD source equipment.
- **VS100RX (HDBaseT Receiver)** – A sink-side implementation, designed for use inside HDTVs, projectors, and other display equipment.

Figure 4 illustrates HDMI transfer over HDBaseT, with the source side (VS100TX) on the left and the sink side (VS100RX) on the right.

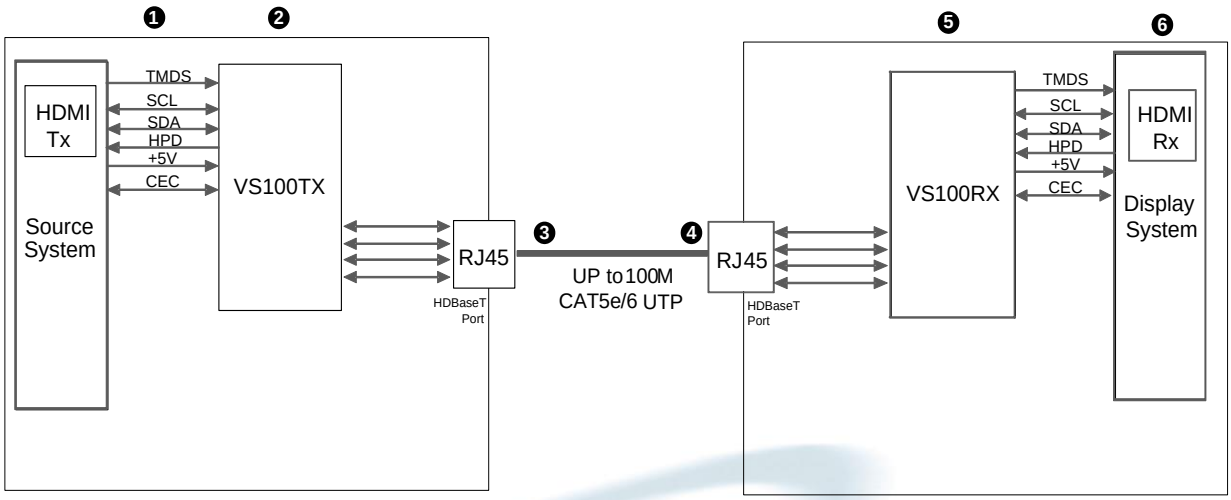


Figure 4: VS100TX – VS100RX – HDMI over HDBaseT

The following is the HDMI data flow:

1. The source system's HDMI physical layer (PHY) transfers its standard Transmission Minimized Differential Signaling (TMDS) and control signals to the VS100TX (instead of directly to the standard HDMI connector).
2. The VS100TX device modulates these signals according to the HDBaseT protocol.
3. The VS100TX device transmits the HDBaseT signals through the RJ45 port over a single standard 100 m / 328 ft LAN cable.
4. The display system receives the HDBaseT transmission through its RJ45 port and transfers it to the VS100RX.
5. The VS100RX device demodulates the HDBaseT signals back to standard HDMI signals.
6. The VS100RX device transparently feeds the received standard HDMI signals to the display system's HDMI sink PHY.

Two types of signals are transmitted by a source system's HDMI PHY (such as, a Blu-ray / DVD player or STB) and received by a display system's HDMI PHY (such as, an LCD or projector):

- **TMDS Signals** – HDMI 1.4 standard data and clock signals.
- **HDMI Control Signals**:
  - Display Data Channel (DDC) – Serial Clock (SCL) and Serial Data Line (SDA).
  - Hot Plug Detect (HPD).
  - +5V.
  - Consumer Electronic Control (CEC).

The VS100TX device can be seamlessly integrated into a standard source system between the HDMI PHY and the HDMI connector in order to modulate these signals (according to the HDBaseT protocol) and transmit them through the RJ45 port. When the VS100TX is either in *Normal Mode* or *Enhanced Mode*, the additional HDMI output port is inactive.

The VS100RX device can be seamlessly integrated into a standard display system so that it receives the HDBaseT signals through its RJ45 port and demodulates them back to standard HDMI signals.

Figure 5 illustrates how HDBaseT can be used to simultaneously transfer HDMI and Ethernet. In this system, the source side is connected to an external Ethernet switch, while on the sink side the Ethernet MAC is embedded in the display system.

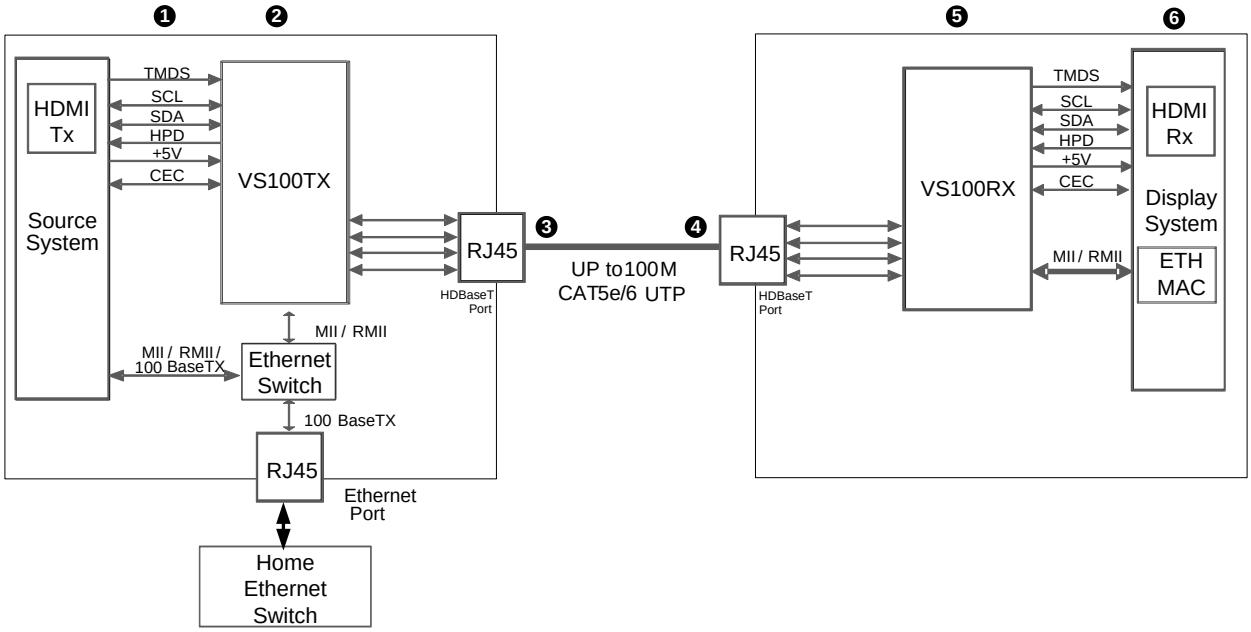


Figure 5: HDMI and Ethernet over HDBaseT – Ethernet Switch at Source

Figure 6 illustrates a system in which the sink part of the entire system is connected to an external Ethernet switch, while on the source side the Ethernet MAC is embedded in the HDBaseT transmitter system.

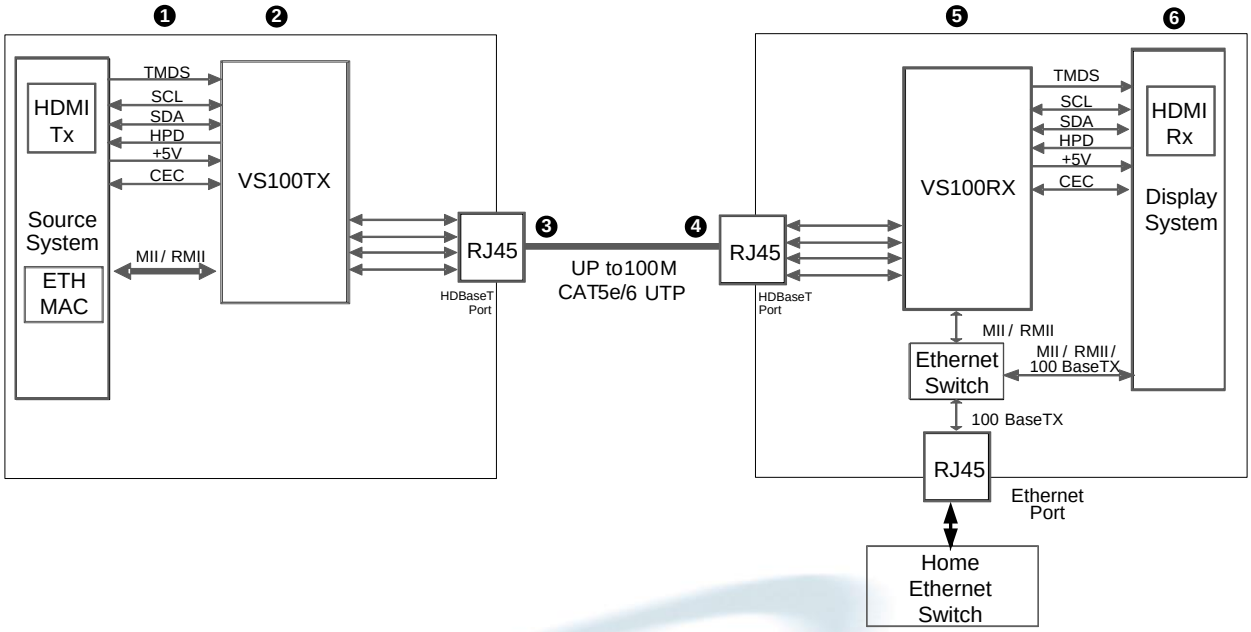


Figure 6: HDMI and Ethernet over HDBaseT – Ethernet Switch at Sink

2.2 HDMI Pass-through on VS100TX

The VS100TX has an additional HDMI Pass-through option that provides transparent backwards compatibility. This ensures continued support of legacy HDMI 1.4 devices. When the VS100TX is in Pass-through mode, the HDBaseT port should be left unused (Figure 7).

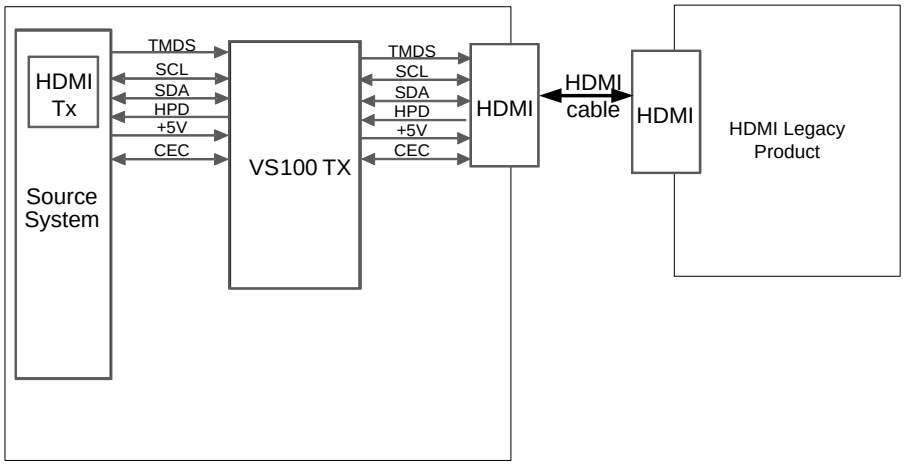


Figure 7: VS100TX in HDMI Pass-through Mode

2.3 Ethernet Fallback

When the VS100 HDBaseT ports are connected to a standard Ethernet device, they automatically revert to operate as 100BaseT Ethernet ports (Figure 8 and Figure 9), according to the IEEE 802.3u specification (i.e., the VS100 device functions as a 100BaseT PHY).

Automatic revert to operate as 100BaseT Ethernet, require the chip to be configured:

- **Automatic operation mode selection or**
- **Manual Operation Mode Selection - Ethernet Fallback**

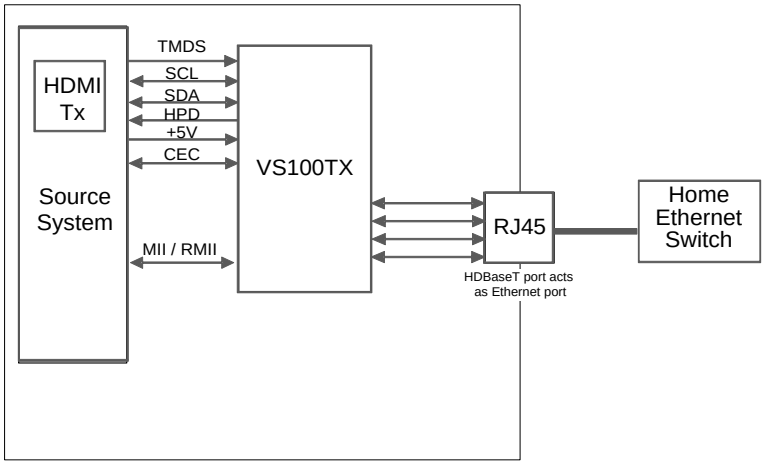


Figure 8: VS100TX in Ethernet Fallback Mode

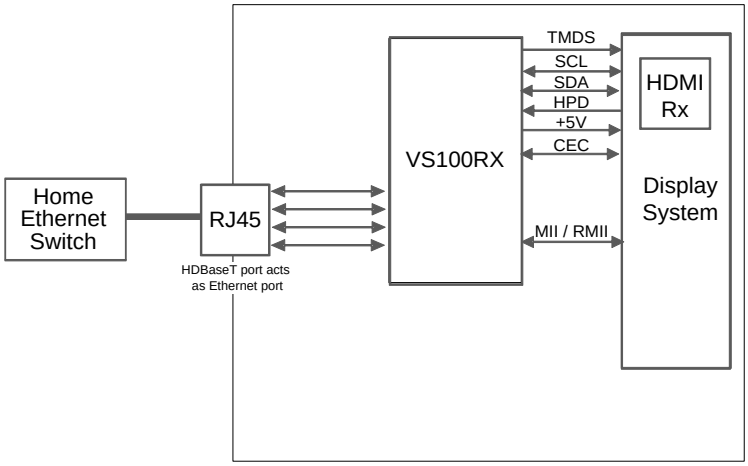


Figure 9: VS100RX in Ethernet Fallback Mode

2.4 Power Over Cable

One of the many important features of the VS100 device family and the HDBaseT technology is its ability to transfer power between the VS100 devices in conjunction with video, audio, control, and Ethernet. Figure 10 schematically illustrates the requirements for power transfer from the VS100TX (power sourcing equipment (PSE)) to the VS100RX (powered device (PD)) where the power is converted to the required voltages. The HDBaseT technology also enables power transfer in the opposite direction – from the VS100RX to the VS100TX.

The HDBaseT technology supports power over cable, including Power over Ethernet (PoE) 802.3af and 802.3at (PoE+).

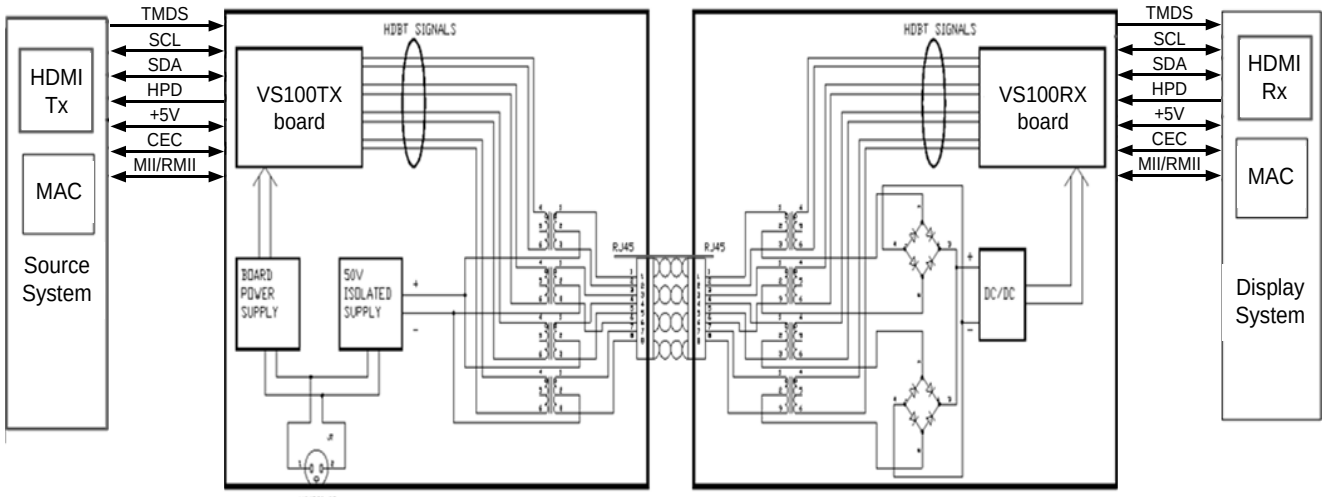


Figure 10: Power Over Cable Transmission from VS100TX to VS100RX

2.5 VS100 Main Functionality

The main functionality of the VS100 includes:

- Transparent transfers of HDMI 1.4 signals, including all controls (DDC, HPD, CEC, and 5V indication).
- Transparent transfers of bidirectional 100 Mb general Reduced Media Independent Interface (RMII) / Media Independent Interface (MII).
- Transparent transfers of up to 3 Mbps of full duplex, bidirectional data, from the Parallel Data bus interface (PDIF).
- Supports HDMI pass-through mode – seamless relaying of HDMI 1.4 signals on the transmitter device.
- Supports HDBaseT fallback to 100BaseT, according to IEEE 802.3u specifications.
- Complies with CISPR / FCC Class B EMC / EMI requirements.
- Supports power over cable, including PoE 802.3af and 802.3at (PoE+).
- Supports auto resolve of twisted pair crossover and semi crossover (between different Rx and Tx pairs), in HDBaseT mode and Ethernet fallback mode.
- Maximum VS100TX to VS100RX latency of 10 usec over 100 m LAN cable.
- Maximum VS100RX to VS100TX latency of 10 usec over 100 m LAN cable.
- I^2C (slave) host interface, for management and monitoring – supporting F/S mode and clock stretching.

2.6 Block Diagrams

Figure 11 and Figure 12 illustrate high-level block diagrams of the VS100TX and VS100RX.

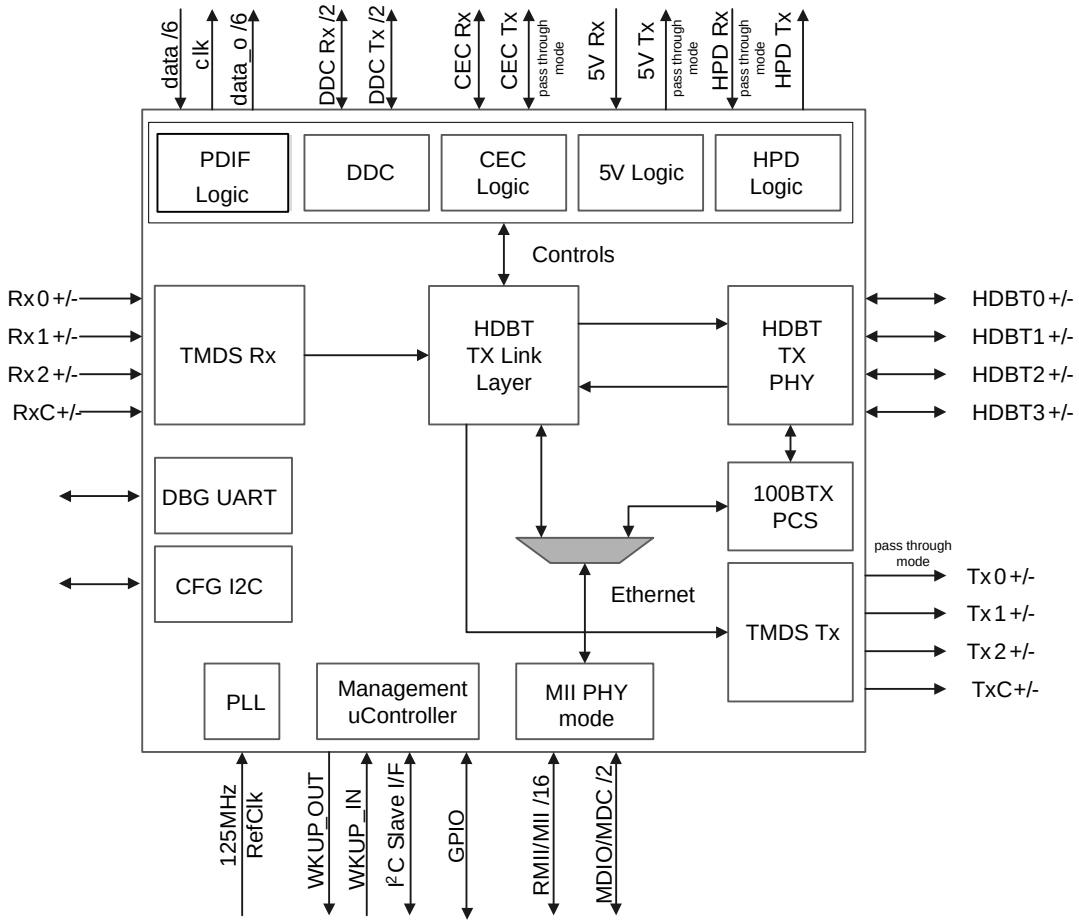


Figure 11: VS100TX High-level Block Diagram

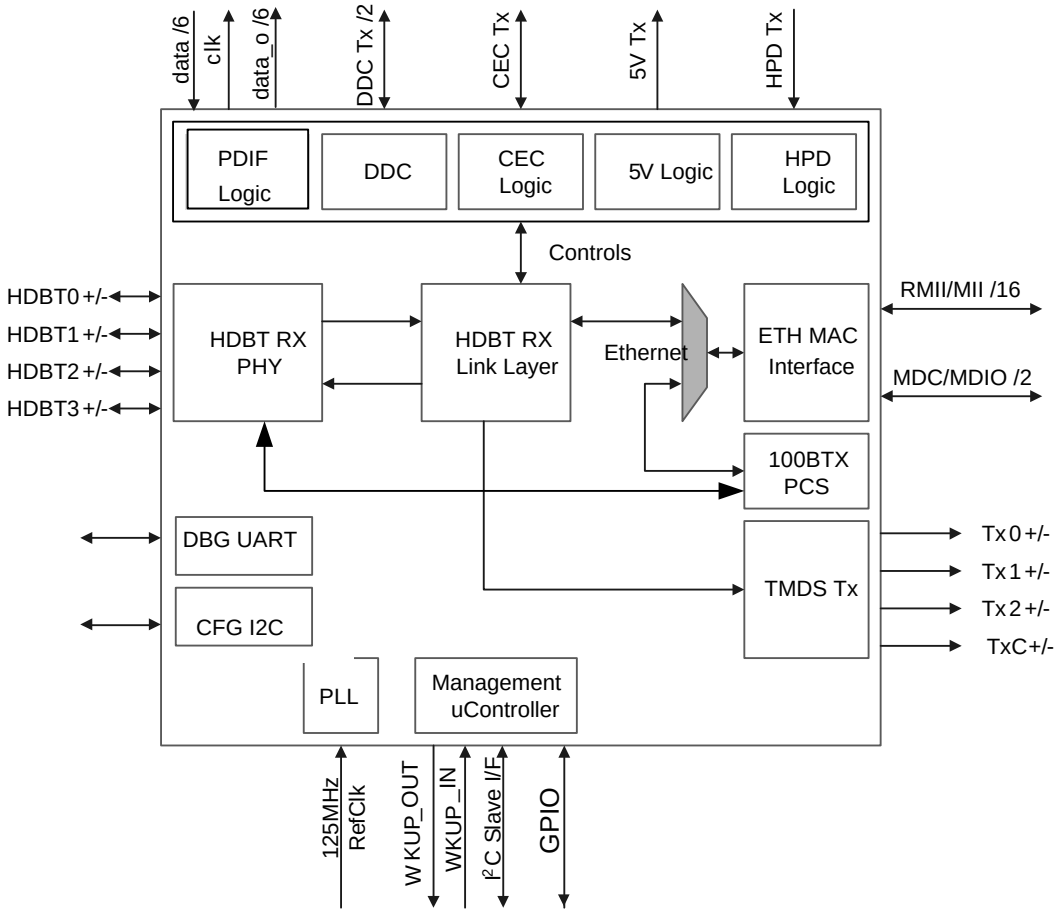


Figure 12: VS100RX High-level Block Diagram

2.7 Configuration and Operation Modes

VS100 devices employ several modes of operation, characterized by:

- The type of data that is transferred.
- The connectivity state of the system.
- The power save requirements of the system.

Table 1 describes the VS100 operation modes.

Table 1: Operation Mode Descriptions

Mode	Video	Controls	Ethernet	Description
HDBaseT	Up to 1080p 48bpp 60Hz	HDMI Controls and PDIF	100BaseT	• Full Bandwidth • Up to 100m / 328ft
Long Reach	Up to 1080p 24bpp 60Hz	HDMI Controls and PDIF	100BaseT	• Long Reach, reduced bandwidth • Up to 150m / 492ft
LPPF1 - Low Power Mode 1	No video	HDMI Controls and PDIF	No Ethernet	• Standby • Up to 150m / 492ft
LPPF2- Low Power Mode 2	No video	HDMI Controls and PDIF	100BaseT	• Standby with Ethernet • Up to 150m/492ft
Ethernet Fallback	No video	None	100BaseT	• Fast Ethernet (with auto-negotiation) • Up to 150m / 492ft
HDMI Pass-through (VS100TX only)	Up to 1080p 30bpp 60Hz	None	No Ethernet	Legacy HDMI on Pass-through port (no HDBaseT link)

2.7.1 Operation Mode Selection Methods

Three mechanisms can be used for selecting the active operation mode of the VS100:

- Manually, by the mode selection pins GPIO[4-7].
- Using the Update Parameter tool.
- By host software, during run time (Host IF commands).

To determine your preferred mode selection method, specify the value of the following two VS100 parameters:

- **MANUAL_OPMODE_SEL** – This parameter determines the mode selection method or the actual selected operation mode after reset, according to the following encoding:
  - **0 (default)** – Apply manual mode selection. After a reset, the operation mode is defined by GPIO[5-7] pins.
  - **1** – Apply manual mode selection with HDBaseT mode selected after reset.
  - **2** – Apply manual mode selection with Long Reach mode selected after reset.
  - **3** – Apply automatic mode selection mechanism after reset.
- **GPIO_OPMODE_strap_mode** – This parameter determines when a mode change commences when changing GPIO[5-7] pins:
  - **0** – Real-Time (default). The mode change commences as a response to the GPIO change during runtime.
  - **1** – After reset. The mode change commences according to the new GPIO setting, only after a reset is applied.

  NOTE:
  This parameter is only relevant when MANUAL_OPMODE_SEL = 0.

In runtime, the operation mode selection is either set to automatic, where the VS100 selects the operation mode, or a host application selects the modes manually using the host interface commands.

In some cases, push buttons may be attached to the GPIO[5-7] pins for manual selection via GPIOs.

Figure 13 summarizes the process of operation mode selection.

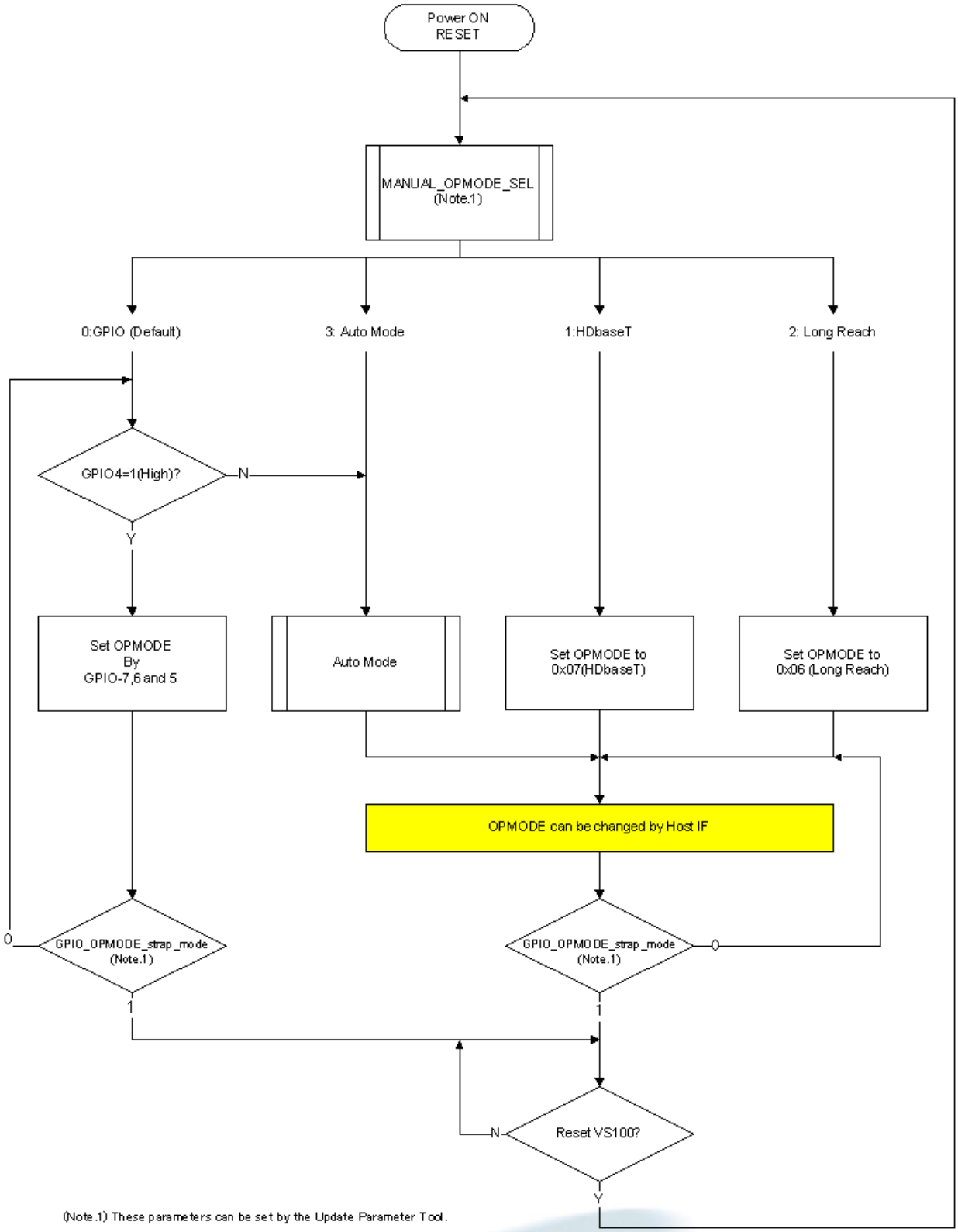


Figure 13: Operation Mode Selection Process

2.7.1.1 Operation Mode Capabilities

Using the Host IF commands, you can disable or enable certain VS100 operation modes from participating in the automatic or manual selection flow. This is referred to as operation mode capabilities. The operation modes that can be enabled or disabled are:

- LPPF2 - Low Power Mode 2
- Bypass
- Ethernet Fallback
- Long Reach

For information on how to enable or disable operational modes, refer to *Valens' Application Note AN1004 - Host Interface*.

NOTE:
When the VS100 initiates a transition to a mode that is disabled at its remote partner (that uses automatic mode selection), the transition does not occur.

2.7.2 Manual Operation Mode Selection

When using manual operation mode selection during runtime, the selection is done by either changing the levels of the GPIO[5-7] lines or by using an appropriate host IF command. Table 2 lists the encoding of the GPIO[5-7] lines for each selection. For more information on how to use the host IF commands, refer to *Valens' Application Note AN1004 - Host Interface*.

Table 2: Manual Operation Mode Selection Codes

Operation Mode Selection Code	Operation Mode
0x7	HDBaseT Mode
0x6	Long Reach
0x5	LPPF2 - Low Power Mode 2
0x4	LPPF1 - Low Power Mode 1
0x3	Reserved
0x2	Reserved
0x1	Ethernet Fallback
0x0	HDMI Pass-through

REMARKS:
When manually selecting HDBaseT or Long Reach, the VS100 may still perform automatic transitions to the low power states LPPF1 or LPPF2 if the remote partner selected them manually.

When both sides use automatic mode selection, Long Reach mode is not selected. At least one of the partners must select Long Reach mode manually for this mode to be applied.

Table 3 presents the system state with regard to mode selection behavior for all possible combinations at both ends of the link. The white cells indicate the state of the system.

Table 3: System State per Selection Mode on Rx and Tx Sides

		Mode Selected on RX Side				
		LPPF1	**LPPF2**	**HDBaseT**	**Long Reach**	**AUTO**
Mode Selected on TX Side	**LPPF1**	LPPF1	LPPF1	LPPF1	LPPF1	LPPF1
	LPPF2	LPPF1	LPPF2	LPPF2	LPPF2	LPPF2
	HDBT	LPPF1	LPPF2	HDBaseT	Long Reach	HDBaseT
	Long Reach	LPPF1	LPPF2	Long Reach	Long Reach	Long Reach
	AUTO	LPPF1	LPPF2	HDBT	Long Reach	AUTO

2.7.3 Automatic Operation Mode Selection

When using automatic operation mode selection, the VS100 uses built-in sensors to determine the mode of operation. These sensors monitor the following:

- Connectivity state of the system.
- Traffic flow.
- Logic state of key signals.

A transition between modes is performed only when both partners of the HDBaseT link agree on the mode by exchanging management messages. If both partners are in automatic mode selection, the source side is the initiator. In this case, the source side negotiates each state transition with its sink side partner.

When one of the partners is configured to manual operation mode selection (typically when managed by host software), the other partner may be placed in automatic mode. In this case, the mode transition negotiation is initiated by the host-managed partner and the auto-mode partner follows through.

2.7.3.1 Automatic Mode Selection State Diagram

Figure 14 illustrates the VS100 transitions between the operation modes when both partners are set to automatic mode selection.

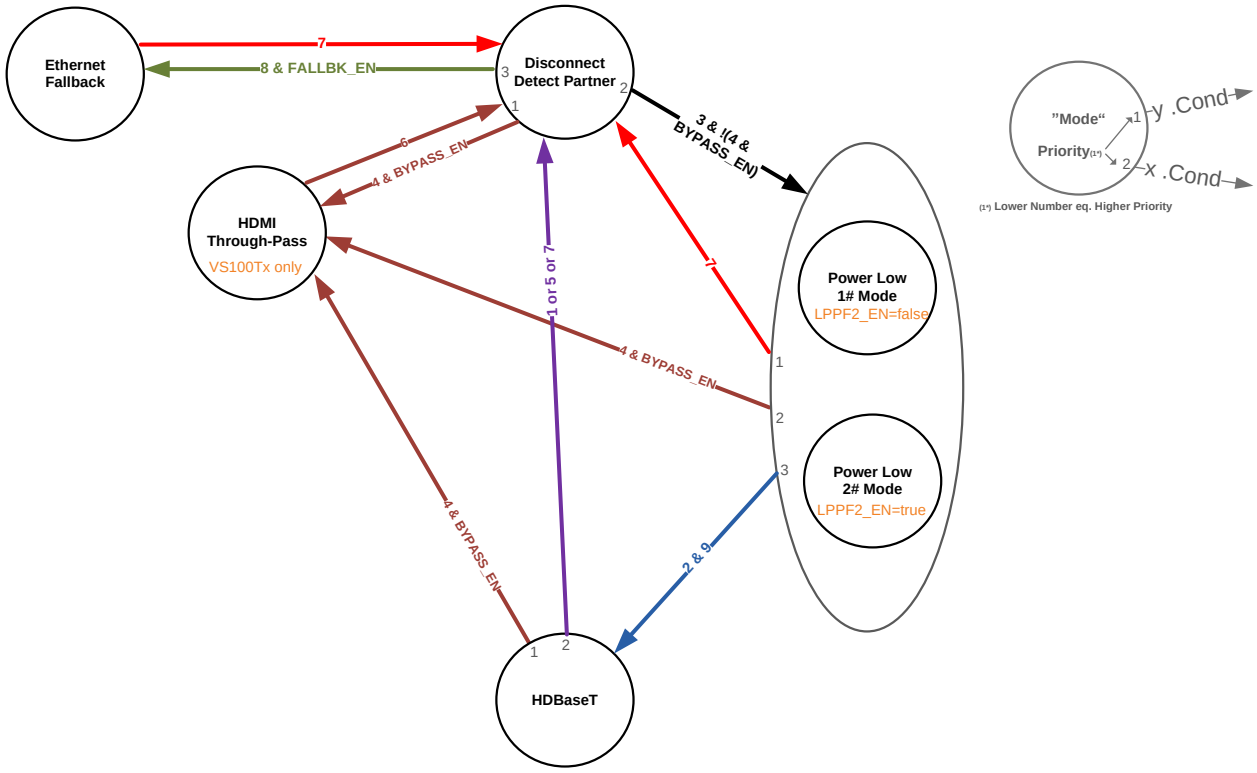


Figure 14: Automatic Operational Mode State Diagram

Table 4 describes the events and conditions that trigger each state transition.

Table 4: State Transition Events

Condition Name	Type	Description
LPPF2_EN	Host IF command	Low Power Mode 2 auto-capability is enabled
BYPASS_EN	Host IF command	Bypass auto-capability is enabled
FALLBK_EN	Host IF command	Fallback auto-capability is enabled
1	HW event	WAKEUP_IN = 0
2	HW event	WAKEUP_IN = 1
3	HW event	HDBaseT link is active
4	HW event	TMDS clock is active and HPD is high in pass-through HDMI connector (Tx chip only)
5	HW event	TMDS clock is inactive or HPD is low in source / sink HDMI connector (Tx / Rx chip, respectively)
6	HW event	TMDS clock is inactive or HPD is low in pass-through port (Tx chip only)
7	HW event	HDBaseT Link is broken

Condition Name	Type	Description
8	HW event	Ethernet is connected on an HDBaseT port
9	HW event	TMDS clock is active and HPD is high in source / sink connectors (Tx / Rx chip, respectively)

2.7.3.2 Choosing between LPPF1 and LPPF2 in Automatic Operation Mode

When both sides of the HDBaseT link (VS100TX and VS100RX) enable LPPF2 in their automatic mode capabilities, a *Detect LPPF* condition results with a transition to LPPF2. When LPPF2 is disabled by either side of the link, *Detect LPPF* always results with a transition to LPPF1.

2.7.3.3 Using WAKEUP_IN and WAKEUP_OUT Pins in Automatic Operation Mode

The WAKEUP_IN pin is used by the host system to indicate its readiness to move between Low Power modes (i.e., LPPF1 or LPPF2) and active mode (i.e., HDBaseT or Long Reach):

- When WAKEUP_IN = high in the host system, it signals the VS100 that the system is ready to move to HDBaseT / Long Reach mode. The device in this case will move to active mode If the link is up and one or both of these conditions apply:
  - TDMS clock is active
  - The remote partner issued a request to move to active mode
- When WAKEUP_IN = low in the host system, it signals the VS100 that the system must enter one of the Low Power modes (i.e., LPPF1 or LPPF2).

The WAKEUP_OUT pin is used by the VS100 to notify the host system of its readiness to move to an active mode (HDBaseT or Long Reach). This signal is set to low when the VS100 is on Low Power mode and high when the conditions to enter active mode are fulfilled. As a result, the host system can use this indication to perform preparations for leaving standby mode.

REMARK:
In an application with no host, the WAKEUP_IN line must be pulled-up (high level).

2.7.4 Force Active Flag

When set, the Force Active flag forces the automatic mode selection mechanism to avoid entering Low Power modes (LPPF1 and LPPF2). In this case, the VS100 ignores the conditions for low power (i.e., WAKEUP_IN = 0 or TMDS clock is not detected for more than 5 seconds) and remains in HDBaseT mode. Setting the Force Active flag can only be done when the VS100 is in automatic mode selection.

Valens recommends activating the Force Active flag in the following scenarios:

- When the traffic over the PDIF lines must be continuous and the system cannot tolerate disturbances caused by mode transitions (see *Mode Transitions* on page 37).
- When the RS232 maximum traffic rate in LPPF (as specified by Table 7) is not sufficient and higher data rates must be supported at all times.

The Force Active flag can be set either by using the appropriate host IF command (see *Valens' Application Note AN1004 - Host Interface*) or by setting the **ForceActiveMode** parameter using

the Update Parameter tool (see *Valens' Application Note AN1033 - Usage of Update Parameter*).

2.7.5 Operation Mode Change Status Interrupt

In automatic mode selection, the GPIO[8] pin can be used as a mode-transition interrupt indication. This interrupt is activated when the conditions for the mode transition occur. The timing behavior of GPIO[8] can be configured by the Update Parameter tool, as follows:

- **Polarity** – Can be set to **active high** or **active low**.
- **GPIO[8] clear method** – Can be set to one of the following:
  - **Automatic** – The signal automatically clears after 200 milliseconds.
  - **Sticky (manual)** – The signal remains active until cleared by the interrupt software routine.

This interrupt is disabled by default and can be enabled / disabled using the Update Parameter tool.

REMARK:
Valens recommends using the following host IF commands when receiving the mode change interrupt:

- **Get link status – As a software indication that the transition is complete.**
- **Get operation mode – As a software indication of the new mode being activated.**

For more information, refer to *Valens' Application Note AN1033 - Usage of Update Parameter* and *Valens' Application Note AN1004 - Host Interface*.

2.7.6 Hardware Configuration

VS100 devices include several hardware configuration options (Table 5). These options are determined by strap pins which are sampled upon system reset.

Table 5: VS100 Strap Pin Configuration

Configuration Option	Pin Name	Description	Default Configuration
i^2c_slave_addr[2:0]	mii_rxd[2:0]	The LS bits of the device I^2C slave address.	0,0,0
rmii_mode	mii_rxd[3]	Selects between MII and RMII modes. • 0 (low): MII. • 1 (high): RMII.	RMII
eeprom_type_select	mii_rx_dv	Selects the EEPROM type: • 0 (low): SPI. • 1 (high): I^2C.	I^2C
ext_boot	mii_rx_err	Selects the CPU boot source: • 0 (low): The CPU boots from an internal ROM. • 1 (high): The CPU boots from an external EEPROM.	Internal

Configuration Option	Pin Name	Description	Default Configuration
eeprom_size	ee_mo,dbg_txd	Selects the EEPROM's address bus width: • 00: 8 bit. • 01: 16 bit. • 10: 17 bit I^2C / 18 bit SPI. (eeprom size >=128K) • 11: No EEPROM connected.	16 bit

3 Interfaces

This section describes the various interfaces of the VS100RX and VS100TX devices. The interfaces are the same for both devices except that the VS100TX has an additional HDMI interface that is used in Pass-through mode.

This section includes the following topics:

- HDBaseT PHY
- HDMI Interface
- MII / RMII
- External Memory
- Host Interface
- GPIO
- Programmable Data Interface (PDIF)

3.1 HDBaseT PHY

VS100 devices use a four-pair UTP cable to transfer HDBaseT data. Figure 15 illustrates conceptual schematics of how the VS100RX and VS100TX devices should be connected to the UTP cable when the HDBaseT is not used to transfer power.

VS100 four-differential HDBaseT pins are connected to a transformer and to pull-up resistors. The transformer is connected to the UTP cable via an RJ45 connector.

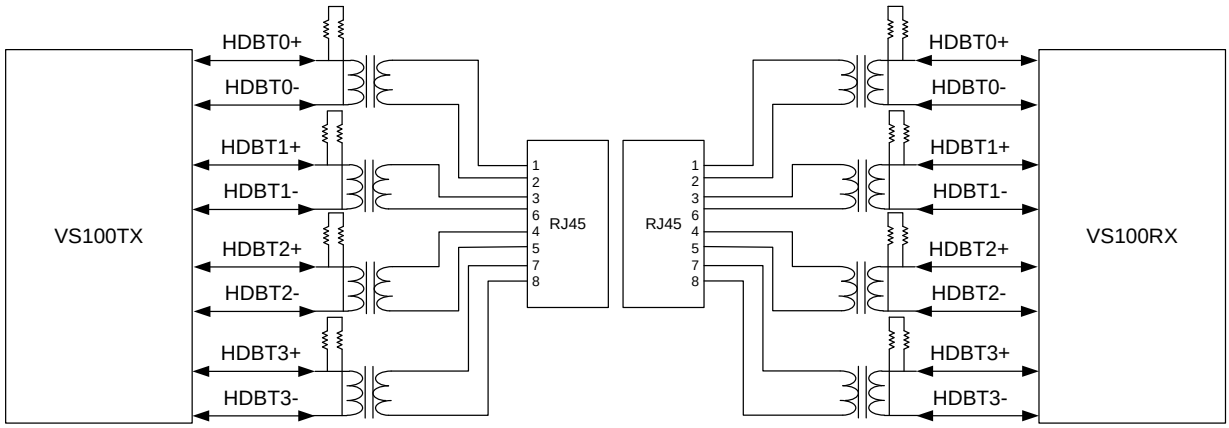


Figure 15: VS100RX and VS100TX HDBaseT Connection Example

This interface is also used in Ethernet fallback mode where the VS100 device is connected to an external Ethernet port.

3.2 HDMI Interface

There are two types of HDMI signals:

- **TMDS Signals** – Contains all the TMDS signals, differential data signals, and the differential clock signal.
- **HDMI Control Signals** – Includes all the HDMI control signals defined in the HDMI 1.4 standard (DDC, 5V, HPD, and CEC).

3.2.1 TMDS Signals

This group contains four pairs of unidirectional differential signals:

- Three differential pairs are used for the HDMI serial data transfer. The data is driven by a transmitter PHY (the VS100RX device in HDBaseT mode or the VS100TX in Pass-through mode). The TMDS data signals are received by the VS100TX device. The data rate on the TMDS data line can reach up to 3.4 Gbps per channel.
- The fourth differential pair is the TMDS clock that is generated by the HDMI transmitter. The frequency of the clock signal is one tenth of the actual serial data rate. The HDMI PHY receiver uses this clock signal to generate the serial clock used for HDMI data recovery.

VS100 HDMI transmitters incorporate specialized capabilities suited to deal with the broad bandwidth of TMDS signals and varying HDMI cable lengths in order to maintain signal quality. For example:

- A TMDS driver with configurable signal pre-emphasis capabilities.
- The VS100 transmitter supports a double termination feature.
- The VS100TX HDMI receiver uses an internal adaptive equalizer to improve its signal detection capabilities. The adaptive equalization process is done automatically after the receiver powers up and the optimal equalizer (in terms of BER) is selected.
- The receiver also handles two termination types – AC and DC termination.

3.2.2 HDMI Control Signals

This group contains the following signals:

- **HPD** – This signal is a sink device output (VS100RX) that is sent towards the source, indicating that the sink E-EDID memory is available for reading. The Hot Plug Detect pin can be asserted only when the +5V Power signal from the source is detected.
- **5V** – This signal is output from the source (VS100TX). HDMI source devices assert the +5V Power signal whenever they use the DDC or TMDS signals.
- **CEC** – The CEC line is used for high-level user control of HDMI-connected devices. VS100RX and VS100TX devices require external pull-up resistors, according to the HDMI 1.4 standard.

- **DDC** – This is a two wire bidirectional I^2C interface used for HDMI control. The connection to the VS100RX and VS100TX devices requires external pull-up resistors, according to the HDMI 1.4 standard. Any HDMI device connected to a VS100 device must support the I^2C clock stretching mechanism.

NOTE:
VS100 devices can support HDMI traffic with HDCP 1.x and 2.2 encryption.

3.3 MII / RMII

The VS100 devices support the MII, RMII, and SMI interfaces. 100BaseT traffic from and to these interfaces may be transferred over the HDBaseT link.

3.3.1 MII IF

The VS100 devices use the standard MII interface (IEEE802.3u) to transfer 100BaseT Ethernet data over the HDBaseT link or in Ethernet fallback mode. Both VS100 devices behave as Ethernet PHY devices and, as such, should be connected to an Ethernet MAC device in order to transfer bidirectional full duplex data.

The MII interface defines a 4-bit wide data path for transmitting and receiving data that is clocked at 25 MHz to provide the required 100 Mbps transfer speed. The MII interface uses two clock signals as references for the interface timing. One clock is used as a reference for the transmit part of the interface and the second is a reference for the receive part of the interface.

The 25 MHz MII clock of the VS100 should not be used for system purposes because in some cases this clock is disabled or reduced in frequency (e.g. LPPF1 and Pass-through modes), and this may cause 3rd-party chipsets (e.g. Ethernet switch) using this clock to malfunction.

NOTE:
If the system design does not require the MII_Tx_ERR_GPIO input to be used, it is should be pulled down on the board via a 1KΩ resistor. This input should not be left unconnected.

3.3.2 RMII IF

VS100 devices also support an RMII interface. In this mode some of the MII interface pins are unused. Some of the MII unused pins are referred to as *multiplexed GPIO pins* and are detailed in Table 8 and Table 9.

The selection between MII and RMII modes of operation is done upon system reset, according to the **rmii_mode** strap pin (Table 5). This selection cannot be changed during operation.

The main differences between MII and RMII are as follows:

- In RMII mode, The widths of the RX and TX data buses are reduced to two bits only (bits number 1,0).
- The clock rate is doubled in order to achieve the required 100 Mbps throughput (i.e., 50 MHz instead of 25 MHz). The 50 MHz RMII clock (pin MII_Rx_CLK) should not be used for system purposes because in some cases this clock is disabled (e.g., LPPF1 and Pass-through

modes), and this may cause 3rd-party chipsets (e.g. Ethernet switch) using this clock to malfunction.

- There is one clock source for the TX and RX signals. This clock source must be external to the VS100 device. Please refer to Valens Application Note AN1005 - *VS100 MII/RMII Interface* for additional information.

3.3.3 Serial Management IF (SMI)

Both VS100 devices support the MII management interface. This is a two-bit interface (a serial data bit and a clock signal) that provides the MAC management functions by addressing the PHY management registers (e.g., resetting the transceiver and setting the transceiver's duplex mode).

3.4 External Memory

VS100 devices must be connected to an external EEPROM or FLASH for storage of the device software and important system parameters. Two types of external memory interfaces are supported:

- Two-wire I^2C interfaces.
- SPI interfaces.

The memory type selection is sampled during reset. The default clock rate is 100 KHz in I^2C and 1 MHz in SPI.

3.5 Host Interface

VS100 devices are self-managed. This implies that most applications can use the devices without any additional management by an external host. Nevertheless, a standard two-bit I^2C slave interface exists to facilitate host configuration or monitoring of the VS100 internal status. VS100 devices support 7-bit I^2C slave addressing and automatic clock stretching for cases in which a device cannot handle the master (host) access bandwidth requirements.

The three LSBs of the VS100 device's slave address are hardware configurable and are sampled upon reset. The other five bits are stored in a register and their default value is 0x5. For more information, refer to *Valens' Application Note AN1004 - Host Interface*.

3.6 GPIO

The VS100 has two types of GPIO pins:

- **Multi-Function GPIO pins** – In addition to their GPIO function, *Multi-Function* GPIO pins serve additional functions. Table 8 and Table 9 describe the default functions of each *Multi-Function* GPIO pin.
- **Dedicated GPIO pins** – Only serve as GPIOs:
  - **GPIO0 to GPIO3** – Configured as output pins and used as LED drivers, as described in Table 6.

- **GPIO4 to GPIO7** – Configured as input pins and used for manual mode selectors. For more information, see *Operation Mode Selection Methods* on page 21 and *Manual Operation Mode Selection* on page 24.
- **GPIO10** – Used for the External RX detect circuit.

NOTE:
All GPIO pins are 3.3 V level voltage. Their input is 5 V tolerant.
Information on the GPIO pins cannot be transferred to the other side of the HDBaseT link (remote side). It can only be used in the local host system (local side).

Table 6: Dedicated GPIO Pins

Pin Name	Type	Default Function
GPIO0	Output	Operation LED. ~1 sec periodic blink indicates device operation.
GPIO1	Output	Link LED: • 0 (low): HDBaseT Link. • Low speed blink: Low Power mode. • High speed blink: Ethernet Fallback mode. • 1 (high): No Link.
GPIO2	Output	HDMI LED: • 0(low): HDMI/DVI Content exists – with HDCP encryption. • 1 (high): No HDMI. • Blink: HDMI/DVI Content exists – without HDCP encryption.
GPIO3	Output	Reserved
GPIO4	Input	Manual Mode Select Enable: • 0(low): Automatic mode. • 1 (high): Manual mode selection. The actual mode is selected by GPIOs 5, 6, and 7.
GPIO5-GPIO7	Input	Manual Mode Selector Code, GPIO5 is LSB.
GPIO8	Output	Operation Mode Change Status (*Operation Mode Change Status Interrupt* on page 28).
GPIO10	Input	External RX Detect circuit input.

3.7 Programmable Data Interface (PDIF)

The Programmable Data bus interface (PDIF) of the VS100 device family is used to transfer low bandwidth communication information over the HDBaseT link. The PDIF interface is a general purpose interface and does not implement any particular communication protocol. It serves as an information pipeline with a predefined capacity. The PDIF is used to facilitate transfer of the following:

- Infra-red (IR).
- UART (RS232).
- Two general purpose channels for transferring data over the HDBaseT link.

3.7.1 PDIF Channel Interface

Table 7 describes how the PDIF channel interface is defined. Each channel is specified for both its HDBT mode performance and LPPF mode performance.

Table 7: PDIF Channel Configuration

PDIF Channel #	Sampling Clock		CTS Use (*), (**)
	HDBT/Long Reach Mode	LPPF Mode	
PDIF_0 (*)	1.62MHz	100 KHz	RS232
PDIF_1	reserved		reserved
PDIF_2	reserved		reserved
PDIF_3 (**)	540KHz	100 KHz	IR
PDIF_4	540KHz	100 KHz	None – Can be used for general purpose traffic.
PDIF_5	540KHz	100 KHz	

REMARKS:
(*) If your product utilizes RS232 communication over the HDBaseT link, allocate PDIF channel #0 in order to comply with HDBaseT CTS. If your product does not utilize RS232 communication over the HDBaseT link, you can use channel #0 for any other proprietary purposes. Your product can still pass CTS without declaring the RS232 feature.

(**) If your product utilizes a CIR channel over the HDBaseT link, allocate PDIF channel #3 in order to comply with HDBaseT CTS. If your product does not utilize CIR channel over the HDBaseT link, you can use channel #3 for any other proprietary purposes. Your product can still pass CTS without declaring the CIR feature.

Each PDIF I/O operates at the 3.3 V level and is 5.0 V input tolerant. PDIF I/Os may drive up to 16 mA current.

The PDIF interface consists of independent non-correlated data channels, transmitting and receiving independent serial data.

VS100 devices contain a PDIF receiver and a PDIF transmitter, enabling the interface to work in full duplex. The PDIF has a maximal aggregated bandwidth of approximately 3.2 Mbps for each direction (receive and transmit), combined for all channels. This number relates to the bit rate after data over-sampling has been taken into account.

Transferring various types of data over the PDIF channels requires careful timing considerations, such as jitter. Valens strongly recommends referring to *Valens' VS100 Application Note AN1007 - PDIF Interface.pdf* for detailed information on using the PDIF channels.

3.7.2 CIR and RS232 Support in Low Power Mode

During Low Power mode of the VS100 (i.e., LPPF1), CIR and RS232 support is limited to the following constraints:

- **CIR** – The CIR signal that is presented to the VS100 on the PDIF pin may be modulated or un-modulated. For compatibility and as a CTS requirement, the CIR presented to the VS100

may be modulated or un-modulated in Active mode, but must be un-modulated in Low Power mode.

- **RS232** – RS232 baud rate is limited to 9600 bps in the Low Power mode (LPPF1/2). Once HDBaseT Active mode is established, the maximal baud rate is 115200 bps.

  NOTE: When running in Automatic Operation mode, the VS100 can be configured to wake-on-RS232. When set (via Update Parameter), transitions on the RS232 interface will cause the VS100 to exit Low Power mode. Following the transition from Low Power mode, additional RS232 data must be detected within 60 seconds, otherwise the VS100 will return to Low Power mode. In order to guarantee a successful wake, the following conditions must met:

  - The user will send a burst of 3 characters over the link (any character will do)
  - The user is responsible to send the characters as a burst and not by keyboard presses
  - These conditions apply to all baud rates (including 19200bps and 115200bps)
- **Mode Transitions** – Upon mode transitions (to and from LPPF1 mode), the CIR and RS232 continuity cannot be guaranteed and some disturbances are expected. Valens advises not transferring these signals during mode transitions.
- **Enable / Disable** – The CIR and RS232 support (in Active as well as Low Power modes) can be enabled or disabled through the Update Parameter tool (see *Valens' Application Note AN1033 - Usage of Update Parameter*). By default, both modes are enabled.

4 Pin Configuration

4.1 VS100TX – Pin Connection Drawing

Matrix	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	EE_CS	EE_MO	EE_SCL_SCK_GPIO	EE_SDA_MI_GPIO	GPIO4	GPIO2	GPIO0	MII_MDC	MII_Rx_CLK	MII_RxD1	MII_COL_GPIO	MII_Tx_EN	MII_TXD0	MII_Tx_CLK	A
B	TEST_CLK_OUT	GPIO10	GPIO9	GPIO7	GPIO5	GPIO3	GPIO1	MII_Rx_ERR	MII_Rx_DV	MII_RxD2	MII_RxD0	MII_CRS_GPIO	MII_TXD1	MII_TXD3_GPIO	B
C	PDIF_DOUT0_GPIO	PDIF_DIN0_GPIO	GPIO11	GPIO12	GPIO8	GPIO6	VSS	MII_MDIO	VDD33V	MII_RxD3	VDD33V	MII_TXD2_GPIO	VSS	MII_Tx_ERR_GPIO	C
D	PDIF_DOUT1_GPIO	PDIF_DIN1_GPIO	PDIF_DOUT5_GPIO	VDD	VDD	VDD	VDD33V	VDD33V	VDD33V	VDD33V	VDD33V	VSS	VSS	VSS	D
E	PDIF_DOUT2_GPIO	PDIF_DIN2_GPIO	PDIF_DIN5_GPIO	VDD	VSS	VSS	VSS	VSS	VSS	VSS	AVDD33_TERM	WAKEUP_OUT	HDMIDES_TMDSDATAP_A_2	HDMIDES_TMDSDATAN_A_2	E
F	PDIF_DOUT3_GPIO	PDIF_DIN3_GPIO	PDIF_CLKOUT	VDD	VSS	VSS	VSS	VSS	VSS	VSS	AVDD33_TERM	WAKEUP_IN	VSS	VSS	F
G	PDIF_DOUT4_GPIO	PDIF_DIN4_GPIO	TDI	VDD	VSS	VSS	VSS	VSS	VSS	VSS	AVDD33	HDMIDES_CEC	HDMIDES_TMDSDATAP_A_1	HDMIDES_TMDSDATAN_A_1	G
H	RCB_REFCLK0_P	RCB_REFCLK0_M	TDO	TCK	VSS	VSS	VSS	VSS	VSS	VSS	AVDD33	HDMIDES_DDC_SCL	VSS	VSS	H
J	DBG_TXD	DBG_RXD	TRST	TMS	VSS	VSS	VSS	VSS	VSS	VSS	AVDD33	HDMIDES_DDC_SDA	HDMIDES_TMDSDATAP_A_0	HDMIDES_TMDSDATAN_A_0	J
K	RESET_IN	TEST_MODE	CFG_SDA	CFG_SCL	VSS	VSS	VSS	VSS	VSS	VSS	HDMISER_ATESTMON_1	HDMIDES_5V	VSS	VSS	K
L	HDSRC_REXT_H	VSS	AVDD10	AVDD10	AVDD10	AVDD10	AVDD10	AVDD10	AVDD10	AVDD10	HDMISER_ATESTMON_0	HDMIDES_HPD	HDMIDES_TMDSCLKP_A	HDMIDES_TMDSCLKN_A	L
M	HDSRC_ATB_HP	HDSRC_ATB_HM	AVDD18	VSS	VSS	VSS	AVDD18	HDMISER_HPD	HDMISER_5V	HDMISER_DDC_SDA	HDMISER_DDC_SCL	HDMISER_CEC	HDMISER_REF	HDMIDES_REF	M
N	HDSRC_0_P	HDSRC_1_M	VSS	VSS	HDSRC_2_P	HDSRC_3_M	VSS	HDMISER_TMDSCLKP	AVDD18	HDMISER_TMDSDATAP_0	VSS	HDMISER_TMDSDATAP_1	AVDD18	HDMISER_TMDSDATAP_2	N
P	HDSRC_0_M	HDSRC_1_P	VSS	VSS	HDSRC_2_M	HDSRC_3_P	VSS	HDMISER_TMDSCLKN	VSS	HDMISER_TMDSDATAN_0	VSS	HDMISER_TMDSDATAN_1	VSS	HDMISER_TMDSDATAN_2	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Figure 16: VS100TX – Pin Connection Drawing (top view)

4.2 VS100RX – Pin Connection Drawing

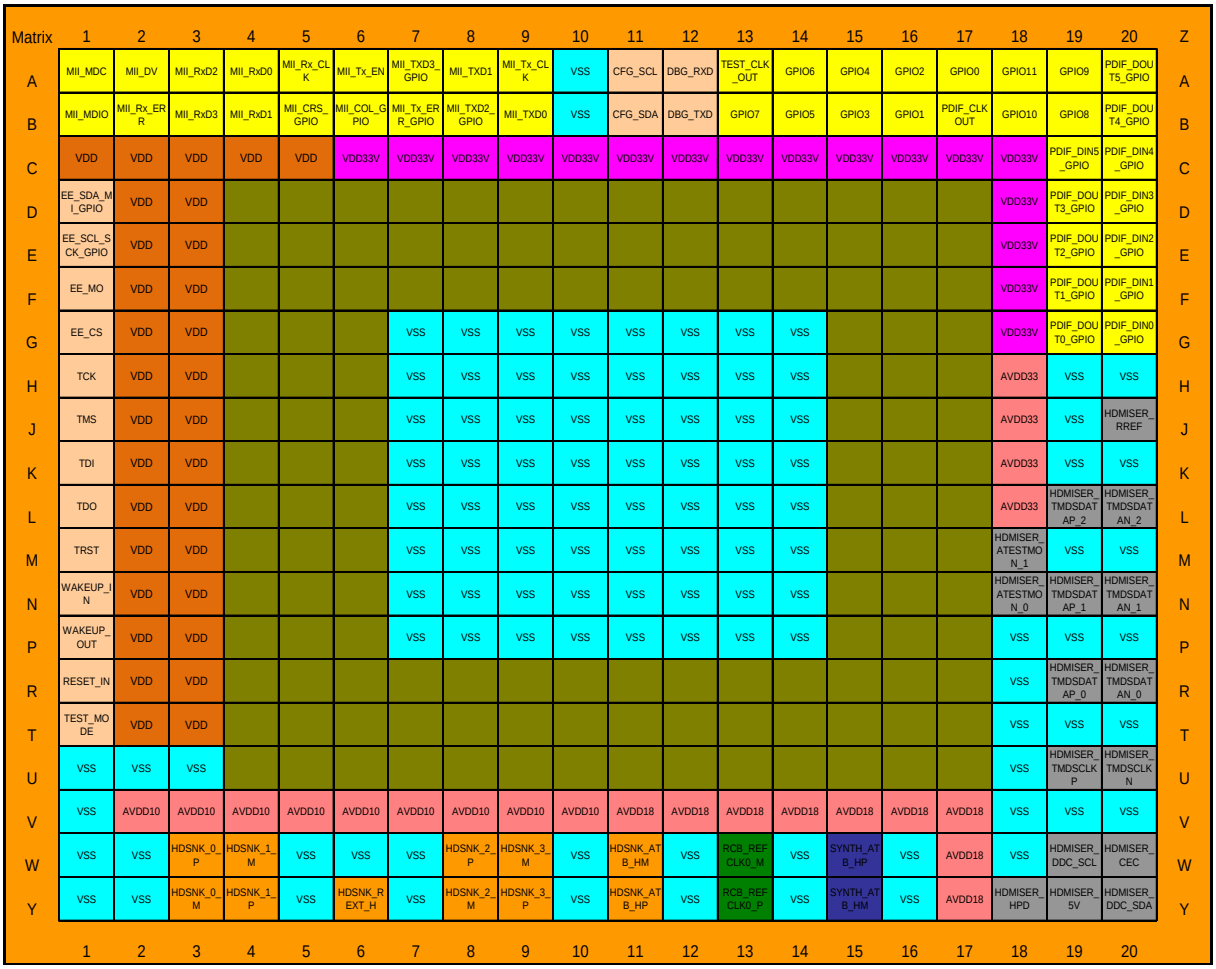


Figure 17: VS100RX – Pin Connection drawing (top view)

4.3 VS100TX – Pin Configuration

The following is the pin configuration of the VS100TX device. All multiplexed pins are by default configured to be active in their functional mode (not GPIO).

Table 8: VS100TX Pin Configuration

Pin Name	Pin type	Type*	Pin number	Description
MII_Tx_CLK	In/Out	PU	A14	MII Transmit Clock(**)
MII_TXD[0-1]	Input	PU	A13, B13	MII Transmit Data Bits 0, 1 A13 = bit 0 B13 = bit 1
MII_TXD[2-3]_GPIO	Input	PU	C12, B14	MII Transmit Data Bits 2, 3
	In/Out			General purpose IO bits 0,1 C12 = MII_TXD[2] / GPIO0 B14 = MII_TXD[3] / GPIO1

Pin Name	Pin type	Type*	Pin number	Description
MII_Tx_ERR_GPIO	Input	PU	C14	MII Transmit Error. If not used, pull down via a 1KΩ resistor.
	In/Out			General purpose IO bits 4
MII_Tx_EN	Input	D	A12	MII Transmit Enable
MII_COL_GPIO	Output	PU	A11	MII Collision Detect
	In/Out			General purpose IO bit 2
MII_CRS_GPIO	Output	PU	B12	MII Carrier Sense
	In/Out			General purpose IO bit 3
MII_Rx_CLK	Output	D	A9	MII Receive Clock (**)
MII_RxD[0-3]	Output	PD,PD,PD,PU	B11, A10, B10, C10	MII Receive Data Bits 0 - 3. B11 = MII_RxD[0] A10 = MII_RxD[1] B10 = MII_RxD[2] C10 = MII_RxD[3]
	Input			Strap option, see Table 5
MII_Rx_DV	Output	PU	B9	MII receive Data Valid.
	Input			Strap option, see Table 5
MII_Rx_ERR	Output	PD	B8	MII Receive Error.
	Input			Strap option, see Table 5
MII_MDC	Input	PU	A8	MII Management Clock
MII_MDIO	In/Out	PU	C8	MII Management Data
EE_SDA_MI_GPIO	In/Out	PU	A4	I2C EEPROM Data or SPI EEPROM VS100 Data in.
				General purpose IO bits 18
EE_SCL_SCK_GPIO	Output	PU	A3	EEPROM Clock for Both Types of EEPROM.
				General purpose IO bits 17
EE_MO	Output	PD	A2	SPI EEPROM VS100 Data Out.
	Input			Strap option, see Table 5
EE_CS	Output	PD	A1	SPI EEPROM chip select
HDMIDES_TMDSDATAP_A_0	Input	TMDS	J13	TMDS Data Lane0 Positive
HDMIDES_TMDSDATAN_A_0	Input	TMDS	J14	TMDS Data Lane0 Negative
HDMIDES_TMDSDATAP_A_1	Input	TMDS	G13	TMDS Data Lane1 Positive
HDMIDES_TMDSDATAN_A_1	Input	TMDS	G14	TMDS Data Lane1 Negative
HDMIDES_TMDSDATAP_A_2	Input	TMDS	E13	TMDS Data Lane2 Positive
HDMIDES_TMDSDATAN_A_2	Input	TMDS	E14	TMDS Data Lane2 Negative
HDMIDES_TMDSCLKP_A	Input	TMDS	L13	TMDS Clock Positive
HDMIDES_TMDSCLKN_A	Input	TMDS	L14	TMDS Clock Negative
HDMIDES_DDC_SCL	In/Out	OD	H12	HDMI DDC Clock

Pin Name	Pin type	Type*	Pin number	Description
HDMIDES_DDC_SDA	In/Out	OD	J12	HDMI DDC Data
HDMIDES_HPD	Output	D	L12	HDMI Hot Plug Detect
HDMIDES_CEC	In/Out	OD	G12	HDMI CEC Bus
HDMIDES_5V	Input	D	K12	HDMI 5v Indication
HDMIDES_RREF	In/Out	A	M14	Current Source Resistor
HDMISER_TMDSDATAP_0	Output	TMDS	N10	TMDS Data Lane0 Positive
HDMISER_TMDSDATAN_0	Output	TMDS	P10	TMDS Data Lane0 Negative
HDMISER_ TMDSDATAP_1	Output	TMDS	N12	TMDS Data Lane1 Positive
HDMISER_ TMDSDATAN_1	Output	TMDS	P12	TMDS Data Lane1 Negative
HDMISER_ TMDSDATAP_2	Output	TMDS	N14	TMDS Data Lane2 Positive
HDMISER_ TMDSDATAN_2	Output	TMDS	P14	TMDS Data Lane2 Negative
HDMISER_TMDSCLKP	Output	TMDS	N8	TMDS Clock Positive
HDMISER_TMDSCLKN	Output	TMDS	P8	TMDS Clock Negative
HDMISER_DDC_SCL	In/Out	OD	M11	HDMI DDC Clock
HDMISER_DDC_SDA	In/Out	OD	M10	HDMI DDC Data
HDMISER_HPD	Input	D	M8	HDMI Hot Plug Detect
HDMISER_CEC	In/Out	OD	M12	HDMI CEC Bus
HDMISER_5V	Output	D	M9	HDMI 5v Indication
HDMISER_RREF	In/Out	A	M13	Current Source Resistor
HDMISER_ATSTMON_1	In/Out	A	K11	Analog Test Monitor. Should be left unconnected.
HDMISER_ATSTMON_0	In/Out	A	L11	Analog Test Monitor. Should be left unconnected.
HDSRC_0_M	In/Out	A	P1	HDBaseT Transmit Channel 0 Negative
HDSRC_0_P	In/Out	A	N1	HDBaseT Transmit Channel 0 Positive
HDSRC_1_M	In/Out	A	N2	HDBaseT Transmit Channel 1 Negative
HDSRC_1_P	In/Out	A	P2	HDBaseT Transmit Channel 1 Positive
HDSRC_2_M	In/Out	A	P5	HDBaseT Transmit Channel 2 Negative
HDSRC_2_P	In/Out	A	N5	HDBaseT Transmit Channel 2 Positive
HDSRC_3_M	In/Out	A	N6	HDBaseT Transmit Channel 3 Negative
HDSRC_3_P	In/Out	A	P6	HDBaseT Transmit Channel 3 Positive
HDSRC_REXT_H	In/Out	A	L1	Current Source Resistor
HDSRC_ATB_HM	In/Out	A	M2	HDSRC analog test bus. Should be left unconnected.
HDSRC_ATB_HP	In/Out	A	M1	HDSRC analog test bus Should be left unconnected.
RCB_REFCLK0_P	Input	LVDS	H1	125MHz reference Clock Positive
RCB_REFCLK0_M	Input	LVDS	H2	125MHz reference Clock Negative
RESET_IN	Input	D	K1	Chip Reset Input

Pin Name	Pin type	Type*	Pin number	Description
GPIO[0-12]	In/Out	PU	A7,B7,A6, B6,A5,B5, C6,B4,C5, B3,B2,C3, C4	General Purpose IO. GPIO11, GPIO12 has interrupt generation capabilities. A7 = GPIO0; B7 = GPIO1; A6 = GPIO2; B6 = GPIO3; A5 = GPIO4; B5 = GPIO5; C6 = GPIO6; B4 = GPIO7; C5 = GPIO8; B3 = GPIO9; B2 = GPIO10; C3 = GPIO11; C4 = GPIO12
PDIF_DIN[0-5]_GPIO (***)	input	PU	C2,D2,E2, F2,G2,E3	Parallel Data Interface Data in C2 = PDIF_DIN[0]; D2 = PDIF_DIN[1]; E2 = PDIF_DIN[2]; F2 = PDIF_DIN[3]; G2 = PDIF_DIN[4]; E3 = PDIF_DIN[5]
	In/Out			General purpose IO bits 5-10 C2 = GPIO0; D2 = GPIO1; E2 = GPIO2; F2 = GPIO3; G2 = GPIO4; E3 =GPIO5
PDIF_DOUT[0-5]_GPIO(***)	Out	PU	C1,D1,E1, F1,G1,D3	Parallel Data Interface Data out C1=PDIF_DOUT[0]; D1=PDIF_DOUT[1]; E1=PDIF_DOUT[2]; F1=PDIF_DOUT[3]; G1=PDIF_DOUT[4]; D3=PDIF_DOUT[5]
	In/Out			General purpose IO bits 11-16 C1=GPIO11; D1=GPIO12; E1=GPIO13; F1=GPIO14; G1=GPIO15; D3=GPIO16
PDIF_CLKOUT	Output	D	F3	Parallel Data Bus Clock Output
WAKEUP_IN	Input	PU	F12	Wakeup Input
WAKEUP_OUT	Output	D	E12	Wakeup Output
DBG_TXD	Output	PU	J1	Debug Transmit Data
	Input			Strap option, see Table 5
DBG_RXD	Input	PU	J2	Debug Receive Data
CFG_SCL	In/Out	PU	K4	Host interface I2C Clock Signal
CFG_SDA	In/Out	PU	K3	Host interface I2C Data Signal
TCK	Input	PU	H4	(reserved - for fab testing only****)
TMS	Input	PU	J4	
TDI	Input	PU	G3	
TDO	Output	D	H3	
TRST	Input	PD	J3	JTAG Reset – Must be pulled down via 1 kohm resistor (reserved - for fab testing only****)
TEST_MODE	Input	D	K2	Chip Test Mode Select Input, must be connected to GND.
TEST_CLK_OUT	Output	D	B1	Test clock out should be left unconnected.

Pin Name	Pin type	Type*	Pin number	Description
VSS	ground	G	C7,C13,D12,D13,D14,E5,E6,E7,E8,E9,E10,F5,F6,F7,F8,F9,F10,F13,F14,G5,G6,G7,G8,G9,G10,H5,H6,H7,H8,H9,H10,H13,H14,J5,J6,J7,J8,J9,J10,K5,K6,K7,K8,K9,K10,K13,K14,L2,M4,M5,M6,N3,N4,N7,N11,P3,P4,P7,P9,P11,P13	
VDD	power	P	D4,D5,D6,E4,F4,G4	1V input
VDD33V	power	P	C9,C11,D7,D8,D9,D10,D11	3.3V input
AVDD10	power	P	L3,L4,L5,L6,L7,L8,L9,L10	analog VDD 1V
AVDD18	power	P	M3,M7,N9,N13	analog VDD 1.8V
AVDD33	power	P	G11,H11,J11	analog VDD 3.3V
AVDD33_TERM	power	P	E11,F11	

* Pad type

- D – Digital pad
- PU – Digital with pullup
- PD – Digital with pulldown
- OD – Digital open drain
- A – Analog pad
- TMDS – TMDS pad
- LVDS – LVDS pad
- P – Power
- G – Ground

(**) – MII/RMII interface related clock signals should not be used for other board purposes. These clocks are inactive in various modes of the system and therefore are not applicable for other interfaces.

(***) – PDIF channel 1 and 2 are reserved and should be left unconnected.

(****) - These pins are JTAG interface used for chip production only. They are not intended for boundary scan testing

4.4 VS100RX – Pin Configuration

The following is the pin configuration of the VS100RX device. All multiplexed pins are by default configured to be active in their functional mode (not GPIO).

Table 9: VS100RX Pin Configuration

Pin Name	Pin type	Pull type	Pin number	Description
MII_Tx_CLK	In/Out	D	A9	MII Transmit Clock(**)
MII_TXD[0-1]	Input	D	B9,A8	MII Transmit Data Bits 0, 1 B9 = MII_TXD[0] A8 = MII_TXD[1]
MII_TXDx_GPIO[2-3]	Input	PU	B8,A7	MII Transmit Data Bits 2, 3 B8 = MII_TXD[2] A7 = MII_TXD[3]
	In/Out			General purpose IO bits 0-1 B8 = GPIO0 A7 = GPIO1
MII_Tx_ERR_GPIO	Input	PU	B7	MII Transmit Error. If not used, pull down via a 1KΩ resistor.
	In/Out			General purpose IO bits 4
MII_Tx_EN	Input	D	A6	MII Transmit Enable
MII_COL_GPIO	Output	PU	B6	MII Collision Detect
	In/Out			General purpose IO bits 2
MII_CRS_GPIO	Output	PU	B5	MII Carrier Sense
	In/Out			General purpose IO bits 3
MII_Rx_CLK	Output	D	A5	MII Receive Clock(**)
MII_RxD[0-3]	Output	PD,PD,PD, PU	A4,B4,A3,B 3	MII Receive Data Bits 0 – 3 A4 = MII_RxD[0]; B4 = MII_RxD[1]; A3 = MII_RxD[2]; B3 = MII_RxD[3]
	Input			Strap option, see Table 5
MII_Rx_DV	Output	PU	A2	MII Data Valid
	Input			Strap option, see Table 5
MII_Rx_ERR	Output	PD	B2	MII Receive Error
	Input			Strap option, see Table 5
MII_MDC	Input	D	A1	MII Management Clock
MII_MDIO	In/Out	D	B1	MII Management Data
EE_SDA_MI_GPIO	In/Out	PU	D1	I^2C EEPROM Data or SPI EEPROM VS100 Data in
				General purpose IO bits 18
EE_SCL_SCK_GPIO	Output	PU	E1	EEPROM Clock for Both Types of EEPROM
				General purpose IO bits 17
EE_MO	Output	PD	F1	SPI EEPROM VS100 Data Out

Pin Name	Pin type	Pull type	Pin number	Description
	Input			Strap option, see Table 5
EE_CS	Output	PD	G1	SPI EEPROM chip select
HDMISER_TMDSDATAP_0	Output	TMDS	R19	TMDS Data Lane0 Positive
HDMISER_TMDSDATAN_0	Output	TMDS	R20	TMDS Data Lane0 Negative
HDMISER_TMDSDATAP_1	Output	TMDS	N19	TMDS Data Lane1 Positive
HDMISER_TMDSDATAN_1	Output	TMDS	N20	TMDS Data Lane1 Negative
HDMISER_TMDSDATAP_2	Output	TMDS	L19	TMDS Data Lane2 Positive
HDMISER_TMDSDATAN_2	Output	TMDS	L20	TMDS Data Lane2 Negative
HDMISER _TMDSCLKP	Output	TMDS	U19	TMDS Clock Positive
HDMISER _TMDSCLKN	Output	TMDS	U20	TMDS Clock Negative
HDMISER_DDC_SCL	In/Out	OD	W19	HDMI DDC Clock
HDMISER_DDC_SDA	In/Out	OD	Y20	HDMI DDC Data
HDMISER_HPD	Input	PD	Y18	HDMI Hot Plug Detect
HDMISER_CEC	In/Out	OD	W20	HDMI CEC Bus
HDMISER_5V	Output	D	Y19	HDMI 5 Volt control
HDMISER_RREF	In/Out	A	J20	Current Source Resistor
HDMISER_ATSTMON_0	In/Out	A	N18	HDMI serializer Analog Test Monitor. Should be left unconnected.
HDMISER_ATSTMON_1	In/Out	A	M18	HDMI serializer Analog Test Monitor. Should be left unconnected.
HDSNK_0_M	In/Out	A	Y3	HDBaseT Channel 0 Negative
HDSNK_0_P	In/Out	A	W3	HDBaseT Channel 0 Positive
HDSNK_1_M	In/Out	A	W4	HDBaseT Channel 1 Negative
HDSNK_1_P	In/Out	A	Y4	HDBaseT Channel 1 Positive
HDSNK_2_M	In/Out	A	Y8	HDBaseT Channel 2 Negative
HDSNK_2_P	In/Out	A	W8	HDBaseT Channel 2 Positive
HDSNK_3_M	In/Out	A	W9	HDBaseT Channel 3 Negative
HDSNK_3_P	In/Out	A	Y9	HDBaseT Channel 3 Positive
HDSNK_REXT_H	In/Out	A	Y6	Current Source Resistor
HDSNK_ATB_HM	In/Out	A	W11	RECEIVER Analog test bus negative Should be left unconnected.
HDSNK_ATB_HP	In/Out	A	Y11	RECEIVER Analog test bus positive Should be left unconnected.
RCB_REFCLK0_P	Input	LVDS	Y13	125MHz reference Clock Positive
RCB_REFCLK0_M	Input	LVDS	W13	125MHz reference Clock Negative
RESET_IN	Input	D	R1	Chip Reset Input
SYNTH_ATB_HM	In/Out	A	Y15	Synthesizer Analog test bus negative Should be left unconnected.
SYNTH_ATB_HP	In/Out	A	W15	Synthesizer Analog test bus positive Should be left unconnected.

Pin Name	Pin type	Pull type	Pin number	Description
GPIO[0-11]	In/Out	PU	A17,B16,A16,B15,A15,B14,A14,B13,B19,A19,B18,A18	General Purpose IO. GPIO10, GPIO11 has interrupt generation capabilities. A17 = GPIO0; B16 = GPIO1; A16 = GPIO2; B15 = GPIO3; A15 = GPIO4; B14 = GPIO5; A14 = GPIO6; B13 = GPIO7; B19 = GPIO8; A19 = GPIO9; B18 = GPIO10; A18 = GPIO11
PDIF_DIN[0-5]_GPIO (***)	Input	PU	G20,F20,E20,D20,C20,C19	Parallel Data Interface Data in. G20 = PDIF_DIN[0]; F20 = PDIF_DIN[1]; E20 = PDIF_DIN[2]; D20 = PDIF_DIN[3]; C20 = PDIF_DIN[4]; C19 = PDIF_DIN[5]
	In/Out			General purpose IO bits 5-10 G20 = GPIO5; F20 = GPIO6; E20 = GPIO7; D20 = GPIO8; C20 = GPIO9; C19 = GPIO10
PDIF_DOUT[0-5]_GPIO (***)	Output	PU	G19,F19,E19,D19,B20,A20	Parallel data Interface Data out G19 = PDIF_DOUT[0]; F19 = PDIF_DOUT[1]; E19 = PDIF_DOUT[2]; D19 = PDIF_DOUT[3]; B20 = PDIF_DOUT[3]; A20 = PDIF_DOUT[4]
	In/Out			General purpose IO bits 11-16 G19=GPIO11; F19=GPIO12; E19=GPIO13; D19=GPIO14; B20=GPIO15; A20=GPIO16
PDIF_CLKOUT	Output	PU	B17	Parallel Data Bus Clock Output
	In/Out			General purpose IO bit 19
WAKEUP_IN	Input	D	N1	Wakeup Input
WAKEUP_OUT	Output	D	P1	Wakeup Output
DBG_TXD	Output	PU	B12	Debug Transmit Data.
	Input			Strap option, see Table 5
DBG_RXD	Input	D	A12	Debug Receive Data
CFG_SCL	In/Out	OD	A11	Host interface I^2C Clock Signal
CFG_SDA	In/Out	OD	B11	Host interface I^2C Data Signal
TCK	Input	PU	H1	(reserved - for fab testing only****)
TMS	Input	PU	J1	
TDI	Input	PU	K1	
TDO	Output	D	L1	
TRST	Input	PU	M1	JTAG Reset – Must be pulled down via 1 kohm resistor (reserved - for fab testing only****)
TEST_MODE	Input	D	T1	Chip Test Mode Select Input, must be connected to GND.
TEST_CLK_OUT	Output	D	A13	Test clock out should be left unconnected.

Pin Name	Pin type	Pull type	Pin number	Description
VSS	ground	G	A10,B10,G7-G14,H7-H14,H19,H20,J7-J14, J19,K7-K14,K19,K20,L7-L14,M7-M14,M19,M20,N7-N14,P7-P14,P18-P20,R18,T18-T20,U1-U3,U18,V1,V18-V20,W1,W2,W5-W7,W10,W12,W14,W16,W18,Y1,Y2,Y5,Y7,Y10,Y12,Y14,Y16	
VDD	power	P	C1-C5,D2,D3,E2,E3,F2,F3,G2,G3,H2,H3,J2,J3,K2,K3,L2,L3,M2,M3,N2,N3,P2,P3,R2,R3,T2,T3	VDD 1V
VDD33V	power	P	C6-C18,D18,E18,F18,G18	VDD 3.3V
AVDD10	power	P	V2-V10	analog VDD 1V
AVDD18	power	P	V11-V17,W17,Y17	
AVDD33	power	P	H18,J18,K18,L18	

* Pad type

- D – Digital pad
- PU – Digital with pull-up
- PD – Digital with pull-down
- OD – Digital open drain
- A – Analog pad
- TMDS – TMDS pad
- LVDS – LVDS pad
- P – Power
- G- Ground

(**) – MII/RMII interface related clock signals should not be used for other board purposes. These clocks are inactive in various modes of the system and therefore are not applicable for other interfaces.

(***) – PDIF channel 1 and 2 are reserved and should be left unconnected.

(****) - These pins are JTAG interface used for chip production only. They are not intended for boundary scan testing.

5 Electrical Specifications

5.1 Absolute Maximum Rating

Table 10: VS100RX Absolute Maximum Rating

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_i	Digital Inputs voltage		-0.3		5.5	V
T_A	Operating Temperature range		-40		85	°C
T_{STG}	Storage Temperature range		-40		150	°C
V_{DD}	VDD		-0.2		1.1	V
V_{DDIO}	VDD33V		-0.2		3.6	V
V_{DDA18}	AVDD18		-0.2		1.98	V
V_{DDA10}	AVDD10		-0.2		1.1	V
V_{DDA33}	AVDD33		-0.2		3.6	V

Table 11: VS100TX Absolute Maximum Rating

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_I	Digital Inputs voltage		0		5.5	V
T_A	Operating Temperature range		-40		85	°C
T_{STG}	Storage Temperature range		-40		150	°C
V_{DD}	VDD		-0.2		1.1	V
V_{DDIO}	VDD33V		-0.2		3.6	V
V_{DDA18}	AVDD18		-0.2		1.98	V
V_{DDA10}	AVDD10		-0.2		1.1	V
V_{DDA33}	AVDD33		-0.2		3.6	V
V_{TERM33}	AVDD33_TERM		-0.2		3.6	V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this datasheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Important note: please refer to Valens Application Note "AN1011 – Thermal Considerations" for additional guidance regarding the industrial temperature range of -40C to +85C.

5.2 Power Supply Ratings

Table 12: VS100RX Power Supply Current Consumption

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{VDD33}	3.3V Supply Current (V_{DDIO} , V_{DDA33} , V_{TERM33})	HDBaseT and HDMI 4K2K / 24bpp / 30Hz		72	84	mA
I_{VDD18}	1.8V Supply Current (V_{DDA18})			469	490	mA
I_{VDD10}	1.0V Supply Current (V_{DD} , V_{DDA10})			2248	2592	mA
I_{VDD33}	3.3V Supply Current (V_{DDIO} , V_{DDA33} , V_{TERM33})	HDBaseT and HDMI 1080p / 36bpp / 60Hz		55	70	mA
I_{VDD18}	1.8V Supply Current (V_{DDA18})			410	445	mA
I_{VDD10}	1.0V Supply Current (V_{DD} , V_{DDA10})			2200	2400	mA
I_{VDD33}	3.3V Supply Current (V_{DDIO} , V_{DDA33} , V_{TERM33})	Standby –(LPPF1) Low Power Mode #1		20	22	mA
I_{VDD18}	1.8V Supply Current (V_{DDA18})			82	90	mA
I_{VDD10}	1.0V Supply Current (V_{DD} , V_{DDA10})			162	203	mA
I_{VDD33}	3.3V Supply Current (V_{DDIO} , V_{DDA33} , V_{TERM33})	Standby – (LPPF2) Low Power Mode #2		22	24	mA
I_{VDD18}	1.8V Supply Current (V_{DDA18})			172	190	mA
I_{VDD10}	1.0V Supply Current (V_{DD} , V_{DDA10})			270	343	mA
I_{VDD33}	3.3V Supply Current (V_{DDIO} , V_{DDA33} , V_{TERM33})	Ethernet Fallback		22	24	mA
I_{VDD18}	1.8V Supply Current (V_{DDA18})			128	141	mA
I_{VDD10}	1.0V Supply Current (V_{DD} , V_{DDA10})			190	235	mA
I_{VDD33}	3.3V Supply Current (V_{DDIO} , V_{DDA33} , V_{TERM33})	Disconnect State		20	22	mA
I_{VDD18}	1.8V Supply Current (V_{DDA18})			171	188	mA
I_{VDD10}	1.0V Supply Current (V_{DD} , V_{DDA10})			377	471	mA

Table 13: VS100TX Power Supply Current Consumption

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{VDD33}	3.3V Supply Current (V_{DDIO} , V_{DDA33} , V_{TERM33})	HDBaseT and HDMI 4K2K / 24bpp / 30Hz		166	172	mA
I_{VDD18}	1.8V Supply Current (V_{DDA18})			262	272	mA
I_{VDD10}	1.0V Supply Current (V_{DD} , V_{DDA10})			649	821	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{VDD33}	3.3V Supply Current (V_{DDIO} , V_{DDA33} , V_{TERM33})	HDBaseT and HDMI 1080p / 36bpp / 60Hz		160	162	mA
I_{VDD18}	1.8V Supply Current (V_{DDA18})			265	272	mA
I_{VDD10}	1.0V Supply Current (V_{DD} , V_{DDA10})			600	779	mA
I_{VDD33}	3.3V Supply Current (V_{DDIO} , V_{DDA33} , V_{TERM33})	Standby - Low Power Mode #1		20	22	mA
I_{VDD18}	1.8V Supply Current (V_{DDA18})			48	53	mA
I_{VDD10}	1.0V Supply Current (V_{DD} , V_{DDA10})			96	120	mA
I_{VDD33}	3.3V Supply Current (V_{DDIO} , V_{DDA33} , V_{TERM33})	Standby - Low Power Mode #2		20	22	mA
I_{VDD18}	1.8V Supply Current (V_{DDA18})			100	111	mA
I_{VDD10}	1.0V Supply Current (V_{DD} , V_{DDA10})			168	211	mA
I_{VDD33}	3.3V Supply Current (V_{DDIO} , V_{DDA33} , V_{TERM33})	Ethernet Fallback		13	14	mA
I_{VDD18}	1.8V Supply Current (V_{DDA18})			78	86	mA
I_{VDD10}	1.0V Supply Current (V_{DD} , V_{DDA10})			116	146	mA
I_{VDD33}	3.3V Supply Current (V_{DDIO} , V_{DDA33} , V_{TERM33})	Disconnect State		15	17	mA
I_{VDD18}	1.8V Supply Current (V_{DDA18})			130	143	mA
I_{VDD10}	1.0V Supply Current (V_{DD} , V_{DDA10})			258	323	mA

5.3 Reference Clock Requirements

Either LVDS oscillator or CMOS oscillator may be used to generate a 125MHz reference clock input. LVDS is recommended due to it's lower jitter and phase noise.

5.3.1 LVDS oscillator's requirements

The LVDS oscillator should comply with the following requirements:

Table 14: LVDS Oscillator Requirements

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Note
F_{CLK}	Reference clock frequency			125		MHz	
F_{TOL}	Input clock frequency	includes aging,	-100		+100	PPM	

	tolerance	temperature change and supply voltage swing					
F_{DCD}	Reference clock duty cycle		40	50	60	%	
$T_{FALL/RISE}$	Rise / Fall Time	20% - 80% differential	260		2400	pSec	
V_I	Single-ended Input Voltage Range		0		1.89	V	
$\|V_{ID}\|$	Differential input voltage range		100		600	mV	Fig2
V_{CM}	Common-mode input range		600	1200	1800	mV	
R_{IN}	Input differential resistance		80		120	Ω	

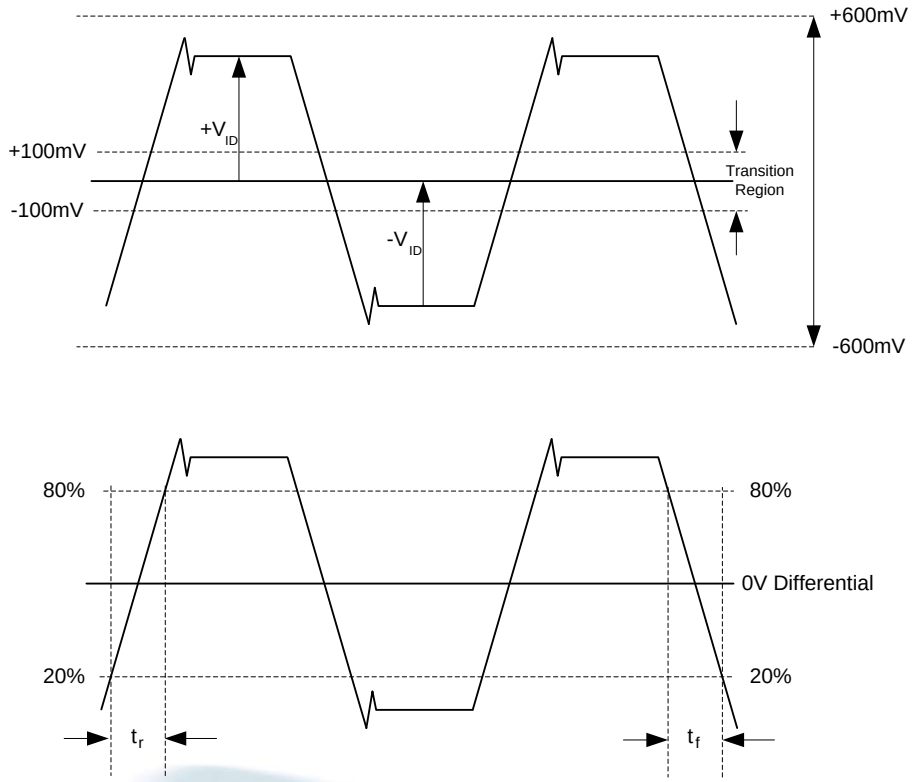


Figure 18: Input Reference Clock Wave Diagram

5.3.2 CMOS oscillator's requirements

The CMOS Oscillator should comply with the following requirements:

- Frequency: 125MHz.
- Accuracy: ±100ppm in any time. This includes aging, temperature change and supply voltage swing.
- Phase noise: must be kept below the phase noise mask specified in Table 15.

Table 15: Phase Noise Mask

Freq(Hz)	Phase Noise (dBc/Hz)
1	-30
10	-60
1e2	-90
1e3	-127
1e4	-148
1e5	-150
1e10	-150

Refer to AN1001: HW Design Guidelines for schematics illustrating how to connect LVDS or CMOS oscillators to the VS100RX/TX chipset.

5.4 Recommended Operating Conditions

5.4.1 Electrical Characteristics

Table 16: VS100RX Electrical Specification

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Digital pads (pad types D, PD, PU and OD)						
V_{IH}	Input voltage high	Digital pads	2.0		5.5	V
V_{IL}	Input voltage low		-0.3		0.8	V
R_{PU}	Pull-up resistor		63	92	142	KΩ
R_{PD}	Pull-down resistor		57	91	159	KΩ
C_{IN}	Input capacitance				2	pF

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	Output voltage High		2.4			V
V_{OL}	Output voltage Low				0.4	V
LVDS pads						
Vd	Input clock amplitude	Differential peak-to-peak	200		1200	mV
Vc	Input clock common-mode		600		1800	mV
HDBT transceiver						
V_{hdbt_vcm}	HDBaseT common mode operational voltage (Transformer central tap)		1.71	1.8 ± 5%	1.89	V
V_{hdbt_vdiff}	HDBaseT operation differential peak-2-peak voltage				3.4	V
V_{hdbt_vse}	HDBaseT single ended pin voltage	HDBaseT mode	0.85		2.75	V
		Fallback mode	0.75		2.85	V
TMDS Drivers DC specification						
AVcc	TMDS reference voltage		3.135	3.3	3.465	V
V_{OFF}	Single-ended standby (off) output voltage	Compliance point TP1 as defined in Section 4.2.4 of HDMI Specification V1.4.	AVcc-0.01		AVcc+0.01	V
V_{SWING}	Single-ended output swing voltage	Compliance point TP1 as defined in Section 4.2.4 of HDMI Specification V1.4.	400		600	mV
V_H	Single-ended high level output voltage	if attached Sink supports TMDSCLK<= 165Mhz	AVcc-0.01		AVcc+0.01	V
		if attached Sink supports TMDSCLK > 165Mhz	AVcc – 0.2		AVcc+0.01	V
V_L	Single-ended low level output voltage	if attached Sink supports TMDSCLK<= 165Mhz	AVcc – 0.6		AVcc–0.4	V
		if attached Sink supports TMDSCLK > 165Mhz	AVcc – 0.7		AVcc–0.4	V
R_{LOAD}	50 ohm resistor loads Source Termination		45	50	55	Ω

Table 17: VS100TX Electrical Specification

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Digital pads						
VIH	Input voltage high	Digital pads	2.0		5.5	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIL	Input voltage low		-0.3		0.8	V
C_{IN}	Input capacitance				2	pF
R_{PU}	Pull-up resistor		63	92	142	KΩ
R_{PD}	Pull-down resistor		57	91	159	KΩ
V_{OH}	Output voltage High		2.4			V
V_{OL}	Output voltage Low				0.4	V
LVDS pads						
Vd	Input clock amplitude	Differential peak-to-peak	200		1200	mV
Vc	Input clock common-mode		600		1800	mV
HDBT transceiver						
V_{hdbt_vcm}	HDBaseT common mode operational voltage (Transformer central tap)		1.71	1.8 ± 5%	1.89	V
V_{hdbt_vdiff}	HDBaseT operation differential peak-2-peak voltage				3.4	V
V_{hdbt_vse}	HDBaseT single ended pin voltage	HDBaseT mode	0.85		2.75	V
		Fallback mode	0.75		2.85	V
TMDS Receivers DC specification						
V_{TH}	Differential Input Threshold (+)				+75	mV
V_{TL}	Differential Input Threshold (-)		-75			mV
$\|V_{ID}\|$	Differential Input Voltage (pk-pk)	Refer tp HDMI specification 1.4 for further details	150		1560	mV
V_{ICM1}	Input common mode	Vterm33=3300+	Vterm33 -400	3300	Vterm33 -37.5	mV
V_{ICM2}	Input common mode	Vterm33 = 3.3V +/- 5%	Vterm33 -10	3300	Vterm33+10	mV
$R_{IN(SE)}$	Single ended input impedance			50		Ω
TMDS Drivers DC specification						
AVcc	TMDS reference voltage		3.135	3.3	3.465	V
V_{OFF}	Single-ended standby (off) output voltage	Compliance point TP1 as defined in Section 4.2.4 of HDMI Specification V1.4.	AVcc-0.01		AVcc+0.01	V
V_{SWING}	Single-ended output swing voltage	Compliance point TP1 as defined in Section 4.2.4 of HDMI Specification V1.4.	400		600	mV
V_H	Single-ended high level output	if attached Sink	AVcc-0.01		AVcc+0.01	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	voltage	supports TMDSCLK<= 165Mhz				
		if attached Sink supports TMDSCLK > 165Mhz	AVcc–0.2		AVcc + 0.01	V
V_L	Single-ended low level output voltage	if attached Sink supports TMDSCLK<= 165Mhz	AVcc–0.6		AVcc – 0.4	V
		if attached Sink supports TMDSCLK > 165Mhz	AVcc–0.7		AVcc – 0.4	V
R_{LOAD}	50 ohm resistor loads (Source Termination)		45	50	55	Ω

Table 18: VS100RX Power Supply

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	VDD		Typ-5%	1.0	Typ+5%	V
V_{DDIO}	VDD33V		Typ-5%	3.3	Typ+5%	V
V_{DDA18}	AVDD18		Typ-5%	1.8	Typ+5%	V
V_{DDA10}	AVDD10		Typ-5%	1.0	Typ+5%	V
V_{DDA33}	AVDD33		Typ-5%	3.3	Typ+5%	V

Table 19: VS100TX power supply

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	VDD		Typ-5%	1.0	Typ+5%	V
V_{DDIO}	VDD33V		Typ-5%	3.3	Typ+5%	V
V_{DDA18}	AVDD18		Typ-5%	1.8	Typ+5%	V
V_{DDA10}	AVDD10		Typ-5%	1.0	Typ+5%	V
V_{DDA33}	AVDD33		Typ-5%	3.3	Typ+5%	V
V_{TERM33}	AVDD33_TERM		Typ-5%	3.3	Typ+5%	V

5.4.2 Timing

5.4.2.1 Reset Signal Timing

The RESET_IN signal must be held active at leaset Trst-hd msec after all chip supply voltages are stable. (i.e. VDD, VDD33V, AVDD10, AVDD18 and AVDD33).

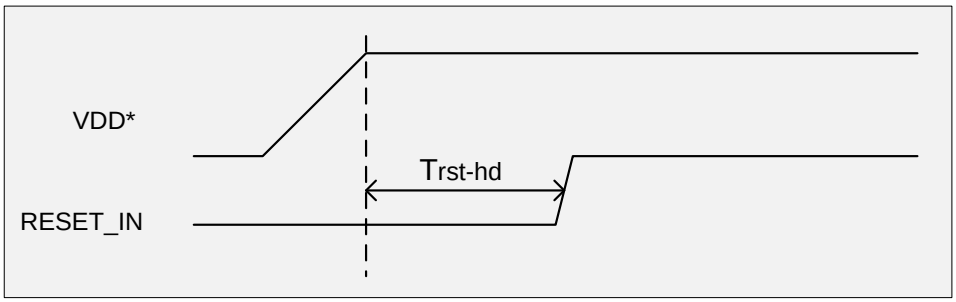


Figure 19: Reset Signal Timing

5.4.2.2 AC Specification

Table 20: VS100RX AC Specification

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
General						
	Reference clock frequency			125		MHz
	Reference clock frequency tolerance		-100		+100	PPM
	Reference clock duty cycle		40	50	60	%
T_{rst-hd}	RESET_IN hold time after power supply stabilization		1			µs

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Digital pads MII						
T_{MII_FS}	MII_Tx_CLK, MII_RX_CLK frequency			25		MHz
T_{MII_DC}	MII_Tx_CLK, MII_RX_CLK duty cycle		35		65	%
T_{MII_DLY}	MII_RX_DV, MII_RXD[3:0], MII_Rx_ERR output delay	relative to RX_CLK	10		30	ns
T_{MII_SU}	MII_TX_EN, MII_TXD[1:0], MII_TXD[3:2]_GPIO, MII_TX_ERR_GPIO setup	relative to TX_CLK	10			ns
T_{MII_HD}	MII_TX_EN, MII_TXD[1:0], MII_TXD[3:2]_GPIO, MII_TX_ERR_GPIO hold	relative to TX_CLK	0			ns
T_{MDIO_TC}	MII_MDC period		400			ns
T_{MDIO_SU}	MII_MDIO setup	MDIO sourced by MAC	10			ns
T_{MDIO_HD}	MII_MDIO hold	MDIO sourced by MAC	10			ns
T_{MDIO_DY}	MII_MDIO delay	MDIO source by PHY	0		300	ns
RMII mode						
T_{RMII_FS}	MII_Tx_CLK frequency			50		MHz
T_{RMII_DC}	MII_Tx_CLK duty cycle		35		65	%
T_{RMII_SU}	MII_TXD[1:0], MII_TX_EN, MII_RXD[1:0], MII_Rx_DV, MII_RX_ERR data setup	relative to MII_Tx_CLK rising edge	4			ns
T_{RMII_HD}	MII_TXD[1:0], MII_TX_EN, MII_RXD[1:0], MII_Rx_DV, MII_RX_ERR data hold	relative to MII_Tx_CLK rising edge	2			ns
EEPROM (I^2C)						
Same as the Host interface (I^2C), see below						
EEPROM SPI						
Support all standard devices, maximum clock rate = 5MHz						
$t_{HD;DAT}$	Data hold time	0				Ns
$t_{SU;DAT}$	Data set-up time	50				ns
Host interface (I^2C)						
		Standard Mode		Fast Mode		
		Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	100	0	400	KHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0		0.6		us
t_{LOW}	LOW period of the SCL clock	4.7		1.3		us
t_{HIGH}	HIGH period of the SCL clock	4.0		0.6		us
$t_{SU;STA}$	Set-up time for a repeated START condition	4.7		0.6		us

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{HD;DAT}$	Data hold time	0	3.45	0	0.9	us
$t_{SU;DAT}$	Data set-up time	250		100(1*)		ns
t_r	Rise time of both SDA and SCL signals		1000	$20+0.1C_b$(2*)	300	ns
t_f	Fall time of both SDA and SCL signals		300	$20+0.1C_b$(2*)	300	ns
$t_{SU;STO}$	Set-up time for STOP condition	4.0		0.6		us
t_{BUF}	Bus free time between a STOP and START condition	4.7		1.3		us
C_b	Capacitive load for each bus line		400		400	pF
(1*) A Fast-mode I2C-bus device can be used in a Standard-mode I2C -bus system, but the requirement tSU;DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr max + tSU;DAT = 1000 + 250 = 1250 ns (according to the Standard-mode I2C -bus specification) before the SCL line is released. (2*) Cb = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall-times are allowed.						
TMDS Drivers specification						
-	Maximum serial data rate				3.4	Gbps
$F_{TMDSCLK}$	TMDS output clock frequency	On HDMISER_TMDSCLKP/N outputs	25		340	MHz
$P_{TMDSCLK}$	TMDSCLK period	R_L=50Ω ±10%	2.94		40	ns
t_{CDC}	TMDSCLK duty cycle	tCDC = tCPH / PTMDSCLK R_L=50Ω ±10%	40	50	60	%
t_{CPH}	TMDSCLK high time	R_L=50Ω ±10%	4	5	6	UI
t_{CPL}	TMDSCLK low time	R_L=50Ω ±10%	4	5	6	UI
	TMDSCLK jitter [1]	R_L=50Ω ±10%			0.25	UI
$t_{SK(P)}$	Intra-Pair (Pulse) skew. (between a pair lanes)	R_L=50Ω ±10%			0.15	UI
$t_{SK(PP)}$	Inter-Pair (Pulse) skew (between different pairs).	R_L=50Ω ±10%			2	UI
t_r	Differential output signal rise time	20% to 80%, RL = 50Ω±10%	75			ps
t_f	Differential output signal fall time	20% to 80%, RL = 50Ω±10%	75			ps

Table 21: VS100TX AC Specification

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
General						
	Reference clock frequency	LVDS levels		125		MHz
	Input clock frequency tolerance		-100		+100	PPM
	Reference clock duty cycle		40	50	60	%
T_{rst-hd}	RESET_IN hold time after power supply stabilization		1			µs
Digital pads MII						

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{MII_FS}	MII_Tx_CLK, MII_RX_CLK frequency			25		MHz
T_{MII_DC}	MII_Tx_CLK, MII_RX_CLK duty cycle		35		65	%
T_{MII_DLY}	MII_RX_DV, MII_RXD[3:0], MII_Rx_ERR output delay	relative to RX_CLK	10		30	ns
T_{MII_SU}	MII_TX_EN, MII_TXD[1:0], MII_TXD[3:2]_GPIO, MII_TX_ERR_GPIO setup	relative to TX_CLK	10			ns
T_{MII_HD}	MII_TX_EN, MII_TXD[1:0], MII_TXD[3:2]_GPIO, MII_TX_ERR_GPIO hold	relative to TX_CLK	0			ns
T_{MDIO_TC}	MII_MDC period		400			ns
T_{MDIO_SU}	MII_MDIO setup	MDIO sourced by MAC	10			ns
T_{MDIO_HD}	MII_MDIO hold	MDIO sourced by MAC	10			ns
T_{MDIO_DY}	MII_MDIO delay	MDIO source by PHY	0		300	ns
RMII mode						
T_{RMII_FS}	MII_Tx_CLK frequency			50		MHz
T_{RMII_DC}	MII_Tx_CLK duty cycle		35		65	%
T_{RMII_SU}	MII_TXD[1:0], MII_TX_EN, MII_RXD[1:0], MII_Rx_DV, MII_RX_ERR data setup	relative to MII_Tx_CLK rising edge	4			ns
T_{RMII_HD}	MII_TXD[1:0], MII_TX_EN, MII_RXD[1:0], MII_Rx_DV, MII_RX_ERR data hold	relative to MII_Tx_CLK rising edge	2			ns
EEPROM (I^2C)						
Same as the Host interface (I^2C), see below						
EEPROM SPI						
Supports all standard devices, maximum clock rate = 5MHz						
Host Interface (I^2C)						

		Standard Mode		Fast Mode		
		Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	100	0	400	KHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0		0.6		us
t_{LOW}	LOW period of the SCL clock	4.7		1.3		us
t_{HIGH}	HIGH period of the SCL clock	4.0		0.6		us
$t_{SU;STA}$	Set-up time for a repeated START condition	4.7		0.6		us
$t_{HD;DAT}$	Data hold time	0	3.45	0	0.9	us
$t_{SU;DAT}$	Data set-up time	250		$100^{(1*)}$		ns
t_r	Rise time of both SDA and SCL signals		1000	$20+0.1C_b{}^{(2*)}$	300	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_f	Fall time of both SDA and SCL signals		300	$20+0.1C_b$(2*)	300	ns
$t_{SU;STO}$	Set-up time for STOP condition	4.0		0.6		us
t_{BUF}	Bus free time between a STOP and START condition	4.7		1.3		us
C_b	Capacitive load for each bus line		400		400	pF
(1*) A Fast-mode I2C-bus device can be used in a Standard-mode I2C -bus system, but the requirement tSU;DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr max + tSU;DAT = 1000 + 250 = 1250 ns (according to the Standard-mode I2C -bus specification) before the SCL line is released. (2*) Cb = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall-times are allowed.						
TMDS Receivers specification						
-	Maximum serial data rate				3.4	Gbps
F_{PCLK}	TMDS Input clock frequency	On HDMIDES_TMDSCLKP/N	25		340	MHz
Intra-pair skew tolerance		$F_{PCLK} \leq 225MHz$			0.4	UI
		$F_{PCLK} > 225MHz$			0.15UI + 112ps	mixed
Inter per skew					2UI + 1.78ns	mixed
	Input Clock Jitter Tolerance	Relative to Ideal Recovered Clock as defined in HDMI specification 1.4			0.30	UI
TMDS Drivers specification						
-	Maximum serial data rate				3.4	Gbps
$F_{TMDSCLK}$	TMDS output clock frequency	On HDMISER_TMDSCLKP/N outputs	25		340	MHz
$P_{TMDSCLK}$	TMDSCLK period	R_L=50Ω ±10%	2.94		40	ns
t_{CDC}	TMDSCLK duty cycle	tCDC = tCPH / PTMDSCLK R_L=50Ω ±10%	40	50	60	%
t_{CPH}	TMDSCLK high time	R_L=50Ω ±10%	4	5	6	UI
t_{CPL}	TMDSCLK low time	R_L=50Ω ±10%	4	5	6	UI
	TMDSCLK jitter [1]	R_L=50Ω ±10%			0.25	UI
$t_{SK(P)}$	Intra-Pair (Pulse) skew. (between a pair lanes)	R_L=50Ω ±10%			0.15	UI
$t_{SK(PP)}$	Inter-Pair (Pulse) skew (between different pairs).	R_L=50Ω ±10%			2	UI
t_r	Differential output signal rise time	20% to 80%, R_L = 50Ω±10%	75			ps
t_f	Differential output signal fall time	20% to 80%, R_L = 50Ω±10%	75			ps

Relative to ideal recovery clock as specified in Section 4.2.3 of HDMI specification, V1.3a.

5.5 ESD Ratings

Table 22: ESD Ratings

Test	Value	Unit
HBM (per JEDEC JS-001)	± 2000	V
CDM (per JEDEC JESD22-C101)	± 500	
Latch Up (per JEDEC JESD78)	± 100	mA
	Over-voltage: 1.5x supply at 85°C	

6 Package Mechanical Specification

6.1 VS100TX package mechanical specification

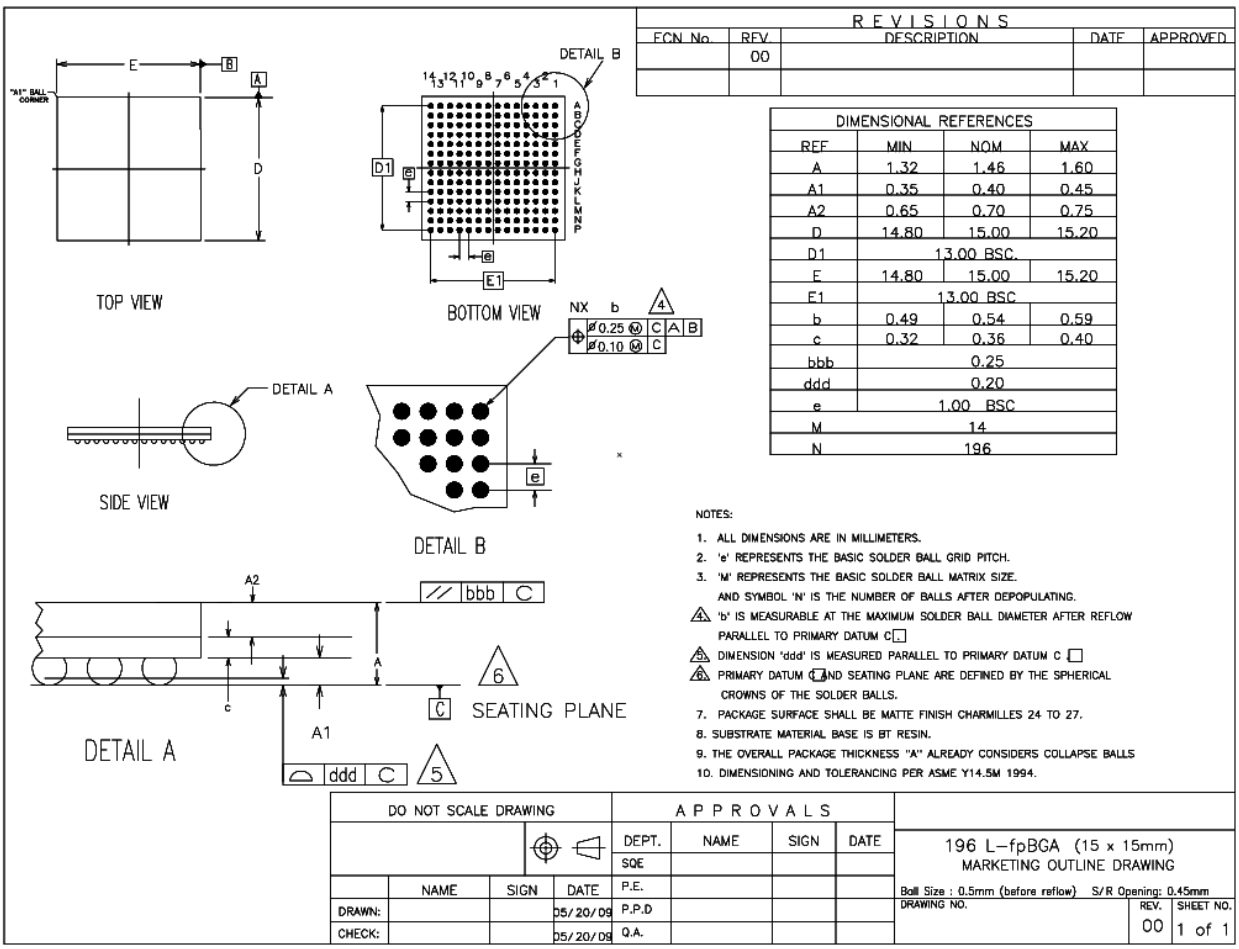


Figure 20: VS100TX – Mechanical Information

6.2 VS100TX package details

RoHS & Green Compliant, 196-pin LBGA, 15mm x 15mm

6.3 VS100RX package mechanical specification

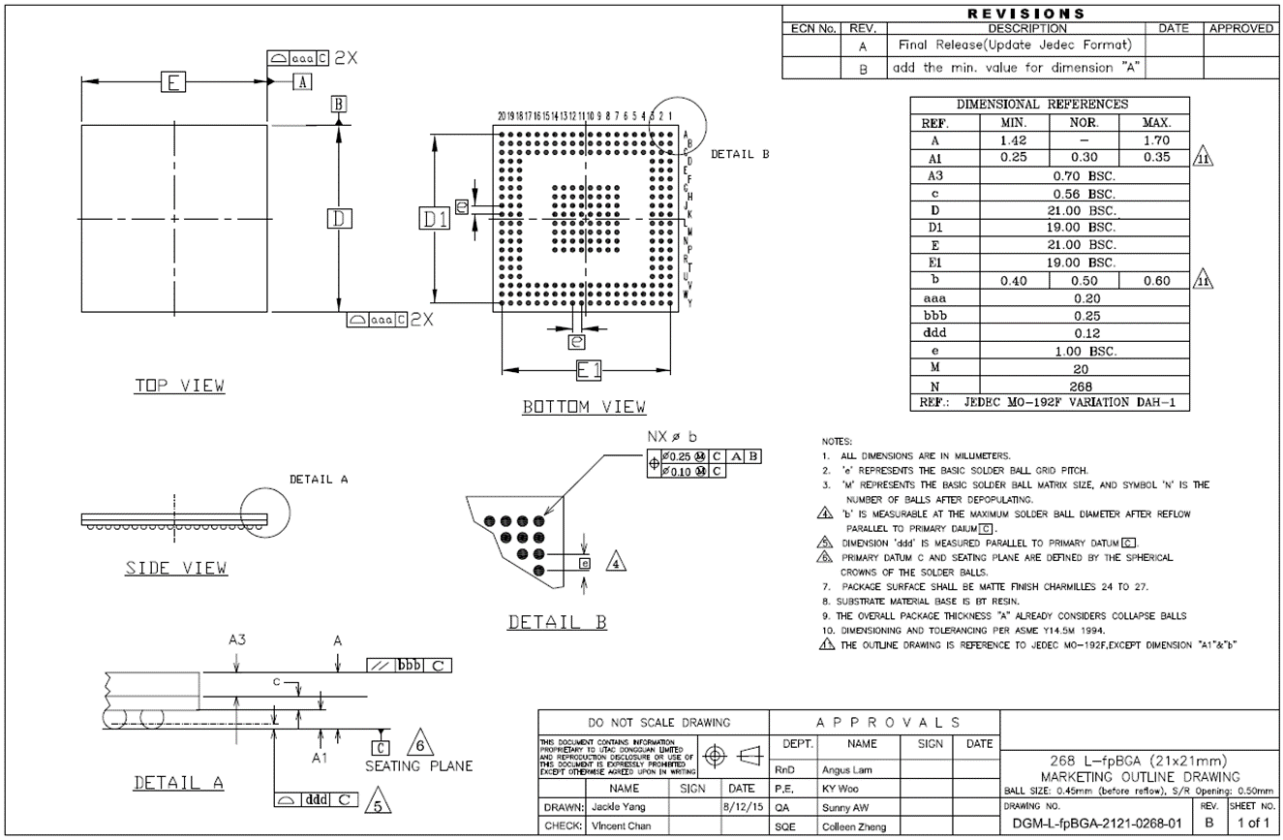


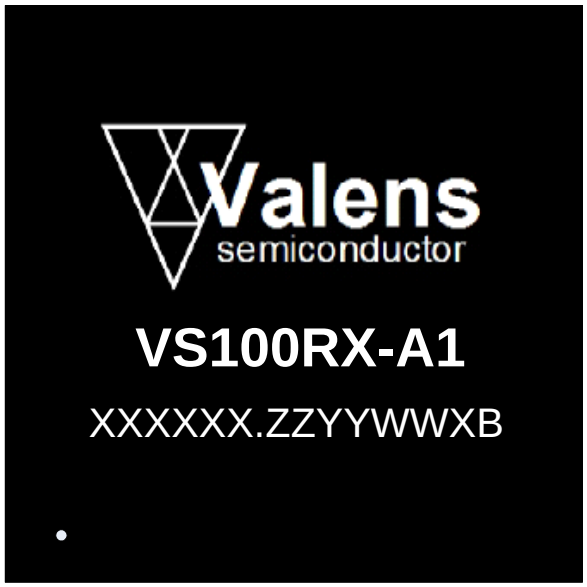
Figure 21: VS100RX – Mechanical Information

6.4 VS100RX package details

RoHS & Green Compliant, 268-pin LBGA, 21mm x 21mm

6.5 VS100 chipset Marking Diagram

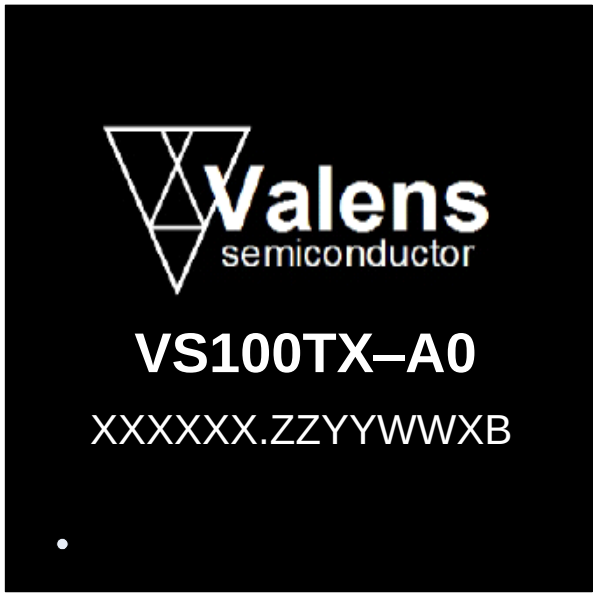
6.5.1 VS100Rx Device



Product Part Number:
VS100RX-A1

Wafer lot #: XXXXXX.ZZ
Assembly Year: YY
Assembly Work Week: WW
Assembly lot split #: X (X= A,B,C or D)
Product identifier: B

6.5.2 VS100Tx Device



Product Part Number:
VS100TX-A0

Wafer lot #: XXXXXX.ZZ
Assembly Year: YY
Assembly Work Week: WW
Assembly lot split #: X (X= A,B,C or D)
Product identifier: B

6.6 Ordering Codes

Ordering Code	Item Description
VS100TX-A0	Valens VS100 transmitter chip
VS100RX-A1	Valens VS100 receiver chip