

### ● General Description

The AGM035N10A combines advanced trench MOSFET technology with a low resistance package to provide extremely low  $R_{DS(ON)}$ .

This device is ideal for load switch and battery protection applications.

### ● Features

- Advance high cell density Trench technology
- Low  $R_{DS(ON)}$  to minimize conductive loss
- Low Gate Charge for fast switching
- Low Thermal resistance

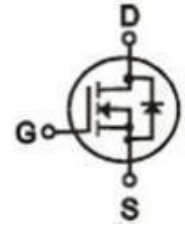
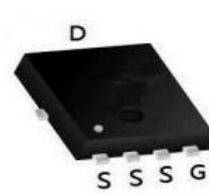
### ● Application

- MB/VGA Vcore
- SMPS 2<sup>nd</sup> Synchronous Rectifier
- POL application
- BLDC Motor driver

### Product Summary

BVDSS	RDS(ON)	ID
100V	3.3mΩ	112A

### PDFN5\*6 Pin Configuration



### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
AGM035N10A	AGM035N10A	PDFN5*6	----	----	3000

**Table 1. Absolute Maximum Ratings (TA=25°C)**

Symbol	Parameter	Value	Unit
VDS	Drain-Source Voltage (VGS=0V)	100	V
VGS	Gate-Source Voltage (VDS=0V)	±20	V
ID	Drain Current-Continuous(Tc=25°C) <b>(Note 1)</b>	112	A
	Drain Current-Continuous(Tc=100°C)	78	A
IDM (pulse)	Drain Current-Continuous@ Current-Pulsed <b>(Note 2)</b>	400	A
PD	Maximum Power Dissipation(Tc=25°C)	104	w
	Maximum Power Dissipation(Tc=100°C)	42	w
EAS	Avalanche energy <b>(Note 3)</b>	375	mJ
TJ,TSTG	Operating Junction and Storage Temperature Range	-55 To 150	°C

**Table 2. Thermal Characteristic**

Symbol	Parameter	Typ	Max	Unit
RθJA	Thermal Resistance Junction-ambient (Steady State) <sup>1</sup>	---	50	°C/W
RθJC	Thermal Resistance Junction-Case <sup>1</sup>	---	1.2	°C/W

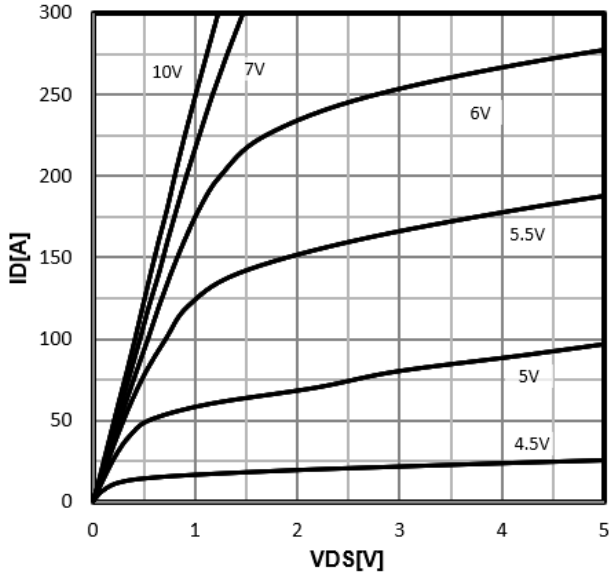
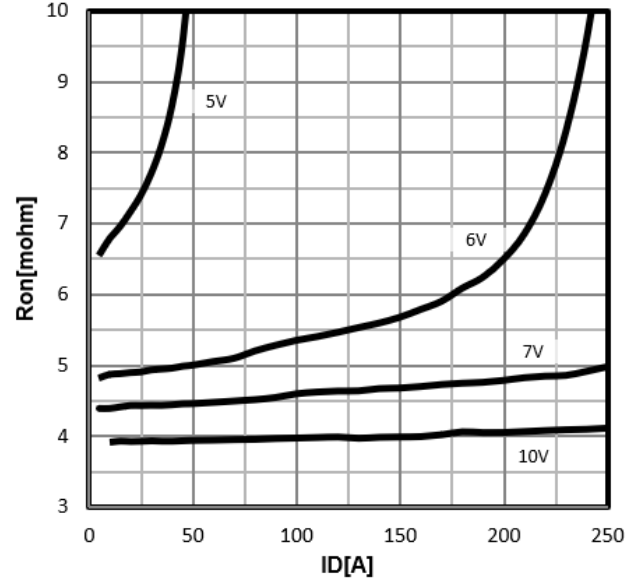
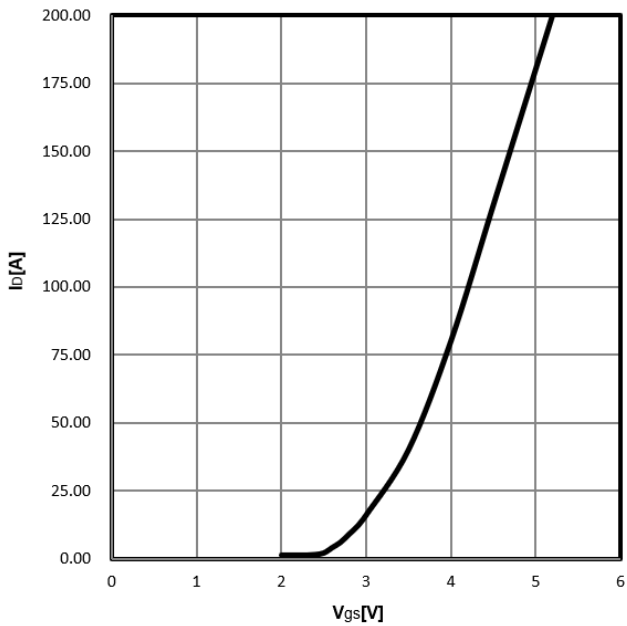
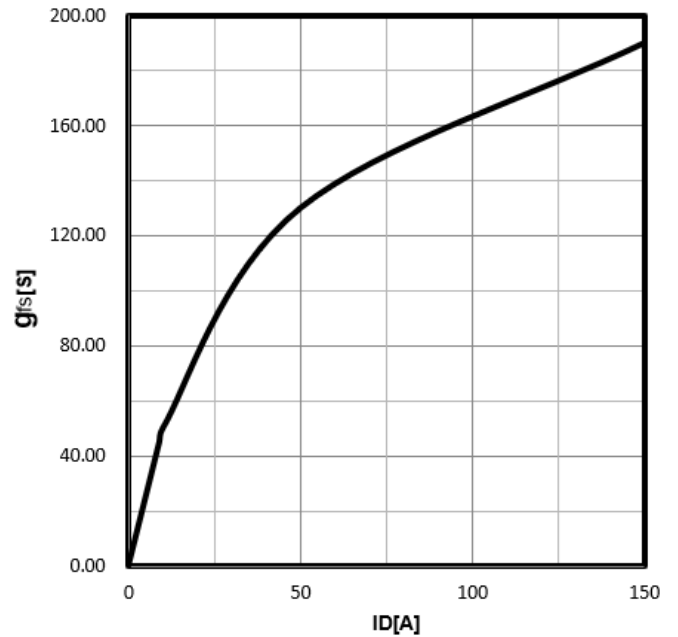
**Table 3. Electrical Characteristics (TA=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>On/Off States</b>						
BVDSS	Drain-Source Breakdown Voltage	VGS=0V ID=250μA	100	--	--	V
IDSS	Zero Gate Voltage Drain Current	VDS=100V, VGS=0V	--	--	1	μA
IGSS	Gate-Body Leakage Current	VGS=±20V, VDS=0V	--	--	±100	nA
VGS(th)	Gate Threshold Voltage	VDS=VGS, ID=250μA	1.2	1.8	2.5	V
gFS	Forward Transconductance	VDS=5V, ID=56A	--	130	--	S
RDS(on)	Drain-Source On-State Resistance	VGS=10V, ID=20A	--	3.3	4.0	mΩ
		VGS=4.5V, ID=15A	--	4.2	5.7	mΩ
<b>Dynamic Characteristics</b>						
Ciss	Input Capacitance	VDS=50V, VGS=0V, F=1MHZ	--	3500	--	pF
Coss	Output Capacitance		--	100	--	pF
Crss	Reverse Transfer Capacitance		--	27	--	pF
Rg	Gate resistance	VGS=0V, VDS=0V, f=1.0MHz	--	2.1	--	Ω
<b>Switching Times</b>						
td(on)	Turn-on Delay Time	VGS=10V, VDS=56V, ID=56A, RGEN=5Ω	--	25	--	nS
tr	Turn-on Rise Time		--	33	--	nS
td(off)	Turn-Off Delay Time		--	95	--	nS
tf	Turn-Off Fall Time		--	75	--	nS
Qg	Total Gate Charge	VGS=10V, VDS=50V, ID=56A	--	67.2	--	nC
Qgs	Gate-Source Charge		--	16.9	--	nC
Qgd	Gate-Drain Charge		--	16.9	--	nC
<b>Source-Drain Diode Characteristics</b>						
ISD	Source-Drain Current(Body Diode)		--	--	112	A
VSD	Forward on Voltage	VGS=0V, IS=56A	--	--	1.2	V
trr	Reverse Recovery Time	IF=20A , dI/dt=100A/μs , TJ=25°C	--	82	--	ns
Qrr	Reverse Recovery Charge		--	180	--	nc

Notes 1.The maximum current rating is package limited.

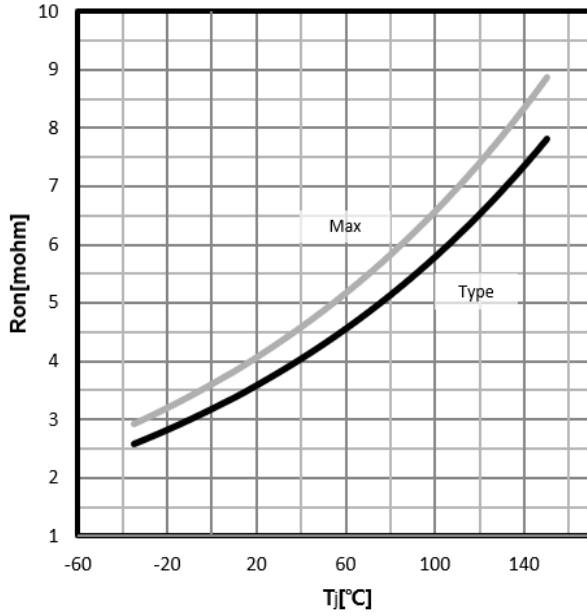
Notes 2.Repetitive Rating: Pulse width limited by maximum junction temperature

Notes 3.EAS condition: TJ=25°C

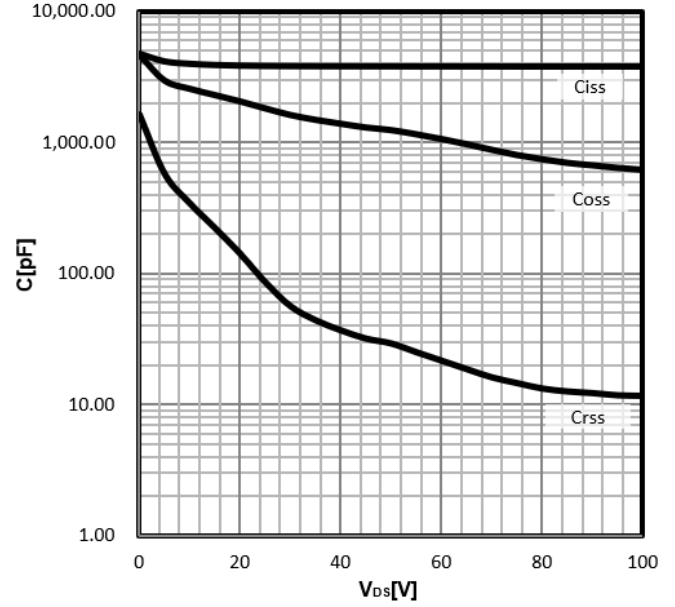
**Characteristics Curve:**
**Typ. output characteristics**  
 $I_D = f(V_{DS})$ 

**Typ. drain-source on resistance**  
 $R_{DS(on)} = f(I_D)$ 

**Typ. transfer characteristics**  
 $I_D = f(V_{GS})$ 

**Typ. forward transconductance**  
 $g_{fs} = f(I_D)$ 


**Drain-source on-state resistance**

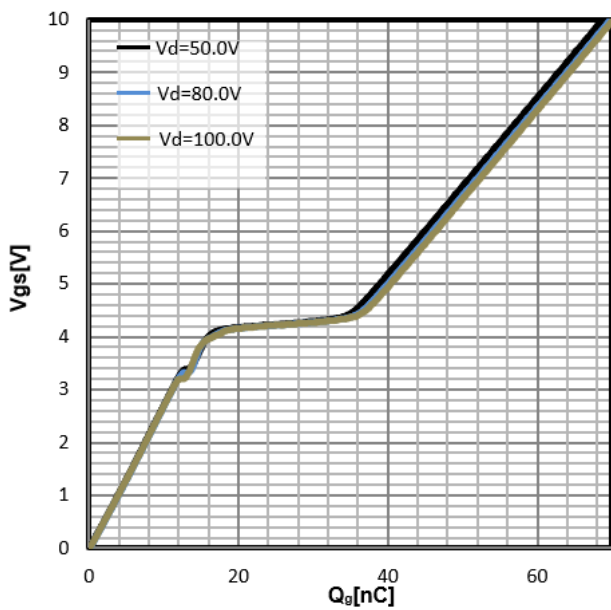
$$R_{DS(on)} = f(T_j); I_D = 56A; V_{GS} = 10V$$


**Typ. capacitances**

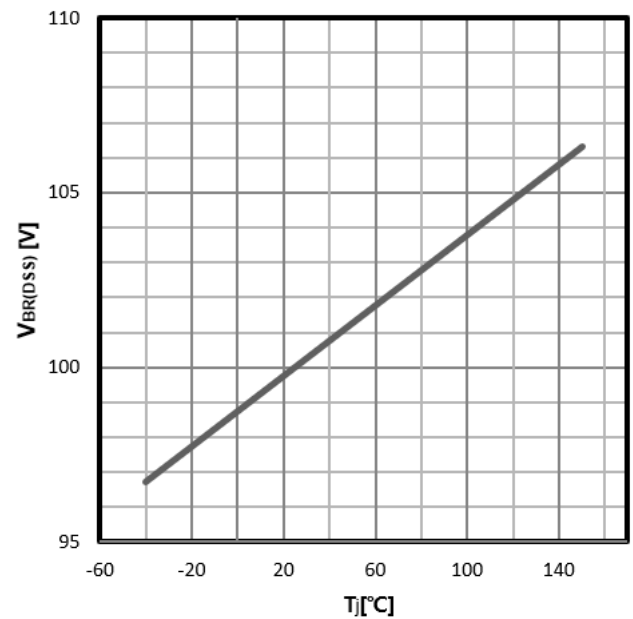
$$C = f(V_{DS}); V_{GS} = 0V; f = 1MHz$$

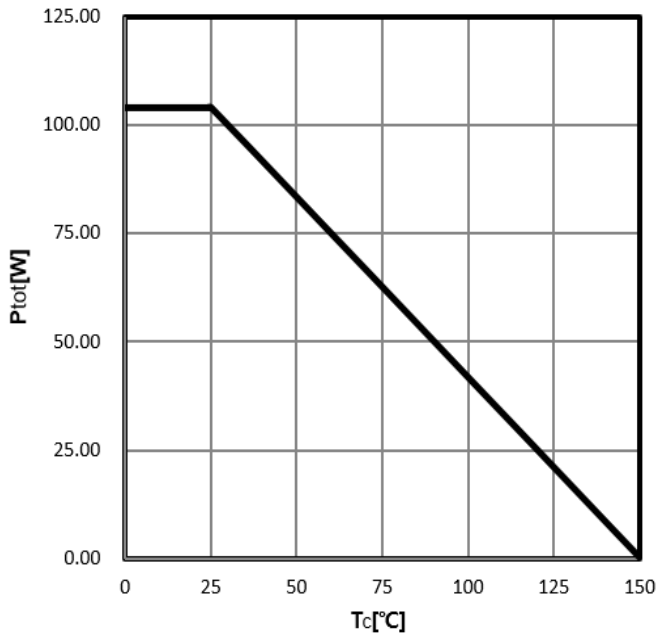
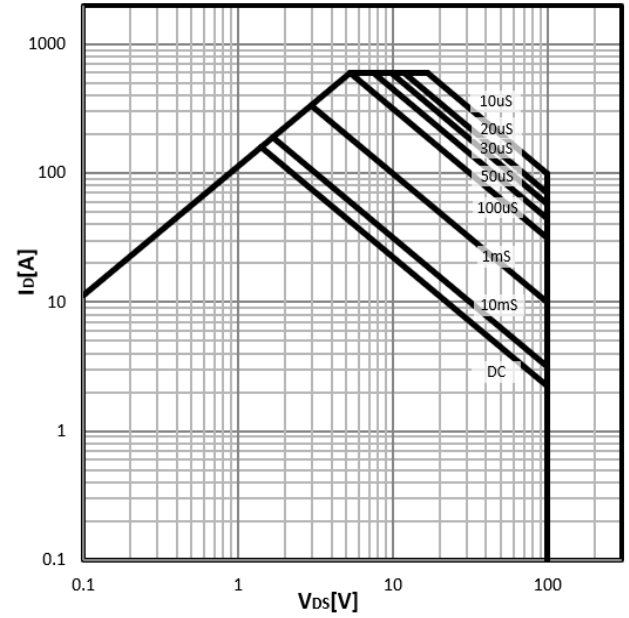

**Typ. gate charge**

$$V_{GS} = f(Q_{gate}); I_D = 20A$$


**Drain-source breakdown voltage**

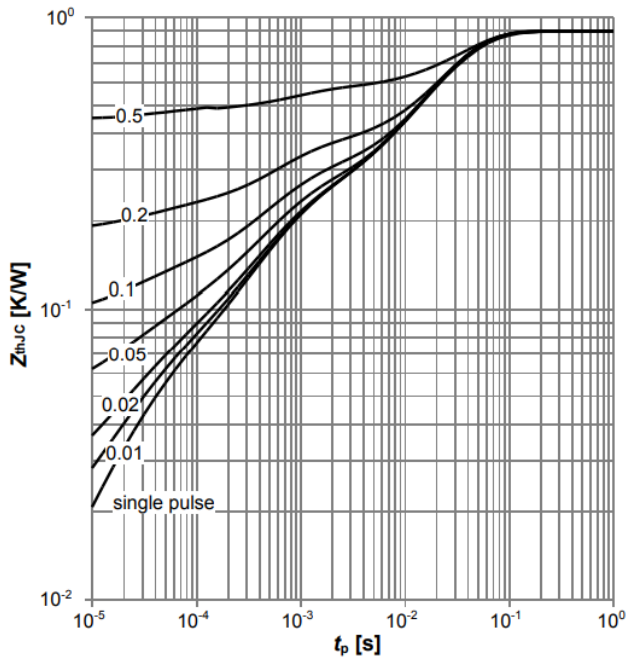
$$V_{BR(DSS)} = f(T_j); I_D = 250\mu A$$



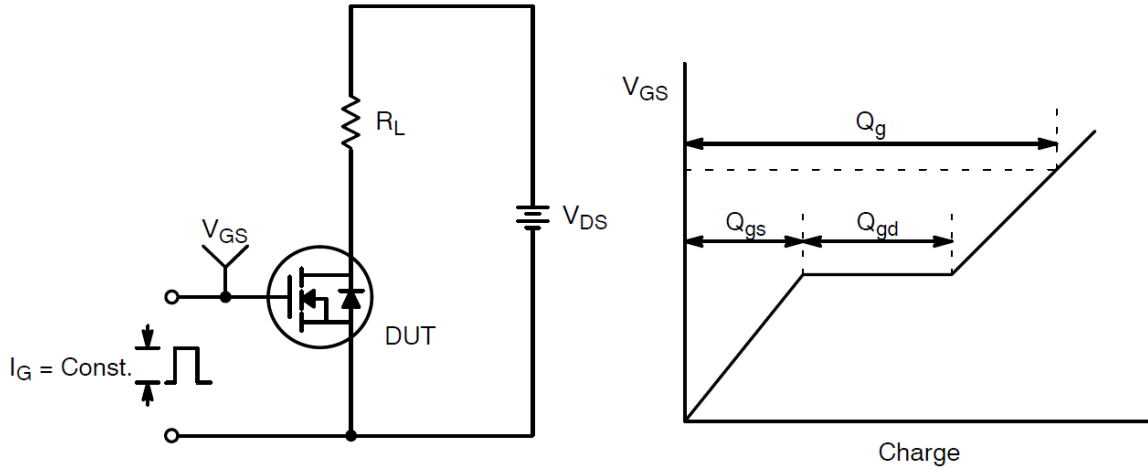
$P_{tot}=f(T_c)$ 

 $I_D=f(V_{DS})$ 


Max. transient thermal impedance

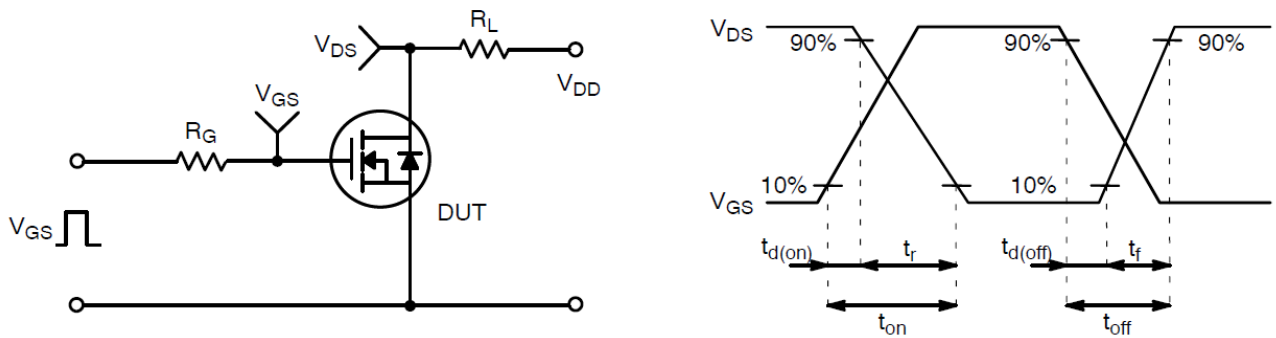
$Z_{thJC}=f(t_p)$



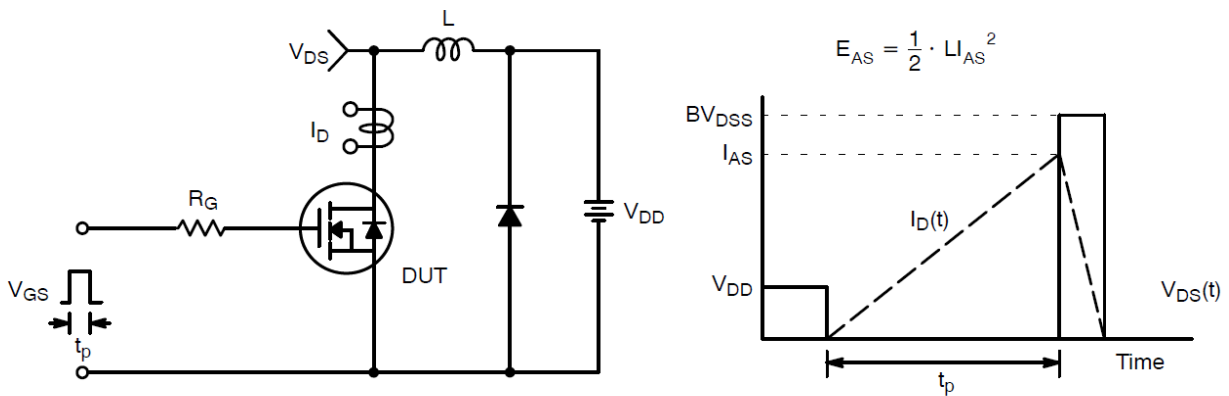
**Test Circuit and Waveform:**



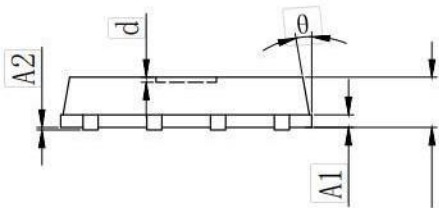
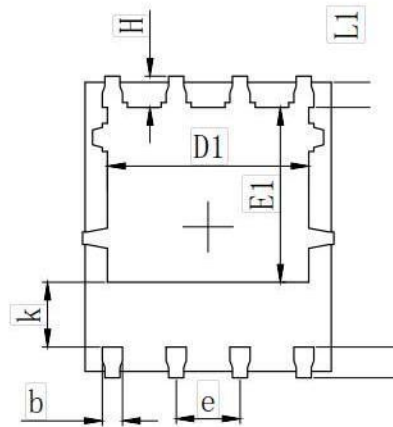
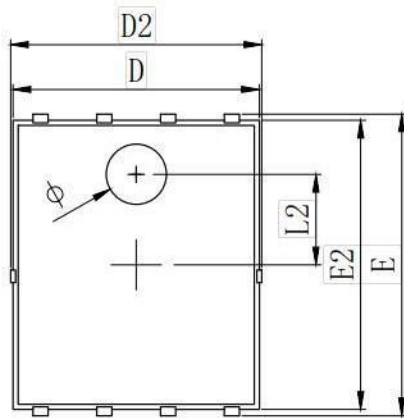
**Gate Charge Test Circuit & Waveform**



**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching Test Circuit & Waveforms**

**•Dimensions (DFN5×6)**


SYMBOL	MILLIMETER		
	MIN	Typ.	MAX
A	0.900	1.000	1.100
A1	0.254 REF.		
A2	0~0.05		
D	4.824	4.900	4.976
D1	3.910	4.010	4.110
D2	4.924	5.000	5.076
E	5.924	6.000	6.076
E1	3.375	3.475	3.575
E2	5.674	5.750	5.826
b	0.350	0.400	0.450
e	1.270 TYP.		
L	0.534	0.610	0.686
L1	0.424	0.500	0.576
L2	1.800 REF.		
k	1.190	1.290	1.390
H	0.549	0.625	0.701
θ	8°	10°	12°
∅	1.100	1.200	1.300
d			0.100


Disclaimer:

The information provided in this document is believed to be accurate and reliable. however, Shenzhen Core Control Electronics Technology Co., Ltd. does not assume any responsibility for the following consequences Do not consider the use of such information or use beyond its scope.

The information mentioned in this document may be changed at any time without notice.

The products and information provided in this document do not infringe patents. Shenzhen Core Control Electronics Technology Co., Ltd. assumes no responsibility for any infringement of any other rights of third parties. The result of using such products and information.

This document is the second version issued on June 10, 2022. This document replaces and Replace all previously provided information.

 It is a registered trademark of Shenzhen Core Control Electronics Technology Co., Ltd.

Copyright © 2017 Shenzhen Core Control Electronics Technology Co., Ltd. all rights reserved.