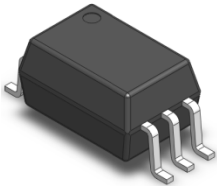


6 PIN SDIP INTELLIGENT POWER and GATE DRIVE INTERFACE PHOTOCOUPLER ELS680-G series

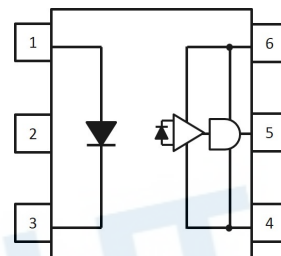
Preliminary



Features

- Compliance Halogens Free (Br < 900 ppm, Cl < 900 ppm, Br+Cl < 1500 ppm)
- Pb free and RoHS compliant
- Compliance with EU REACH.
- High isolation voltage between input and output (Viso=5000 Vrms)
- UL and cUL pending
- VDE pending
- NEMKO pending
- FIMKO pending
- SEMKO pending
- DEMKO pending
- CQC pending

Schematic



A 0.1μF bypass capacitor must be connected between pins 6 and 4³

Pin Configuration

- 1: Anode
- 2: No Connection
- 3: Cathode
- 4: V_{EE}
- 5: V_{out}
- 6: V_{CC}

This is a preliminary specification intended for design purposes and subject to change without prior notice.

Description

The ELS680-G series devices each consists of an infrared emitting diode, optically coupled to a high speed integrated photo detector logic gate with a totem output. The totem pole output eliminates the need for a pull-up resistor and allows for a direct-drive Intelligent Power Module or gate drive. The devices are packaged in a 6-pin small DIP package.

Applications

- IPM Interface Isolation
- Isolated IGBT/MOSFET Gate Drive
- AC and Brushless DC Motor Drives
- Industrial Inverters

Truth Table

Input	Output
H	H
L	L

Absolute Maximum Ratings (Ta=25°C)

	Parameter	Symbol	Rating	Unit
Input	Forward current	I _F	25	mA
	Reverse voltage	V _R	5	V
	Power dissipation	P _{IN}	75	mW
Output	Average Output current	I _{O(AVG)}	60	mA
	Supply voltage	V _{CC}	30	V
	Power dissipation	P _O	270	mW
Total Power Dissipation		P _{TOT}	350	mW
Isolation voltage *1		V _{ISO}	5000	V _{rms}
Operating temperature		T _{OPR}	-40 ~ +100	°C
Storage temperature		T _{STG}	-55 ~ +125	°C
Soldering temperature *2		T _{SOL}	260	°C

Notes:

*1 AC for 1 minute, R.H.= 40 ~ 60% R.H. In this test, pins 1, 2, 3 are shorted together, and pins 4, 5, 6, are shorted together.

*2 For 10 seconds.

Electrical Characteristics (Ta=-40 to 100 °C unless specified otherwise)

Input

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Forward Voltage	V _F	-	1.5	1.8	V	I _F =10mA
Reverse Voltage	I _R	-	-	10	μA	V _R =5V
Input Capacitance	C _{IN}	-	60	-	pF	V _F =0V, f=1MHz

Output

Parameter	Symbol	Min	Typ.	Max.	Unit	Condition
High Level Supply Current	I _{CCH}	-	-	3.2	mA	V _{CC} =5.5V, I _F =10mA
Low Level Supply Current	I _{CCL}	-	-	3.2	mA	V _{CC} =5.5V, I _F =0mA
Logic High Short Circuit Output Current,	I _{OSH}	-	-	-60	mA	V _{CC} =5.5V, I _F =10mA, I _O =Open
Logic Low Short Circuit Output Current,	I _{OSL}	60	-	-	mA	V _{CC} =V _O =5.5V, V _F =0V

Transfer Characteristics (Ta=-40 to 100 °C unless specified otherwise)

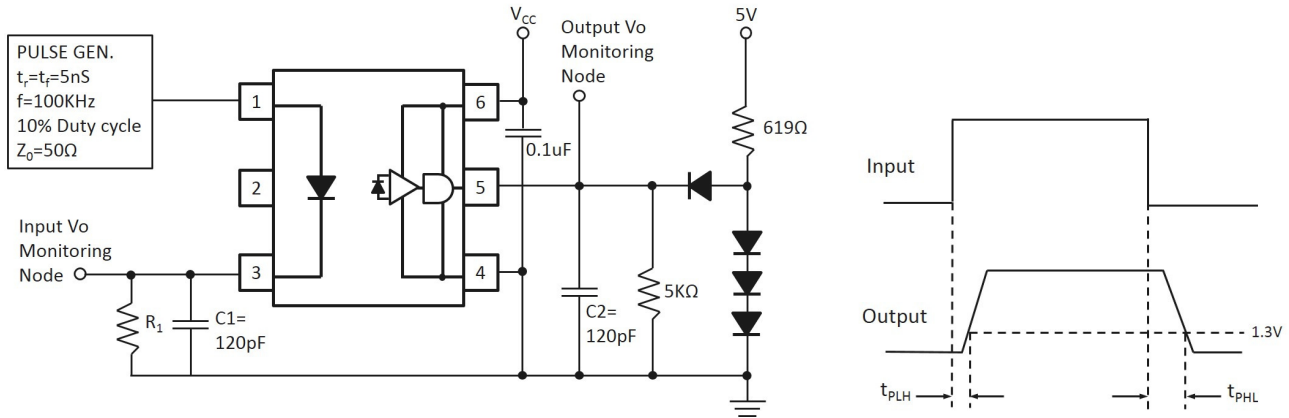
Parameter	Symbol	Min	Typ.	Max.	Unit	Condition
High Level Output Voltage	V _{OH}	V _{CC} -0.5	-	-	V	V _{CC} =4.5V, I _F =10mA, I _O =-0.4mA
Low Level Output Voltage	V _{OL}	-	-	V _{EE} +0.5	V	V _{CC} =4.5V, I _F =0mA, I _O =6.4mA
Input Threshold Current	I _{FT}	-	2.5	5	mA	V _{CC} =4.5V
Input-Output Resistance	R _{I-O}	-	10 ¹²	-	Ω	V _{I-O} =500V DC
Input-Output Capacitance	C _{I-O}	-	0.6	-	pF	V _{I-O} =0V DC, f=1MHz

Switching Characteristics ($T_a=-40$ to $100\text{ }^\circ\text{C}$, $V_{CC}=4.5\text{V}$, $I_F=10\text{mA}$ unless specified otherwise)

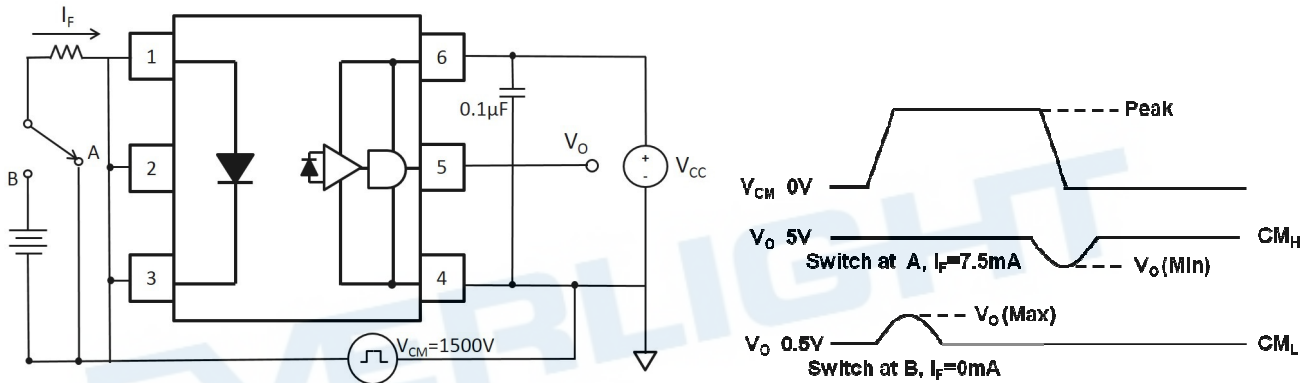
Parameter	Symbol	Min	Typ.	Max.	Unit	Condition
Propagation Delay Time to Output High Level* ⁵	t_{PHL}	-	130	350	ns	$V_{CC}=4.5\text{V}$, $I_F=10\text{mA}$ $T_A=25\text{ }^\circ\text{C}$
Propagation Delay Time to Output Low Level* ⁶	t_{PLH}	-	140	350	ns	$V_{CC}=4.5\text{V}$, $I_F=10\text{mA}$ $T_A=25\text{ }^\circ\text{C}$
Pulse Width Distortion	$ t_{PHL} - t_{PLH} $	-	-	250	ns	$V_{CC}=4.5\text{V}$, $I_F=10\text{mA}$ $T_A=25\text{ }^\circ\text{C}$
Output Rise Time* ⁷	t_r	-	9	-	ns	$V_{CC}=4.5\text{V}$, $I_F=10\text{mA}$ $T_A=25\text{ }^\circ\text{C}$
Output fall time* ⁸	t_f	-	6	-	ns	$V_{CC}=4.5\text{V}$, $I_F=10\text{mA}$ $T_A=25\text{ }^\circ\text{C}$
Common Mode Transient Immunity at Logic High* ³	CM_H	10	-	-	KV/ μs	$V_{CM}=1500\text{Vp-p}$, $I_F=7.5\text{mA}$, $V_{CC}=5\text{V}$, $T_A=25\text{ }^\circ\text{C}$
Common Mode Transient Immunity at Logic Low* ³	CM_L	10	-	-	KV/ μs	$V_{CM}=1500\text{Vp-p}$, $I_F=0\text{mA}$, $V_{CC}=5\text{V}$, $T_A=25\text{ }^\circ\text{C}$

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Switching Time Test Circuit & Waveform



Transient Immunity Test Circuit & Waveform



Note:

- *3 The V_{CC} supply must be bypassed by a 0.1μF capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the package V_{CC} and V_{EE} pins
- *4 Common mode transient immunity in logic high level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse signal V_{CM} , to assure that the output will remain in a logic high state (i.e., $V_O > 2.0\text{V}$).
 Common mode transient immunity in logic low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{CM} , to assure that the output will remain in a logic low state (i.e., $V_O < 0.8\text{V}$)

Order Information

Part Number

ELS680X(Y) -VG

Note

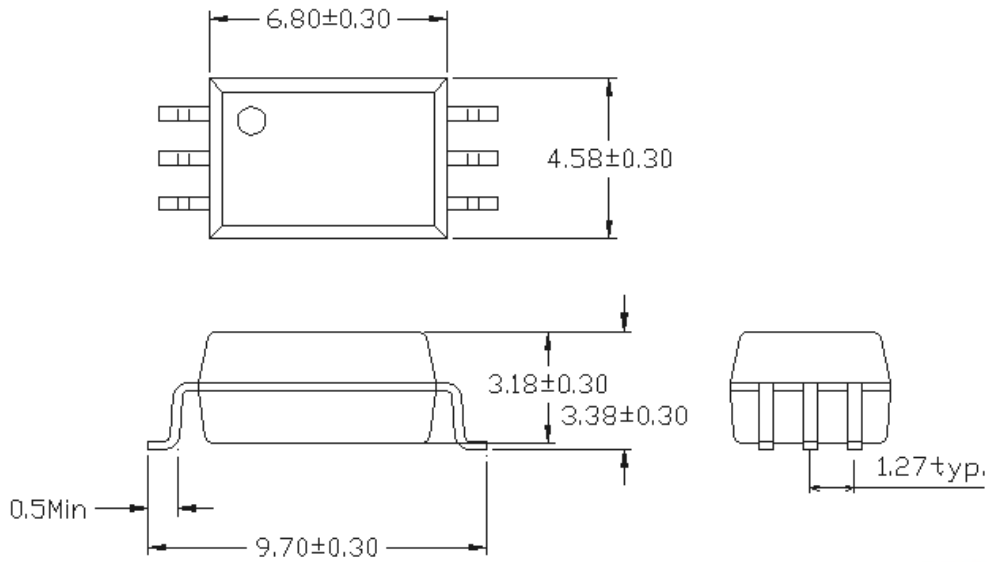
EL = denotes EVERLIGHT
S680 = part no.
X = lead type(P)
Y = Tape and reel option (TA, TB)
V = VDE (optional)
G = Halogens free

Option	Description	Packing quantity
P(TA)	Surface mount lead form + TA tape & reel option	1000 units per reel
P(TB)	Surface mount lead form + TB tape & reel option	1000 units per reel

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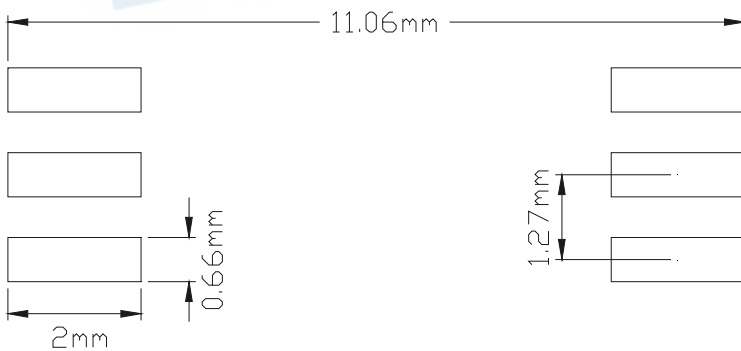
Package Dimension
(Dimensions in mm)

P Type



Recommended pad layout for surface mount leadform

For P Type:



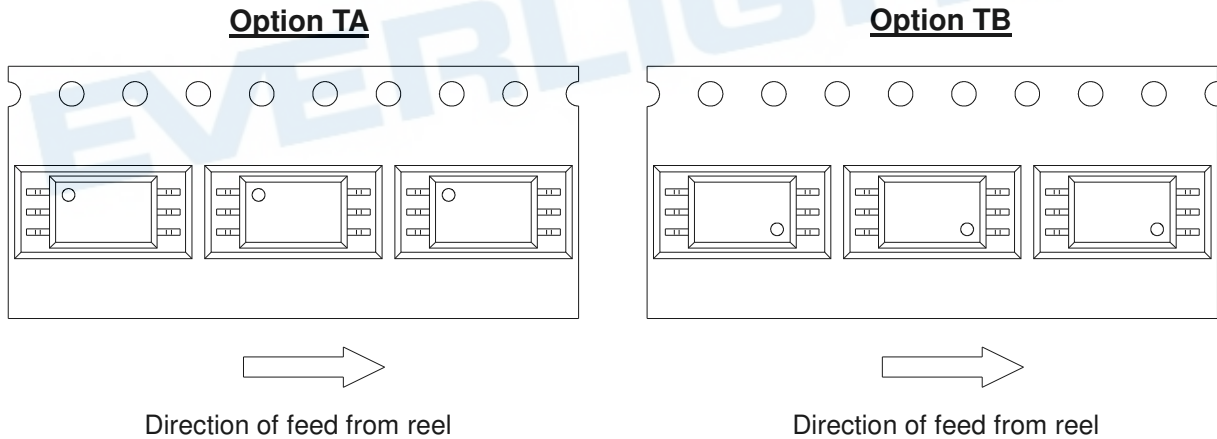
Device Marking



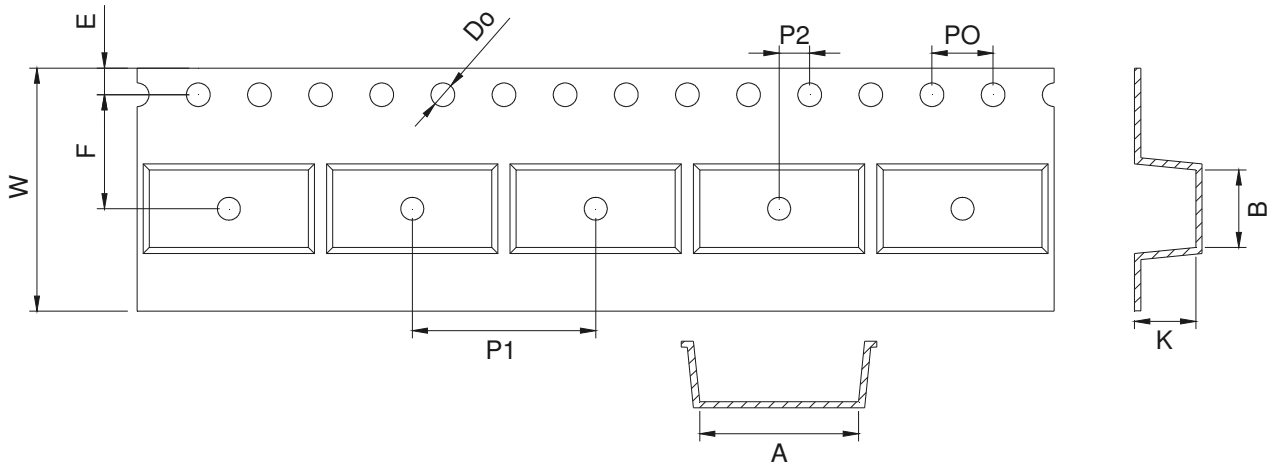
Notes

- T denotes Factory
T : made in Taiwan
- EL denotes EVERLIGHT
- S680 denotes Device Number
- Y denotes 1 digit Year code
- WW denotes 2 digit Week code
- V denotes VDE (optional)

Tape & Reel Packing Specifications



Tape dimension

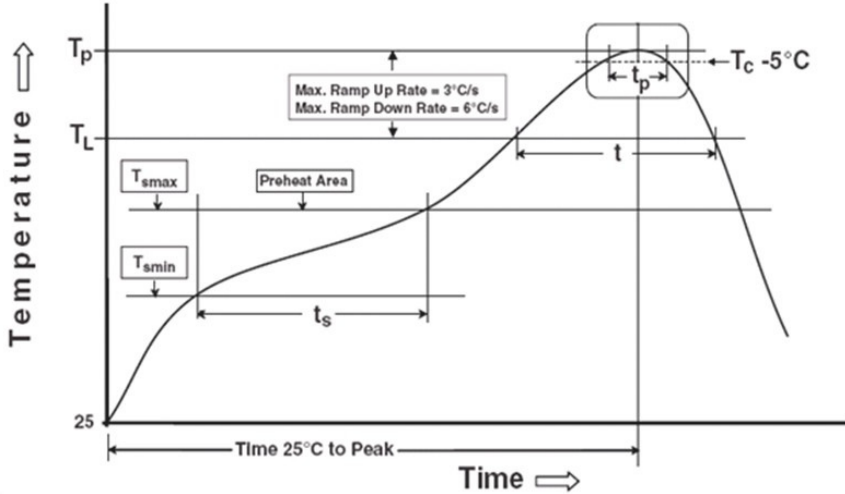


Dimension No.	A	B	Do	E	F	t
Dimension(mm) P	10.4 ± 0.1	5.1 ± 0.1	1.55 ± 0.1	1.75 ± 0.1	7.5 ± 0.1	0.4 ± 0.1
Dimension No.	PO	P1	P2	W	K	
Dimension(mm) P	4.0 ± 0.1	12.0 ± 0.1	2.0 ± 0.1	16.0 ± 0.3	4.0 ± 0.1	

Precautions for Use

1. Soldering Condition

1.1 (A) Maximum Body Case Temperature Profile for evaluation of Reflow Profile



Note:

Reference: IPC/JEDEC J-STD-020D

Preheat

Temperature min (T_{smin})	150 °C
Temperature max (T_{smax})	200 °C
Time (T_{smin} to T_{smax}) (t_s)	60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 °C/second max

Other

Liquidus Temperature (T_L)	217 °C
Time above Liquidus Temperature (t_L)	60-100 sec
Peak Temperature (T_P)	260 °C
Time within 5 °C of Actual Peak Temperature: $T_P - 5^\circ\text{C}$	30 s
Ramp- Down Rate from Peak Temperature	6 °C /second max.
Time 25 °C to peak temperature	8 minutes max.
Reflow times	3 times

DISCLAIMER

1. Above specification may be changed without notice. EVERLIGHT will reserve authority on material change for above specification.
2. The graphs shown in this datasheet are representing typical data only and do not show guaranteed values.
3. When using this product, please observe the absolute maximum ratings and the instructions for use outlined in these specification sheets. EVERLIGHT assumes no responsibility for any damage resulting from use of the product which does not comply with the absolute maximum ratings and the instructions included in these specification sheets.
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