Low Power F0 Detect and Tracking LRA Haptic Driver

Features

- 1MHz I2C Bus
- Integrated 3K Memory
- 12k/24k/48k input wave sampling rate
- F0 detect and tracking
- Advance autobrake engine integrated
- Playback mode:
  - Real time playback
  - Memory playback
  - 1 Trigger playback
  - Cont playback
- Resistance-Based LRA Diagnostics
- Drive signal monitor for LRA protect
- Drive Compensation Over Battery Discharge
- Fast Start Up Time ＜0.4ms
- Dedicated interrupt output pin
- Support automatically switch to standby mode
- Standby current：3uA
- Shutdown current：＜1uA
- Supply voltage range 3 to 5.5V
- Short-Circuit Protection, Over-Temperature Protection, Under-Voltage Protection
- FCQFN 1.37mmX1.37mmX0.4mm-9L Package
- AW86224A included Immersion IP license
- AW86224B included Immersion IP and dedicated software license

Applications

- Mobile phones
- Tablets
- Wearable Devices

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General Description

AW86224A/B is a low cost H-bridge, single chip LRA haptic driver, with F0 detecting and tracking based on BEMF, supporting real time playback, memory playback , Cont playback, and hardware pin trigged playback with fast start up time. All these make the AW86224A/B an ideal candidate for haptic driver.

AW86224A/B integrates a 3KByte SRAM for user-defined waveforms to achieve a variety of vibration experiences, supporting 3 sampling rate(12k/24k/48k) of waveforms loaded in SRAM, supporting output waveform sampling rate up-sampling to 48k.

AW86224A/B integrates an autobrake engine to suppress the aftershocks to zero for different drive waveforms (short or long) on different LRA motors.

AW86224A/B supports LRA fault diagnostic based on resistance measurement and protections of short-circuit, over-temperature and under-voltage.

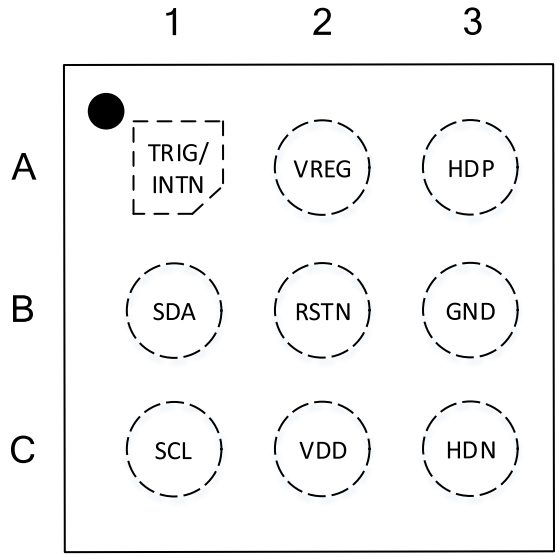
AW86224A/B features configurable automatically switch to standby mode after haptic waveform playback finished. This can less quiescent power consumption. The RSTN pin provides further power saving by fully shut down the whole device. Reused interrupt output pin can detect real time FIFO status and the error status of the chip.

AW86224A/B features general settings are communicated via an I2C-bus interface.

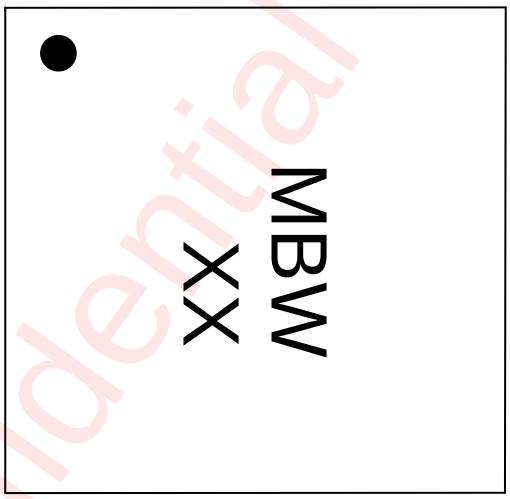
AW86224A/B is available in a FCQFN 1.37mmX1.37mmX0.4mm-9L package.

Pin Configuration and Top Mark

AW86224A/B FCR
(Top View)



AW86224A/B FCR Marking
(Top View)



MBW - AW86224A/B FCR
XX - Production Tracing Code

Figure 1 Pin Configuration and Top Mark

Pin Definition

PIN NUMBER	NAME	TYPE	DESCRIPTION
A1	TRIG/INTN	I/O	Multi-mode pin. Selectable as input trigger (pulse), or output interrupt Default function is INTN, when set as interrupt output, there must be a pullup resistance to be added.
B1	SDA	I/O	I2C bus data input/output(open drain)
C1	SCL	I	I2C bus clock input
A2	VREG	Power	Output of LDO
B2	RSTN	I	Active low hardware reset High: standby/active mode Low: power-down mode
C2	VDD	Power	Chip power supply
A3	HDP	O	Positive haptic driver differential output
B3	GND	Ground	Supply ground
C3	HDN	O	Negative haptic driver differential output

Functional Block Diagram

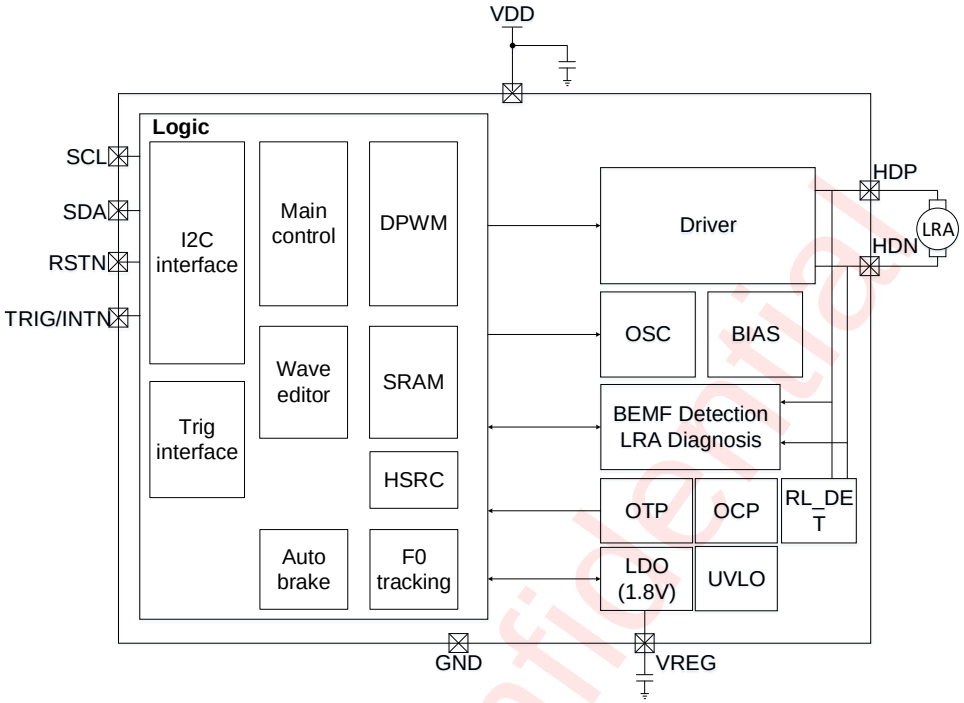


Figure 2 FUNCTIONAL BLOCK DIAGRAM

Typical Application Circuits

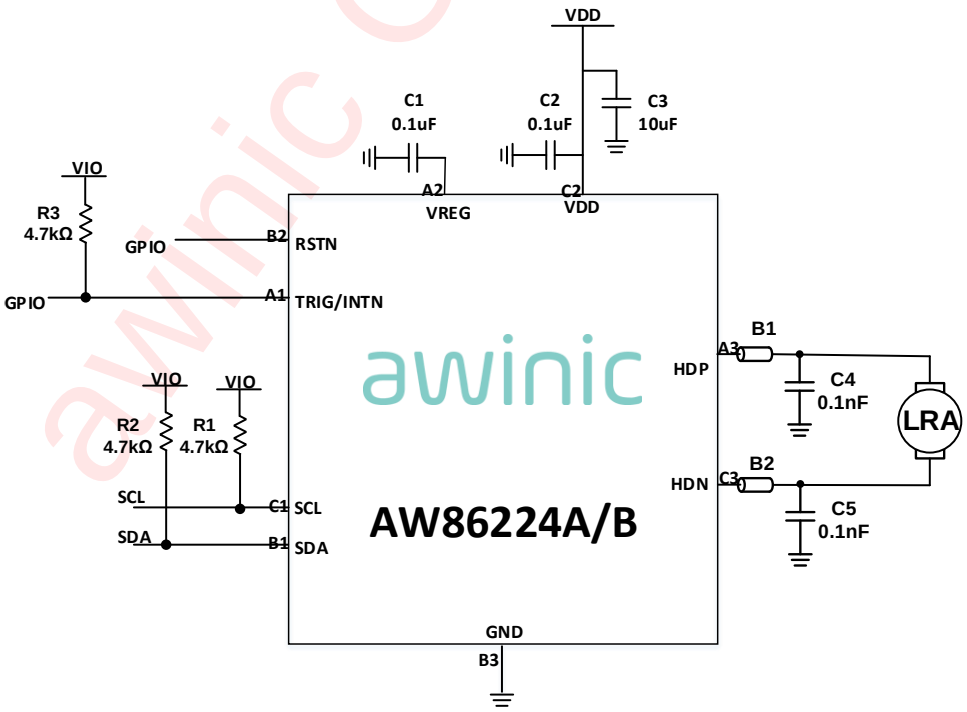


Figure 3 Typical Application Circuit of AW86224A/B

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Notice for Typical Application Circuits:

1: Please place C1，C2，C3 as close to the chip as possible. The capacitors should be placed in the same layer with the AW86224A/B chip.

2: For the sake of driving capability, the power lines (especially the one to VDD) and output lines should be short and wide as possible.

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environment Information	Delivery Form
AW86224AFCR	-40°C ~ 85°C	FCQFN 1.37mmX1.37mmX0.4mm-9L	MBW	MSL1	ROHS+HF	4500 units/ Tape and Reel
AW86224BFCR	-40°C ~ 85°C	FCQFN 1.37mmX1.37mmX0.4mm-9L	MBW	MSL1	ROHS+HF	4500 units/ Tape and Reel

Absolute Maximum Ratings(NOTE 1)

PARAMETERS	RANGE
Supply voltage range VDD	-0.3V to 6.0V
Digital power supply VREG	-0.3V to 2.0V
HDP, HDN(≤VDD+0.3V)	-0.3V to 6.0V
TRIG/INTN , SDA, SCL, RSTN	-0.3V to 6.0V
Minimum load resistance R_L	5Ω
Junction-to-ambient thermal resistance a	120°C/W
Operating free-air temperature range	-40°C to 85°C
Maximum Junction Temperature T_{JMAX}	150°C
Storage Temperature Range T_{STG}	-65°C to 150°C
Lead Temperature(Soldering 10 Seconds)	260°C
ESD(Including CDM)(NOTE 2 3)	
HBM(Human Body Model)	±2KV
CDM(Charge Device Model)	±1.5KV
Latch-up	
Test Condition: JEDEC EIA/JESD78E	+IT: 200mA -IT: -200mA

NOTE 1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE 2：The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ANSI/ESDA/JEDEC JS-001-2017.

NOTE 3：Charge Device Model test method: ANSI/ESDA/JEDEC JS-002-2018.

Electrical Characteristics

Characteristics

Test condition: TA=25°C，VDD=3.6V，RL=8Ω+100μH，f=160Hz (unless otherwise noted)

Symbol	Description	Test Conditions	Min	Typ.	Max	Units
V_{VDD}	Battery supply voltage	On pin VDD	3		5.5	V
V_{VREG}	Voltage at VREG pin		1.65	1.8	1.95	V
V_{IL}	Logic input low level	RSTN/TRIG/INTN/SCL/SDA			0.5	V
V_{IH}	Logic input high level	RSTN/TRIG/INTN/SCL/SDA	1.3			V
V_{OL}	Logic output low level	TRIG/INTN/SDA I_{OUT}=4mA			0.4	V
V_{OS}	Output offset voltage	I^2C signal input 0	-30	0	30	mV
I_{SD}	Shutdown current	RSTN =0V	0	0.1	1	μA
I_{STBY}	Standby current	RSTN=1.8V	0	3	8	μA
I_Q	Quiescent current		0.8	1.3	1.8	mA
UVP	Under-voltage protection voltage		2.6	2.7	2.8	V
	Under-voltage protection hysteresis voltage		50	100	150	mV
T_{SD}	Over temperature protection threshold			160		°C
T_{SDR}	Over temperature protection recovery threshold			130		°C
T_{ON1}	Time from shutdown to standby				3	ms
T_{ON2}	Waveform startup time	From trigger to output signal	0.2	0.4	0.8	ms
HDRIVER						
R_{dson}	Drain-Source on-state resistance	Include NMOS and PMOS, VDD=4.2V	500	750	1000	mΩ
R_{ocp}	Load impedance threshold for over current protection			2		Ω
F_{PWM}	PWM output frequency	VDD=4.2V, PD_HWM=0	95.04	96	96.96	kHz
		VDD=4.2V, PD_HWM=1	47.52	48	48.48	kHz
$F_{CALI\_ACC\_LRA}$	LRA Consistency Calibration accuracy		F0-2	F0	F0+2	Hz
V_{peak}	Output voltage	RL=8Ω+100μH VDD=4.2V	3.3	3.6	4	V
	Output voltage	RL=16Ω+100μH	3.6	3.8	4.2	V

		VDD=4.2V				

I²C Interface Timing

Parameter			fast mode			fast mode plus			UNIT
No.	Symbol	Name	MIN	TYP	MAX	MIN	TYP	MAX	
1	f_{SCL}	SCL Clock frequency			400			1000	kHz
2	t_{LOW}	SCL Low level Duration	1.3			0.5			μs
3	t_{HIGH}	SCL High level Duration	0.6			0.26			μs
4	t_{RISE}	SCL, SDA rise time			0.3			0.12	μs
5	t_{FALL}	SCL, SDA fall time			0.3			0.12	μs
6	$t_{SU:STA}$	Setup time SCL to START state	0.6			0.26			μs
7	$t_{HD:STA}$	(Repeat-start) Start condition hold time	0.6			0.26			μs
8	$t_{SU:STO}$	Stop condition setup time	0.6			0.26			μs
9	t_{BUF}	the Bus idle time START state to STOP state	1.3			0.5			μs
10	$t_{SU:DAT}$	SDA setup time	0.1			0.1			μs
11	$t_{HD:DAT}$	SDA hold time	10			10			ns

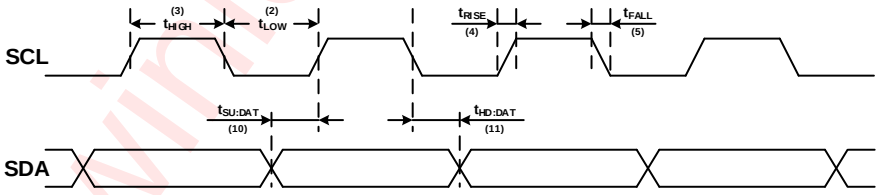


Figure 4 SCL and SDA timing relationships in the data transmission process

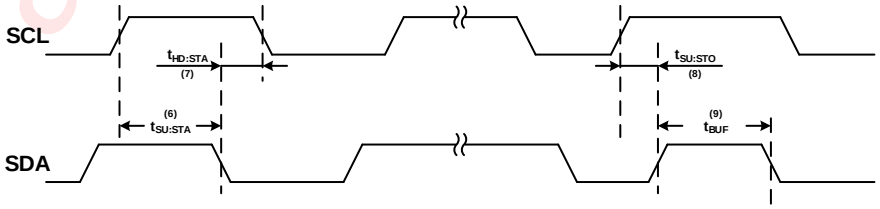


Figure 5 The timing relationship between START and STOP state

Measurement Setup

AW86224A/B features switching digital output, as shown in Figure 6. Need to connect a low pass filter to HDP/HDN output respectively to filter out switch modulation frequency, then measure the differential output of filter to obtain analog output signal.

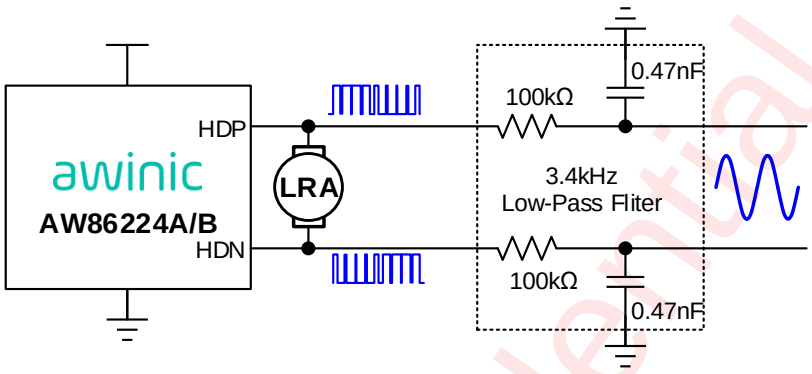


Figure 6 AW86224A/B test setup

Typical Characteristics

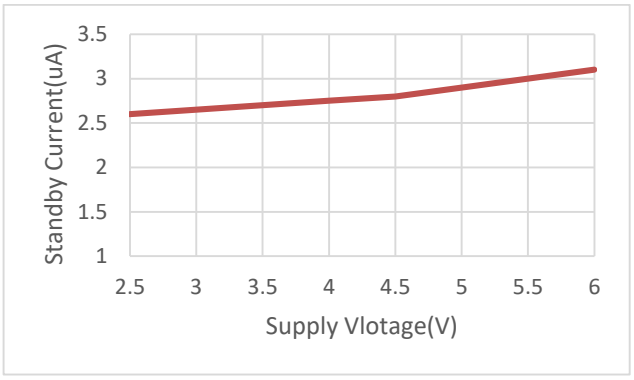


Figure 7 Standby Current Vs Supply Voltage

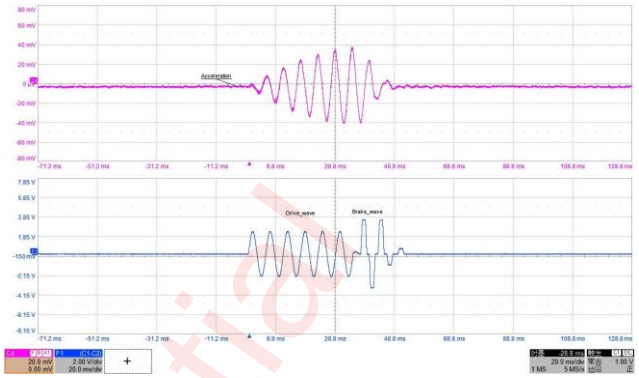


Figure 8 LRA with Automatic Braking

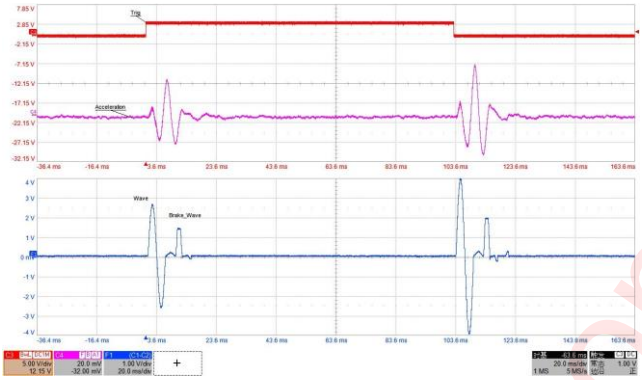


Figure 9 Trig Application

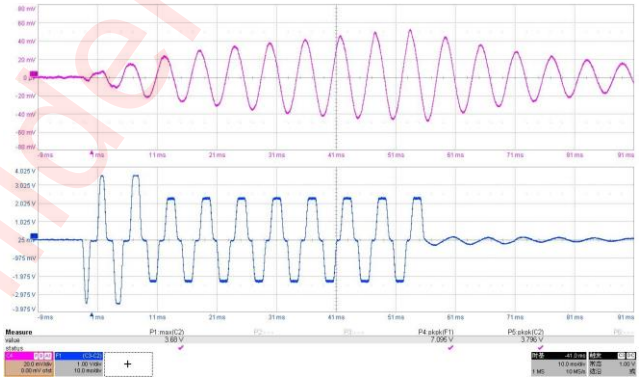


Figure 10 Automatic Resonance Tracking

Detailed Functional Description

Power On Reset

The device provides a power-on reset feature that is controlled by LDO_OK. The reset signal will be generated to perform a power-on reset operation, which will reset all circuits and configuration registers. When the VDD power on, the VREG voltage raises and produce the LDO_OK indication, the reset is over.

Operation Mode

The device supports 3 operation modes.

Table 1 Operating Mode

Mode	Condition	Description
Power-Down	VDD = 0V or RSTN = 0V	Power supply is not ready or RSTN is tie to low. Whole chip shutdown including I²C interface.
Standby	VDD > 2.7V and RSTN = HIGH and no wave is going	Power supply is ready and RSTN is tie to high. Most parts of the device are power down for low power consumption except I²C interface and LDO.
Active	Playing a waveform	Most parts of the device are working

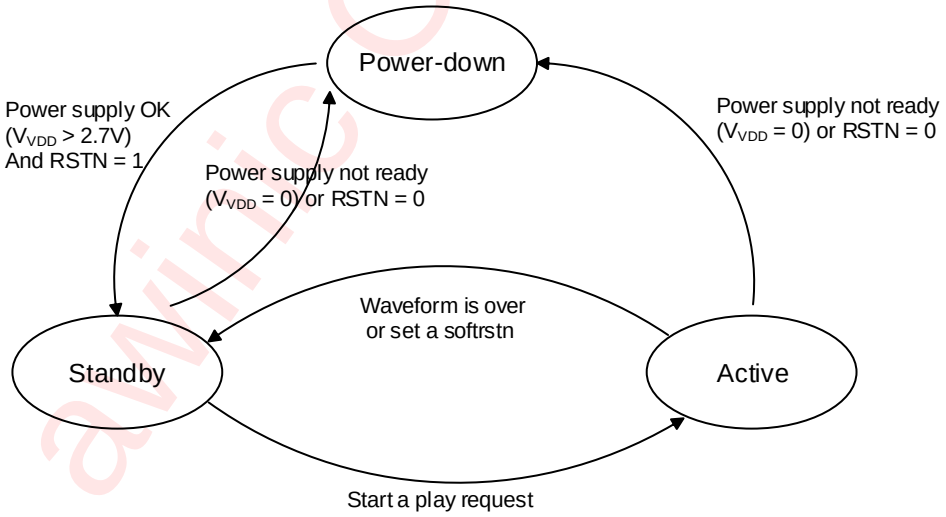


Figure 11 Device operating modes transition

POWER-DOWN MODE

The device switches to power-down mode when the supply voltage is not ready or RSTN pin is set to low.
In this mode, all circuits inside this device will be shut down. I²C interface isn't accessible in this mode, and all of the internal configurable registers and Memory are cleared.
The device will jump out of the power-down mode automatically when the supply voltages are OK and RSTN

pin is set to high.

Standby Mode

The device switches standby mode when the power supply voltages are OK and RSTN pin set to high. In this mode I²C interface is accessible, other modules except LDO module are still powered down. Customer can force device to this mode by setting STANDBY to high. Also in this mode, customer can initialize waveform library in SRAM. Device will be switched to this mode after haptic waveform playback finished.

Active Mode

The device is fully operational in this mode. H-bridge driver circuits will start to work. Users can send a playback request to make device in this mode.

Power On And Power Down Sequence

This device power on sequence is illustrated in the following figure:

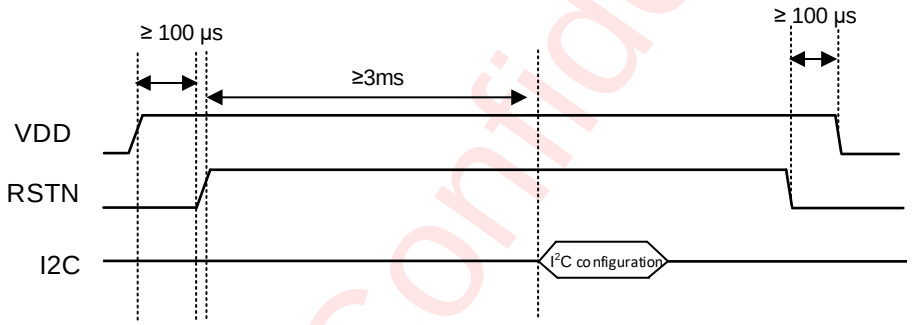


Figure 12 Power On Sequence

Playback Sequence

Make sure the device is not in POWER-DOWN MODE before sending a playback request, then the playback sequence is illustrated in the following figure:

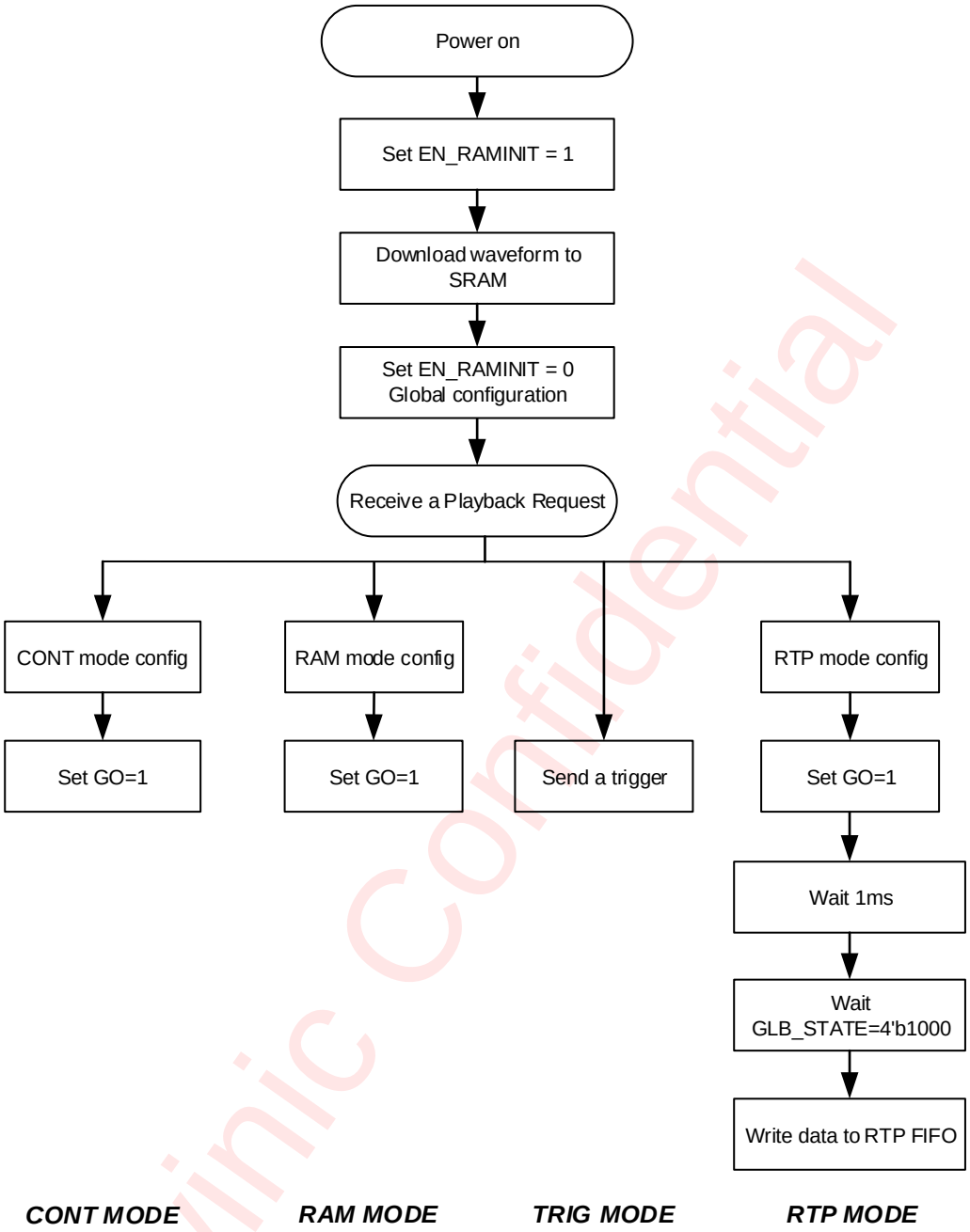


Figure 13 Power up and playback sequence

Software Reset

Writing 0xAA to register SRST(0x00) via I²C interface will reset the device internal circuits except SRAM, including configuration registers.

Battery Voltage Detect

Software can send command to detect the battery voltage.

Detect steps:

- Set EN_RAMINIT to 1 in register 0x43;

- Set VBAT_GO to 1 in register 0x52;
- Wait 3ms;
- Set EN_RAMINIT to 0 in register 0x43;
- Read VBAT in register 0x55 and VBAT_LO in register 0x57.

The code is a 10bit unsigned number.

$$VDD = \frac{6.1 \times (VBAT \times 4 + VBAT\_LO)}{1024}(V)$$

Constant Vibration Strength

The device features power-supply feedback. If the supply voltage discharge over time, the vibration strength remains the same as long as enough supply voltage is available to sustain the required output voltage. It is especially useful for ring application. Power-supply feedback only works in CONT playback mode.

Use steps:

- Set VBAT_MODE to 1 in register 0x43;

Initiates a CONT playback request.

LRA Consistency Calibration

Different motor batches, assembly conditions and other factors can result in f0 deviation of LRA. When the drive waveform does not match the LRA monomer, the vibration may be inconsistent and the braking effect becomes worse, especially for short vibration waveforms. So it's necessary to perform consistency calibration of LRA. Firstly, the power-on f0 detection can be launched to get the f0 of LRA. Secondly the waveform frequency stored in SRAM and the f0 of LRA are used to calculate the code for calibration. The f0 accuracy after LRA consistency calibration is ±2Hz.

LRA Resistance Detect

Software can send command to detect the LRA's resistance.

Detect steps:

- Set EN_RAMINIT to 1 in register 0x43;
- Read D2S_GAIN register and save the result as d2s_gain_pre;
- Set D2S_GAIN with an appropriate with in register 0x49;
- Set RL_OS to 1 in register 0x51;
- Set DIAG_GO to 1 in register 0x52;
- Wait 3ms;
- Set EN_RAMINIT to 0 in register 0x43;
- Restore the value of D2S_GAIN register to d2s_gain_pre;
- Read RL in register 0x53 and RL_LO in register 0x57.

Based on this information host can diagnosis used LRA's status. The code is a 10bit unsigned number.

$$RL = \frac{678 \times (RL \times 4 + RL\_LO)}{1024 \times \mathrm{D2S\_GAIN}}(\Omega)$$

The values of the D2S_GAIN that can be configured for different sizes of RL are listed below. The higher the

RL, the smaller the configurable D2S_GAIN.

Table 2 D2S_GAIN Selection

RL(Ω)	D2S_GAIN
2~30	20
31~60	10

Flexible Haptic Data Playback

The device offers multiple ways to playback haptic effects data. The PLAY_MODE bits select RAM mode, RTP mode, CONT mode. Additional flexibility is provided by the one hardware TRIG pins, which can override PLAY_MODE bit to playback haptic effects data as configuration.

The device contains 3 kB of integrated SRAM to store customer haptic waveforms' data. The whole SRAM is separated to RAM waveform library and RTP FIFO region by base address. And RAM waveform library is including waveform library version, waveform header and waveform data.

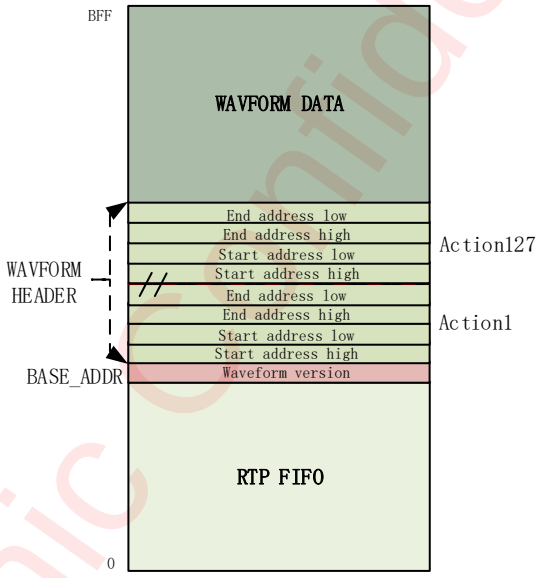


Figure 14 Data structure in SRAM

SRAM mode and TRIG mode playback the waveforms in RAM waveform library and RTP mode playback the waveform data written in RTP FIFO, CONT mode playback non-filtered or filtered square wave with rated drive voltage.

Sram Structure

A RAM waveform library consists of a waveform version byte, a waveform header section, and the waveform data content. The waveform header defines the data boundaries for each waveform ID in the data field, and the waveform data contains a signed data format (2's complement) to specify the magnitude of the drive.

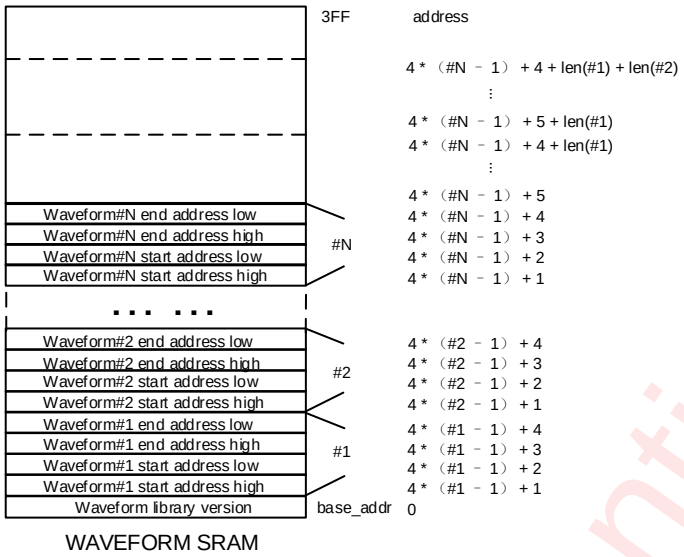


Figure 15 Waveform library data structure

Waveform version:

One byte located on SRAM base address, setting to different value to identify different version of RAM waveform library.

Waveform header:

The waveform header block consist of N-boundary definition blocks of 4 bytes each. N is the number of waveforms stored in the SRAM (N cannot exceed 127). Each of the boundary definition blocks contain the start address (2 bytes) and end address (2 bytes). So the total length of waveform header block are N*4 bytes.

The start address contains the location in the memory where the waveform data associated with this waveform begins.

The end address contains the location in the memory where the waveform data associated with this waveform ends.

The waveform ID is determined after base address is defined. Four bytes begins with the address next to base address are the first waveform ID’s header, and next four bytes are the second waveform ID’s header, and so on.

Waveform data:

The waveform data contains a signed data format (2's complement) to specify the magnitude of the drive. The begin address and end address is specified in waveform ID’s header.

Waveform library initialization steps:

- Before waveform library initialization, make sure the chip is in STANDBY mode;
- Prepare waveform library data including: waveform library version, waveform header fields for waveform in library and waveform data of each waveform;
- Set register EN_RAMINIT=1 in register 0x43, to enable SRAM initial;
- Set base address (register 0x2D, 0x2E);
- Write waveform library data into register 0x42 continually until all the waveform library data written;
- Set register EN_RAMINIT=0, to disable SRAM initial.

Ram Mode

To playback haptic data with RAM mode, the waveform ID must first be configured into the waveform playback queue and then the waveform can be played by writing GO bit register.

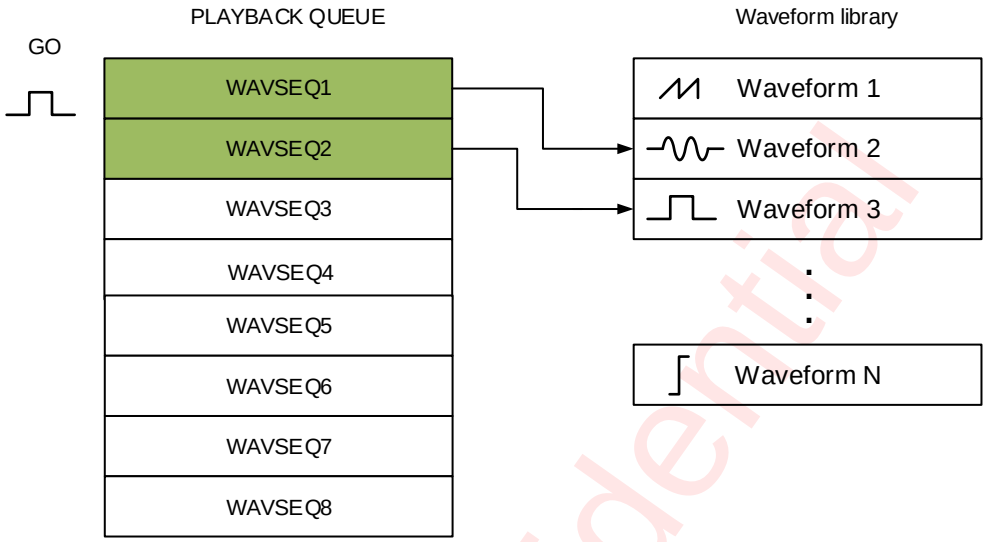


Figure 16 RAM mode playback

The waveform playback queue defines waveform IDs in waveform library for playback. Eight WAVSEQx registers queue up to eight library waveforms for sequential playback. A waveform ID is an integer value referring to the index of a waveform in the waveform library. Playback begins at WAVSEQ1 when the user triggers the waveform playback queue. When playback of that waveform ends, the waveform queue plays the next waveform ID held in WAVSEQ2 (if non-zero). The waveform queue continues in this way until the queue reaches an ID value of zero or until all eight IDs are played whichever comes first.

The waveform ID is a 7-bit number. The MSB of each ID register can be used to implement a delay between queue waveforms. When the MSB is high, bits 6-0 indicate the length of the wait time. The wait time for that step then becomes WAVSEQ[6:0] × wait_time unit. Wait_time unit can be configuration of WAITSLOT register.

The device allows for looping of individual waveforms by using the SEQxLOOP registers. When used, the state machine will loop the particular waveform the number of times specified in the associated SEQxLOOP register before moving to the next waveform. The device allows for looping of the entire playback sequence by using the MAIN_LOOP register. The waveform-looping feature is useful for long, custom haptic playbacks, such as a haptic ringtone.

Playback steps:

- Waveform library must be initialized before playback;
- Set PLAY_MODE bit to 0 in register 0x08;
- Set playback queue registers (0x0A ~ 0x11) as desired;
- Set playback loop registers (0x012~ 0x16) as desired;
- Set GO bit to 1 in register 0x09 to trigger waveform playback;
- Device will be switched to STANDBY mode after haptic waveform playback finished.

Rtp Mode

The real-time playback mode is a simple, single 8-bit register interface that holds an amplitude value. When real-time playback is enabled, begin to enters a register value to RTP_DATA over the I²C will trigger the playback, the value is played until the data sending finished or removes the device from RTP mode.

After FF_AEM or FF_AFM register is configured as 0, HOST can obtain the RTP FIFO almost empty or almost full status through interrupt signal(pin INTN) or read FF_AES or FF_AFS register. RTP FIFO almost empty and almost full threshold can be configured through FIFO_AE and FIFO_AF registers.

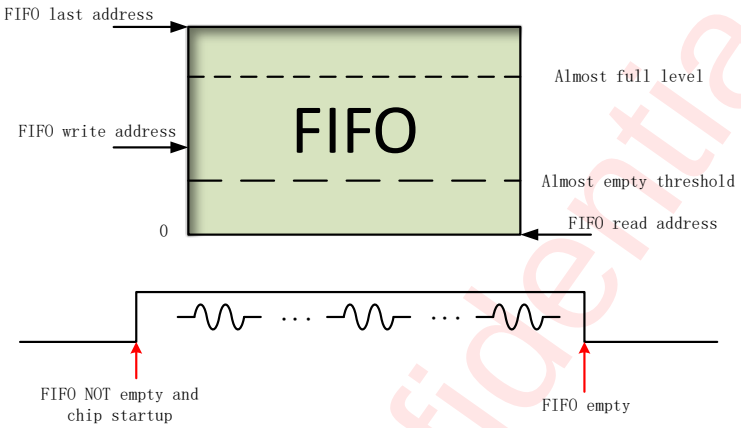


Figure 17 RTP mode playback

Playback steps:

- Prepare RTP data before playback;
- Set PLAY_MODE bit to 1 in register 0x08;
- Set GO bit to 1 in register 0x09 to trigger waveform playback;
- Delay 1ms;
- Check GLB_STATE=4'b1000, if HOST don't send data to FIFO, chip will wait for RTP data coming in this state forever;
- Write RTP data continually to register 0x32 to playback RTP waveform;
- HOST need monitor the full and empty status for RTP FIFO.
- Device will be switched to STANDBY mode after wave data in RTP FIFO is played empty.

Trig Mode

The device has a configuration, multi-mode pin TRIG/INTN. It can serve as a dedicated hardware pin for quickly trigger haptic data playback through configuration register INTN_PIN. Quickly trigger can be configured posedge/negedge/both-edge/level trigger.

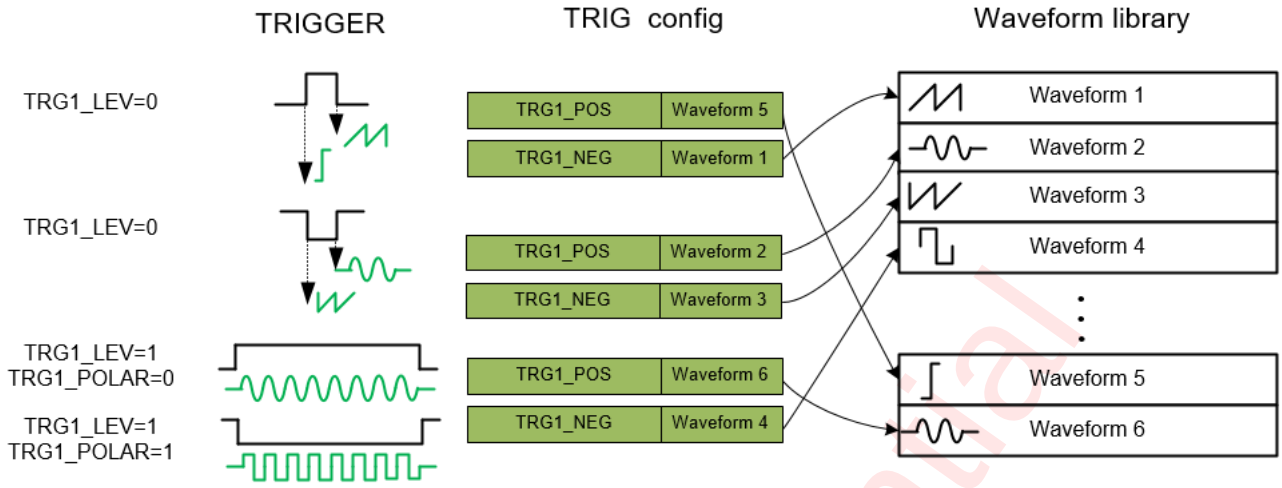


Figure 18 TRIG mode playback

Edge mode or level mode is accessible through configuration register TRG1_LEV. When an edge mode is needed, user should set TRG1_LEV =0. In edge mode, register TRG1SEQ_P and TRG1_POS respectively represent the waveform and enable signal of positive edge, where register TRG1SEQ_N and TRG1_NEG respectively represent the waveform and enable signal of negative edge.

When a level mode is needed, user should set TRG1_LEV =1, and positive level and negative level can be supported by setting register TRG1_POLAR=0 and setting TRG1_POLAR=1.

Table 3 TRIG MODE CONFIG

I2C reg				Trigger	Waveform
TRG1_LVL	TRG1_POLAR	TRG1_POS	TRG1_NEG		
0	X	0	0	-	none
	X	1	0	↑	TRG1SEQ_P
	X	0	1	↓	TRG1SEQ_N
	X	1	1	↑ / ↓	TRG1SEQ_P/ TRG1SEQ_N
1	0	X	X	High level	TRG1SEQ_P
	1	X	X	Low level	TRG1SEQ_N

Playback steps:

- Waveform library must be initialized before playback;
- Set INTN_PIN bit to 0 in register 0x44;
- Set TRG1_MODE bits to 2 in register 0x3A;
- Set trigger playback registers (0x33, 0x36, 0x39, 0x3A, 0x44) as desired;
- Send trigger pulse($\geq 1\mu s$) on TRIG pins to playback waveform;
- Device will be switched to STANDBY mode after haptic waveform playback finished.

Cont Mode

The CONT mode mainly performs two functions: F0 detection and real-time resonance-frequency tracking. F0 detection can be launched by setting EN_F0_DET=1 and BRK_EN =1. When set TRACK_EN=1, real-time resonance-frequency tracking will be launched by tracking the BEMF of actuator constantly. It provides stronger and more consistent vibrations and lower power consumption. If the resonant frequency shifts for any

reason, the function tracks the frequency from cycle to cycle. When TRACK_EN is set to 0, the width of waveform of cont mode is determined by DRV_WIDTH in register 0x1A.

When the EDGE_FRE register is set to 4'b1xxx, the CONT mode outputs a filtered square wave. The edge of filtered square wave is composed of SIN or COS wave whose frequency can be configured by EDGE_FRE register. When SIN_MODE register is set to 1, filtered square wave is composed of COS wave.

Playback steps:

- Set PLAY_MODE = 2 in register 0x08 to enable CONT mode;
- (optional)Set EN_F0_DET = 1 and BRK_EN =1 to enable F0 detection;
- Set cont mode by configuring registers(0x18~0x20 and 0x22);
- Set GO bit to 1 in register 0x09 to trigger waveform playback;
- Delay 1ms;
- If enable F0 detection, get F0 information from registers(0x25~0x28) after GLB_STATE=0;
- Device will be switched to STANDBY mode after haptic waveform playback finished.

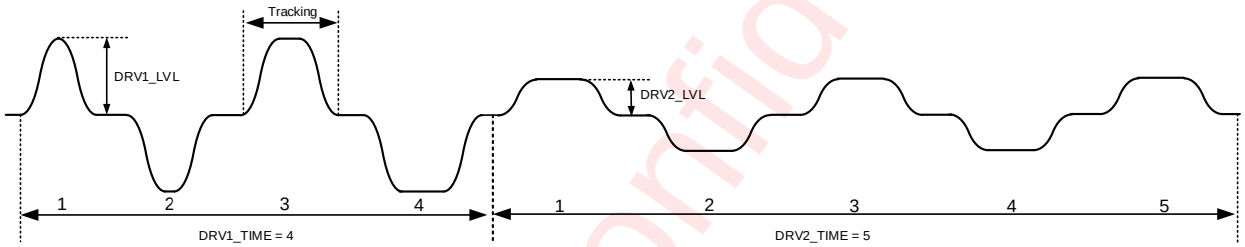


Figure 19 Cont mode playback

Auto Brake Engine

An auto-brake engine is integrated into this device. Users can adjust the brake strength by setting D2S_GAIN in register 0x49. The greater D2S_GAIN, the greater brake strength and the worse loop stability. Auto-brake engine is disabled when setting BRK_EN=0 or BRK_TIME=0.

To enable Auto-brake engine, there are some points to note:

- TRGx_BRK in register 0x39,0x3A should be set to 1 when in TRIG mode;
- Auto-brake engine will not work when EN_F0_DET in register 0x18 is set to 1;
- Auto-brake engine will not work when BRK_TIME in register 0x21 is set to 0;
- Device will be switched to STANDBY mode after haptic waveform playback finished.

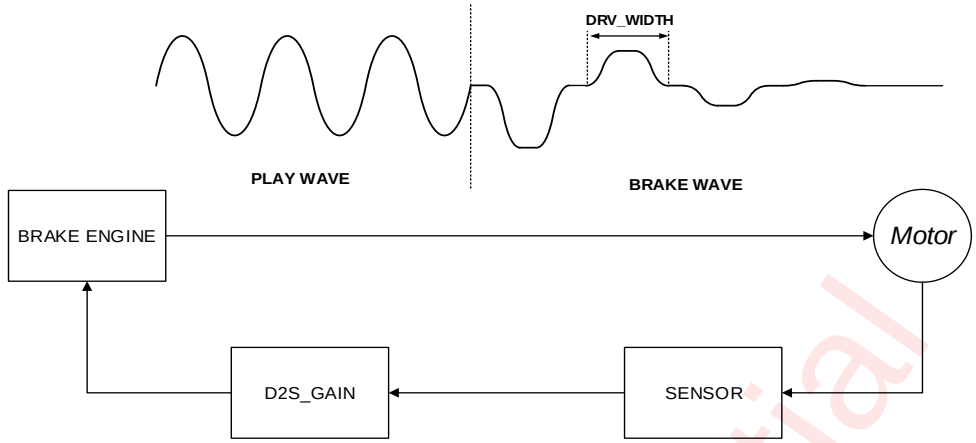


Figure 20 Brake loop

Protection Mechanisms

Over Temperature Protection (OTP)

The device has automatic temperature protection mechanism which prevents heat damage to the chip. It is triggered when the junction temperature is larger than the preset temperature high threshold (default = 160°C). When it happens, the output stages will be disabled. When the junction temperature drops below the preset temperature low threshold (less than 130°C), the output stages will start to operate normally again.

Over Current (Short) Protection (OCP)

The short circuit protection function is triggered when HDP/HDN is short too PVDD/GND or HDP is short to HDN, the output stages will be shut down to prevent damage to itself. When the fault condition is disappeared, the output stages of device will restart.

VDD Under Voltage Lock Out Protection (UVLO)

The device has a battery monitor that monitors the VDD level to ensure that is above threshold 2.7V, In the event of a VDD drop, the device immediately power down the H-bridge driver and latches the UVLO flag.

Drive Data Error Protection (DDEP)

When haptic data sent to drive LRA is error such as: a DC data or almost DC data, it will cause the LRA heat to brake. The device configurable immediately power down the H-bridge driver and latched the DDEP flag.

I²C Interface

This device supports the I²C serial bus and data transmission protocol in fast mode at 400kHz and fast mode plus at 1000kHz. This device operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O pin SDA and I pin SCL. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 4.7kΩ. This device can support different high level (1.8V~3.3V) of this I²C interface.

Device Address

The I²C device address (7-bit) is 0x58 and cannot be set.

Data Validation

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

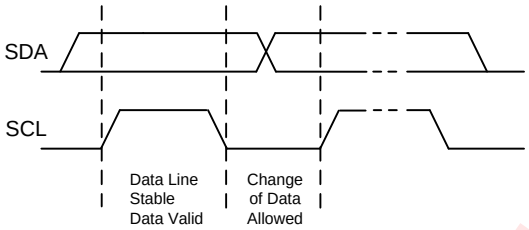


Figure 21 Data Validation Diagram

General I²C Operation

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. The device is addressed by a unique 7-bit address; the same device can send and receive data. In addition, Communications equipment has distinguished master from slave device: In the communication process, only the master device can initiate a transfer and terminate data and generate a corresponding clock signal. The devices using the address access during transmission can be seen as a slave device.
SDA and SCL connect to the power supply through the current source or pull-up resistor. SDA and SCL default is a high level. There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus.
START state: The SCL maintain a high level, SDA from high to low level
STOP state: The SCL maintain a high level, SDA pulled low to high level
Start and Stop states can be only generated by the master device. In addition, if the device does not produce STOP state after the data transmission is completed, instead re-generate a START state (Repeated START, Sr), and it is believed that this bus is still in the process of data transmission. Functionally, Sr state and START state is the same. As shown in Figure 22.

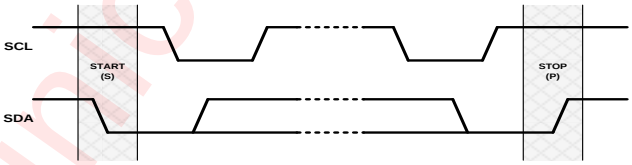


Figure 22 START and STOP state generation process

In the data transmission process, when the clock line SCL maintains a high level, the data line SDA must remain the same. Only when the SCL maintain a low level, the data line SDA can be changed, as shown in Figure 23. Each transmission of information on the SDA is 9 bits as a unit. The first eight bits are the data to be transmitted, and the first one is the most significant bit (Most Significant Bit, MSB), the ninth bit is an confirmation bit (Acknowledge, ACK or A), as shown in Figure 24. When the SDA transmits a low level in ninth clock pulse, it means the acknowledgment bit is 1, namely the current transmission of 8 bits' data is confirmed, otherwise it means that the data transmission has not been confirmed. Any amount of data can be transferred between START and STOP state.

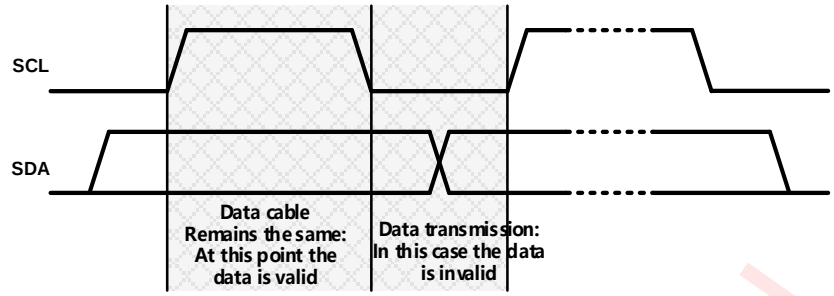


Figure 23 The data transfer rules on the I²C bus

The whole process of actual data transmission is shown in Figure 24. When generating a START condition, the master device sends an 8-bit data, including a 7-bit slave addresses (Slave Address), and followed by a "read / write" flag ($R/\overline{W}$). The flag is used to specify the direction of transmission of subsequent data. The master device will produce the STOP state to end the process after the data transmission is completed. However, if the master device intends to continue data transmission, you can directly send a Repeated START state, without the need to use the STOP state to end transmission.

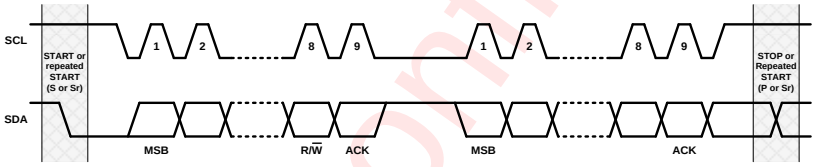


Figure 24 Data transmission on the I²C bus

Write Process

Writing process refers to the master device write data into the slave device. In this process, the transfer direction of the data is always unchanged from the master device to the slave device. All acknowledge bits are transferred by the slave device, in particular, the device as the slave device, the transmission process in accordance with the following steps, as shown in Figure 25:

Master device generates START state. The START state is produced by pulling the data line SDA to a low level when the clock SCL signal is a high level.

Master device transmits the 7-bits device address of the slave device, followed by the "read / write" flag (flag $R/\overline{W} = 0$);

The slave device asserts an acknowledgment bit (ACK) to confirm whether the device address is correct;

The master device transmits the 8-bit register address to which the first data byte will written；

The slave device asserts an acknowledgment (ACK) bit to confirm the register address is correct;

Master sends 8 bits of data to register which needs to be written;

The slave device asserts an acknowledgment bit (ACK) to confirm whether the data is sent successfully;

If the master device needs to continue transmitting data by sending another pair of data bytes, just need to repeat the sequence from step 6. In the latter case, the targeted register address will have been auto-incremented by the device.

The master device generates the STOP state to end the data transmission.

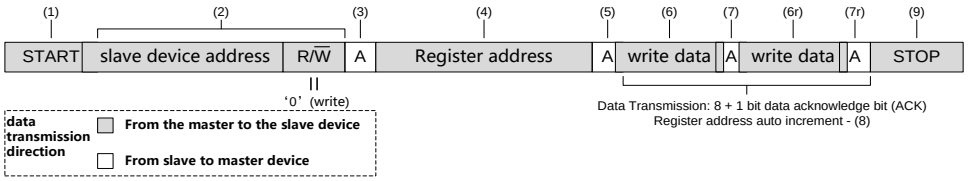


Figure 25 Writing process (data transmission direction remains the same)

Read Process

Reading process refers to the slave device reading data back to the master device. In this process, the direction of data transmission will change. Before and after the change, the master device sends START state and slave address twice, and sends the opposite "read/write" flag. In particular, AW86224A/B as the slave device, the transmission process carried out by following steps listed in Figure 26:
Master device asserts a start condition;

Master device transmits the 7 bits address of the device, and followed by a "read / write" flag ($R/\overline{W}$ = 0);
The slave device asserts an acknowledgment bit (ACK) to confirm whether the device address is correct;
The master device transmits the register address to make sure where the first data byte will read;
The slave device asserts an acknowledgment (ACK) bit to confirm whether the register address is correct or not;
The master device restarts the data transfer process by continuously generating STOP state and START state or a separate Repeated START;

Master sends 7-bits address of the slave device and followed by a read / write flag (flag $R/\overline{W}$ = 1) again;
The slave device asserts an acknowledgment (ACK) bit to confirm whether the register address is correct or not;
Master transmits 8 bits of data to register which needs to be read;
The slave device sends an acknowledgment bit (ACK) to confirm whether the data is sent successfully;
The device automatically increments register address once after sent each acknowledge bit (ACK),
The master device generates the STOP state to end the data transmission.

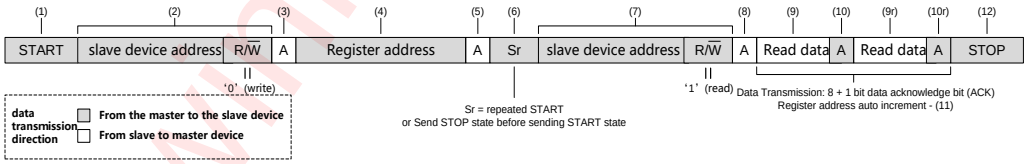


Figure 26 Reading process (data transmission direction remains the same)

CHIP ID

CHIPID(2-bit) consists of CHIPID_H and CHIPID_L. The features of CHIPID are shown in the following table.

Table 4 CHIPID feature

CHIPID (0x64)	Product
CHIPID_H	0: AW86223/AW86224/AW86225 1: AW86214

CHIPID_L	0: AW86224/AW86225 1: AW86223/AW86214

Register Configuration

Register List

ADDR	NAME	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x00	SRST	WO	RESET								0x00
0x01	SYSST	RO			UVLS	FF_AES	FF_AFS	OCDS	OTS	DONES	0x10
0x02	SYSINT	RC			UVLI	FF_AEI	FF_AFI	OCDI	OTI	DONEI	0x10
0x03	SYSINTM	RW			UVLM	FF_AEM	FF_AFM	OCDM	OTM	DONEM	0x3F
0x04	SYSST2	RO					LDO_OK				0x01
0x07	PLAYCFG2	RW	GAIN								0x80
0x08	PLAYCFG3	RW			STOP_MODE			BRK_EN	PLAY_MODE		0x04
0x09	PLAYCFG4	RW							STOP	GO	0x00
0x0A	WAVCFG1	RW	SEQ1WAIT	WAVSEQ1							0x01
0x0B	WAVCFG2	RW	SEQ2WAIT	WAVSEQ2							0x00
0x0C	WAVCFG3	RW	SEQ3WAIT	WAVSEQ3							0x00
0x0D	WAVCFG4	RW	SEQ4WAIT	WAVSEQ4							0x00
0x0E	WAVCFG5	RW	SEQ5WAIT	WAVSEQ5							0x00
0x0F	WAVCFG6	RW	SEQ6WAIT	WAVSEQ6							0x00
0x10	WAVCFG7	RW	SEQ7WAIT	WAVSEQ7							0x00
0x11	WAVCFG8	RW	SEQ8WAIT	WAVSEQ8							0x00
0x12	WAVCFG9	RW	SEQ1LOOP				SEQ2LOOP				0x00
0x13	WAVCFG10	RW	SEQ3LOOP				SEQ4LOOP				0x00
0x14	WAVCFG11	RW	SEQ5LOOP				SEQ6LOOP				0x00
0x15	WAVCFG12	RW	SEQ7LOOP				SEQ8LOOP				0x00
0x16	WAVCFG13	RW		WAITSLOT			MAINLOOP				0x00
0x18	CONTCFG1	RW	EDGE_FRE				EN_F0_DET			SIN_MODE	0xE1
0x19	CONTCFG2	RW	F_PRE								0x8D
0x1A	CONTCFG3	RW	DRV_WIDTH								0x6A
0x1C	CONTCFG5	RW					BRK_GAIN				0x08
0x1D	CONTCFG6	RW	TRACK_EN	DRV1_LVL							0xFF
0x1E	CONTCFG7	RW		DRV2_LVL							0x50
0x1F	CONTCFG8	RW	DRV1_TIME								0x04
0x20	CONTCFG9	RW	DRV2_TIME								0x06
0x21	CONTCFG10	RW	BRK_TIME								0x08
0x22	CONTCFG11	RW	TRACK_MARGIN								0x0F
0x25	CONTRD14	RO	F_LRA_F0_H								0x00
0x26	CONTRD15	RO	F_LRA_F0_L								0x00
0x27	CONTRD16	RO	CONT_F0_H								0x00
0x28	CONTRD17	RO	CONT_F0_L								0x00
0x2D	RTPCFG1	RW					BASE_ADDR_H				0x38
0x2E	RTPCFG2	RW	BASE_ADDR_L								0x00
0x2F	RTPCFG3	RW	FIFO_AEH				FIFO_AFH				0x26
0x30	RTPCFG4	RW	FIFO_AEL								0x00
0x31	RTPCFG5	RW	FIFO_AFL								0x00
0x32	RTPDATA	RW	RTP_DATA								0x00
0x33	TRGCFG1	RW	TRG1_POS	TRG1SEQ_P							0x01
0x36	TRGCFG4	RW	TRG1_NEG	TRG1SEQ_N							0x01
0x39	TRGCFG7	RW	TRG1_POLAR	TRG1_LEV	TRG1_BRK						0x22
0x3A	TRGCFG8	RW				TRG1_MODE		TRG1_STOP			0x20
0x3C	GLBCFG2	RW	START_DLY								0x04
0x3E	GLBCFG4	RW	GO_PRIO						TRG1_PRIO		0x1B
0x3F	GLBRD5	RO					GLB_STATE				0x00
0x40	RAMADDRH	RW					RAMADDRH				0x00
0x41	RAMADDRL	RW	RAMADDRL								0x00
0x42	RAMDATA	RW	RAMDATA								0x00
0x43	SYSCTRL1	RW	VBAT_MODE				EN_RAMINIT	EN_FIR			0x04

0x44	SYSCTRL2	RW	WAKE	STANDBY		INTN_PIN		WAVDAT_MODE	0x28
0x49	SYSCTRL7	RW		GAIN_BYPASS			D2S_GAIN		0x14
0x4C	PWMCFG1	RW	PRC_EN	PRCTIME					0xA0
0x4D	PWMCFG2	RW			PD_HWM				0x28
0x4E	PWMCFG3	RW	PR_EN	PRLVL					0xBF
0x4F	PWMCFG4	RW	PRTIME						0x32
0x51	DETCFG1	RW			RL_OS		CLK_ADC		0x02
0x52	DETCFG2	RW					VBAT_GO	DIAG_GO	0x00
0x53	DET_RL	RO	RL						0x00
0x55	DET_VBAT	RO	VBAT						0x00
0x57	DET_LO	RO		VBAT_LO			RL_LO		0x00
0x53	TRIMCFG3	RW		TRIM_LRA					0x00
0x64	CHIPID	RO		CHIPID_H				CHIPID_L	
0x77	ANACFG8	RW	TRTF_CTRL_HDRV						0x00

Register Detailed Description

Note: Reserved register should not be write

SRST: (Address 00h)

Bit	Symbol	R/W	Description	Default
7:0	RESET	WO	All configuration registers will be reset to default value after 0xaa is written	0x00

SYSST: (Address 01h)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RO	Not used	0
5	UVLS	RO	1: VDD voltage is under UV voltage (2.7V)	0
4	FF_AES	RO	1: RTP FIFO almost empty	1
3	FF_AFS	RO	1: RTP FIFO almost full	0
2	OCDS	RO	1: Over Current status	0
1	OTS	RO	1: Over Temperature status	0
0	DONES	RO	1: The indication of playback	0

SYSINT: (Address 02h)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RC	Not used	0
5	UVLI	RC	When UVLI=1, it means UVLS has been 1 at least once since the last read	0
4	FF_AEI	RC	When FF_AEI=1, it means FF_AES has been 1 at least once since the last read	1
3	FF_AFI	RC	When FF_AFI=1, it means FF_AFS has been 1 at least once since the last read	0
2	OCDI	RC	When OCDI=1, it means OCDS has been 1 at least once since the last read	0
1	OTI	RC	When OTI=1, it means OTS has been 1 at least once since the last read	0
0	DONEI	RC	When DONEI=1, it means DONES has been 1 at least once since the last read	0

SYSINTM: (Address 03h)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RW	Not used	0
5	UVLM	RW	Interrupt mask for UVLI: 0: INTN pin will be pulled down when UVLI=1 1: INTN pin will not be pulled down when UVLI=1	1
4	FF_AEM	RW	Interrupt mask for FF_AEI: 0: INTN pin will be pulled down when FF_AEI=1 1: INTN pin will not be pulled down when FF_AEI=1	1
3	FF_AFM	RW	Interrupt mask for FF_AFI: 0: INTN pin will be pulled down when FF_AFI=1 1: INTN pin will not be pulled down when FF_AFI=1	1

2	OCDM	RW	Interrupt mask for OCDI: 0: INTN pin will be pulled down when OCDI=1 1: INTN pin will not be pulled down when OCDI=1	1
1	OTM	RW	Interrupt mask for OTI: 0: INTN pin will be pulled down when OTI=1 1: INTN pin will not be pulled down when OTI=1	1
0	DONEM	RW	Interrupt mask for DONEI: 0: INTN pin will be pulled down when DONEI=1 1: INTN pin will not be pulled down when DONEI=1	1

SYSST2: (Address 04h)

Bit	Symbol	R/W	Description	Default
7:4	Reserved	RO	Not used	0
3	LDO_OK	RO	LDO OK indication	0
2:0	Reserved	RO	Not used	1

PLAYCFG2: (Address 07h)

Bit	Symbol	R/W	Description	Default
7:0	GAIN	RW	gain setting for waveform data of RAM/RTP/TRIG mode, GAIN=code/128 GAIN_BYPASS=1, can be changed when playing GAIN_BYPASS=0, cannot be changed when playing	0x80

PLAYCFG3: (Address 08h)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RW	Not used	0
5	STOP_MODE	RW	0: stop when current wave is over 1: stop right now	0
4:3	Reserved	RW	Not used	0
2	BRK_EN	RW	When set 1, enable auto brake after RTP/RAM/CONT playback mode is stopped	1
1:0	PLAY_MODE	RW	Waveform play mode for GO TRIG: b00: RAM mode b01: RTP mode b10: CONT mode b11: no play	0

PLAYCFG4: (Address 09h)

Bit	Symbol	R/W	Description	Default
7:2	Reserved	RW	Not used	0
1	STOP	RW	when set 1, stop the current playback mode	0
0	GO	RW	RAM/RTP/CONT mode playback trig bit when set to 1, chip will playback one of the paly mode.	0

WAVCFG1: (Address 0Ah)

Bit	Symbol	R/W	Description	Default
7	SEQ1WAIT	RW	When set to 1, WAVSEQ1 means wait time, else means wave sequence number	0
6:0	WAVSEQ1	RW	Wait time (code*WAITSLOT) or wave sequence number	1

WAVCFG2: (Address 0Bh)

Bit	Symbol	R/W	Description	Default
7	SEQ2WAIT	RW	When set to 1, WAVSEQ2 means wait time, else means wave sequence number	0
6:0	WAVSEQ2	RW	Wait time (code*WAITSLOT) or wave sequence number	0

WAVCFG3: (Address 0Ch)

Bit	Symbol	R/W	Description	Default
7	SEQ3WAIT	RW	When set to 1, WAVSEQ3 means wait time, else means wave sequence number	0

6:0	WAVSEQ3	RW	Wait time (code*WAITSLOT) or wave sequence number	0

WAVCFG4: (Address 0Dh)

Bit	Symbol	R/W	Description	Default
7	SEQ4WAIT	RW	When set to 1, WAVSEQ4 means wait time, else means wave sequence number	0
6:0	WAVSEQ4	RW	Wait time (code*WAITSLOT) or wave sequence number	0

WAVCFG5: (Address 0Eh)

Bit	Symbol	R/W	Description	Default
7	SEQ5WAIT	RW	When set to 1, WAVSEQ5 means wait time, else means wave sequence number	0
6:0	WAVSEQ5	RW	Wait time (code*WAITSLOT) or wave sequence number	0

WAVCFG6: (Address 0Fh)

Bit	Symbol	R/W	Description	Default
7	SEQ6WAIT	RW	When set to 1, WAVSEQ6 means wait time, else means wave sequence number	0
6:0	WAVSEQ6	RW	Wait time (code*WAITSLOT) or wave sequence number	0

WAVCFG7: (Address 10h)

Bit	Symbol	R/W	Description	Default
7	SEQ7WAIT	RW	When set to 1, WAVSEQ7 means wait time, else means wave sequence number	0
6:0	WAVSEQ7	RW	Wait time (code*WAITSLOT) or wave sequence number	0

WAVCFG8: (Address 11h)

Bit	Symbol	R/W	Description	Default
7	SEQ8WAIT	RW	When set to 1, WAVSEQ8 means wait time, else means wave sequence number	0
6:0	WAVSEQ8	RW	Wait time (code*WAITSLOT) or wave sequence number	0

WAVCFG9: (Address 12h)

Bit	Symbol	R/W	Description	Default
7:4	SEQ1LOOP	RW	Control the loop number of the first sequence: b0000~b1110: play code+1 time b1111: playback infinitely until STOP set to 1 or SEQ1LOOP ≠0xF	0
3:0	SEQ2LOOP	RW	Control the loop number of the second sequence: b0000~b1110: play code+1 time b1111: playback infinitely until STOP set to 1 or SEQ2LOOP ≠0xF	0

WAVCFG10: (Address 13h)

Bit	Symbol	R/W	Description	Default
7:4	SEQ3LOOP	RW	control the loop number of the third sequence b0000~b1110: play code+1 time b1111: playback infinitely until STOP set to 1 or SEQ3LOOP ≠0xF	0
3:0	SEQ4LOOP	RW	control the loop number of the fourth sequence b0000~b1110: play code+1 time b1111: playback infinitely until STOP set to 1 or SEQ4LOOP ≠0xF	0

WAVCFG11: (Address 14h)

Bit	Symbol	R/W	Description	Default
7:4	SEQ5LOOP	RW	control the loop number of the fifth sequence b0000~b1110: play code+1 time b1111: playback infinitely until STOP set to 1 or SEQ5LOOP ≠0xF	0
3:0	SEQ6LOOP	RW	control the loop number of the sixth sequence b0000~b1110: play code+1 time b1111: playback infinitely until STOP set to 1 or SEQ6LOOP ≠0xF	0

WAVCFG12: (Address 15h)				
Bit	Symbol	R/W	Description	Default
7:4	SEQ7LOOP	RW	control the loop number of the seventh sequence b0000~b1110: play code+1 time b1111: playback infinitely until STOP set to 1 or SEQ7LOOP ≠0xF	0
3:0	SEQ8LOOP	RW	control the loop number of the eighth sequence b0000~b1110: play code+1 time b1111: playback infinitely until STOP set to 1 or SEQ8LOOP ≠0xF	0

WAVCFG13: (Address 16h)				
Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Not used	0
6:5	WAITSLOT	RW	Unit of wait time b00: (1/WAVDAT_MODE)s b01: (8/WAVDAT_MODE)s b10: (64/WAVDAT_MODE)s b11: (512/WAVDAT_MODE)s	0
4	Reserved	RW	Not used	0
3:0	MAINLOOP	RW	control the main loop number b0000~b1110: play code+1 time b1111: playback infinitely until STOP set to 1 or MAINLOOP ≠ 0xF	0

CONTCFG1: (Address 18h)				
Bit	Symbol	R/W	Description	Default
7:4	EDGE_FRE	RW	Define the edge frequency b1000: 200Hz b1001: 210Hz b1010: 260Hz b1011: 280Hz b1100: 300Hz b1101: 600Hz b1110: 700Hz b1111: 800Hz b0000-b0111: play non-filtered square wave in CONT mode	14
3	EN_F0_DET	RW	F0 detection mode enable 0: disable 1: enable	0
2:1	Reserved	RW	Not used	0
0	SIN_MODE	RW	Edge mode for filtered square wave of CONT mode: 0: sine 1: cos	1

CONTCFG2: (Address 19h)				
Bit	Symbol	R/W	Description	Default
7:0	F_PRE	RW	Set the value of F0, F0=(24K/code)Hz	0x8D

CONTCFG3: (Address 1Ah)				
Bit	Symbol	R/W	Description	Default
7:0	DRV_WIDTH	RW	half cycle drive time(code/48K s) of brake, this value must be smaller than half cycle time of F0. DRV_WIDTH is recommended to be configured as(24k/F0)-8-TRACK_MARGIN-BRK_GAIN	0x6A

CONTCFG5: (Address 1Ch)				
Bit	Symbol	R/W	Description	Default

7:4	Reserved	RW	Not used	0
3:0	BRK_GAIN	RW	Gain factor of brake	8

CONTCFG6: (Address 1Dh)

Bit	Symbol	R/W	Description	Default
7	TRACK_EN	RW	Track switch: 0: disable 1: enable	1
6:0	DRV1_LVL	RW	Level for the first cont drive. When VBAT_MODE=1: no load output voltage=6.1*DRV1_LVL/128(V); if (6.1*DRV1_LVL)/VDD > 128, no load output voltage=VDD; When VBAT_MODE=0: no load output voltage=VDD*DRV1_LVL/128(V)	0x7F

CONTCFG7: (Address 1Eh)

Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Not used	0
6:0	DRV2_LVL	RW	Level for the second cont drive. When VBAT_MODE=1: no load output voltage=6.1*DRV1_LVL/128(V); if (6.1*DRV1_LVL)/VDD > 128, no load output voltage=VDD; When VBAT_MODE=0: no load output voltage=VDD*DRV1_LVL/128(V)	0x50

CONTCFG8: (Address 1Fh)

Bit	Symbol	R/W	Description	Default
7:0	DRV1_TIME	RW	Number of half cycle for the first cont drive	4

CONTCFG9: (Address 20h)

Bit	Symbol	R/W	Description	Default
7:0	DRV2_TIME	RW	Number of half cycle for the second cont drive.	6

CONTCFG10: (Address 21h)

Bit	Symbol	R/W	Description	Default
7:0	BRK_TIME	RW	The number of half cycle of brake mode	8

CONTCFG11: (Address 22h)

Bit	Symbol	R/W	Description	Default
7:0	TRACK_MARGIN	RW	Margin value of tracking, the smaller margin, the higher tracking accuracy and the lower loop stability(unit: 1/48K s)	15

CONTRD14: (Address 25h)

Bit	Symbol	R/W	Description	Default
7:0	F_LRA_F0_H	RO	High 8 bit of the measure value for the f0 of LRA in the f0 detection mode F0=(384000/(F_LRA_F0_H*256+F_LRA_F0_L))Hz	0

CONTRD15: (Address 26h)

Bit	Symbol	R/W	Description	Default
7:0	F_LRA_F0_L	RO	Low 8 bit of the measure value for the f0 of LRA in the f0 detection mode F0=(384000/(F_LRA_F0_H*256+F_LRA_F0_L))Hz	0

CONTRD16: (Address 27h)

Bit	Symbol	R/W	Description	Default

7:0	CONT_F0_H	RO	The measure value for the f0 of LRA in the continuous detection mode(high eight bits) F0=(384000/(CONT_F0_H*256+CONT_F0_L))Hz	0

CONTRD17: (Address 28h)

Bit	Symbol	R/W	Description	Default
7:0	CONT_F0_L	RO	The measure value for the f0 of LRA in the continuous detection mode(low eight bits) F0=(384000/(CONT_F0_H*256+CONT_F0_L))Hz	0

RTPCFG1: (Address 2Dh)

Bit	Symbol	R/W	Description	Default
7:4	Reserved	RW	Not used	3
3:0	BASE_ADDR_H	RW	High four bits of start address of wave SRAM BASE_ADDR = BASE_ADDR_H * 256 + BASE_ADDR_L	0x08

RTPCFG2: (Address 2Eh)

Bit	Symbol	R/W	Description	Default
7:0	BASE_ADDR_L	RW	Low eight bits of start address of wave SRAM BASE_ADDR = BASE_ADDR_H * 256 + BASE_ADDR_L	0

RTPCFG3: (Address 2Fh)

Bit	Symbol	R/W	Description	Default
7:4	FIFO_AEH	RW	High four bits of RTP FIFO almost empty threshold FIFO_AE = FIFO_AEH * 256 + FIFO_AEL	0x02
3:0	FIFO_AFH	RW	High four bits of RTP FIFO almost full threshold FIFO_AF = FIFO_AFH * 256 + FIFO_AFL	0x06

RTPCFG4: (Address 30h)

Bit	Symbol	R/W	Description	Default
7:0	FIFO_AEL	RW	Low eight bits of RTP FIFO almost empty threshold FIFO_AE = FIFO_AEH * 256 + FIFO_AEL	0x00

RTPCFG5: (Address 31h)

Bit	Symbol	R/W	Description	Default
7:0	FIFO_AFL	RW	Low eight bits of RTP FIFO almost full threshold FIFO_AF = FIFO_AFH * 256 + FIFO_AFL	0x00

RTPDATA: (Address 32h)

Bit	Symbol	R/W	Description	Default
7:0	RTP_DATA	RW	RTP mode , data write entry, when data written into this register, the data will be written into RTP FIFO	0

TRGCFG1: (Address 33h)

Bit	Symbol	R/W	Description	Default
7	TRG1_POS	RW	TRG1 rising edge enable/disable control 0: disable 1: enable	0
6:0	TRG1SEQ_P	RW	TRIG1 posedge trigged wave sequence number	1

TRGCFG4: (Address 36h)

Bit	Symbol	R/W	Description	Default
7	TRG1_NEG	RW	TRG1 falling edge enable/disable control 0: disable 1: enable	0

6:0	TRG1SEQ_N	RW	TRIG1 negedge trigged wave sequence number	1

TRGCFG7: (Address 39h)

Bit	Symbol	R/W	Description	Default
7	TRG1_POLAR	RW	TRIG1 pin active polarity, when host supply positive level, this bit set to 0, else set to 1	0
6	TRG1_LEV	RW	TRG1 mode control 0: edge 1: level	0
5	TRG1_BRK	RW	When set 1, enable auto brake after TRG1 playback mode is stopped	1
4:0	Reserved	RW	Not used	2

TRGCFG8: (Address 3Ah)

Bit	Symbol	R/W	Description	Default
7:5	Reserved	RW	Not used	1
4:3	TRG1_MODE	RW	TRIG pin playback mode selection b00: PWM_LRA mode b00: PWM_ERM mode b10: TRIG mode b11: None This product does not support PWM_LRA and PM_ERM modes, users must configure this register as TRIG mode after powering on	0
2	TRG1_STOP	RW	When set 1, TRG1 playback mode can be stopped immediately	0
1:0	Reserved	RW	Not used	0

GLBVFG2: (Address 3Ch)

Bit	Symbol	R/W	Description	Default
7:0	START_DLY	RW	Startup delay time, unit time is (1/48k)s	4

GLBCFG4: (Address 3Eh)

Bit	Symbol	R/W	Description	Default
7:6	GO_PRIO	RW	Priority value of GO TRIG High priority can interrupt the playback of low priority, and low priority cannot interrupt the playback of high priority. When the priority settings are consistent, the default priority will be implemented	0
5:2	Reserved	RW	Not used	6
1:0	TRG1_PRIO	RW	Priority value of TRIG1 pin High priority can interrupt the playback of low priority, and low priority cannot interrupt the playback of high priority. When the priority settings are consistent, the default priority will be implemented	3

GLBRD5: (Address 3Fh)

Bit	Symbol	R/W	Description	Default
7:4	Reserved	RO	Not used	0
3:0	GLB_STATE	RO	The state of glb state b0000: STANDBY b0110: CONT b0111: RAM b1000: RTP b1001: TRIG b1011: BRAKE	0

RAMADDRH: (Address 40h)

Bit	Symbol	R/W	Description	Default
7:4	Reserved	RW	Not used	0
3:0	RAMADDRH	RW	SRAM address high 4 bits	0

RAMADDRL: (Address 41h)				
Bit	Symbol	R/W	Description	Default
7:0	RAMADDRL	RW	SRAM address low eight bits	0

RAMDATA: (Address 42h)				
Bit	Symbol	R/W	Description	Default
7:0	RAMDATA	RW	SRAM data entry	0

SYSCTRL1: (Address 43h)				
Bit	Symbol	R/W	Description	Default
7	VBAT_MODE	RW	VDD adjust mode: 0: software adjust mode 1: hardware adjust mode	0
6:4	Reserved	RW	Not used	0
3	EN_RAMINIT	RW	Enable clock: 1: open the digital module clock 0: close the digital module clock	0
2	EN_FIR	RW	Set enable of FIR filter	1
1:0	Reserved	RW	Not used	0

SYSCTRL2: (Address 44h)				
Bit	Symbol	R/W	Description	Default
7	WAKE	RW	Chip enable control 1: force the chip to enter active mode	0
6	STANDBY	RW	Chip disable control: 1: force the chip to enter standby mode	0
5:4	Reserved	RW	Not used	2
3	INTN_PIN	RW	Multi-mode PIN control: 0: INTN/TRIG used as TRIG1 1: INTN/TRIG used as INTN	1
2	Reserved	RW	Not used	0
1:0	WAVDAT_MODE	RW	Waveform data sample rate selection: b00: 24Khz b01: 48kHz others: 12KHz rate	0

SYSCTRL7: (Address 49h)				
Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Not used	0
6	GAIN_BYPASS	RW	0: gain cannot be changed when playing 1: gain can be changed when playing	0
5:3	Reserved	RW	Not used	2
2:0	D2S_GAIN	RW	Set D2S gain: b000: 1 b001: 2 b010: 4 b011: 5 b100: 8 b101: 10 b110: 20 b111: 40	4

PWMCFG1: (Address 4Ch)				
Bit	Symbol	R/W	Description	Default
7	PRC_EN	RW	Set enable of output signal protection mode of pwm: 0: disable	1

			1: HDP/HDN output voltage ≥ 124/128*VDD maintains (PRCTIME/3k)s, HDP/HDN is pulled down protectively	
6:0	PRCTIME	RW	Set protection time of output signal protection mode of pwm, unit time is (1/3k) s.	0x20

PWMCFG2: (Address 4Dh)

Bit	Symbol	R/W	Description	Default
7:5	Reserved	RW	Not used	1
4	PD_HWM	RW	shutdown half wave modulate 0: half wave mode 1: full wave mode	0
3:0	Reserved	RW	Not used	8

PWMCFG3: (Address 4Eh)

Bit	Symbol	R/W	Description	Default
7	PR_EN	RW	Set enable of input signal protection mode of pwm: 0: disable 1: HDP/HDN output voltage >= PRLVL/128*VDD maintains (PRTIME/3k)s, HDP/HDN is pulled down protectively	1
6:0	PRLVL	RW	Set protection voltage of output signal protection mode of pwm	0x3F

PWMCFG4: (Address 4Fh)

Bit	Symbol	R/W	Description	Default
7:0	PRTIME	RW	Set protection time of input signal protection mode of pwm, unit time is (1/3k) s.	0x32

DETCFG1: (Address 51h)

Bit	Symbol	R/W	Description	Default
7:5	Reserved	RW	Not used	0
4	RL_OS	RW	Set diagnostic mode 0:disable 1:RL	0
3	Reserved	RW	Not used	0
2:0	CLK_ADC	RW	Set frequency of ADC clock b000: 12MHz b001: 6MHz b010: 3MHz b011: 1.5MHz b100: 0.75MHz b101: 0.375MHz b110: 0.1875MHz b111: 0.09375MHz	2

DETCFG2: (Address 52h)

Bit	Symbol	R/W	Description	Default
7:2	Reserved	RW	Not used	0
1	VBAT_GO	RW	Set the enabled of VBAT mode	0
0	DIAG_GO	RW	Set the enabled of DIAG mode	0

DET_RL: (Address 53h)

Bit	Symbol	R/W	Description	Default
7:0	RL	RO	The measured value of resistance of LRA in DIAG mode(high eight bits) RL=((RL*4+RL_LO)*678)/(1024*d2s_gain)Ω	0

DET_VBAT: (Address 55h)

Bit	Symbol	R/W	Description	Default
7:0	VBAT	RO	The measured value of VDD in VBAT mode(high eight bits) VDD=((VBAT*4+VBAT_LO)*6.1/1024)V	0

DET_LO: (Address 57h)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RO	Not used	0
5:4	VBAT_LO	RO	The measured value of VDD in VBAT mode(low two bits) VDD=((VBAT*4+VBAT_LO)*6.1/1024)V	0
3:2	Reserved	RO	Not used	0
1:0	RL_LO	RO	the Measured value of resistance of LRA in DIAG mode(low two bits) RL=((RL*4+RL_LO)*678)/(1024*d2s_gain)Ω	0

TRIMCFG3: (Address 5Ah)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RW	Not used	0
5:0	TRIM_LRA	RW	Register LRA trim setting Trimming OSC frequency adaptive for LRA resonant frequency deviation, rate = 0.18%~0.26% b000000: LRA(1+0%)(LRA real resonant frequency) b000001~b011111: LRA(1+n*rate) b111111~b100000: LRA(1-n*rate)	0

CHIPID: (Address 64h)

Bit	Symbol	R/W	Description	Default
7	Reserved	RO	Not used	1
6	CHIPID_H	RO	Enable I2C address selection pin 0: disable(AW86223/AW86224/AW86225) 1: enable(AW86214)	0
5:1	Reserved	RO	TRIM data	
0	CHIPID_L	RO	Distinguish between 9pin chip and 12pin chip 0: 9pin chip(AW86224/AW86225) 1: 12pin chip(AW86223/AW86214)	0

ANACFG8: (Address 77h)

Bit	Symbol	R/W	Description	Default
7:6	TRTF_CTRL_HDRV	RW	HDP and HDN rising time control b00: Trise = 60ns b01: Trise = 20ns b10: Trise = 16ns b11: Trise = 4ns	0
5:0	Reserved	RW	Not used	0

Application Information

Capacitors Selection

SUPPLY DECOUPLING CAPACITOR（CS）

The device requires adequate power supply decoupling. Place a low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1μF. This choice of capacitor and placement helps with higher frequency transients, spikes, or digital hash on the line. Additionally, placing this decoupling capacitor close to the device is important, as any parasitic resistance or inductance between the device and the capacitor causes efficiency loss. In addition to the 0.1μF ceramic capacitor, place a 10μF capacitor on the VDD supply trace. This larger capacitor acts as a charge reservoir, providing energy faster than the board supply, thus helping to prevent any droop in the supply voltage.

OUTPUT BEADS, CAPACITORS

The device output is a square wave signal, which causing switch current at the output capacitor, increasing static power consumption, and therefore output capacitor should not be too large, 0.1nF ceramic capacitors is recommended.

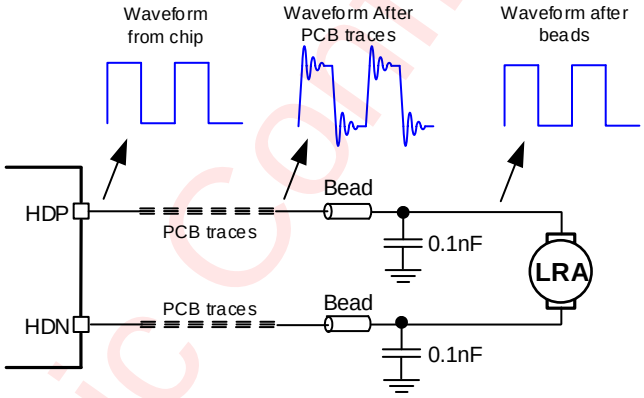


Figure 27 Ferrite Chip Bead and capacitor

The device output is a square wave signal. The voltage across the capacitor will be much larger than the VDD voltage after increasing the bead capacitor. It suggested the use of rated voltage above 10V capacitor. At the same time a square wave signal at the output capacitor switching current form, the static power consumption increases, so the output capacitance should not be too much which is recommended 0.1nF ceramic capacitor rated voltage of 10V. If you want to get better EMI suppression performance, can use 1nF, rated voltage 10V capacitor, but quiescent current will increase.

PCB Layout Consideration

To obtain the optimal performance, PCB layout should be considered carefully. The suggested Layout is illustrated in the following diagram:

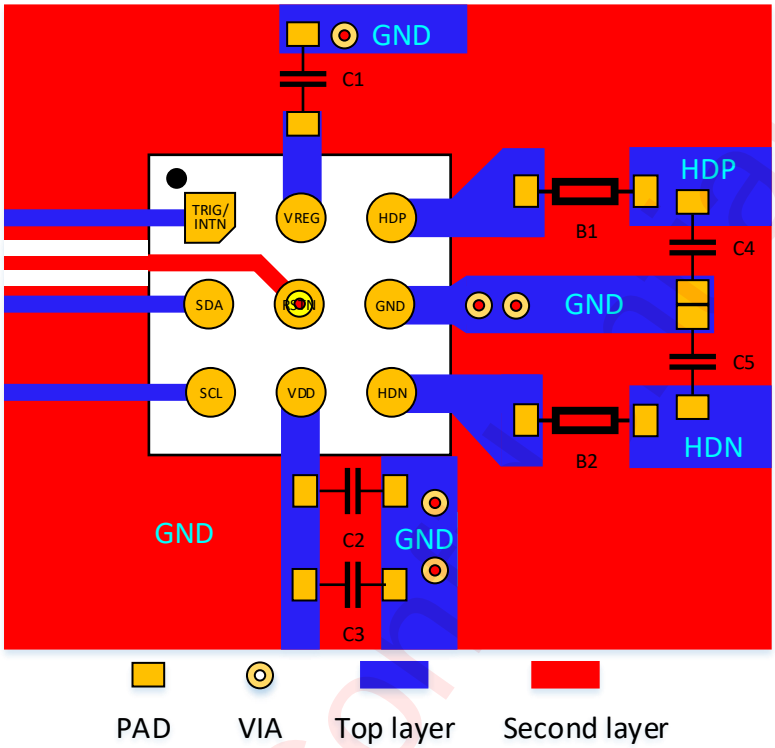


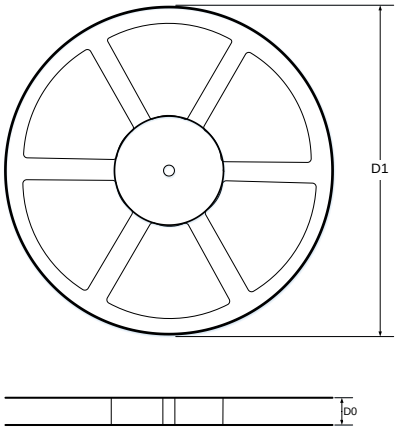
Figure 28 AW86224A/B Board Layout

PCB Layout Guidelines:

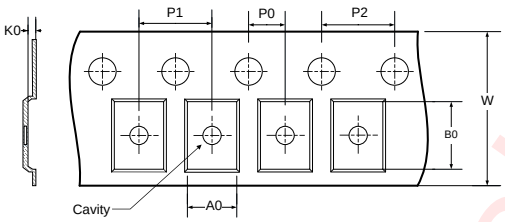
1. Devices around the chip should be placed as close as possible to the chip pins.
2. I2C are recommended to be shield by gnd.
3. VDD/VREG power supply lines are as short and thick as possible. The current flow capacity of the traces not be less than $\frac{VDD}{(RL+Rdson)*\eta}$. (RL is motor DC impedance, Rdson takes 0.75Ω, η is chip overall efficiency takes 80%)
4. HDP/HDN lines are as short and thick as possible. and the current flow capacity of the traces not be less than $\frac{VDD}{(RL+Rdson)}$
5. HDP, HDN are recommended to be shield by gnd, away from interfering sources (especially FLY capacitors of high power charge IC), otherwise F0 detection may be inaccurate.

Tape And Reel Information

REEL DIMENSIONS

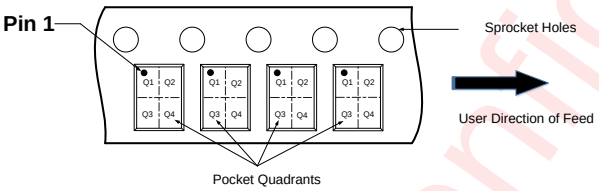


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

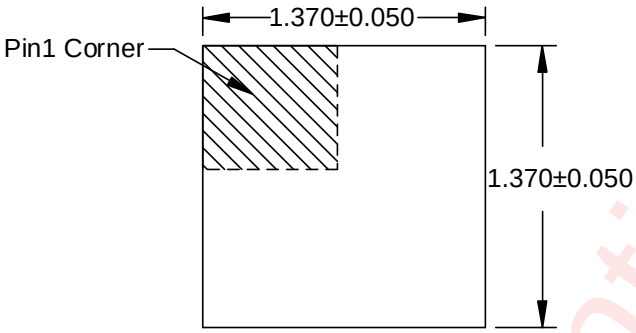


DIMENSIONS AND PIN1 ORIENTATION

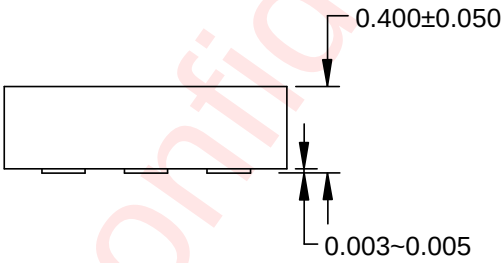
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178.0±1.0	8.4+2.0/-0.0	1.55±0.05	1.55±0.05	0.55±0.05	2.00±0.05	4.00±0.10	4.00±0.10	8.00+0.30/-0.10	Q1

All dimensions are nominal

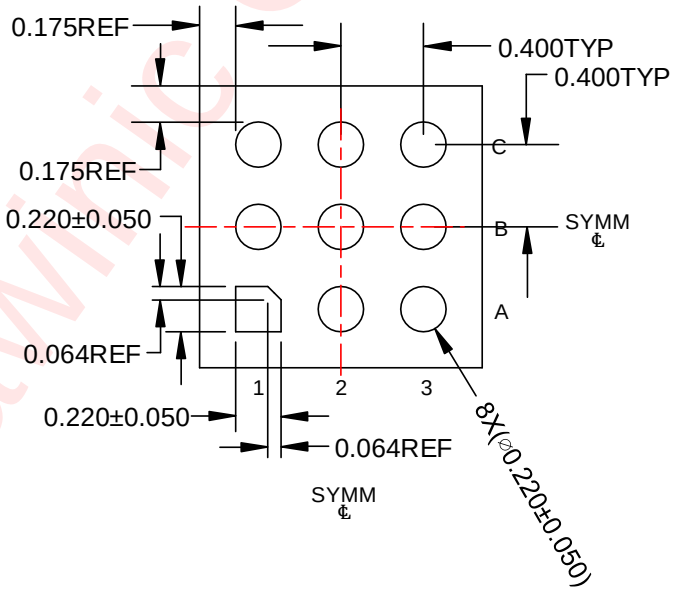
Package Description



TOP VIEW



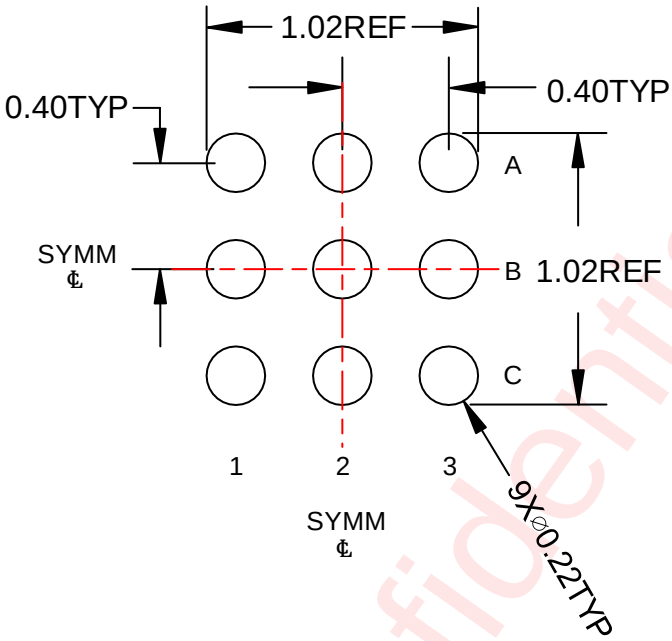
SIDE VIEW

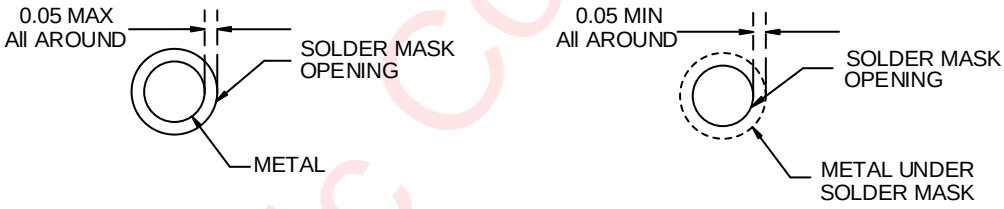


BOTTOM VIEW

Unit:mm

Land Pattern Data





NON-SOLDER MASK DEFINED

SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Change Record
V1.0	April 2021	Official Version
V1.1	April 2021	Modify Pin Definition
V1.2	June 2021	Modify Pin Definition and Waveform library initialization steps
V1.3	August 2021	Modify Register Detailed Description and Detailed Functional Description
V1.4	September 2021	Modify Detailed Functional Description
V1.5	September 2021	Modify CHIP ID
V1.6	November 2021	Modify Electrical Characteristics
V1.7	November 2021	Modify AMR and Detailed Functional Description

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