LONTIUM SEMICONDUCTOR CORPORATION

ClearEdge™ Technology

LT9611UXC

Dual-Port MIPI DSI/CSI to HDMI2.0 with Audio

Datasheet

1. Features

- **Single/Dual-Port MIPI DSI/CSI Receiver**
  - Compliant with D-PHY1.2 & DSI1.3 & CSI-2 1.3
  - Integrated DSC1.2 decoder
  - 1/2 configurable ports
  - 1 clock lane and 1/2/3/4 configurable data lanes per port
  - 80Mbps~2Gbps per data lane
  - Skew calibration
  - Programmable receiver equalizer
  - Support data lane swap(arbitrarily) and polarity inversion(independent)
  - 3D support: two ports simultaneously receiving L and R frames or odd-L/even-R alternative pixels
  - DSI support both burst mode and non-burst mode
  - DSI support video formats:
    DSC/CSC disabled: Packed 16/18/24/30/36-bit RGB, Loosely Packed 18-bit RGB, Packed 16/24-bit YCbCr4:2:2, Loosely Packed 20-bit YCbCr4:2:2, Packed 12-bit YCbCr4:2:0
    DSC disabled, CSC enabled: Packed 16/18/24/30/36-bit RGB, Loosely Packed 18-bit RGB, Packed 16/24-bit YCbCr4:2:2, Loosely Packed 20-bit YCbCr4:2:2
    DSC enabled, CSC disabled: Packed 24-bit RGB, Packed 16-bit YCbCr4:2:2, Packed 12-bit YCbCr4:2:0
    DSC/CSC enabled: Packed 24-bit RGB, Packed 16-bit YCbCr4:2:2
  - CSI support video formats:
    DSC/CSC disabled: RGB565/666/888, YUV422 8/10-bit, Legacy YUV420 8-bit
    DSC disabled, CSC enabled: RGB565/666/888, YUV422 8/10-bit
    DSC enabled, CSC disabled: RGB888, YUV422 8-bit, Legacy YUV420 8-bit
    DSC/CSC enabled: RGB888, YUV422 8-bit
- **Digital Audio Input**
  - I2S interface supporting 2-channel audio, with sample rates of 32~192 kHz and sample sizes of 16~24 bits
  - SPDIF interface supporting PCM, Dolby Digital, DTS digital audio at up to 192kHz frame rate
  - IEC60958 or IEC61937 compatible
- **HDMI2.0 Transmitter**
  - Compliant with HDMI2.0b, HDMI1.4 and DVI1.0
  - Compliant with HDCP2.2 and HDCP1.4
  - Data rate up to 6Gbps
  - On-die back termination
  - Programmable transmitter swing and pre-emphasis
  - AC-couple capable
  - Support channel swap(arbitrarily) and polarity inversion(independent)
  - Support 4k@60Hz
  - Supported 3D formats: side-by-side(full)
  - Supported video formats:
    DSC/CSC disabled: 24/30/36-bit RGB, 16/20/24-bit YCbCr4:2:2, 8-bit YCbCr4:2:0
    DSC disabled, CSC enabled: 24-bit RGB/YCbCr4:4:4, 16-bit YCbCr4:2:2
    DSC enabled, CSC disabled: 24-bit RGB, 16-bit YCbCr4:2:2, 8-bit YCbCr4:2:0
    DSC/CSC enabled: 24-bit RGB/YCbCr4:4:4, 16-bit YCbCr4:2:2
  - HDR support
  - Support TMDS scrambling for EMI/RFI reduction
  - Support SCDC
  - 5V tolerance DDC/HPD I/Os
- **Miscellaneous**
  - CSC: RGB <-> YUV444 <-> YUV422
  - Integrated CEC Controller
  - External oscillator
  - Integrated microprocessor
  - Embedded SPI flash for firmware and HDCP keys
  - GPIOs for system controls
  - Integrated 100/400kHz I2C slave
  - Firmware update through SPI or I2C interface
  - Power supply: 3.3V for I/O and 1.2V for core
  - ESD 4kV HBM
  - Temperature Range: -40℃ ~ +85℃
  - Package: QFN64 (7.5mm*7.5mm)

2. General Description

The LT9611UXC is a high performance MIPI DSI/CSI to HDMI2.0 converter for STB, DVD applications.

The MIPI DSI/CSI input features configurable single-port or dual-port with 1 high-speed clock lane, and 1~4 high-speed data lanes operating at maximum 2Gbps/lane, which can support a total bandwidth of up to 16Gbps. LT9611UXC supports burst mode DSI video data transferring, also supports flexible video data mapping path. Integrated DSC decoder implements up to 1:3 visually lossless decompression which reduces bandwidth

requirement for UHD video transport, also power consumption and EMI.

The HDMI2.0 output supports data rate up to 6Gbps which provides sufficient bandwidth for 4k@60Hz video. Also HDCP2.2 is supported for data encryption.

Two digital audio input interfaces are available, I2S and SPDIF. The I2S interface supports 2-ch LPCM and the SPDIF interface supports 2-ch LPCM or compressed audio, both at maximum 192kHz sample rate.

The device is capable of automatic operation which is enabled by an integrated microprocessor that uses an embedded SPI flash for firmware storage. System control is also available through the configuration I2C slave interface.

3. Applications

- STB
- DVD/BD
- PTV Box

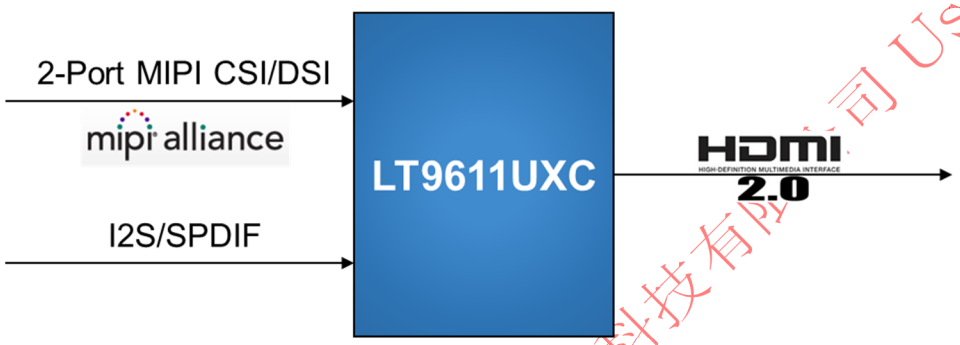


Figure 3.1 Application Diagram

4. Ordering Information

Table 4.1 Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
LT9611UXC	-40℃ to +85℃	QFN64 (7.5*7.5)	Tray

Table of Contents

5. Revision History

Version	Owner	Content	Date
R0.5	HF X	Initial datasheet creation	04/03/2018
R0.6	HF X	Fixed typos	04/17/2018
R0.7	HF X	Updated SPDIF channel number(8->2)	07/18/2018
R0.8	HF X	Added pin description about UART	07/25/2018

6. Pinning Information

6.1 Pin Configuration

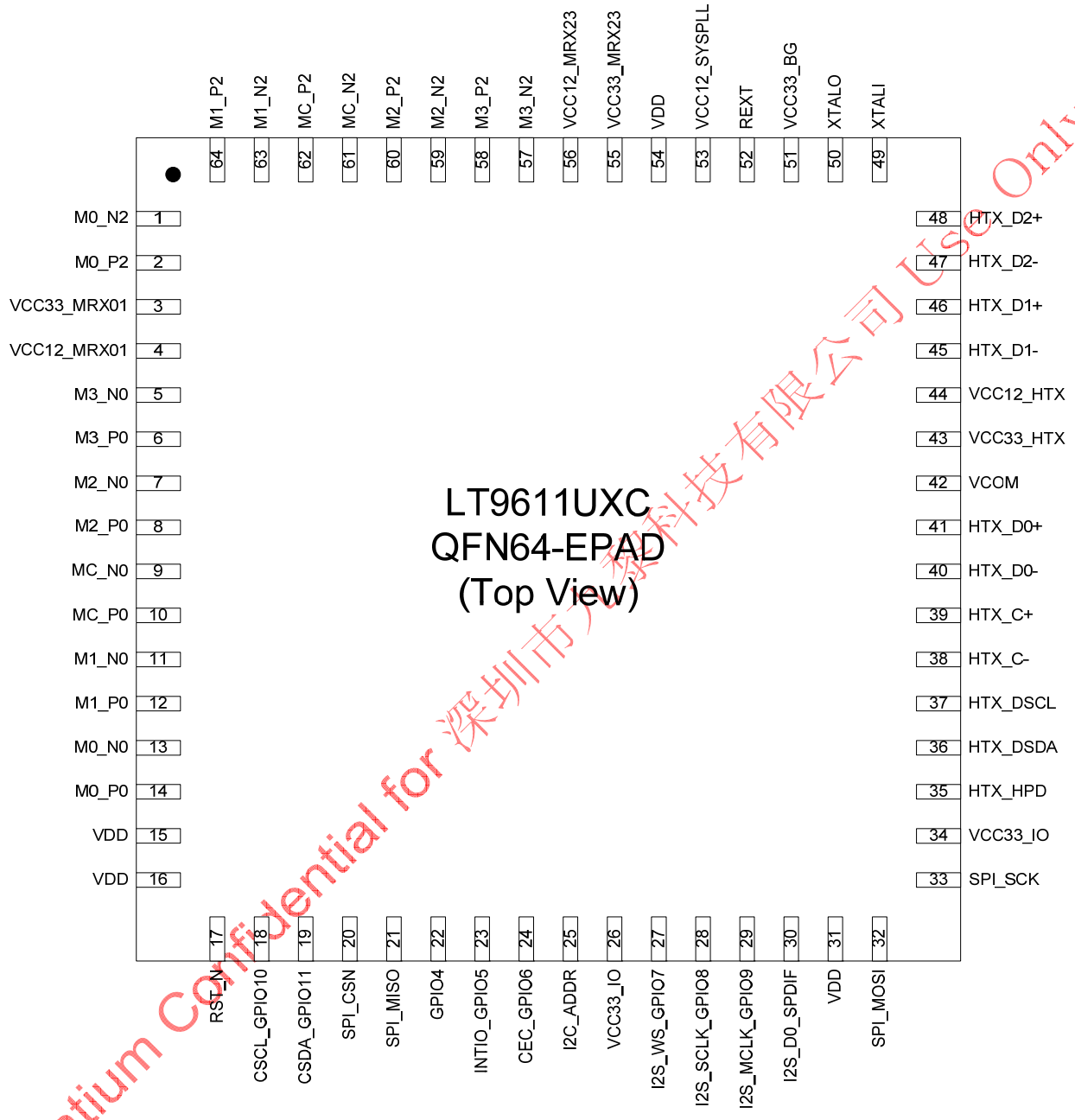


Figure 6.1.1 Pin Configuration

6.2 Pin Description

Table 6.2.1 Pin Description

Pin#	Pin Name	I/O Type	I/O Dir	Description
3	VCC33_MRX01	PG	I	Power rail of 3.3V MIPI RX port 0&1 power
4	VCC12_MRX01	PG	I	Power rail of 1.2V MIPI RX port 0&1 power
15,16,31,54	VDD	PG	I	Power rail of 1.2V digital core power
26,34	VCC33_IO	PG	I	Power rail of 3.3V I/O power
43	VCC33_HTX	PG	I	Power rail of 3.3V HDMI TX power
44	VCC12_HTX	PG	I	Power rail of 1.2V HDMI TX power
51	VCC33_BG	PG	I	Power rail of 3.3V BG power
53	VCC12_SYSPLL	PG	I	Power rail of 1.2V system PLL power
55	VCC33_MRX23	PG	I	Power rail of 3.3V MIPI RX port 2&3 power
56	VCC12_MRX23	PG	I	Power rail of 1.2V MIPI RX port 2&3 power
5	M3_N0	Analog	I	MIPI RX port 0 data lane 3 negative input
6	M3_P0	Analog	I	MIPI RX port 0 data lane 3 positive input
7	M2_N0	Analog	I	MIPI RX port 0 data lane 2 negative input
8	M2_P0	Analog	I	MIPI RX port 0 data lane 2 positive input
9	MC_N0	Analog	I	MIPI RX port 0 clock lane negative input
10	MC_P0	Analog	I	MIPI RX port 0 clock lane positive input
11	M1_N0	Analog	I	MIPI RX port 0 data lane 1 negative input
12	M1_P0	Analog	I	MIPI RX port 0 data lane 1 positive input
13	M0_N0	Analog	I	MIPI RX port 0 data lane 0 negative input
14	M0_P0	Analog	I	MIPI RX port 0 data lane 0 positive input
57	M3_N2	Analog	I	MIPI RX port 2 data lane 3 negative input
58	M3_P2	Analog	I	MIPI RX port 2 data lane 3 positive input
59	M2_N2	Analog	I	MIPI RX port 2 data lane 2 negative input
60	M2_P2	Analog	I	MIPI RX port 2 data lane 2 positive input
61	MC_N2	Analog	I	MIPI RX port 2 clock lane negative input
62	MC_P2	Analog	I	MIPI RX port 2 clock lane positive input
63	M1_N2	Analog	I	MIPI RX port 2 data lane 1 negative input
64	M1_P2	Analog	I	MIPI RX port 2 data lane 1 positive input
1	M0_N2	Analog	I	MIPI RX port 2 data lane 0 negative input
2	M0_P2	Analog	I	MIPI RX port 2 data lane 0 positive input
38	HTX_C-	Analog	O	HDMI TX clock channel negative output
39	HTX_C+	Analog	O	HDMI TX clock channel positive output
40	HTX_D0-	Analog	O	HDMI TX data channel 0 negative output
41	HTX_D0+	Analog	O	HDMI TX data channel 0 positive output
42	VCOM	Analog	I	HDMI TX AC-couple biasing common ground
45	HTX_D1-	Analog	O	HDMI TX data channel 1 negative output
46	HTX_D1+	Analog	O	HDMI TX data channel 1 positive output
47	HTX_D2-	Analog	O	HDMI TX data channel 2 negative output
48	HTX_D2+	Analog	O	HDMI TX data channel 2 positive output
17	RST_N	Schmitt	I	Active low reset input
18	CSCL_GPIO10	LVTTL	I/O	Configuration I2C SCL signal, also shared as general purpose I/O 10. It can be used as UART

Pin#	Pin Name	I/O Type	I/O Dir	Description
				RX for debug.
19	CSDA_GPIO11	LVTTL	I/O	Configuration I2C SDA signal, also shared as general purpose I/O 11
20	SPI_CSN	LVTTL	I/O	Chip selection for SPI interface
21	SPI_MISO	LVTTL	I/O	Serial data master-in-slave-out for SPI interface
22	GPIO4	LVTTL	I/O	General purpose I/O 4. It can be used as UART TX for debug.
23	INTIO_GPIO5	LVTTL	I/O	Interrupt I/O, also shared as general purpose I/O 5. It can be used as UART TX or RX for debug.
24	CEC_GPIO6	LVTTL	I/O	HDMI RX CEC signal, also shared as general purpose I/O 6. It can be used as UART TX for debug.
27	I2S_WS_GPIO7	LVTTL	I/O	Audio I2S word selection output, also shared as general purpose I/O 7. It can be used as UART TX for debug.
28	I2S_SCLK_GPIO8	LVTTL	I/O	Audio I2S serial clock output, also shared as general purpose I/O 8. It can be used as UART TX for debug.
29	I2S_MCLK_GPIO9	LVTTL	I/O	Audio I2S master clock output, also shared as general purpose I/O 9. It can be used as UART TX for debug.
30	I2S_D0_SPDIF	LVTTL	O	Audio I2S serial data 0 output, also shared as audio SPDIF output
32	SPI_MOSI	LVTTL	I/O	Serial data master-out-slave-in for SPI interface
33	SPI_SCK	LVTTL	I/O	Serial clock for SPI interface
35	HTX_HPD	Schmitt	I	HDMI TX HPD signal
36	HTX_DSDA	Schmitt，OD	I/O	HDMI TX DDC/SCDC channel SDA signal
37	HTX_DSCL	Schmitt，OD	I/O	HDMI TX DDC/SCDC channel SCL signal
49	XTALI	LVTTL	I	24MHz crystal oscillator input
50	XTALO	LVTTL	O	24MHz crystal oscillator output
25	I2C_ADDR	Analog	I	Configuration I2C device address selection
52	REXT	Analog	O	Analog current reference. A resistor of 7.68kΩ (1％) should tie this pin to ground.
65	EPAD	N/A	O	Exposed pad which should be connected to ground

7. Function Description

7.1 Function Block Diagram

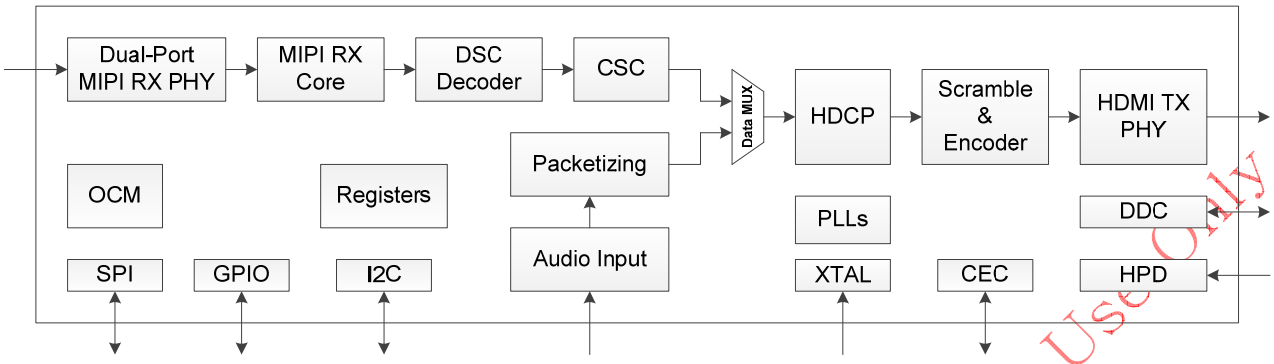


Figure 7.1.1 Function Block Diagram

8. Specification

8.1 Absolute Maximum Conditions

Table 8.1.1 Absolute Maximum Conditions

Symbol	Description	Min	Typ	Max	Unit
VCC33_MRX01, VCC33_IO, VCC33_HTX, VCC33_BG, VCC33_MRX23	3.3V Power Supply Voltage	-0.3		3.9	V
VCC12_MRX01, VDD, VCC12_HTX, VCC12_SYSPLL, VCC12_MRX23	1.2V Power Supply Voltage	-0.3		1.5	V
V_I	CMOS Terminal Input Voltage Range	-0.3		3.9	V
V_O	CMOS Terminal Output Voltage Range	-0.3		3.9	V
T_S	Storage Temperature	-60		140	℃
ESD	HBM Electrostatic Discharge Level		4000		V

Notes:
1. Permanent device damage may occur if absolute maximum conditions are exceeded.
2. Function operation should be restricted to the conditions described under Normal Operating Conditions.

8.2 Normal Operating Conditions

Table 8.2.1 Normal Operating Conditions

Symbol	Description	Min	Typ	Max	Unit
VCC33_MRX01, VCC33_IO, VCC33_HTX, VCC33_BG, VCC33_MRX23	3.3V Power Supply Voltage	2.97	3.3	3.63	V
VCC12_MRX01, VDD, VCC12_HTX, VCC12_SYSPLL, VCC12_MRX23	1.2V Power Supply Voltage	1.08	1.2	1.32	V
VCC_N	Power Supply Voltage Noise			50	mV
T_A	Operating Free-air Temperature	-40	27	85	℃

8.3 DC Characteristics

Table 8.3.1 DC Characteristics

MIPI HS Line RX DC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
$V_{CMRX(DC)}$	Common-mode voltage HS receive mode	70		330	mV
V_{IDTH}	Differential input high threshold			70	mV
V_{IDTL}	Differential input low threshold	-70			mV
V_{IHHS}	Single-ended input high voltage			460	mV
V_{ILHS}	Single-ended input low voltage	-40			mV
Z_{ID}	Differential input impedance	80	100	125	Ω
MIPI LP Line RX DC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
V_{IH}	Logic 1 input voltage ,data rate<1.5Gbps	880			mV
	Logic 1 input voltage ,data rate>1.5Gbps	740			mV
V_{IL}	Logic 0 input voltage, not in ULP State			550	mV
$V_{IL-ULPS}$	Logic 0 input voltage, ULP State			300	mV
V_{HYST}	Input hysteresis	25			mV
TMDS TX DC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
V_H	Single-ended high level output voltage	VCC33_HTX-400		VCC33_HTX+10	mV
V_L	Single-ended low level output voltage	VCC33_HTX-1000		VCC33_HTX-200	mV
V_{SWING}	Single-ended output swing voltage	200		600	mV
R_{TX_TERM}	Single-ended source termination resistance	37.5	50	75	Ω

8.4 AC Characteristics

Table 8.4.1 AC Characteristics

MIPI HS Line RX AC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
$\Delta V_{CMRX(HF)}$	Common-mode interference beyond 450MHz			200	mV
$\Delta V_{CMRX(LF)}$	Common-mode interference between 50MHz - 450MHz	-50		50	mV
C_{CM}	Common-mode termination			60	pF
MIPI LP Line RX AC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
e_{SPIKE}	Input pulse rejection			300	V.ps
T_{MIN-RX}	Minimum pulse width response	20			ns
V_{INT}	Peak interference amplitude			200	mV
f_{INT}	Interference frequency	450			MHz

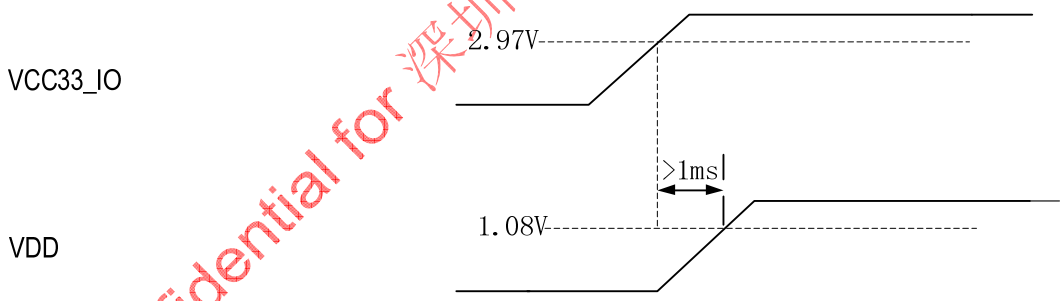
TMDS TX AC Specifications					
Symbol	Parameter	Min	Typ	Max	Unit
t_R/t_F	Rise time / fall time (20%-80%)	75			ps
$T_{TX\_INTRA\_SKEW}$	Intra-pair skew at source connector			$0.15T_{bit}$	ps
$T_{TX\_INTER\_SKEW}$	Inter-pair skew at source connector			$0.2T_{character}$	ns
V_{high}	Maximum differential output voltage			780	mV
V_{low}	Minimum differential output voltage	-780			mV
D_{CLOCK}	TMDS clock duty cycle	40	50	60	%
T_{TX_JITTER}	TMDS clock jitter			$0.3T_{bit}$	ps

8.5 Power Consumption

Table 8.5.1 Power Consumption

Condition	Supply Current(3.3V)	Supply Current(1.2V)	Unit
4k60Hz, 2-port RX, DSC disabled	TBD	TBD	mA
4k60Hz, 2-port RX, DSC enabled	TBD	TBD	mA
1080p, 1-port RX, DSC disabled	TBD	TBD	mA

8.6 Power-up and Reset Sequence



Note: 1.2V power should be set up at least 1ms later than 3.3V power, the reset signal should be released after 1.2V power is ready.

Figure 8.6.1 Power-up and Reset Sequence

9. Package Information

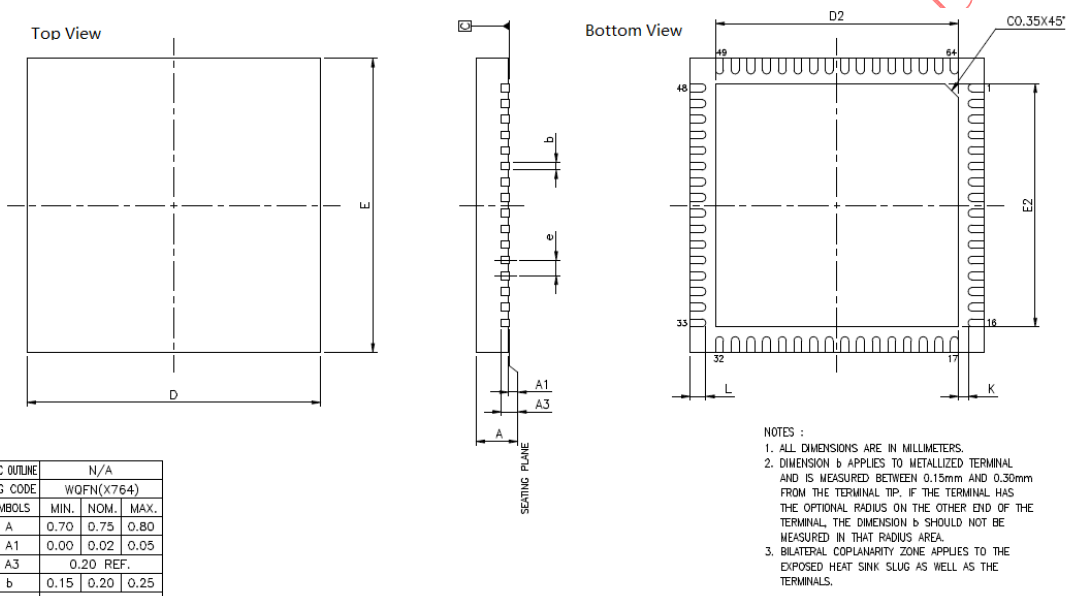
9.1 ePad Enhancement

The LT9611UXC is packaged in a 64-lead QFN package with ePad.

The ePad needs to be soldered to the PCB. The information in the following paragraphs is provided for applications which solder the ePad to the PCB.

The ePad must not be electrically connected to any other voltage level except ground. A clearance of at least 0.25mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid any electrical shorts.

9.2 Package Dimensions



JEDEC OUTLINE	N/A		
PKG CODE	WQFN(X764)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF.		
b	0.15	0.20	0.25
D	7.50 BSC		
E	7.50 BSC		
e	0.40 BSC		
L	0.30	0.40	0.50
K	0.20	—	—

	E2			D2			LEAD FINISH		JEDEC CODE
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
252X252 MIL	6.10	6.20	6.25	6.10	6.20	6.25	X	V	N/A

Figure 9.2.1 Package Dimensions

Visit our corporate web page at: www.lontiumsemi.com
Technical support: support@lontium.com
Sales: sales@lontium.com