



正基科技股份有限公司

SPECIFICATION

SPEC. NO. : _____ REV : 1.0

DATE : 06.06.2015

PRODUCT NAME : AP6212A

| | APPROVED | CHECKED | PREPARED | DCC ISSUE |
|------|----------|---------|----------|-----------|
| NAME | | | | |

AMPAK

AP6212A

WiFi+Bluetooth 4.1+FM RX
SIP Module Spec Sheet

Revision History

| Date | Revision Content | Revised By | Version |
|------------|-------------------|------------|---------|
| 2015/06/06 | - Initial Release | Brian | 1.0 |
| | | | |
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1. Introduction

AMPAK Technology would like to announce a low-cost and low-power consumption module which has all of the WiFi, Bluetooth and FM functionalities. The highly integrated module makes the possibilities of web browsing, VoIP, Bluetooth headsets, FM radio functional applications and other applications. With seamless roaming capabilities and advanced security, also could interact with different vendors' 802.11b/g/n Access Points in the wireless LAN.

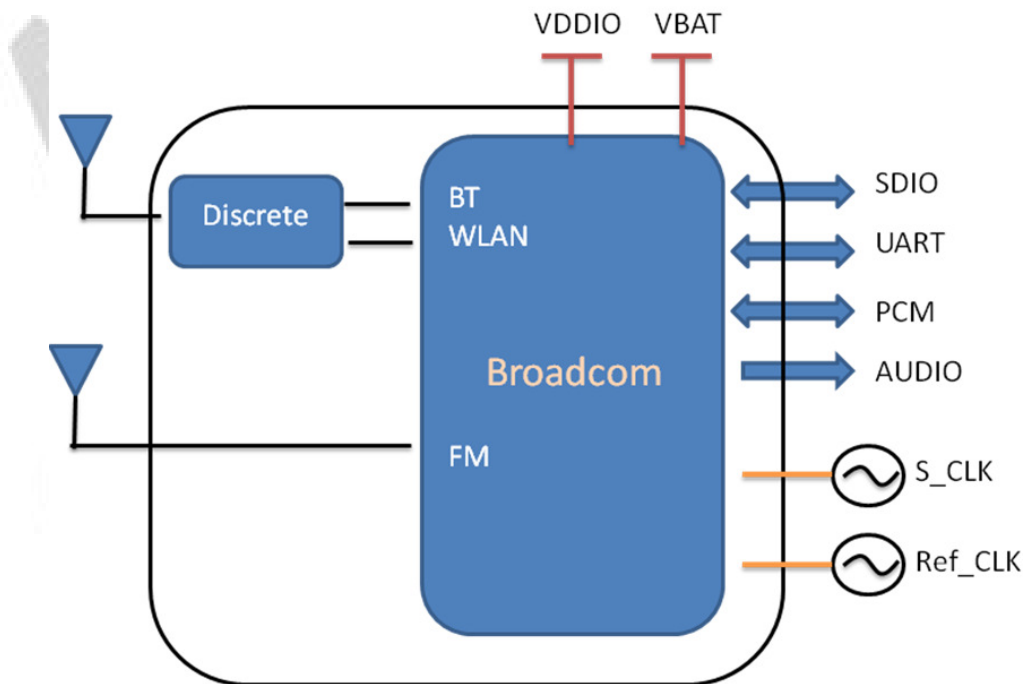
The wireless module complies with IEEE 802.11 b/g/n standard and it can achieve up to a speed of 72.2Mbps with single stream in 802.11n draft, 54Mbps as specified in IEEE 802.11g, or 11Mbps for IEEE 802.11b to connect to the wireless LAN. The integrated module provides SDIO interface for WiFi, UART / I2S / PCM interface for Bluetooth and UART / I2S / PCM interface for FM.

This compact module is a total solution for a combination of WiFi + BT + FM technologies. The module is specifically developed for Smart phones and Portable devices.

2. Features

- 802.11b/g/n single-band radio
- Bluetooth V4.0(HS) with integrated Class 1.5 PA and Low Energy (BLE) support
- Concurrent Bluetooth, FM (RX) RDS/RBDS, and WLAN operation
- Simultaneous BT/WLAN receive with single antenna
- WLAN host interface options:
 - SDIO v2.0 — up to 50 MHz clock rate
- BT host digital interface:
 - UART (up to 4 Mbps)
- FM multiple audio routing options: I2S, PCM, eSCO, A2DP
- IEEE Co-existence technologies are integrated die solution
- ECI — enhanced coexistence support, ability to coordinate BT SCO transmissions around WLAN receives

A simplified block diagram of the module is depicted in the figure below.



3. Deliverables

3.1 Deliverables

The following products and software will be part of the product.

- Module with packaging
- Evaluation Kits
- Software utility for integration, performance test.
- Product Datasheet.
- Agency certified pre-tested report with the adapter board.

3.2 Regulatory certifications

The product delivery is a pre-tested module, without the module level certification. For module approval, the platform's antennas are required for the certification.

4. General Specification

4.1 General Specification

| | |
|-----------------------|--|
| Model Name | AP6212A |
| Product Description | Support WiFi/Bluetooth/FM functionalities |
| Dimension | L x W x H: 12 x 12 x 1.5 (typical) mm |
| WiFi Interface | SDIOV2.0 |
| BT Interface | UART / PCM |
| FM Interface | UART / PCM / Audio |
| Operating temperature | -30°C to 85°C |
| Storage temperature | -40°C to 85°C |
| Humidity | Operating Humidity 10% to 95% Non-Condensing |

4.2 Voltages

4.2.1 Absolute Maximum Ratings

| Symbol | Description | Min. | Max. | Unit |
|-----------|-------------------------------------|------|------|------|
| VBAT | Input supply Voltage | -0.5 | 5.5 | V |
| WL_VIO_SD | Digital/Bluetooth/SDIO/ I/O Voltage | -0.5 | 3.6 | V |

4.2.2 Recommended Operating Rating

The module requires two power supplies: VBAT and VDDIO.

| | Min. | Typ. | Max. | Unit |
|-----------------------|------|------|------|-------|
| Operating Temperature | -30 | 25 | 85 | deg.C |
| VBAT | 3.0 | 3.6 | 4.8 | V |
| VDDIO | 1.7 | 3.3 | 3.6 | V |

5. WiFi RF Specification

5.1 2.4GHz RF Specification

Conditions : VBAT=3.6V ; VDDIO=3.3V ; Temp:25°C

| Feature | Description |
|--|--|
| WLAN Standard | IEEE 802.11b/g/n, WiFi compliant |
| Frequency Range | 2.400 GHz ~ 2.497 GHz (2.4 GHz ISM Band) |
| Number of Channels | 2.4GHz : Ch1 ~ Ch14 |
| Modulation | 802.11b : DQPSK, DBPSK, CCK 802.11 g/n : OFDM /64-QAM, 16-QAM, QPSK, BPSK |
| Output Power | 802.11b /11Mbps : 16 dBm ± 1.5 dB @ EVM ≤ -9dB |
| | 802.11g /54Mbps : 15 dBm ± 1.5 dB @ EVM ≤ -25dB |
| | 802.11n /65Mbps : 14 dBm ± 1.5 dB @ EVM ≤ -28dB |
| Receive Sensitivity (11n,20MHz) @10% PER | - MCS=0 PER @ -85 dBm, typical |
| | - MCS=1 PER @ -84 dBm, typical |
| | - MCS=2 PER @ -82 dBm, typical |
| | - MCS=3 PER @ -80 dBm, typical |
| | - MCS=4 PER @ -77 dBm, typical |
| | - MCS=5 PER @ -73 dBm, typical |
| | - MCS=6 PER @ -71 dBm, typical |
| | - MCS=7 PER @ -68 dBm, typical |
| Receive Sensitivity (11g) @10% PER | - 6Mbps PER @ -86 dBm, typical |
| | - 9Mbps PER @ -85 dBm, typical |
| | - 12Mbps PER @ -85 dBm, typical |
| | - 18Mbps PER @ -83 dBm, typical |
| | - 24Mbps PER @ -81 dBm, typical |
| | - 36Mbps PER @ -78 dBm, typical |
| | - 48Mbps PER @ -73 dBm, typical |
| | - 54Mbps PER @ -71 dBm, typical |
| Receive Sensitivity (11b) @8% PER | - 1Mbps PER @ -90 dBm, typical |
| | - 2Mbps PER @ -88 dBm, typical |
| | - 5.5Mbps PER @ -87 dBm, typical |
| | - 11Mbps PER @ -84 dBm, typical |
| Data Rate | 802.11b : 1, 2, 5.5, 11Mbps |
| | 802.11g : 6, 9, 12, 18, 24, 36, 48, 54Mbps |

| | |
|--------------------------------------|--|
| Data Rate (20MHz ,Long GI,800ns) | 802.11n: 6.5, 13, 19.5, 26, 39, 52, 58.5, 65Mbps |
| Data Rate (20MHz ,short GI,400ns) | 802.11n : 7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65,72.2Mbps |
| Maximum Input Level | 802.11b : -10 dBm |
| | 802.11g/n : -20 dBm |
| Antenna Reference | Small antennas with 0~2 dBi peak gain |

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6. Bluetooth Specification

6.1 Bluetooth Specification

Conditions : VBAT=3.6V ; VDDIO=3.3V ; Temp:25 °C

| Feature | Description | | |
|---|---------------------------------------|-----------------|-------------|
| General Specification | | | |
| Bluetooth Standard | Bluetooth V4.0 of 1, 2 and 3 Mbps. | | |
| Host Interface | UART | | |
| Antenna Reference | Small antennas with 0~2 dBi peak gain | | |
| Frequency Band | 2402MHz ~ 2480MHz | | |
| Number of Channels | 79 channels | | |
| Modulation | FHSS, GFSK, DPSK, DQPSK | | |
| RF Specification | | | |
| | Min. | Typical. | Max. |
| Output Power (Class 1.5) | | 9 dBm | |
| Sensitivity @ BER=0.1% for GFSK (1Mbps) | | -86 dBm | |
| Sensitivity @ BER=0.01% for $\pi/4$ -DQPSK (2Mbps) | | -86 dBm | |
| Sensitivity @ BER=0.01% for 8DPSK (3Mbps) | | -80 dBm | |
| Maximum Input Level | GFSK (1Mbps):-20dBm | | |
| | $\pi/4$ -DQPSK (2Mbps) :-20dBm | | |
| | 8DPSK (3Mbps) :-20dBm | | |

7. FM Specification

7.1 FM Specification (TBD)

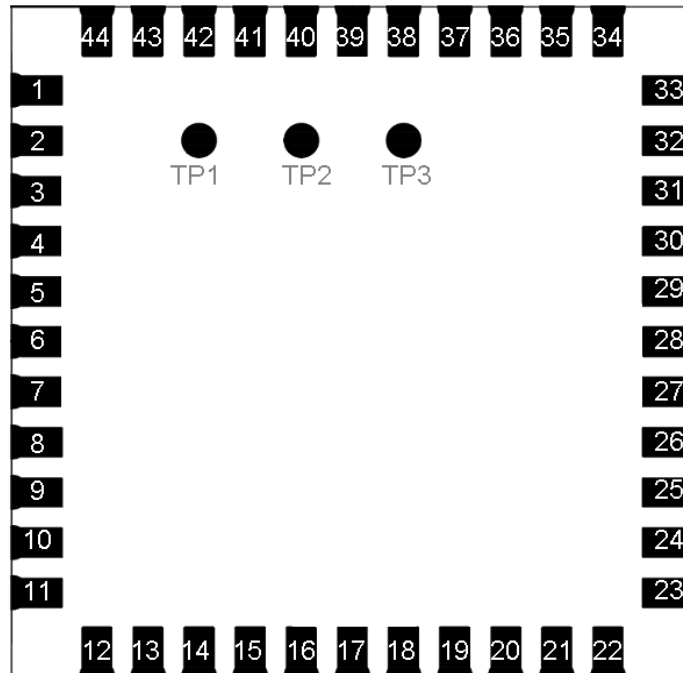
Conditions : VBAT=3.6V ; VDDIO=3.3V ; Temp:25 °C

| Feature | Description | | | | | |
|--|---|---------------|-----|-----|------|----|
| General Specification | | | | | | |
| Frequency Band | 76MHz-108MHz | | | | | |
| Host Interface | HCI UART, I2S/PCM | | | | | |
| Channel step | 50 KHz | | | | | |
| Analog Audio output load | $R_L > 30K\Omega$, $C_L > 20pF$ | | | | | |
| Characteristics | Condition | MIN | TYP | MAX | UNIT | |
| Transmitter (FM Tx load = 120nH, Q>30) | Output Power Level | | | | dBuV | |
| | Audio harmonic distortion (fmod=1KHz, $\Delta f=75KHz$, Pilot $\Delta f=6.75KHz$) | | | | % | |
| | Audio SNR ($\Delta f=22.5KHz$, I2S audio in SNR \geq 57dB) | MONO | | | | dB |
| | | Stereo | | | | |
| Receiver (FM Tx Antenna = 120nH, Q>30) | RDS Sensitivity | | | | dBm | |
| | Audio harmonic distortion (Vin=1mV, $\Delta f=75KHz$) | fmod= 1KHz | | | | % |
| | | fmod= 3KHz | | | | |
| | Maximum SNR (fmod=1KHz, $\Delta f=22.5$ KHz, BW=300Hz to 15KHz) | MONO | | | | dB |
| | | Stereo | | | | |
| RF input power level | | | | | dBuV | |

8. Pin Assignments

8.1 Pin Outline

< TOP VIEW >



8.2 Pin Definition

| NO | Name | Type | Description |
|----|--------------|------|---|
| 1 | GND | — | Ground connections |
| 2 | WL_BT_ANT | I/O | RF I/O port |
| 3 | GND | — | Ground connections |
| 4 | FM_RX | I | FM radio RF input antenna port |
| 5 | NC | — | Floating (Don't connected to ground) |
| 6 | BT_WAKE | I | HOST wake-up Bluetooth device |
| 7 | BT_HOST_WAKE | O | Bluetooth device to wake-up HOST |
| 8 | CLK_REQ | O | The CLK_REQ polarity is active-high. Add an external 100KR pull down resistor to ensure the signal is deasserted when the BCM43438 powers up or resets when VDDIO is present. |
| 9 | VBAT | P | Main power voltage source input |
| 10 | XTAL_IN | I | Crystal input |
| 11 | XTAL_OUT | O | Crystal output |

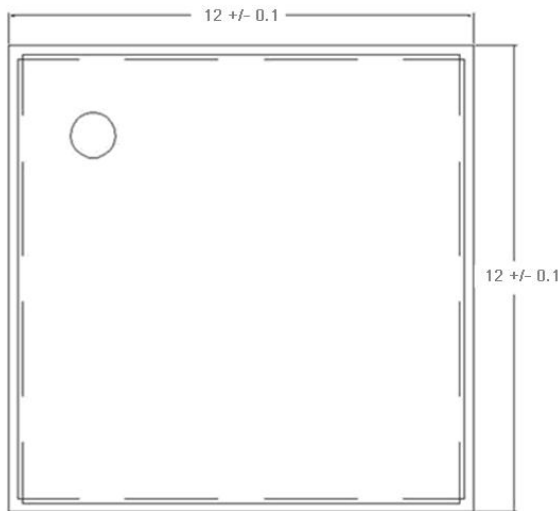
| | | | |
|----|---------------|-----|--|
| 12 | WL_REG_ON | I | Internal regulators power enable/disable |
| 13 | WL_HOST_WAKE | O | WLAN to wake-up HOST |
| 14 | SDIO_DATA_2 | I/O | SDIO data line 2 |
| 15 | SDIO_DATA_3 | I/O | SDIO data line 3 |
| 16 | SDIO_DATA_CMD | I/O | SDIO command line |
| 17 | SDIO_DATA_CLK | I/O | SDIO clock line |
| 18 | SDIO_DATA_0 | I/O | SDIO data line 0 |
| 19 | SDIO_DATA_1 | I/O | SDIO data line 1 |
| 20 | GND | — | Ground connections |
| 21 | VIN_LDO_OUT | P | Internal Buck voltage generation pin |
| 22 | VDDIO | P | I/O Voltage supply input |
| 23 | VIN_LDO | P | Internal Buck voltage generation pin |
| 24 | LPO | I | External Low Power Clock input (32.768KHz) |
| 25 | PCM_OUT | O | PCM Data output |
| 26 | PCM_CLK | I/O | PCM clock |
| 27 | PCM_IN | I | PCM data input |
| 28 | PCM_SYNC | I/O | PCM sync signal |
| 29 | NC | — | Floating (Don't connected to ground) |
| 30 | NC | — | Floating (Don't connected to ground) |
| 31 | GND | — | Ground connections |
| 32 | NC | — | Floating (Don't connected to ground) |
| 33 | GND | — | Ground connections |
| 34 | BT_RST_N | I | Low asserting reset for Bluetooth core |
| 35 | NC | — | Floating (Don't connected to ground) |
| 36 | GND | — | Ground connections |
| 37 | GPIO4 | I/O | WiFi Co-existence pin with LTE |
| 38 | GPIO3 | I/O | WiFi Co-existence pin with LTE |
| 39 | GPIO2 | I/O | WiFi Co-existence pin with LTE |
| 40 | GPIO1 | I/O | WiFi Co-existence pin with LTE |
| 41 | UART_RTS_N | O | Bluetooth/FM UART interface |
| 42 | UART_TXD | O | Bluetooth/FM UART interface |
| 43 | UART_RXD | I | Bluetooth/FM UART interface |
| 44 | UART_CTS_N | I | Bluetooth/FM UART interface |
| 45 | TP1 | O | FM Analog AUDIO left output |
| 46 | TP2 | O | FM Analog AUDIO right output |
| 47 | TP3 (NC) | — | Floating (Don't connected to ground) |

9. Dimensions

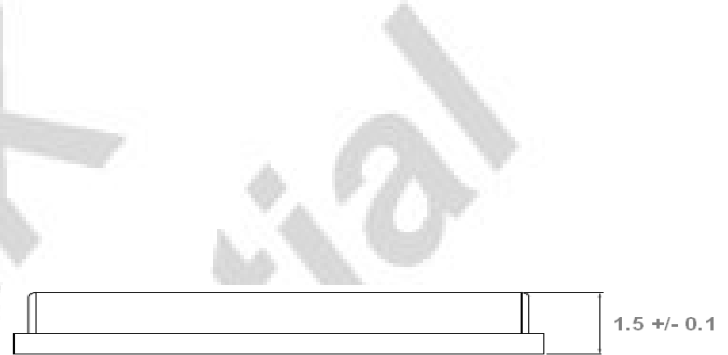
9.1 Physical Dimensions

(Unit: mm)

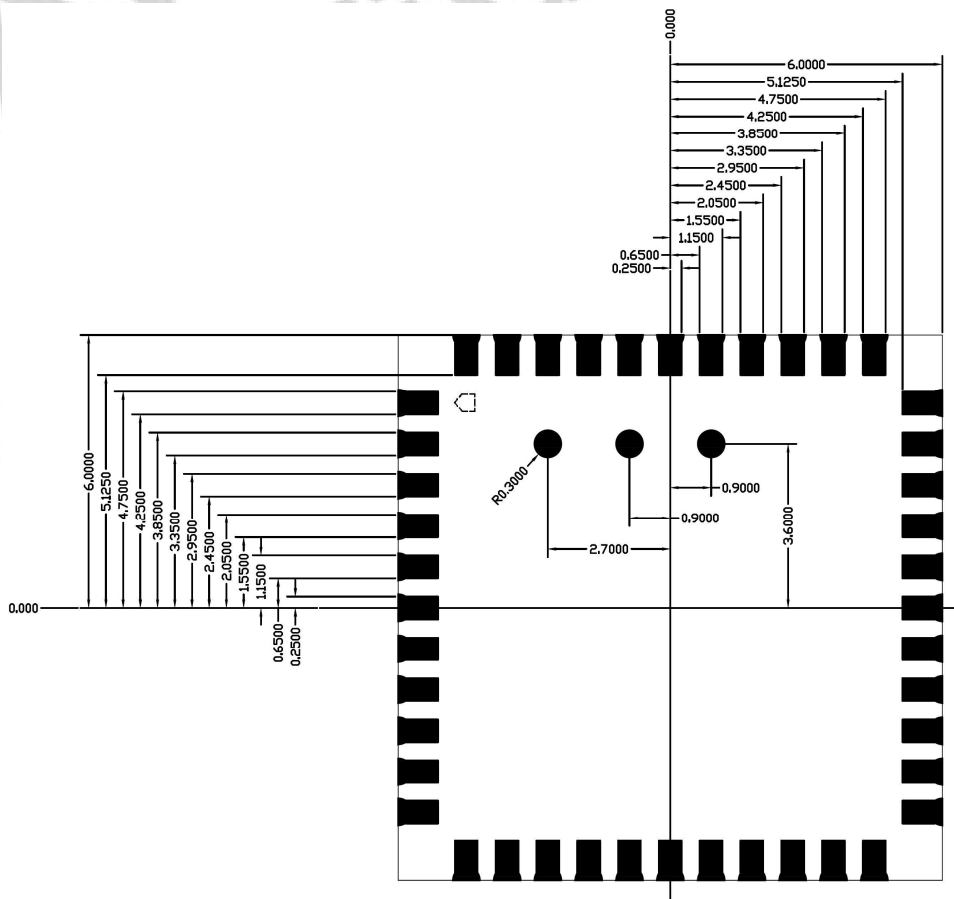
< TOP VIEW >



< Side View >



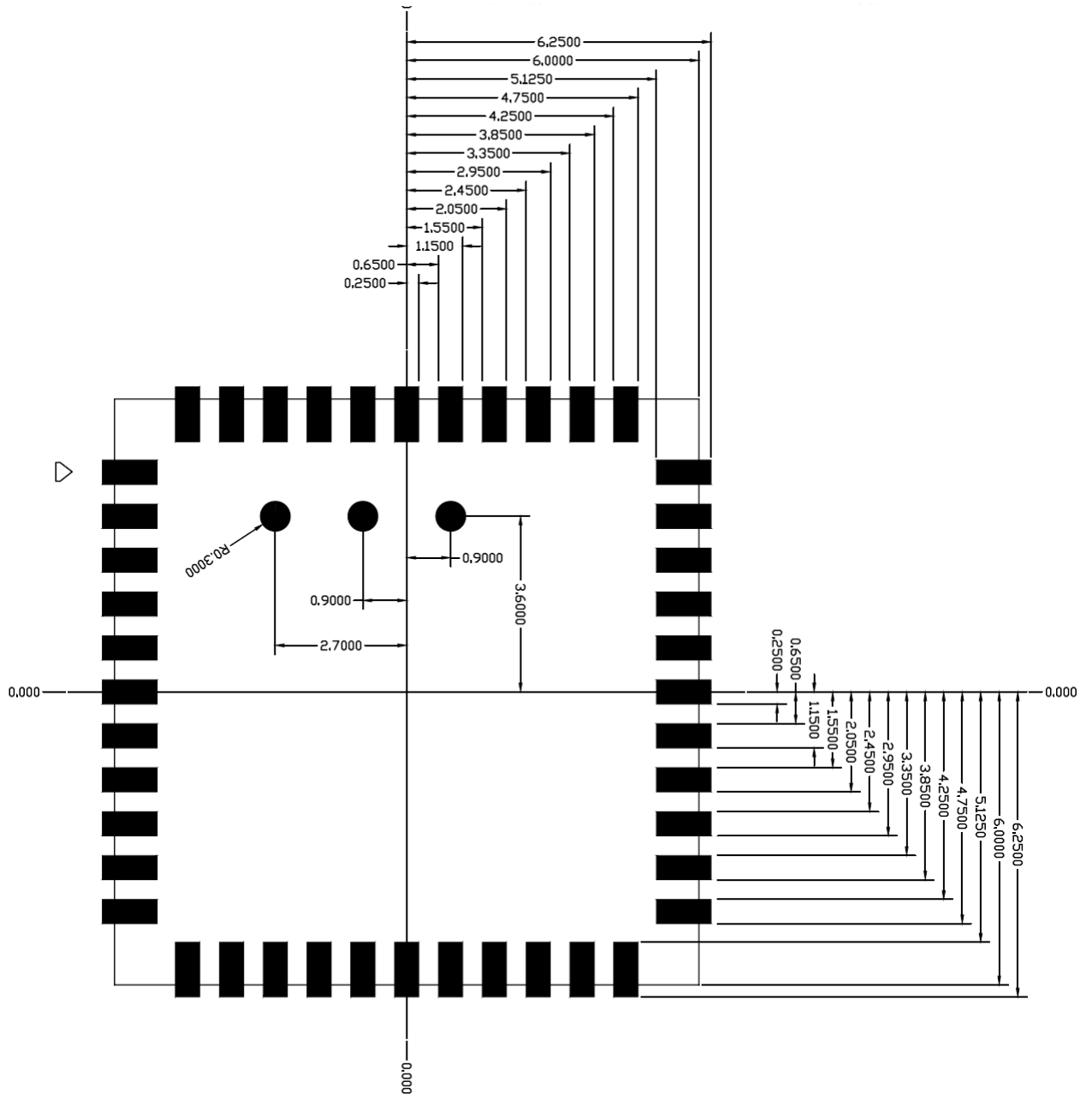
< TOP VIEW >



9.2 Layout Recommendation

(Unit: mm)

< TOP VIEW >



10. External clock reference

External LPO signal characteristics

| Parameter | Specification | Units |
|--|--------------------------------------|---------|
| Nominal input frequency | 32.768 | kHz |
| Frequency accuracy | ±30 | ppm |
| Duty cycle | 30 - 70 | % |
| Input signal amplitude | 400 to 1800 | mV, p-p |
| Signal type | Square-wave | - |
| Input impedance | >100k <5 | Ω pF |
| Clock jitter (integrated over 300Hz – 15KHz) | <1 | Hz |
| Output high voltage | 0.7V _{io} - V _{io} | V |

External Ref_CLK signal characteristics

| No. | Item | Symb. | Electrical Specification | | | | Remark |
|-----|------------------------------|------------------|--------------------------|------|------|-------|-----------------------|
| | | | Min. | Type | Max. | Units | |
| 1 | Nominal Frequency | F0 | 26.00000 | | | MHz | |
| 2 | Mode of Vibration | | Fundamental | | | | |
| 3 | Frequency Tolerance | ΔF/F0 | -10 | - | 10 | ppm | at 25°C±3°C |
| 4 | Operating Temperature Range | T _{OPR} | -30 | - | 85 | °C | |
| 5 | Frequency Stability | TC | -10 | - | 10 | ppm | |
| 6 | Storage Temperature | T _{STG} | -55 | - | 125 | °C | |
| 7 | Load capacitance | CL | - | 16 | | pF | |
| 8 | Equivalent Series Resistance | ESR | - | - | 50 | Ω | |
| 9 | Drive Level | DL | - | 100 | 200 | μW | |
| 10 | Insulation Resistance | IR | 500 | - | - | MΩ | At 100V _{DC} |
| 11 | Shunt Capacitance | C0 | - | - | 3 | pF | |
| 12 | Aging Per Year | Fa | -2 | - | 2 | ppm | First Year |

10.1 SDIO Pin Description

The module supports SDIO version 2.0 for 4-bit modes (100 Mbps), and high speed 4-bit (50 MHz clocks – 200 Mbps). It has the ability to stop the SDIO clock and map the interrupt signal into a GPIO pin. This 'out-of-band' interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force the control of the gated clocks from within the WLAN chip is also provided.

- ❖ Function 0 Standard SDIO function (Max BlockSize / ByteCount = 32B)
- ❖ Function 1 Backplane Function to access the internal System On Chip (SOC) address space (Max BlockSize / ByteCount = 64B)
- ❖ Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max BlockSize/ByteCount=512B)

SDIO Pin Description

| SD 4-Bit Mode | |
|---------------|--------------------------|
| DATA0 | Data Line 0 |
| DATA1 | Data Line 1 or Interrupt |
| DATA2 | Data Line 2 or Read Wait |
| DATA3 | Data Line 3 |
| CLK | Clock |
| CMD | Command Line |

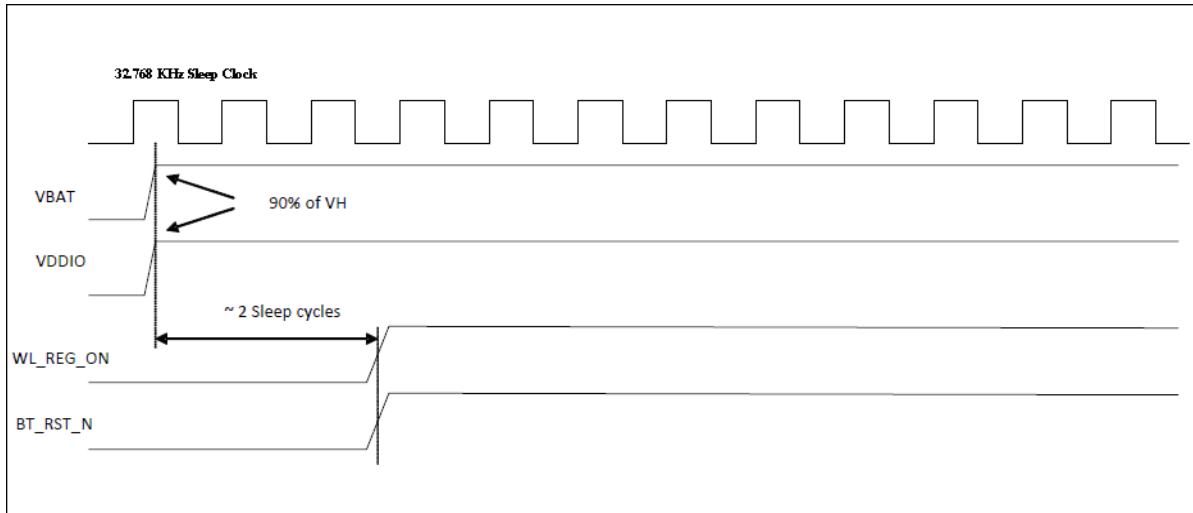
11. Host Interface Timing Diagram

11.1 Power-up Sequence Timing Diagram

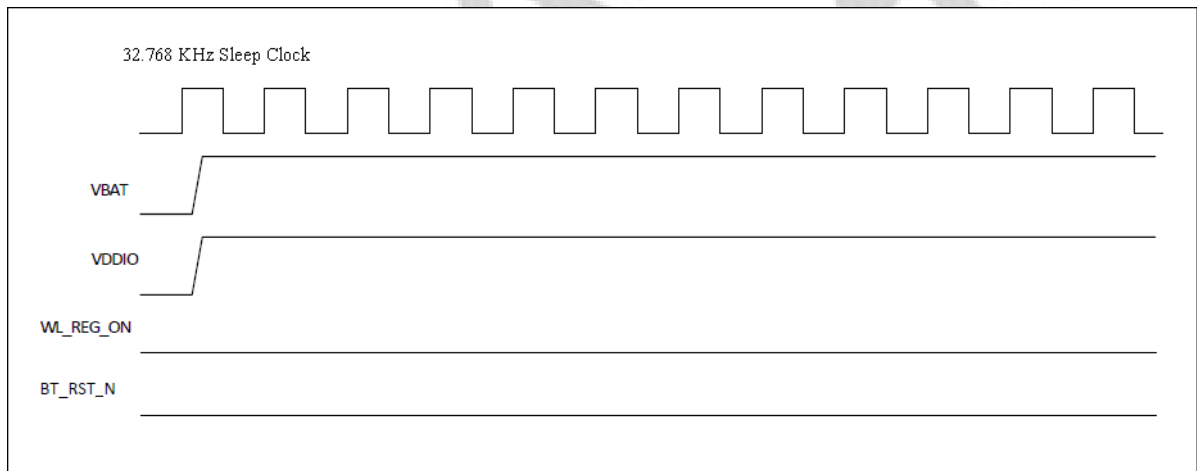
The module has signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN and internal regulator blocks. These signals are described below.

Additionally, diagrams are provided to indicate proper sequencing of the signals for various operating states. The timing value indicated are minimum required values: longer delays are also acceptable.

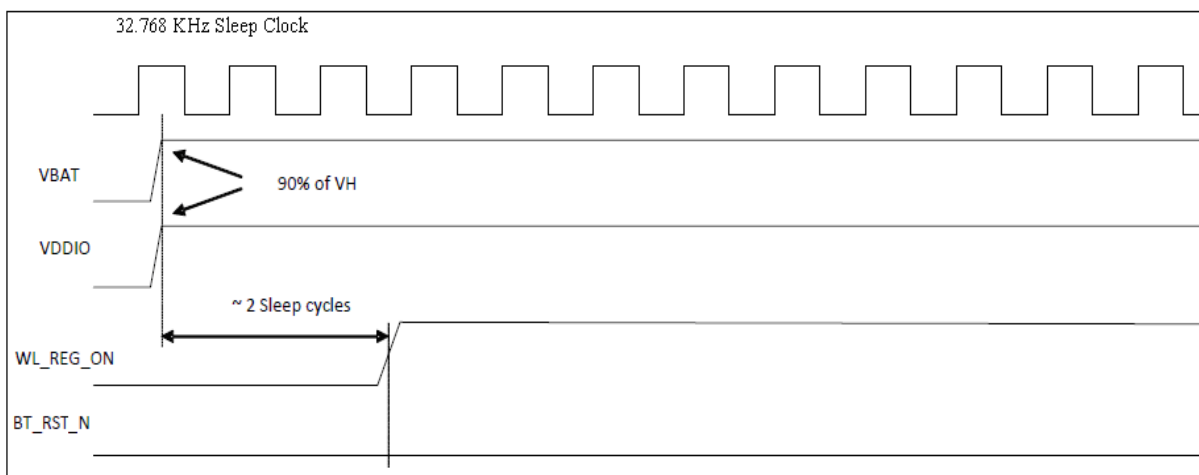
- ※ WL_REG_ON: Used by the PMU to power up the WLAN section. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset.
- ※ BT_RST_N: Low asserting reset for Bluetooth and FM only. This pin has no effect on WLAN and does not control any PMU functions. This pin must be driven high or low (not left floating).



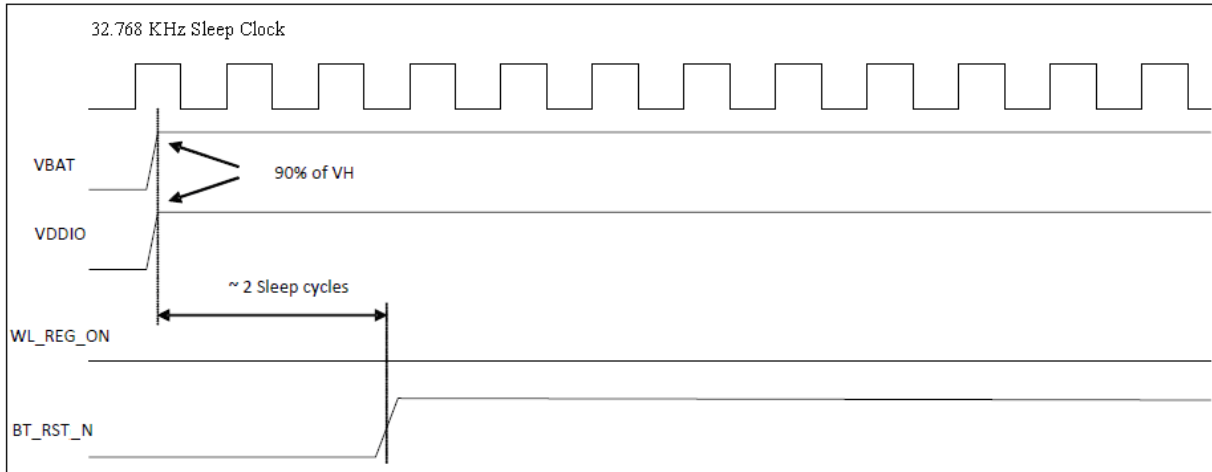
WLAN=ON, Bluetooth=ON



WLAN=OFF, Bluetooth=OFF

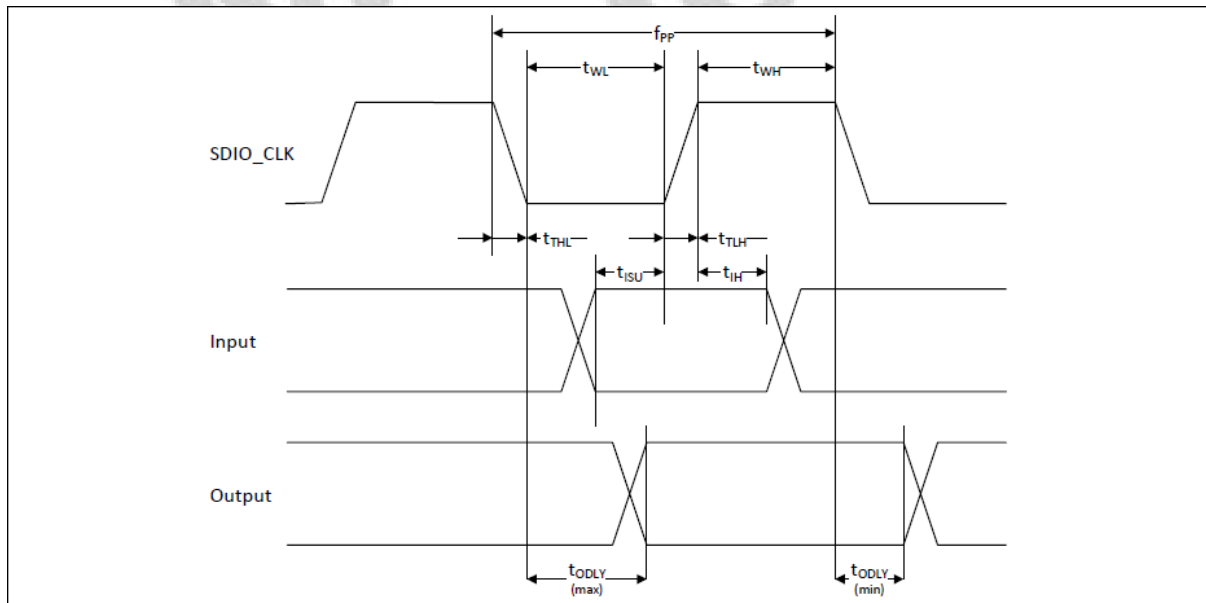


WLAN=ON, Bluetooth=OFF



WLAN=OFF, Bluetooth=ON

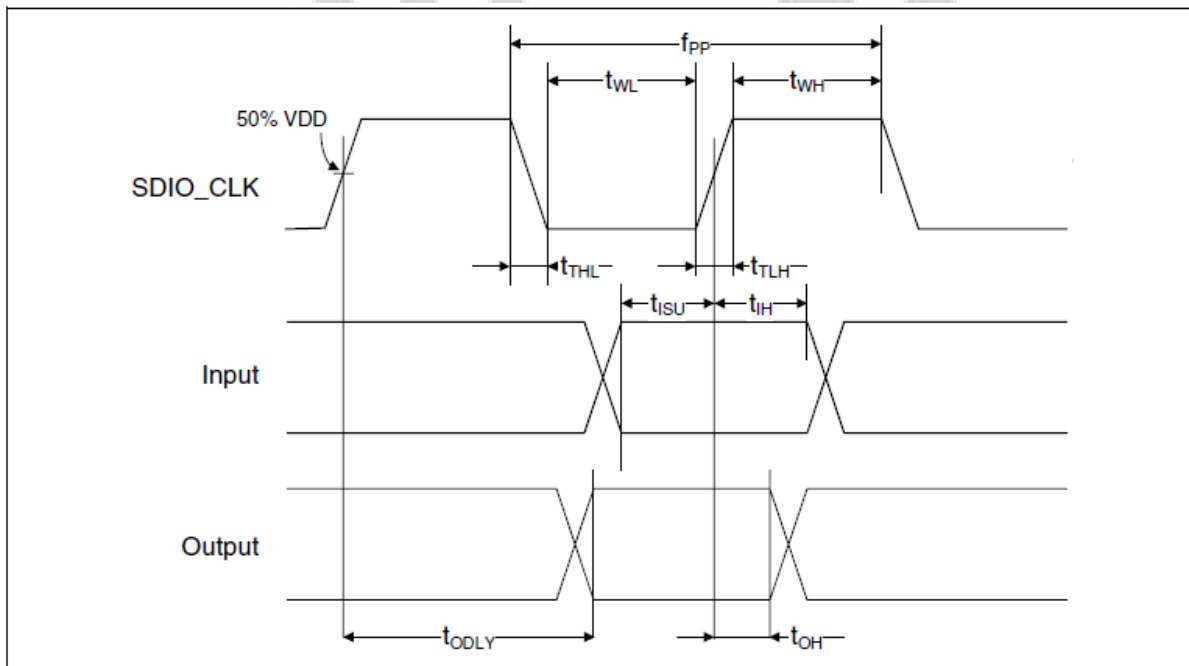
11.2 SDIO Default Mode Timing Diagram



| Parameter | Symbol | Minimum | Typical | Maximum | Unit |
|--|--------|---------|---------|---------|------|
| SDIO CLK (All values are referred to minimum VIH and maximum VIL^b) | | | | | |
| Frequency-Data Transfer mode | fPP | 0 | - | 25 | MHz |
| Frequency-Identification mode | fOD | 0 | - | 400 | kHz |
| Clock low time | tWL | 10 | - | - | ns |
| Clock high time | tWH | 10 | - | - | ns |
| Clock rise time | tTLH | - | - | 10 | ns |
| Clock low time | tTHL | - | - | 10 | ns |
| Inputs: CMD, DAT (referenced to CLK) | | | | | |
| Input setup time | tISU | 5 | - | - | ns |
| Input hold time | tIH | 5 | - | - | ns |
| Outputs: CMD, DAT (referenced to CLK) | | | | | |
| Output delay time - Data Transfer mode | tODLY | 0 | - | 14 | ns |
| Output delay time - Identification mode | tODLY | 0 | - | 50 | ns |

a. Timing is based on CL ≤ 40pF load on CMD and Data.
 b. min(Vih) = 0.7 x VDDIO and max(Vil) = 0.2 x VDDIO.

11.3 SDIO High Speed Mode Timing Diagram



| Parameter | Symbol | Minimum | Typical | Maximum | Unit |
|--|--------|---------|---------|---------|------|
| SDIO CLK (All values are referred to minimum VIH and maximum VIL^b) | | | | | |
| Frequency-Data Transfer mode | fPP | 0 | - | 50 | MHz |
| Frequency-Identification mode | fOD | 0 | - | 400 | kHz |
| Clock low time | tWL | 7 | - | - | ns |
| Clock high time | tWH | 7 | - | - | ns |
| Clock rise time | tTLH | - | - | 3 | ns |
| Clock low time | tTHL | - | - | 3 | ns |
| Inputs: CMD, DAT (referenced to CLK) | | | | | |
| Input setup time | tISU | 6 | - | - | ns |
| Input hold time | tIH | 2 | - | - | ns |
| Outputs: CMD, DAT (referenced to CLK) | | | | | |
| Output delay time - Data Transfer mode | tODLY | - | - | 14 | ns |
| Output hold time | tOH | 2.5 | - | - | ns |
| Total system capacitance (each line) | CL | - | - | 40 | pF |

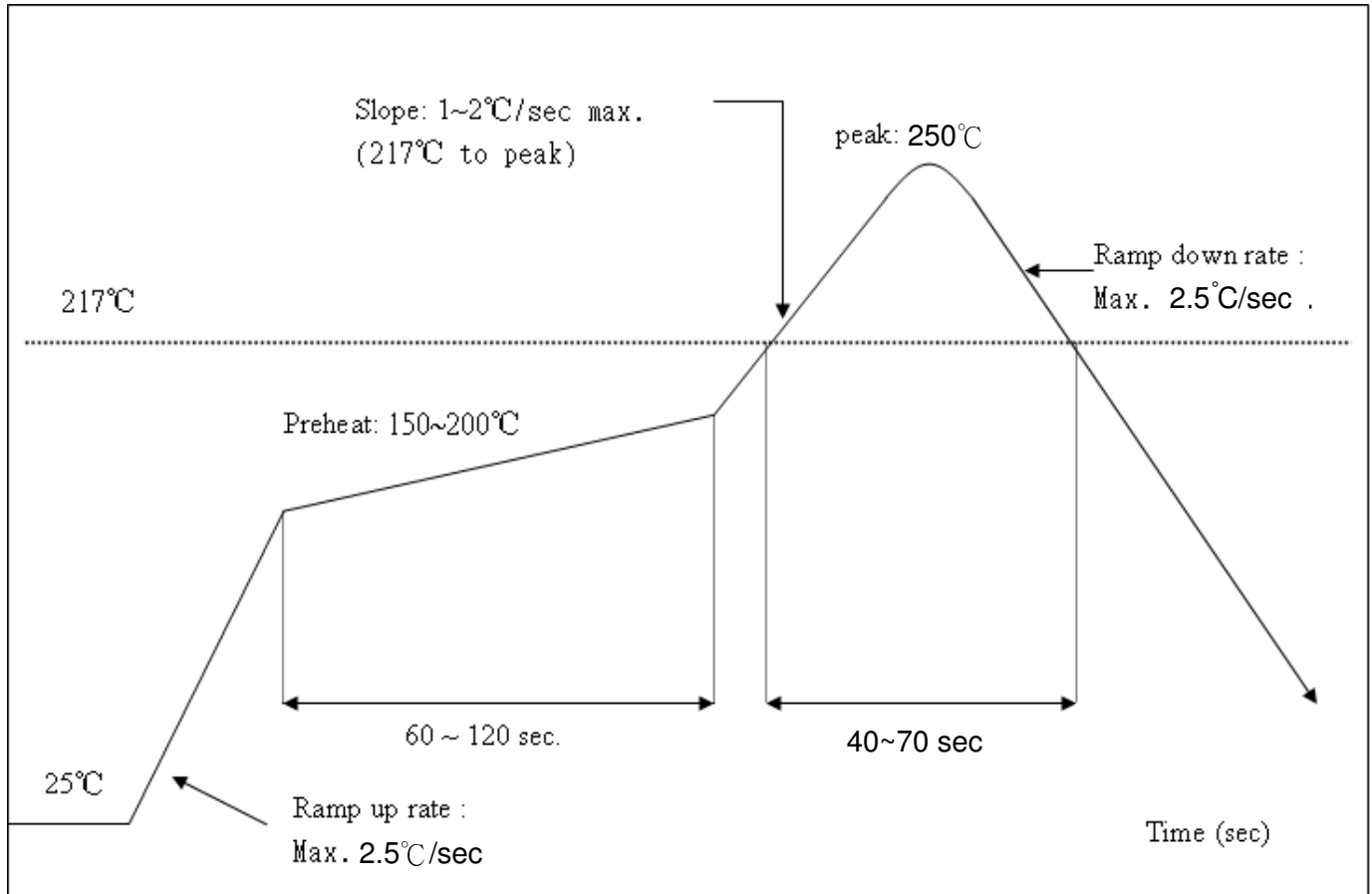
a. Timing is based on CL ≤ 40pF load on CMD and Data.
 b. min(Vih) = 0.7 x VDDIO and max(Vil) = 0.2 x VDDIO.

12. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <math>< 250^{\circ}\text{C}</math>

Number of Times : ≤ 2 times

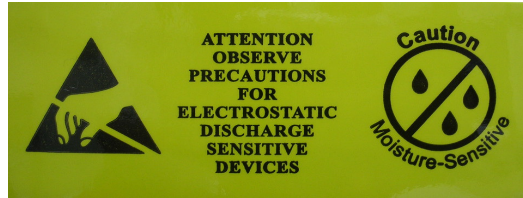


GO!


13. Package Information

13.1 Label



Label A → Anti-static and humidity notice







Label B → MSL caution / Storage Condition

| | | |
|---|--|-------------------------------|
|  | Caution This bag contains MOISTURE-SENSITIVE DEVICES | LEVEL <input type="text"/> |
| | If blank, see adjacent bar code label | |
| <ol style="list-style-type: none"> Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH) Peak package body temperature: _____ °C <small>If blank, see adjacent bar code label</small> After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be <ol style="list-style-type: none"> Mounted within: _____ hours of factory conditions <small>If blank, see adjacent bar code label</small> ≤30°C/60% RH, or Stored per J-STD-033 Devices require bake, before mounting, if: <ol style="list-style-type: none"> Humidity Indicator Card reads >10% for level 2a - 5a devices or >60% for level 2 devices when read at 23 ± 5°C 3a or 3b are not met If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure | | |
| Bag Seal Date: _____ <small>If blank, see adjacent bar code label</small> | | |
| Note: Level and body temperature defined by IPC/JEDEC J-STD-020 | | |

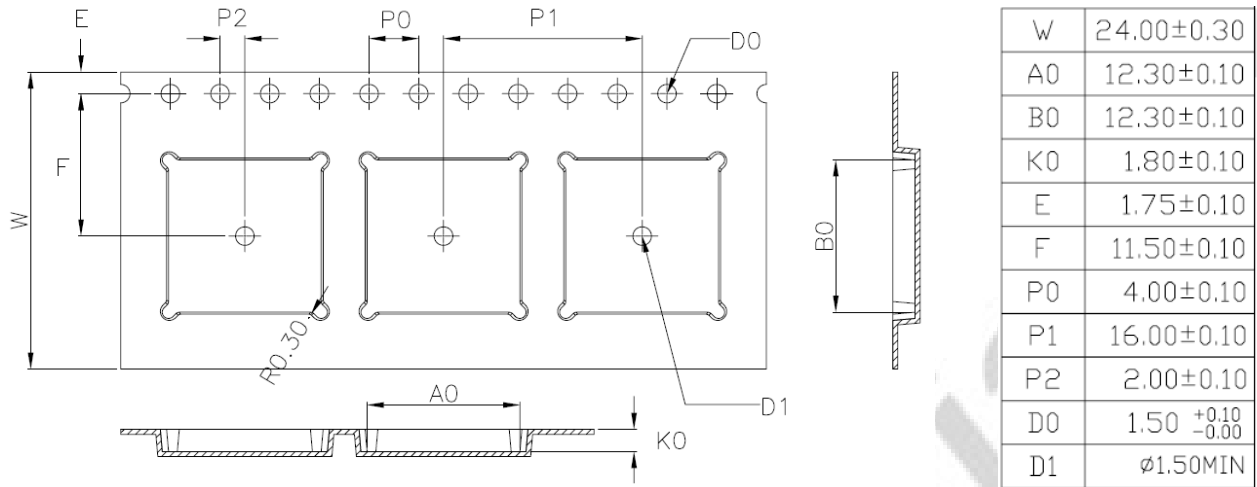
Label C → Inner box label .

| | |
|--------------------|--|
| PKG S/N : |  9PKG12013100001 |
| Model: |  XXXXXXXXXXXX |
| P/N : |  99P-W01-0048R |
| Qty : |  1500 |
| Date Code : |  1205 |
| Lot Code : |  T0C102B |

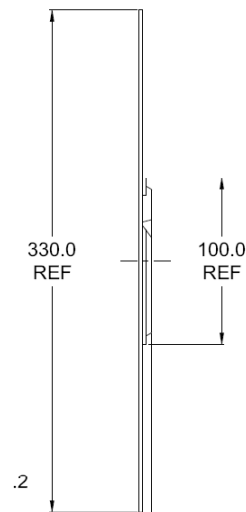
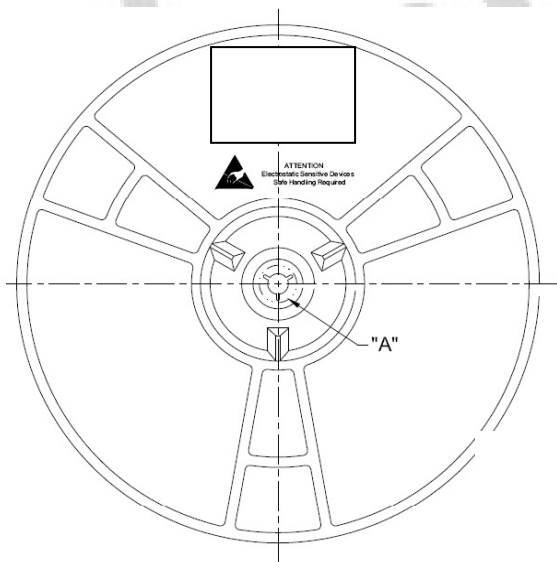
Label D → Carton box label .

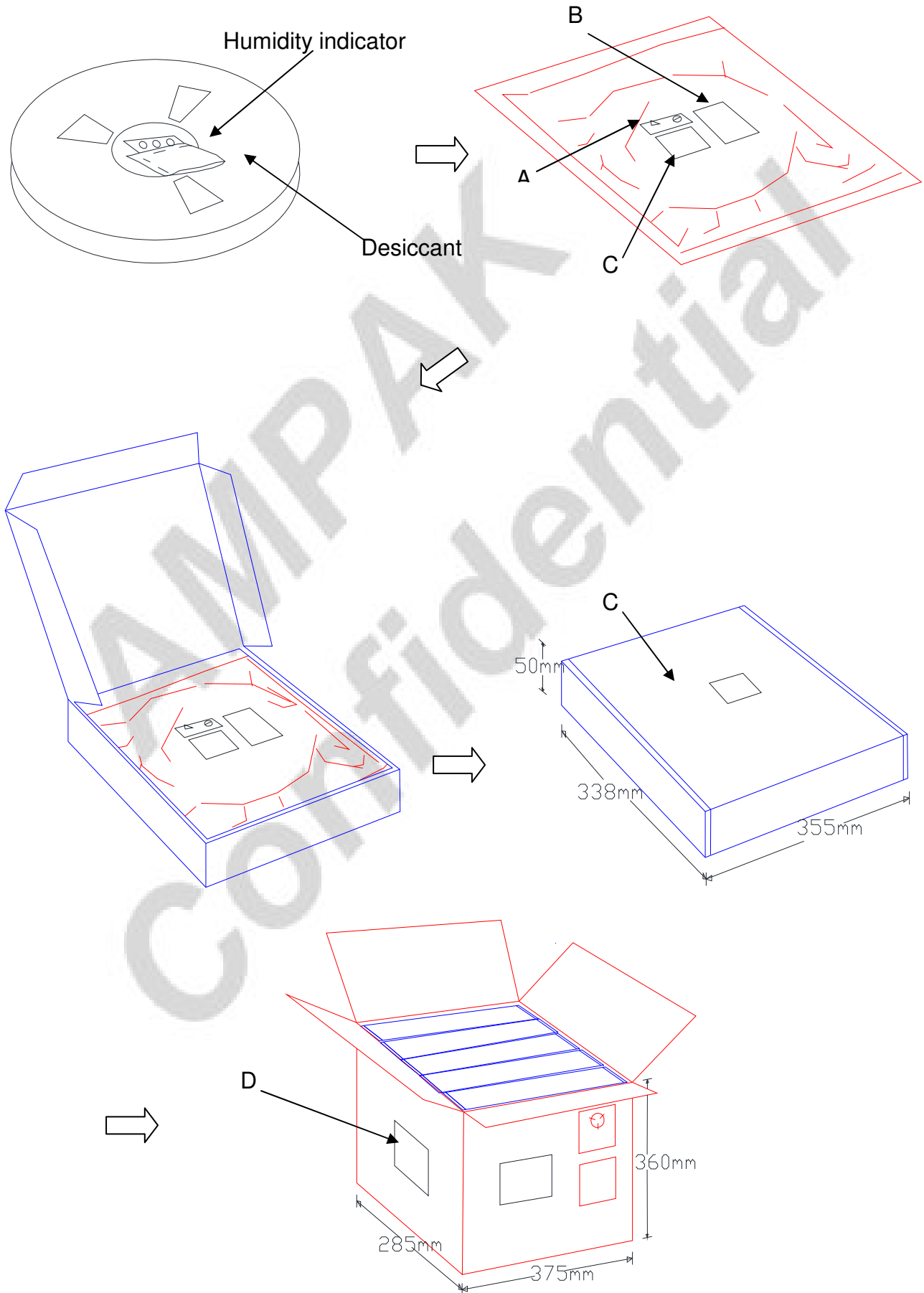
| | |
|-------------------------|--|
| AMPAK Technology | |
| Model Name : |  XXXXXXXXXXXX |
| Part No : |  99P-W01-0048R |
| Quantity : |  7500 ea |
| Lot DIC : |  20081000033 |
| Manufacture : |  2012/02/22 |

13.2 Dimension




1. 10 sprocket hole pitch cumulative tolerance ±0.20.
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481-D requirements.
5. Thickness : 0.30±0.05mm.
6. Packing length per 22" reel : 98.5 Meters.(1:3)
7. Component load per 13" reel : 1500 pcs.





13.3 MSL Level / Storage Condition

| | | | | |
|---|---|--|-------|---|
|  | <p>Caution This bag contains MOISTURE-SENSITIVE DEVICES</p> | <table border="1" style="margin: auto;"> <tr><td style="padding: 2px;">LEVEL</td></tr> <tr><td style="text-align: center; font-size: 2em; padding: 10px;">4</td></tr> </table> | LEVEL | 4 |
| LEVEL | | | | |
| 4 | | | | |
| <p>Do not open except under controlled conditions</p> | | | | |
| <p>1. Calculated shelf life in sealed bag: 12 months at < 40°C and < 90% relative humidity(RH)</p> | | | | |
| <p>225°C 240°C 250°C 260°C</p> | | | | |
| <p>2. Peak package body temperature: <input type="checkbox"/> <input type="checkbox"/> <input checked="" type="checkbox"/> <input type="checkbox"/></p> | | | | |
| <p>3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must</p> <p style="margin-left: 20px;">a) Mounted within: 48 hours of factory conditions < 30°C/60% RH, OR</p> <p style="margin-left: 20px;">b) Stored at < 10% RH</p> | | | | |
| <p>4. Devices require bake, before mounting, if:</p> <p style="margin-left: 20px;">a) Humidity Indicator Card is > 10% when read at 23±5°C</p> <p style="margin-left: 20px;">b) 3a or 3b not met</p> | | | | |
| <p>5. If baking is required, devices may be baked for 24 hours at 125±5°C</p> | | | | |
| <p>Note : If device containers cannot be subjected to high temperature or shorter bake times are desired, reference IPC/JEDEC J-STD-033 for bake procedure</p> | | | | |
| <p>Bag Seal Date: See-SEAL DATE LABEL</p> | | | | |
| <p>Note: Level and body temperature defined by IPC/JEDEC J-STD-020</p> | | | | |

※NOTE : Accumulated baking time should not exceed 96hrs