



PXN012-60QL

N-channel 60 V, 11.5 mOhm, logic level Trench MOSFET in MLPAK33

8 July 2021

Product data sheet

1. General description

General purpose, 42 A rated, logic level N-channel enhancement mode Power MOSFET in MLPAK33 package.

2. Features and benefits

- Logic level compatibility
- Trench MOSFET technology
- Thermally efficient package in a small form factor (3.3 mm x 3.3 mm footprint)

3. Applications

- Secondary side synchronous rectification
- DC-to-DC converters
- Motor drive
- LED lighting
- Load switching
- Auxiliary control
- Fan control

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	-	60	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{sp} = 25\text{ °C}; \text{Fig. 2}$	-	-	42	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}; \text{Fig. 1}$	-	-	34.7	W
T_j	junction temperature		-55	-	150	°C
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 10\text{ A}; T_j = 25\text{ °C}; \text{Fig. 9}$	-	9.8	11.5	mΩ
		$V_{GS} = 4.5\text{ V}; I_D = 10\text{ A}; T_j = 25\text{ °C}; \text{Fig. 9}$	-	14	17.6	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 10\text{ A}; V_{DS} = 30\text{ V}; V_{GS} = 4.5\text{ V}; T_j = 25\text{ °C}; \text{Fig. 11}; \text{Fig. 12}$	-	4.3	-	nC
$Q_{G(tot)}$	total gate charge		-	9.64	-	nC
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 3.5\text{ A}; T_{j(init)} = 25\text{ °C}; \text{unclamped}$	[1]	-	90	mJ

N-channel 60 V, 11.5 mOhm, logic level Trench MOSFET in MLPAK33

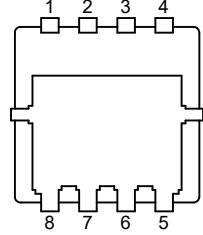
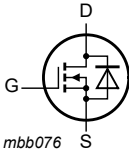
Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Source-drain diode							
Q_r	recovered charge	$I_S = 10\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 30\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 15	[2]	-	13	-	nC

[1] Protected by 100% test

[2] includes capacitive recovery

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>MLPAK33 (SOT8002-1)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
5	D	drain		
6	D	drain		
7	D	drain		
8	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PXN012-60QL	MLPAK33	plastic thermal enhanced surface mounted package; mini leads; 8 terminals; pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body	SOT8002-1

7. Marking

Table 4. Marking codes

Type number	Marking code
PXN012-60QL	7AB

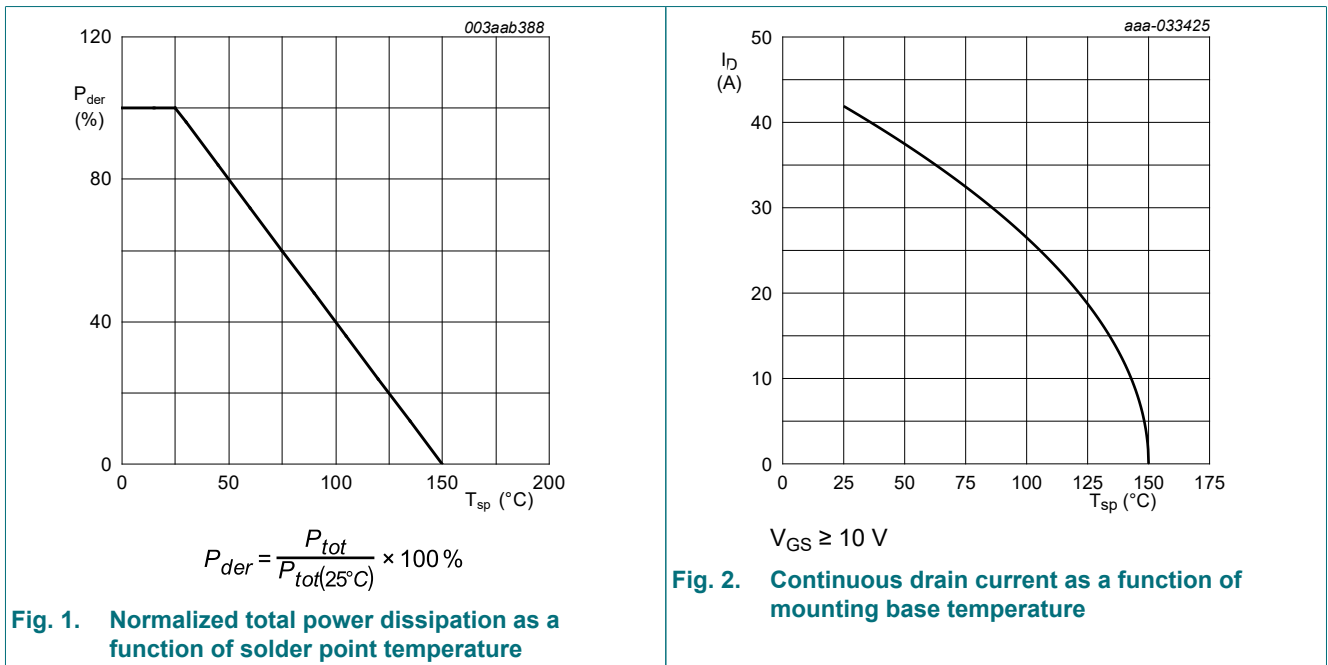
8. Limiting values

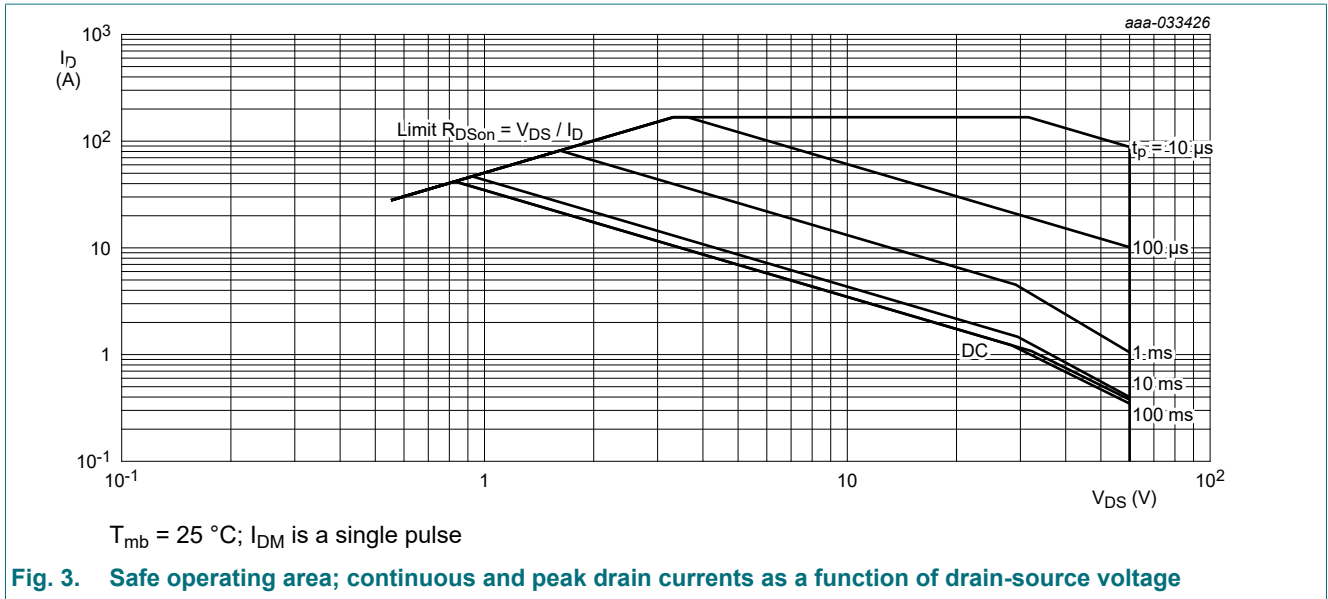
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 150 °C	-	60	V
V _{GS}	gate-source voltage		-20	20	V
P _{tot}	total power dissipation	T _{sp} = 25 °C; Fig. 1	-	34.7	W
I _D	drain current	V _{GS} = 10 V; T _{sp} = 25 °C; Fig. 2	-	42	A
		V _{GS} = 10 V; T _{sp} = 100 °C; Fig. 2	-	26	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{sp} = 25 °C; Fig. 3	-	168	A
T _{stg}	storage temperature		-55	150	°C
T _j	junction temperature		-55	150	°C
T _{slid(M)}	peak soldering temperature		-	260	°C
Source-drain diode					
I _S	source current	T _{sp} = 25 °C	-	29	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{sp} = 25 °C	-	168	A
Avalanche ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 3.5 A; T _{j(init)} = 25 °C; unclamped	[1]	-	90 mJ
I _{AS}	non-repetitive avalanche current	T _{j(init)} = 25 °C	[1]	-	3.5 A

[1] Protected by 100% test

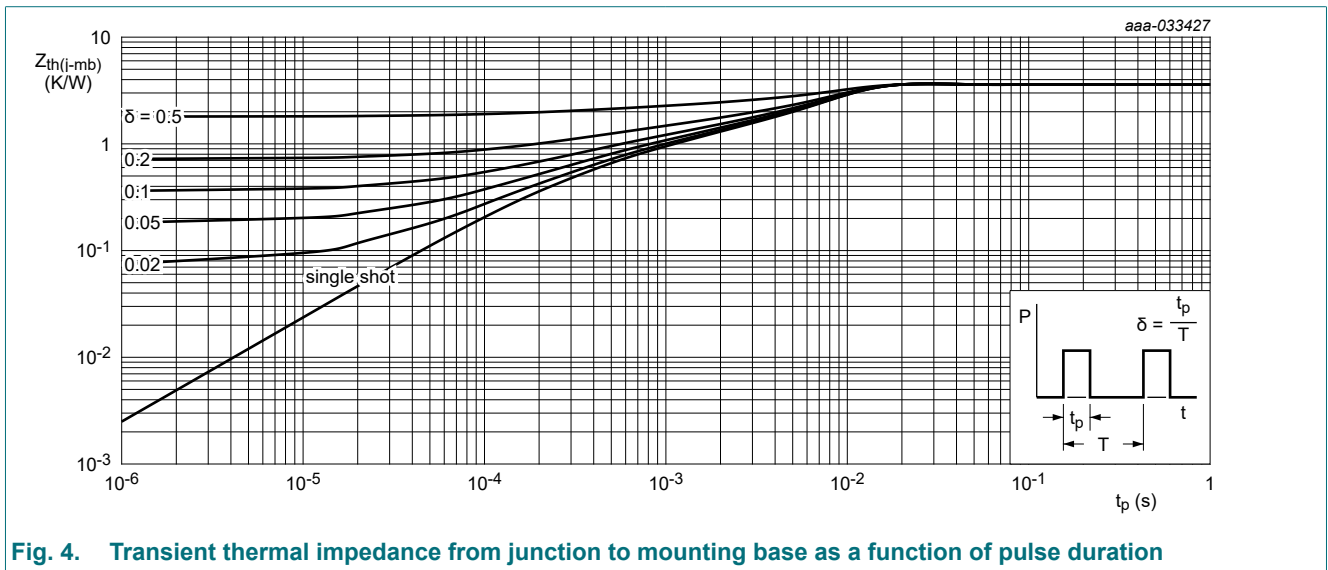




9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	Fig. 4	-	3	3.6	K/W



10. Characteristics

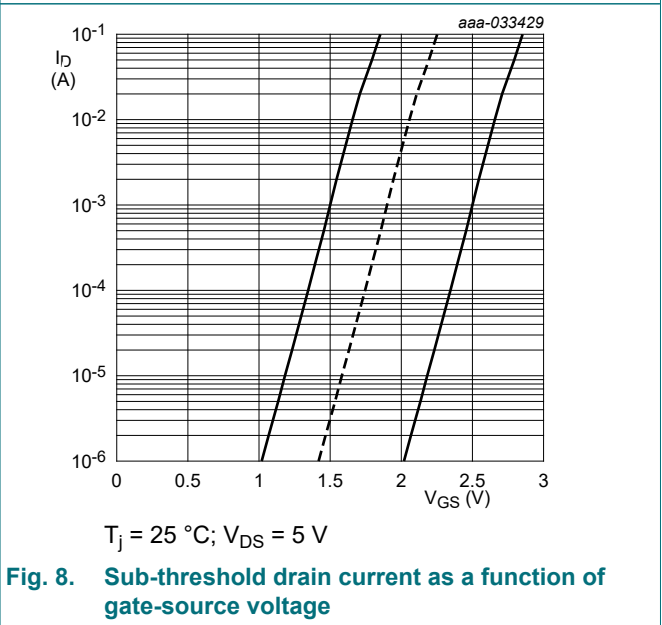
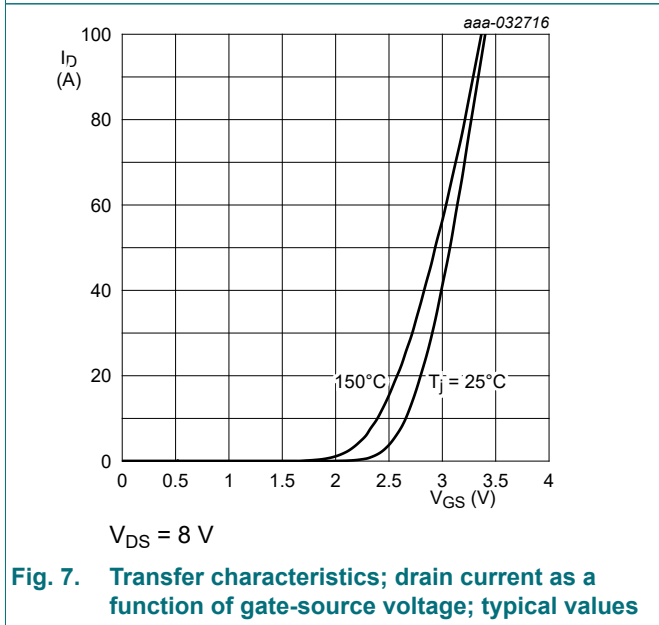
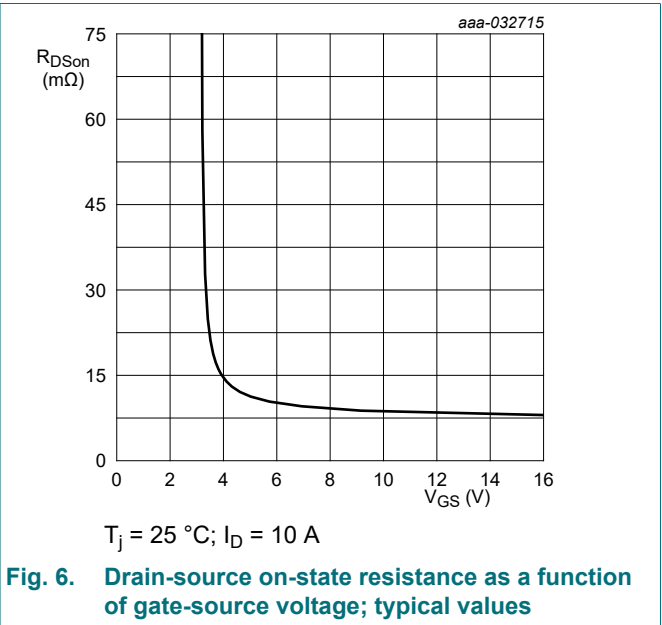
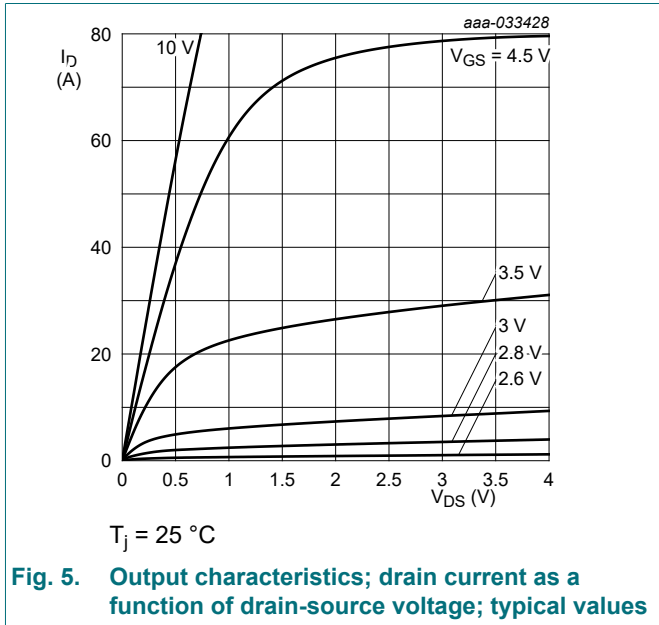
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	60	70	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	-	64	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C; \text{ Fig. 8}$	1.5	1.9	2.5	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 150 \text{ }^\circ C$	0.9	-	-	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ C$	-	-	2.9	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ C \leq T_j \leq 150 \text{ }^\circ C$	-	-4.7	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.01	1	μA
		$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ C$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ }^\circ C; \text{ Fig. 9}$	-	9.8	11.5	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 150 \text{ }^\circ C; \text{ Fig. 10}$	-	-	20	m Ω
		$V_{GS} = 4.5 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ }^\circ C; \text{ Fig. 9}$	-	14	17.6	m Ω
		$V_{GS} = 4.5 \text{ V}; I_D = 10 \text{ A}; T_j = 150 \text{ }^\circ C; \text{ Fig. 10}$	-	-	30	m Ω
R_G	gate resistance	$f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$	-	1.66	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 10 \text{ A}; V_{DS} = 30 \text{ V}; V_{GS} = 4.5 \text{ V}; T_j = 25 \text{ }^\circ C; \text{ Fig. 11}; \text{ Fig. 12}$	-	9.64	-	nC
		$I_D = 10 \text{ A}; V_{DS} = 30 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ }^\circ C; \text{ Fig. 11}; \text{ Fig. 12}$	-	18.77	-	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 4.5 \text{ V}; T_j = 25 \text{ }^\circ C; \text{ Fig. 11}; \text{ Fig. 12}$	-	9.54	-	nC
Q_{GS}	gate-source charge	$I_D = 10 \text{ A}; V_{DS} = 30 \text{ V}; V_{GS} = 4.5 \text{ V}; T_j = 25 \text{ }^\circ C; \text{ Fig. 11}; \text{ Fig. 12}$	-	3	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	1.6	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	1.4	-	nC
Q_{GD}	gate-drain charge		-	4.3	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 10 \text{ A}; V_{DS} = 30 \text{ V}; T_j = 25 \text{ }^\circ C; \text{ Fig. 11}; \text{ Fig. 12}$	-	3.1	-	V
C_{iss}	input capacitance	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C; \text{ Fig. 13}$	-	957	-	pF
C_{oss}	output capacitance		-	386	-	pF
C_{rss}	reverse transfer capacitance		-	31	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 3 \text{ } \Omega; V_{GS} = 4.5 \text{ V}; R_{G(ext)} = 5 \text{ } \Omega; T_j = 25 \text{ }^\circ C$	-	8.8	-	ns
t_r	rise time		-	18.5	-	ns
$t_{d(off)}$	turn-off delay time		-	12.2	-	ns
t_f	fall time		-	10.9	-	ns

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Q_{oss}	output charge	$V_{GS} = 0\text{ V}$; $V_{DS} = 30\text{ V}$; $f = 1\text{ MHz}$; $T_j = 25\text{ }^\circ\text{C}$	-	18	-	nC
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 10\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 14	-	0.82	1.2	V
t_{rr}	reverse recovery time	$I_S = 10\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$;	-	22.1	-	ns
Q_r	recovered charge	$V_{DS} = 30\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 15	[1]	13	-	nC

[1] includes capacitive recovery



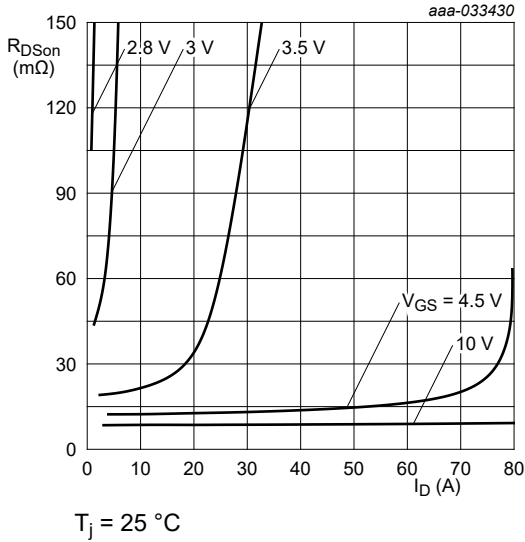
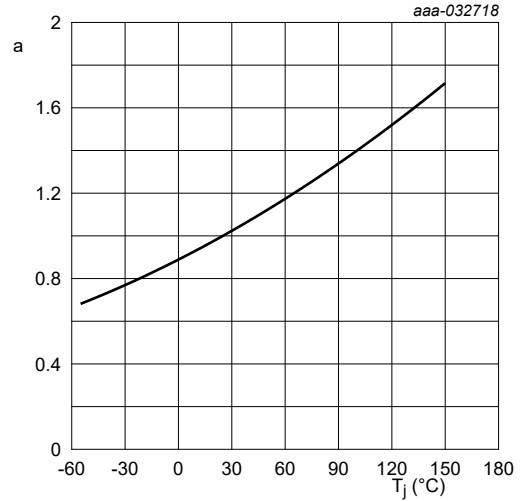


Fig. 9. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DS(on)}}{R_{DS(on), (25^\circ\text{C})}}$$

Fig. 10. Normalized drain-source on-state resistance factor as a function of junction temperature

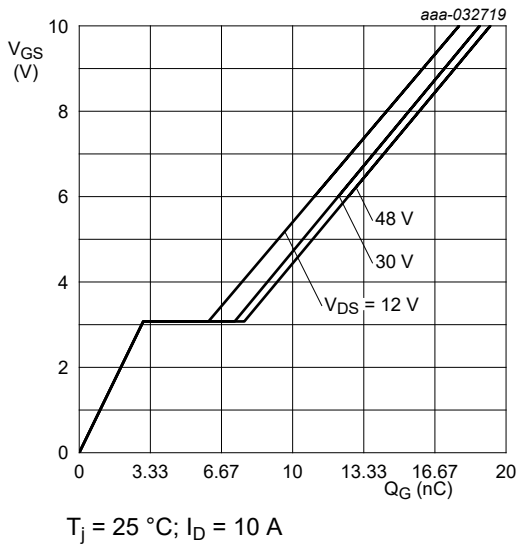


Fig. 11. Gate-source voltage as a function of gate charge; typical values

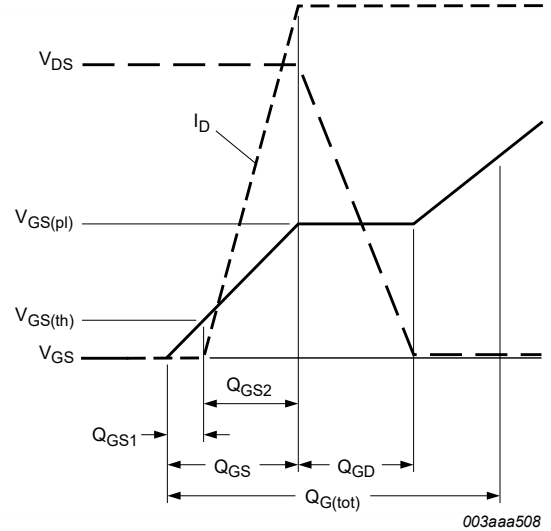
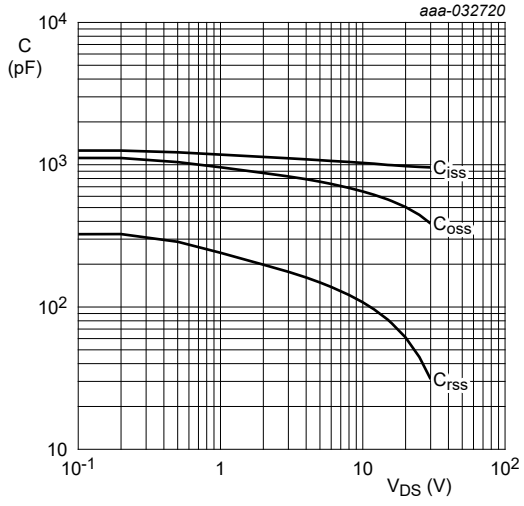
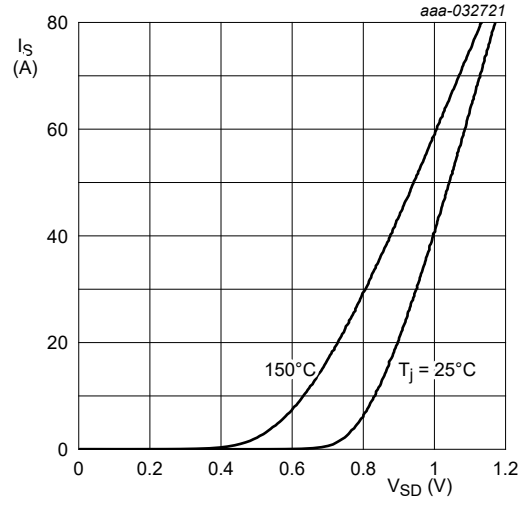


Fig. 12. Gate charge waveform definitions



$V_{GS} = 0$ V; $f = 1$ MHz

Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0$ V

Fig. 14. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

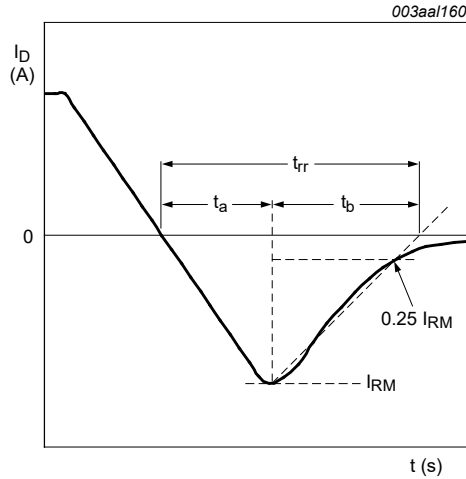
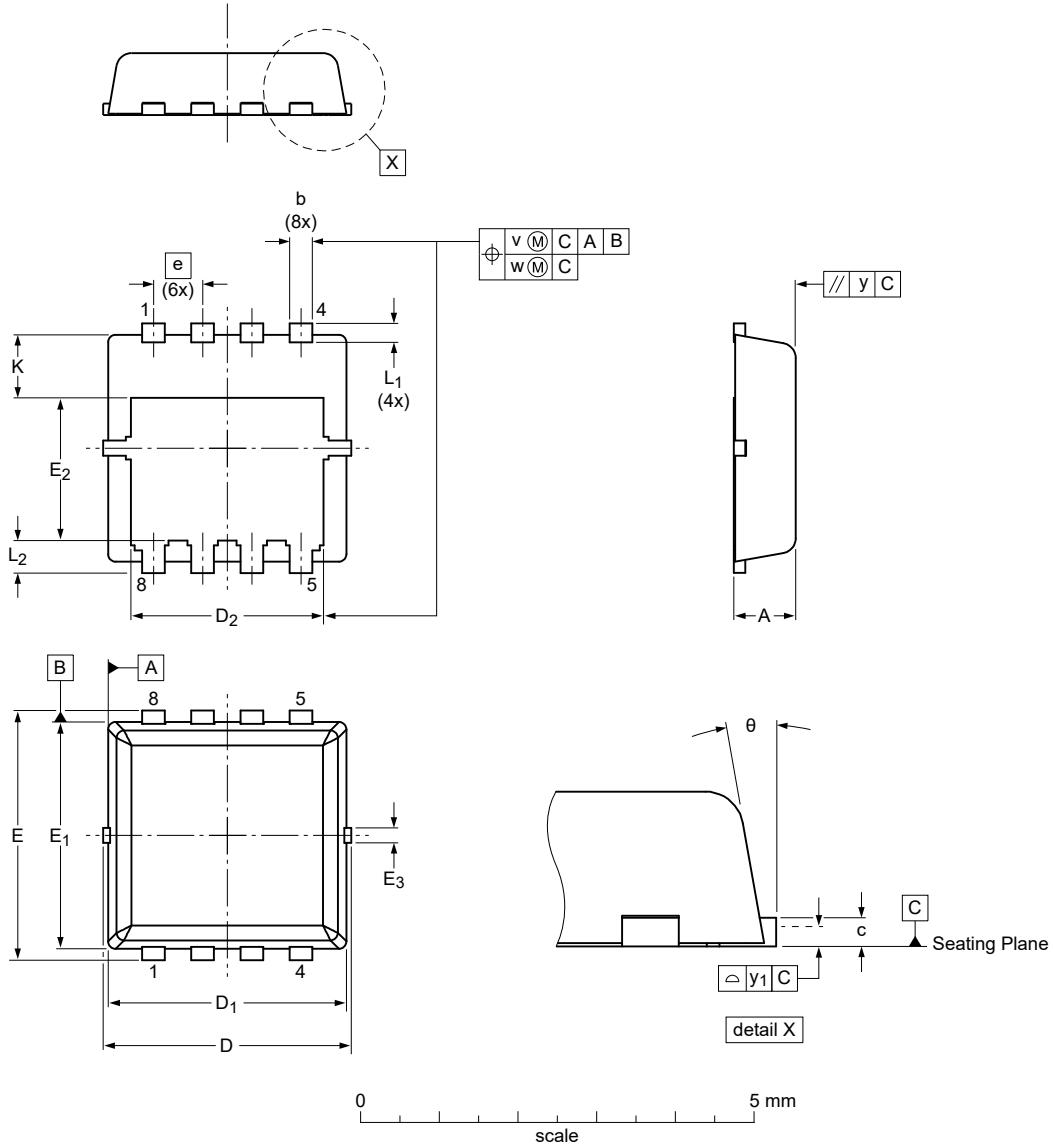


Fig. 15. Reverse recovery timing definition

11. Package outline

MLPAK33: plastic thermal enhanced surface mounted package; mini leads; 8 terminals;
pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body

SOT8002-1



Dimensions (mm are the original dimensions)

Unit	A	b	c	D	D ₁	D ₂	e	E	E ₁	E ₂	E ₃	K	L ₁	L ₂	θ	y	y ₁	v	w
max	0.90	0.35	0.18	3.50	3.25	2.65		3.50	3.10	1.99	0.25		0.40	0.58	12°				
mm nom	0.80	0.30	0.15	3.30	3.15	2.55	0.65	3.30	3.00	1.89	0.20	0.65 (ref)	0.25	0.43	10°	0.05	0.05	0.1	0.05
min	0.70	0.25	0.12	3.10	3.05	2.45		3.10	2.90	1.79	0.15		0.10	0.28	8°				

sot8002-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	EIAJ			
SOT8002-1						19-12-19 20-01-09

Fig. 16. Package outline MLPAK33 (SOT8002-1)

12. Soldering

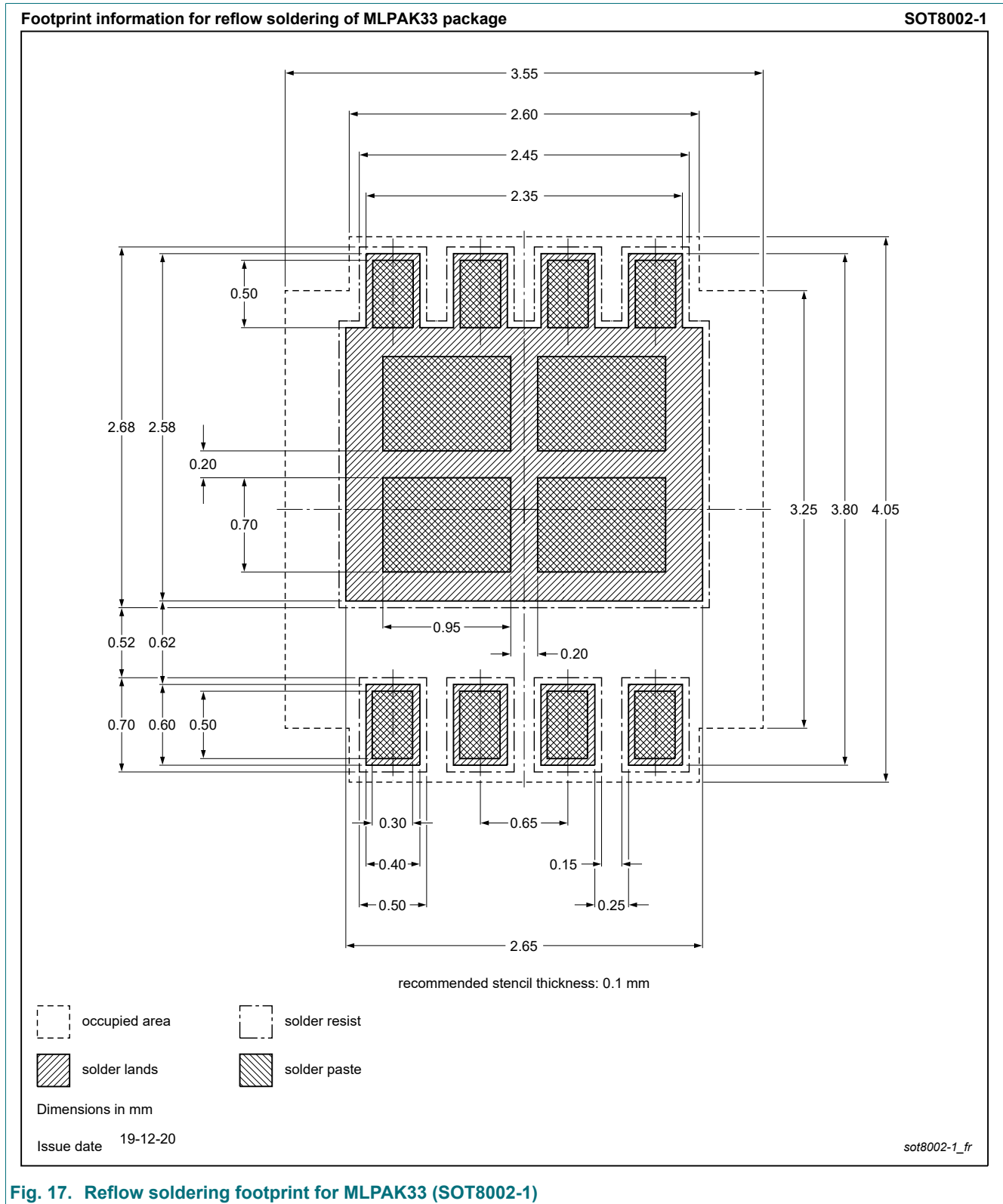


Fig. 17. Reflow soldering footprint for MLPAK33 (SOT8002-1)

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Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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