Valens

VS2310/VS2000 Family Data Sheet

Version 3.6

Valens First in HDBaseT

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Revision History

Revision	Date	Author	Description
1.0	June 2014	Daniel Shwartzberg	First Draft
1.1	July 2014	Daniel Shwartzberg	Miscellaneous updates
1.11	July 2014	Daniel Shwartzberg	Updated section 6.2 on SW Strap Pins
1.2	September 2014	Daniel Shwartzberg	Updates for MP release: - Added thermal properties (Chapter 9) - Clarifications/updates to sections 1.4, 1.6.1, 3.1.2, 3.5, 3.6.1, 3.8, 5.3, 6.1 and 6.2
1.3	December 2014	Daniel Shwartzberg	Pinout modifications reflected in: • Functional signal tables • Non-functional signal tables • Interface diagrams • BGA diagrams Table clarifying CATx cable ranges in features list Pin count added to features list MAC block is intended for future use MSIO pin compatibility with VS100 Series PDIF pins Debug port description CMOS 125 MHz Oscillator Requirements I^2S T-Adaptor pin change, section 3.8
1.4	December 2014	Daniel Shwartzberg	Sections 3.2.1.1 and 6.1: When Ethernet functionality is not required, set the Ethernet interface to MII in order to ensure correct operation of the HDBaseT link.
1.5	January 2015	Daniel Shwartzberg	Updated interface diagrams
1.6	March 2015	Daniel Shwartzberg	Power consumption ratings Fiber-or-copper selection soft strap LPPF clarifications
1.7	April 2015	Daniel Shwartzberg	MSIO support GPIO[16], GPIO[17]: weak PD -> 4.7K-10K PD

			External flash memory size: 1 MB Modified non-functional definition in RX: balls V6, V7 I^2C interface direction clarification
1.8	June 2015	Daniel Shwartzberg	New features: • USB support for Isochronous mode • Support for up to 7 USB devices • Support for DigIF interface in future release • Support for multi-streaming: HDMI port + LVDS port
1.9	July 2015	Daniel Shwartzberg	Modified Tables: • External Power on Reset Timing • PDIF-MSIO Compatibility
2.0	August 2015	Daniel Shwartzberg	Naming changes (no customer impact); Added DigIF level shifter for RGB applications
2.1	November 2015	Daniel Shwartzberg	Updates to pin lists: • FU_J4 changed from “Reserved” to “Reserved. Must be tied to ground.” • FU_D5 changed from “Reserved. Must be tied to 3.3V external weak pull-up resistor” to “Reserved. Must be tied to 3.3V external 1K pull-up resistor”. • FU_C19 changed from “Reserved. Must be tied to 3.3V external weak pull-up resistor” to “Reserved. Must be tied to 3.3V external 1K pull-up resistor”.
2.2	November 2015	Daniel Shwartzberg	• Added note that LVDS is supported over 90m Cat5e cable or 100m Cat6 cable • Clarified directions on LVDS/HDI AC characteristics • Updated 5V behavior (section 3.1.2) • Added I2C section • Updated external power on reset timings (section 7.5.3.1, “Option 2”) • Added note on USB D+/D- behavior
2.3	February 2016	Daniel Shwartzberg	• Corrected Tj parameter description in tables 25 and 26
2.4	March 2016	Daniel Shwartzberg	• Added additional modes in power consumption tables • Corrected TX ball count on page 24 • Added note on heatsink isolation sticker for RX (Section 8.2)
2.5	May 2016	Daniel Shwartzberg	• Added Operating Mode table (Table 21) • 25MHz crystal oscillator is reserved for future use

2.6	July 2016	Daniel Shwartzberg	• Corrected figures 8 and 10 – MII_MDIO is part of Ethernet MII/RMII interface • Corrected typo in Table 24 – polarity of MII_COL/GPIO[2] reversed • Corrected typo in heading 6.3.1 (MSIO_DO[4]) • Added auto-LPPF mode (section 5.3.1) • Added "LPPF1 in Auto-LPPF Mode with USB Trigger" to power consumption tables
2.7	December 2016	Daniel Shwartzberg	• Added new soft strap functionality on GPIO[22] • Updated Quality and Environmental policy (Section 10) • Removed obsolete MSIO_CLKOUT functionality • Additional information on MSIO functionality (including use of 10:1 oversampling ratio) • Added LED blink rates • Added limitations of MSIO + Ethernet in Long Reach mode • Added BT.1120 interface (text, pin lists) • Added ESD ratings
2.8	January 2017	Daniel Shwartzberg	• Clarification for embedded BT-1120 controls • Added RMII clock limitations/recommendations
2.9	March 2017	Daniel Shwartzberg	• Added BT-1120 format support and electrical characteristics • Updated functional signal tables "If Not Used" columns (tables 5, 8, 11, 14) and "Description" columns (tables 6, 9, 12, 15)
3.0	June 2017	Daniel Shwartzberg	• Added SPI interface DC characteristics (tables 34 and 35) • Added clarifications to limitations of Long Reach mode (section 5.2.4.1) • Added additional power ratings for HDI bus • Added note on I^2S DAC • Corrected CIRTypeInPolarity default typo in section 6.3.4.
3.1	September 2017	Yaki Sfadya	• Updated support for daisy-chain topology
3.2	September 2017	Yaki Sfadya	• Updated marking information and ordering codes
3.3	May 2018	Yaki Sfadya	• Corrected typo in section 7.5.3.1 POR_BYPASS =0
3.4	August 2018	Yaki Sfadya	• Added note about using the RMII or SGMII interface rather than the MII.
3.5	January 2019	Yaki Sfadya	• Added JTAG interface and updated pin out • Corrected pin T5 description to ETH

3.6	November 2019	Yaki Sfadya	• Updated HDCP2.2-> HDCP2.x (include HDCP2.3)

Glossary

Term	Definition
ARC	Audio Return Channel
AFE	Analog Front End
AV	Audio Video / Audio-Visual
CE	Consumer Electronics
CEC	Consumer Electronic Control
CIR	Consumer Infrared
EVK	Evaluation Kit
CTS	Compliance Test Specification
DDC	Display Data Channel
DVI	Digital Visual Interface
EEPROM	Electronically Erasable Programmable Read-Only Memory
GPIO	General Purpose Input Output
HD	High Definition
HDBT	HDBaseT
HDCD	HDBaseT Configuration Database
HDCP	High-Bandwidth Digital Content Protection
HDMI	High Definition Multimedia Interface
HIF	Host Interface
HLIC	HDBaseT Link Internal Controls
HPD	Hot Plug Detect
I/F	Interface
IC	Integrated Circuit
I^2C	Inter IC
I^2S	Inter IC Sound
KVM	Keyboard / Video / Mouse
LPPF	Low Power Partial Functionality
LSB	Least Significant Bit
LVDS	Low-Voltage Differential Signaling
MSIO	Multi Serial Input Output
MAC	Media Access Control Layer
MCU	Microcontroller Unit
RoHS	Restriction of Hazardous Substances
SNR	Signal-to-Noise Ratio
MIB	Management Information Base
MSB	Most Significant Bit
OM	Operation Mode

Term	Definition
PHY	Physical Layer
PoE	Power Over Ethernet
PRBS	Pseudo Random Bit Stream
RIF	Register Interface
SERDES	SERializer DESerializer
SPDIF	Sony/Philips Digital Interface Format
SPI	Serial Peripheral Interface
STB	Set-Top Box
UART	Universal Asynchronous Receive Transmit
USB	Universal Serial Bus

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1 Introduction

This specification provides a detailed description of the Valens VS2310/VS2000 product family. Each chipset in the family includes an HDBaseT transmitter chip and an HDBaseT receiver chip. The specification provides essential information required for designing a VS2310/VS2000 embedded application.

1.1 About the VS2310/VS2000 Family

Valens Semiconductor developed the VS2310/VS2000 product family to enable high-quality, wired connectivity of a 5Play feature set over a single LAN cable/Fiber Optics. The 5Play feature set includes:

- Uncompressed high-definition (HD) video content
- High-fidelity digital audio
- 100BaseTX Ethernet
- Various control/data formats including USB2.0, SPDIF and I2S audio, I2C, RS232 and consumer infrared (CIR).
- Up to 100W of power using PoH (does not apply to fiber media)

The VS2310/VS2000 Product Family is based on HDBaseT™ technology – the first technology to enable simplified, long-distance wired connectivity of uncompressed HD multimedia content over a single, standard 100-meter CATx (CAT5e/6/6a/7) cable or fiber optics.

The table below compares availability of features amongst VS2310/VS2000 family members:

Table 1: VS2000 Family Feature Comparison Table

Part #	HDBaseT over CATx Cable	HDMI	Enet	I2C	UART	HDBaseT Digital Interface (HDI I/O)	I2S	SPDIF	MSIO	CIR	USB	HDCP	VS2311 Compatible (Valens Fiber Optic Solution)
VS2000	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	No	Yes	No
VS2310	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

1.2 Main Applications

The VS2310/VS2000 products are ideal for the following applications:

- HDMI / DVI extenders over CATx / fiber optics cables

- NxK AV matrixes
- AV receivers
- HD projectors
- Industrial PCs
- Single wire TVs and two-box TVs
- KVM (Keyboard, Video, Mouse) extension
- Digital signage displays
- Multi-stream video switching / distribution / aggregation, and daisy chaining
- Delivering uncompressed video and controls over fiber optics (together with the VS2311)

NOTE

Not all applications are supported by all members of the VS2310/VS2000 product family.

1.3 Typical Application Examples

1.3.1 KVM/HDMI Extender Application

This application example shows an HDBaseT HDMI extender/KVM extender. On the transmitter side, a Full HD or Ultra HD HDMI AV source is connected to the HDMI interface of the VS2310TX chip. An Ethernet device is connected via the SGMII interface to connect the system to the Ethernet network. In addition, for the KVM case, a PC may be connected as a USB2.0 host.

On the receiver side, a monitor, display, or Ethernet-enabled smart-TV device is connected to the HDMI interface for AV content. The device is connected to the home network via the SGMII interface. A mouse-keyboard device is connected via the USB2.0 device interface.

Infrared control signals received at the VS2310RX side are transferred back and blasted at the VS2310TX side by the IR blaster.

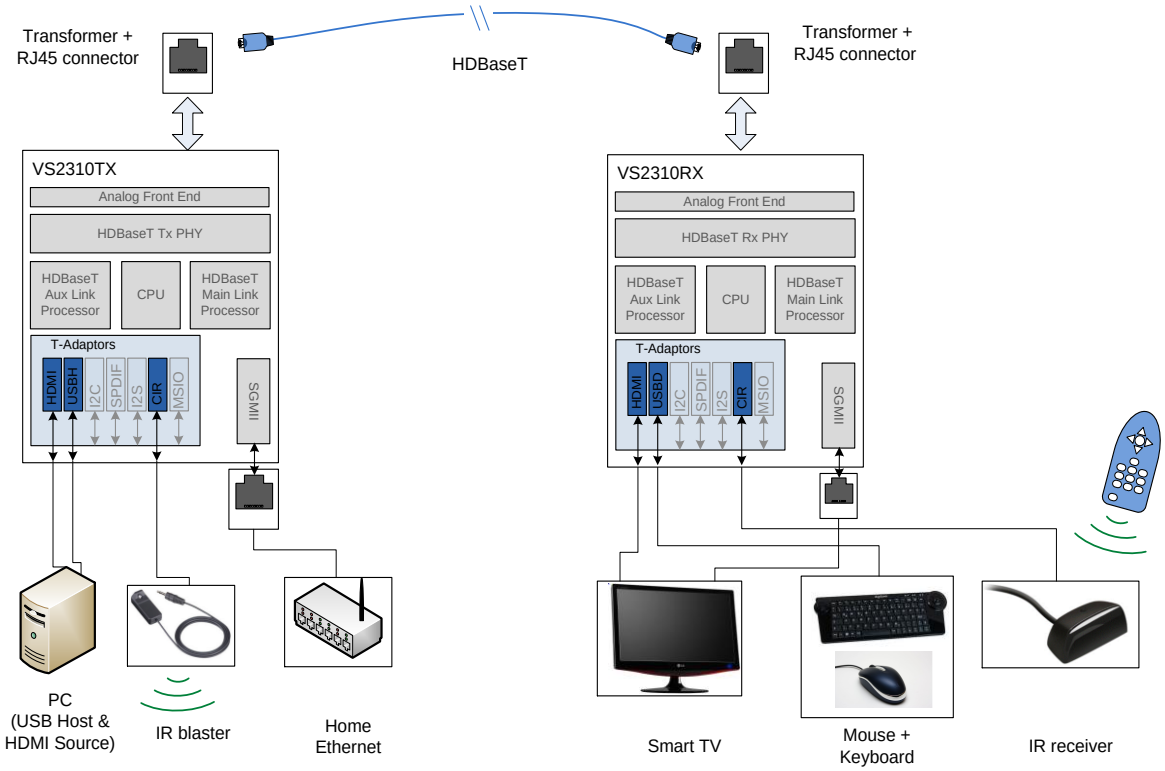


Figure 1: KVM/HDMI Extender Application with Ethernet Support

Note that an HDMI extender application can also be achieved using the VS2000 chipset (since USB support is not required).

1.3.2 A Dual Hop Daisy-Chain Signage Application

This application example is comprised of three devices. Two HDMI AV sources are connected to the device on the left hand side. A multi-stream AV content is delivered over the HDBaseT link to the first hop device. This device comprises of both VS2310RX and a VS2310TX chip. The chips are gluelessly connected using the HDI interface. The first hop device outputs HDMI AV content to Monitor A. An additional hop connects another device providing HDMI AV content to monitor B. Each hop comprises a LAN cable up to 100 meters in length.

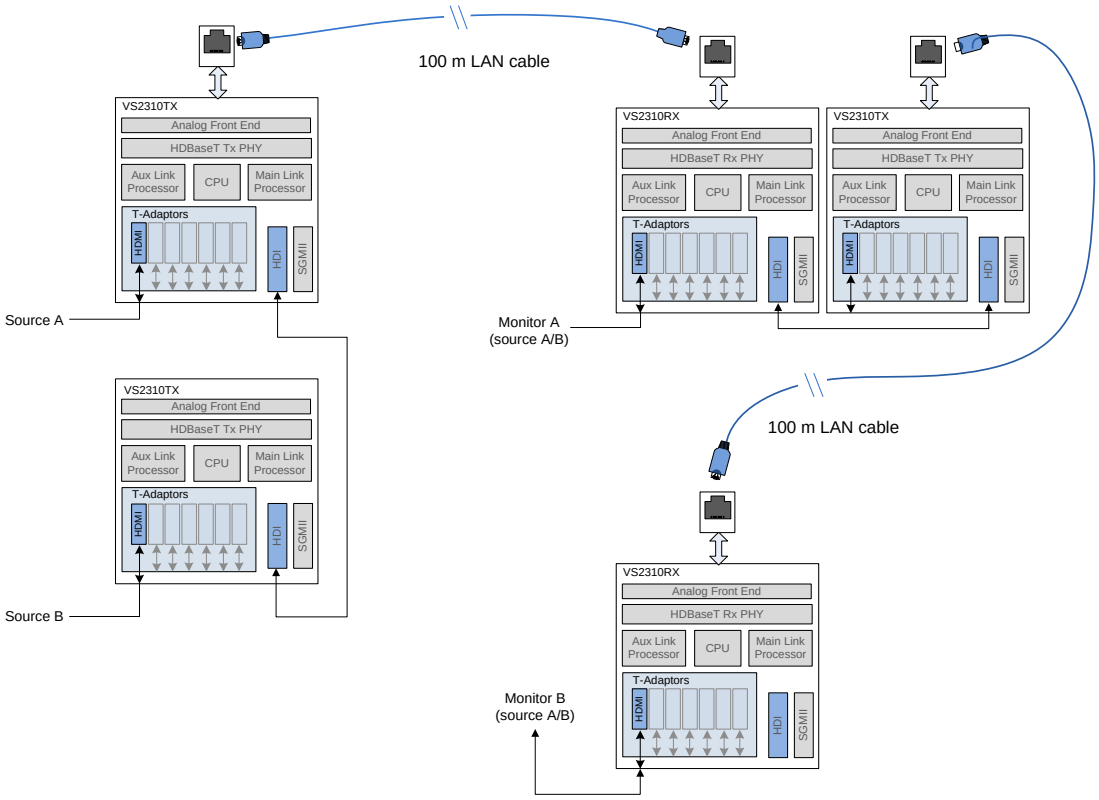


Figure 2: A Dual Hop Daisy-Chain Signage Application

1.3.3 Fiber Optics Extender Application

The application below illustrates an extender over fiber optics media. On the left of the diagram, the VS2310 HDI interface is connected to Valens VS2311TX chip. This chip implements an HDBaseT over a fiber optic port. Using the VS2310+VS2311 bundle, an SFP+ optical transceiver may be used to deploy a long reach optical link carrying HDBaseT traffic. The HDBaseT traffic is recovered at the remote side by an inverse operation (optical transceiver → VS2311RX → VS2310RX HDI port).

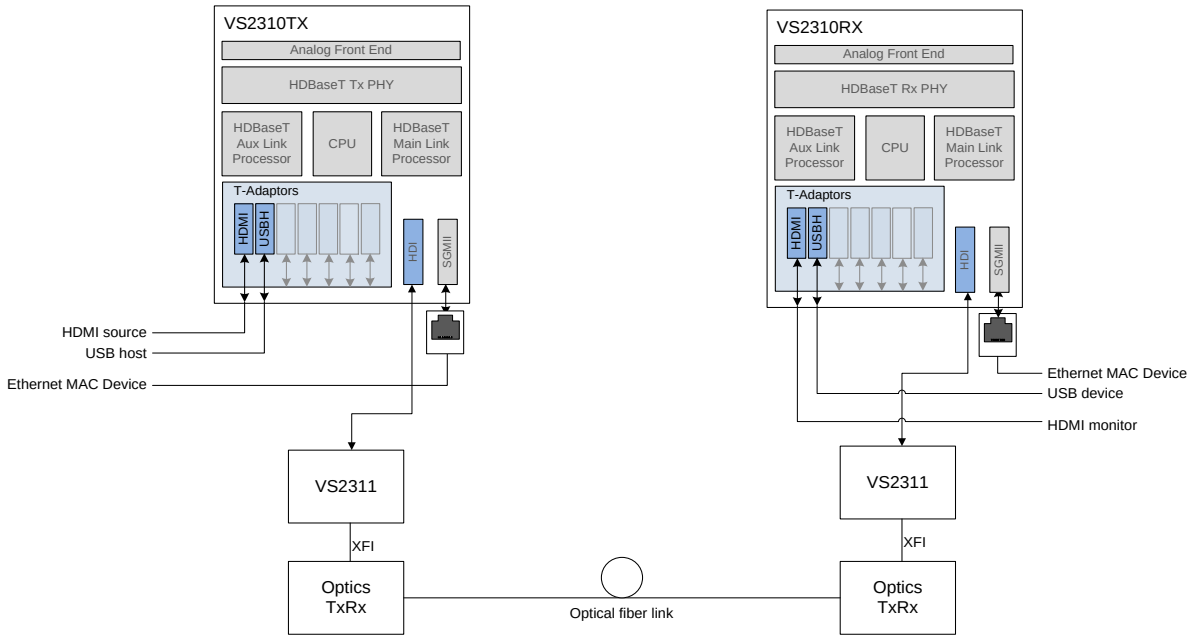


Figure 3: Fiber Optics Application

1.4 HDBaseT Technology Overview

Valens HDBaseT™ technology empowers **5Play™** digital connectivity between high-definition video sources and remote displays. HDBaseT™ enables plug-and-play delivery of multimedia traffic over a single 100 meter (328 foot) CATx cable:

- Video – Uncompressed high-definition/3D video in up to 4K resolution
- Audio – Any standard digital audio format
- Ethernet – 100BaseTX Ethernet
- Control – Various control signals including CEC, RS-232, and IR
- Power – Up to 100W using Power-over-Cable (PoH) technology

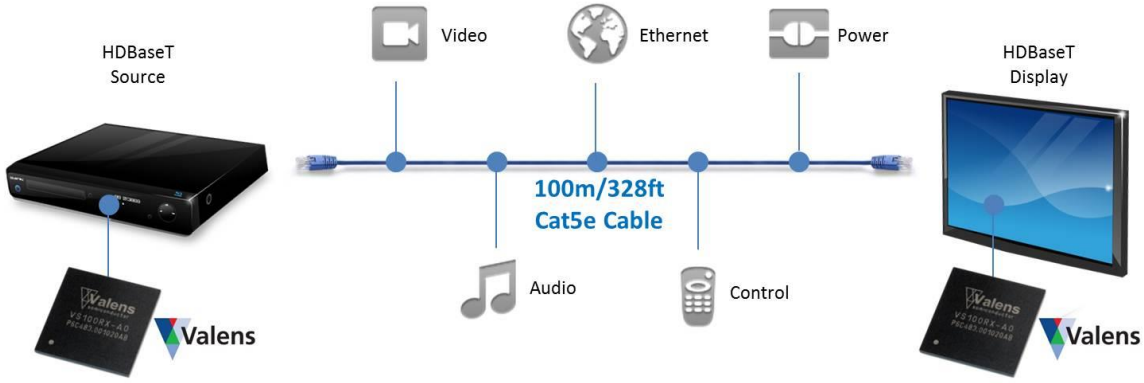


Figure 4: HDBaseT Technology

Video

HDBaseT™ delivers Ultra HD (4K2K@30Hz with YCbCr 4:4:4 and 4K2K@60Hz with YCbCr 4:2:0) formats of up to 1080p@60Hz@48 b/pixel, and 3D – to a network of devices, or over a point-to-point connection. HDBaseT™ provides a transparent transport mechanism for HDMI chipsets, thus supporting all key features of HDMI 2.0, including HPD, 5V, CEC, EDID and HDCP. Valens' proprietary video coding scheme ensures the highest video quality with zero latency.

Audio

As with video, HDBaseT™ Audio is transparently transported directly from the HDMI chipset, thus supporting all standard formats, such as Dolby Digital, DTS, Dolby TrueHD, DTS HD-Master Audio and more.

Ethernet

HDBaseT™ supports 100 Mbps Ethernet capabilities, enabling televisions, hi-fi equipment, computers, and other consumer electronic devices to communicate with each other and access stored multimedia content, including video streaming, images and music. Relying on the same physical infrastructure, HDBaseT™ also supports Ethernet Fallback Mode. In this

mode, if you plug an HDBaseT device into an Ethernet-only infrastructure, the device will automatically "realize" it and will enable only the Ethernet capabilities of the connection.

Controls

HDBaseT™ delivers a variety of multipurpose control signals, including Consumer Electronic Controls (CEC), RS-232, USB (VS2310 only), and infrared. Since HDBaseT™ also supports an Ethernet channel, IP-based control can be employed as well. This opens up endless possibilities for equipment manufacturers, from remote device control to fully managed networks.

The control plane supports additional bandwidth of up to 250 Mbps for applications requiring extra capacity.

Power

As part of its 5Play™ feature-set, HDBaseT™ supports transmission of up to 100W of DC power over the same CATx cable. Now, you can provide power without requiring access to an electic outlet – enhancing device mobility.

1.5 HDBaseT Channel Terminology

The HDBaseT channel consists of two distinct asymmetric unidirectional channels:

- *Main Channel* – Directed downstream from the HDBaseT transmitter to the HDBaseT receiver, carrying uncompressed multimedia content (HDMI, USB, SPDIF, GP MSIO, UART, CIR, I2S) as well as the transmitter to receiver portion of the Ethernet data content and multimedia controls.
- *Auxiliary Return Channel* – Directed upstream from the HDBaseT receiver to the HDBaseT transmitter, carrying the return channel controls and the receiver to transmitter portion of the data content.

The HDBaseT Transmitter and Receiver chips are labeled VS2310TX/VS2000TX and VS2310RX/VS2000RX, respectively. The HDBaseT transmitter is used to connect the HD source equipment (STBs, Blu-ray / DVD players, etc.) while the HDBaseT receiver is used to connect the sink equipment (monitors, TVs, projectors, etc.).

1.6 VS2310/VS2000 Chipset Overview

The figure below is a block diagram illustrating the main functional blocks of the VS2310TX/RX and VS2000TX/RX devices:

1.6.1 Block Diagrams

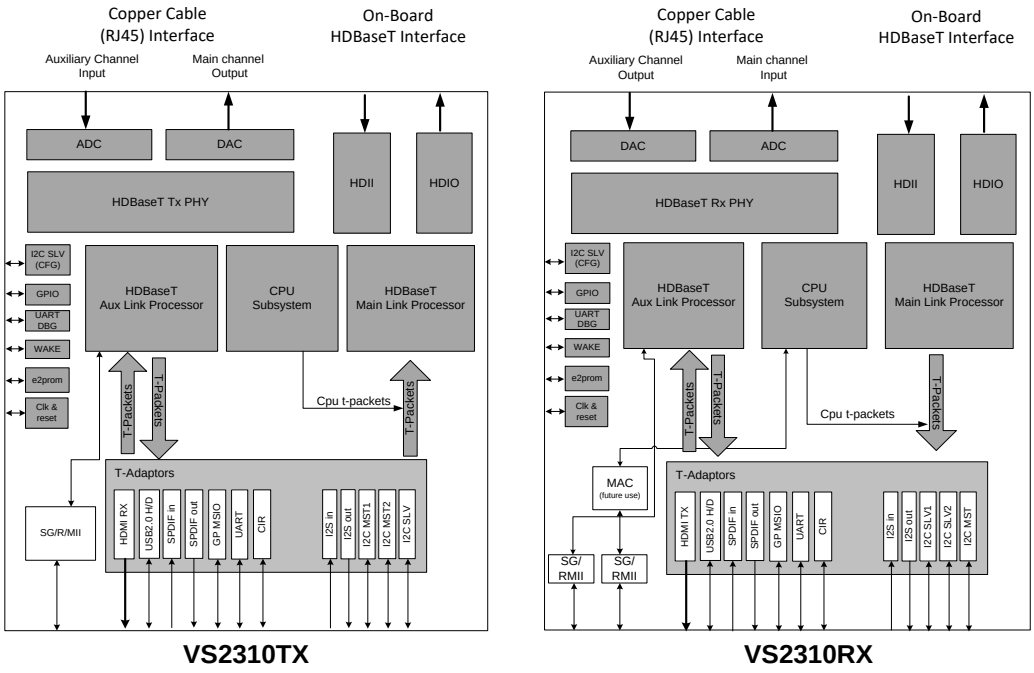


Figure 5: VS2310TX and VS2310RX Block Diagrams

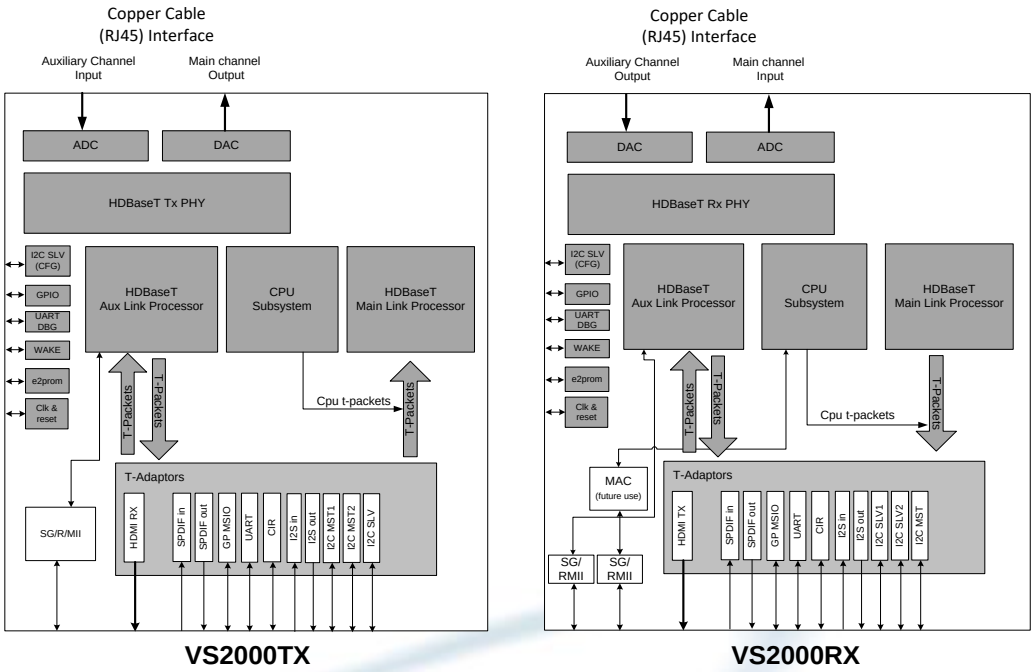


Figure 6: VS2000TX and VS2000RX Block Diagrams

1.6.2 Features

- Two-device chipsets, including TX for the video source side, and RX for the video sink side:
  - VS2310TX and VS2310RX
  - VS2000TX and VS2000RX
- Compliant with HDBaseT 2.0 Specification supporting 5Play™convergence over a single CATx (CAT5e/6/6a/7) cable.
  - Audio, Video, Control, Ethernet, USB 2.0 (VS2310 only) and Power
  - HDBaseT transmission ranges according to CATx cable type:

Table 2: VS2310/VS2000 Family CATx Cable Range Specification

Cable Type	Range	Pixel Clock Rate	Video Data Rate	Supported Video
CAT5e	100 m	<=225 MHz	<= 5.3 Gbps (HD Video)	Up to 1080p, 60 Hz, 36 bpp (data rates lower than 5.3 Gbps or below 225 MHz TMDS clock).
	90 m	>225 MHz	> 5.3 Gbps (Ultra HD Video)	1080p 60 Hz 48 bpp, 1080p 60 Hz 3D, 4K2K/30Hz/4:4:4 and 4K2K/60Hz/4:2:0 video formats
CAT6/CAT6a/CAT7	100 m			

- Native HDMI with all its components
  - Fully compliant with HDMI 1.4, and compatible with HDMI 2.0 (4K2K 60Hz with 4:2:0 coding)
  - EDID adjustment mechanism for HDMI2.0 at pixel clock higher than 340 MHz
  - HDCP 1.x, 2.x compliant
  - Advanced DSP capabilities and analog front-end design enhance noise immunity and cable impairment immunity
- Native UART, CIR, I2S audio and S/PDIF audio support
- Support for UART, CIR in Low power mode
- Maximum 300 Mbps upstream data rate budget
- Backward compatible to HDBaseT 1.0 Specification and legacy HDBaseT products
- Exceptional cable ranges with maximum traffic rate, offering up to 100 meters over CATx cable, supporting uncompressed HD video in the following formats:
  - Up to 297Mhz HDMI pixel clock
  - Support for 4k 2k / 30Hz / 24bpp with 4:4:4 pixel format

- Support for 4k 2k / 60Hz / 24bpp with 4:2:0 pixel format

- Up to 150 meters in long-reach mode:
  - Up to 4 Gbps HDBaseT Traffic rate
  - HDMI Pixel Frequency 148.5Mhz
  - Video Format 1080p / 60Hz / 24bpp
- Support for 4/2/1 lane operation (2 / 1 lanes in future firmware release)
- Coexistence with PoE (802.3af), PoE+ (802.3at) and PoH
- Video interfaces: Glueless HDMI interface: directly connectable to all TMDS, DDC, CEC and HPD HDMI signals (TMDS, DDC, CEC, 5V and HPD)
- Transfer various control and audio formats over the HDBaseT link including:
  - High quality audio over S/PDIF standard I/F
  - High quality audio over I2S standard I/F
  - RS232 for standard UART control protocol
  - IR – for infra-red control unit
  - I2C – both slave and master interfaces
  - MSIO – 6 general purpose fast serial channels for delivering any proprietary user format
- Ethernet Interface
  - Delivers 100BaseTX Ethernet auxiliary channel alongside the HDBaseT channel in both directions (upstream and downstream)
  - Support for SGMII, RMII and MII MAC interfaces (connectable to MAC / Switch)
- System Interfaces
  - RS232 for external debugger
  - I2C slave for External Host interface
  - SPI boot Flash Interface
- USB 2.0 support (VS2310 only)
  - Configurable either as Host or as a Device USB port
- Support for BT.1120 interface
- HDI input and HDI output proprietary digital interface for on-board inter-chip connectivity and applications (VS2310 only)
  - Support for 8 Gbps inter-device on-board connectivity
  - HDBaseT Packets over inter-chip interconnection for additional flexibility

- Glueless interface to VS2311TX/RX fiber optic device (currently supported)

- Package Dimensions:
  - VS2310TX/VS2000TX: LFBGA 21mm x 21mm, 356-ball grid (20 x 20)
  - VS2310RX/VS2000RX: HSBGA 23 mm x 23 mm, 484-ball grid (22 x 22)
  - Ball pitch 1 mm
- Absolute maximum rated junction temperature: minimum -40°C, maximum +125°C

2 Pin Configuration and Ball Diagram

2.1 Interface Diagrams

The interface diagrams in the following sections details the signal groups of the various interfaces. The brackets below each interface group indicate for which part the interface is available.

2.1.1 VS2310 Interface Diagrams

2.1.1.1 VS2310TX Interface Diagram

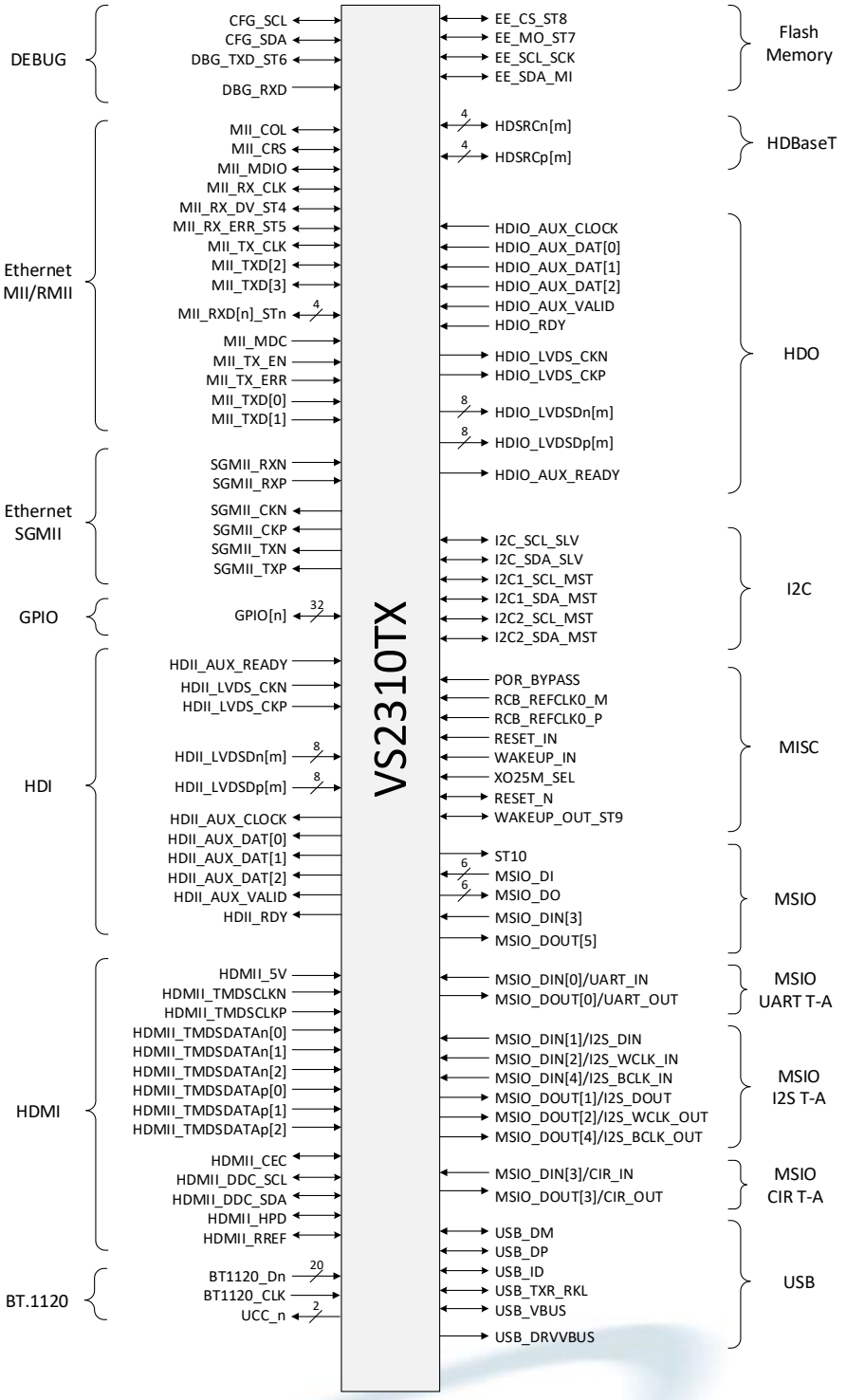


Figure 7: VS2310TX I/F Signal Block Diagram

2.1.1.2 VS2310Rx Interface Diagram

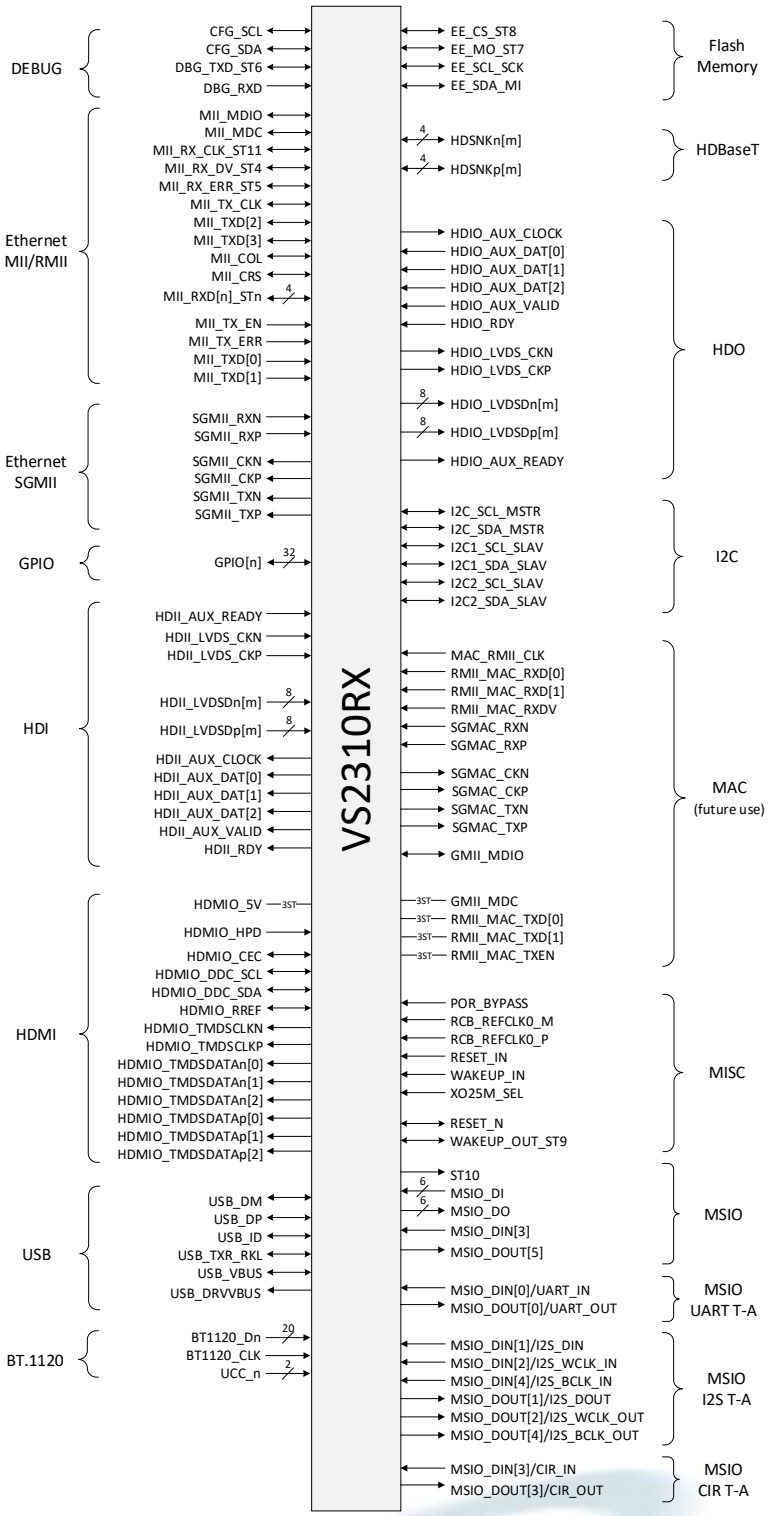


Figure 8: VS2310RX I/F Signal Block Diagram

2.1.2 VS2000 Interface Diagrams

2.1.2.1 VS2000TX Interface Diagram

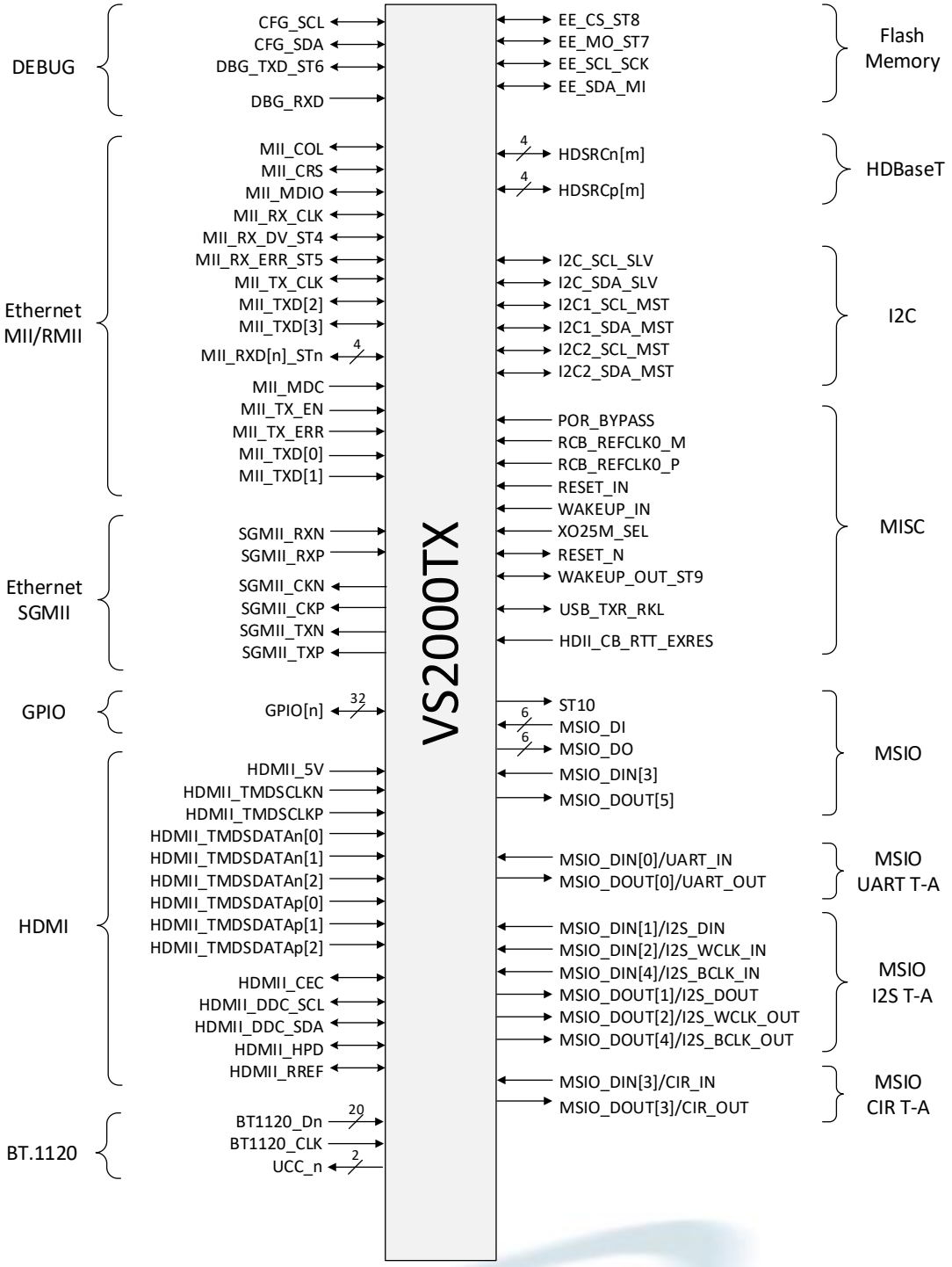


Figure 9: VS2000TX I/F Signal Block Diagram

2.1.2.2 VS2000Rx Interface Diagram

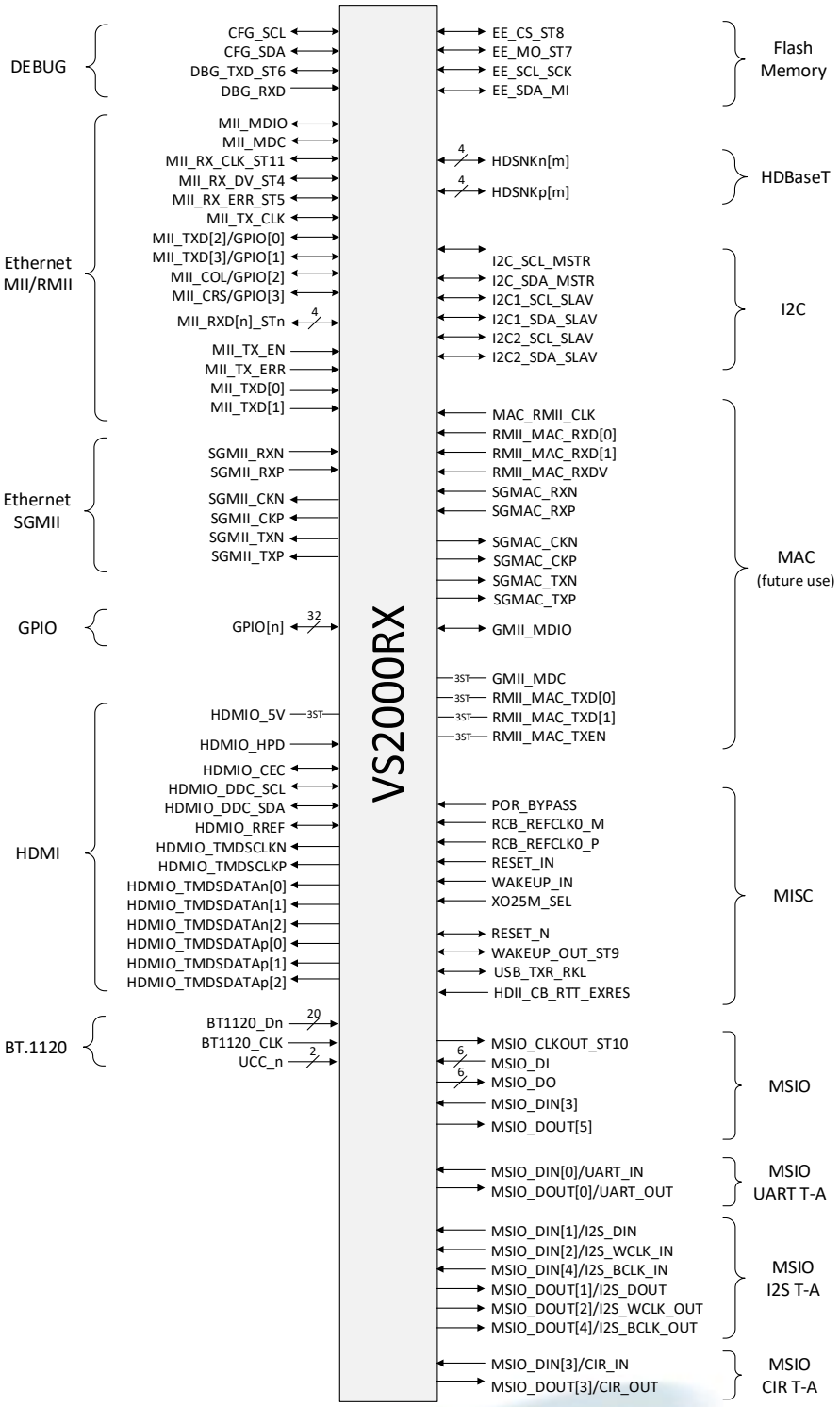


Figure 10: VS2000RX I/F Signal Block Diagram

2.2 Pin Type Convention

2.2.1 IO Pad Types

The VS2310/VS2000 pin types and their descriptions are listed below:

Table 3: VS2310/VS2000 Pin Types

Pin Type	Description
Input	Digital input pad
Output	Digital output pad
IO	Bidirectional IO digital pad
Input [PU/PD]	Digital input pad [with integrated pull-up/pull-down resistor]
Output [PU/PD]	Digital output pad [with integrated pull-up/pull-down resistor]
IO, PU	Bidirectional IO digital pad with integrated pull-up resistor
IO, PD	Bidirectional IO digital pad with integrated pull-down resistor
AIO	Analog bidirectional pad
AI	Analog input pad
AO	Analog output pad
03State	Digital output pad with tri-state buffer
XTAL	Crystal I/O pad

2.2.2 Unused Pins

If your application does not use one or more interfaces, you should implement the connectivity of the interface's balls according to the *If Not Used* column in Table 5 for the TX chip and Table 11 for the RX chip.

The following conventions are used to connect unused pins:

Table 4: VS2310/VS2000 Unused Pin Types

Category	Connection Requirement
NC	Safe to leave unconnected (floating)
GND	Must be connected to a ground
WPD	Must be connected to a ground via a weak pull-down resistor
WPU	Must be connected to 3.3V supply via a weak pull-up resistor
1KPD	Must be connected to a ground via 1Kohm resistor
1KPU	Must be connected to a 3.3V supply via 1Kohm resistor

2.3 VS2310TX/VS2000TX Signal Description

2.3.1 VS2310TX Signal Description

Table 5 below provides information on each pin of the VS2310TX chip. Pins with more than one function use the following convention:

- F1: <function 1 description>
- F2: <function 2 description>
- ST: <strap function description>

Selecting between functions of multi-functional pins is performed by either using VS2310 chip parameters or asserting strap pins. For more details, refer to the section in Chapter 6 that corresponds with the relevant interface category.

2.3.1.1 Tx Functional Signals

Table 5: VS2310TX Functional Signal Table

Signal Name	Ball#	Pad Type	I/F category	If Not Used	Functional Description
BT1120_D19	L3	Input, PD	BT.1120	NC	BT.1120 – Input Chroma bit 9
BT1120_D18	K3	Input, PD	BT.1120	NC	BT.1120 – Input Chroma bit 8
BT1120_D17	L2	Input, PD	BT.1120	NC	BT.1120 – Input Chroma bit 7
BT1120_D16	K2	Input, PD	BT.1120	NC	BT.1120 – Input Chroma bit 6
BT1120_D15	M3	Input, PD	BT.1120	NC	BT.1120 – Input Chroma bit 5
BT1120_D14	K1	Input, PD	BT.1120	NC	BT.1120 – Input Chroma bit 4
BT1120_D13	N3	Input, PD	BT.1120	NC	BT.1120 – Input Chroma bit 3
BT1120_D12	L1	Input, PD	BT.1120	NC	BT.1120 – Input Chroma bit 2
BT1120_D11	N2	Input, PD	BT.1120	NC	BT.1120 – Input Chroma bit 1
BT1120_D10	M2	Input, PD	BT.1120	NC	BT.1120 – Input Chroma bit 0
BT1120_D9	P3	Input, PD	BT.1120	NC	BT.1120 – Input Luminance bit 9
BT1120_D8	M1	Input, PD	BT.1120	NC	BT.1120 – Input Luminance bit 8
BT1120_D7	P2	Input, PD	BT.1120	NC	BT.1120 – Input Luminance bit 7
BT1120_D6	N1	Input, PD	BT.1120	NC	BT.1120 – Input Luminance bit 6
BT1120_D5	R3	Input, PD	BT.1120	NC	BT.1120 – Input Luminance bit 5
BT1120_D4	P1	Input, PD	BT.1120	NC	BT.1120 – Input Luminance bit 4
BT1120_D3	R2	Input, PD	BT.1120	NC	BT.1120 – Input Luminance bit 3
BT1120_D2	R1	Input, PD	BT.1120	NC	BT.1120 – Input Luminance bit 2
BT1120_D1	T2	Input, PD	BT.1120	NC	BT.1120 – Input Luminance bit 1
BT1120_D0	T1	Input, PD	BT.1120	NC	BT.1120 – Input Luminance bit 0
BT1120_CLK	T3	Input, PD	BT.1120	NC	BT.1120 – Input clock
UCC_0	K4	O3State	BT.1120	NC	BT.1120 – HDcctv Upstream Communication Channel 0

Signal Name	Ball#	Pad Type	I/F category	If Not Used	Functional Description
UCC_1	L4	O3State	BT.1120	NC	BT.1120 – HDcctv Upstream Communication Channel 1
CFG_SCL	U9	IO,PU	DEBUG	NC	Host interface I2C clock Signal
CFG_SDA	U10	IO,PU	DEBUG	NC	Host interface I2C data Signal
DBG_RXD	U8	input,PU	DEBUG	NC	Debug Receive Data (I)
DBG_TXD_ST6	U5	IO,PU	DEBUG	1K PD	Debug Transmit Data (O);ST: strap bit #6
EE_CS_ST8	W4	IO,PD	FLASH	Must Use	SPI FLASH chip select; ST: strap bit #8
EE_MO_ST7	U4	IO,PD	FLASH	1K PU	SPI FLASH MO (master Out); ST: strap bit #7
EE_SCL_SCK	V4	IO,PU	FLASH	Must Use	Clock for Both I2C and SPI FLASHs (O)
EE_SDA_MI	Y4	IO,PU	FLASH	Must Use	I2C FLASH SDA or SPI FLASH MI (Master In)
GPIO[16]	H17	IO,PU	GPIO	4.7K-10K PD	General purpose IO bit #16 (IO). Must be tied to external 4.7K-10K pulldown resistor in all applications.
GPIO[17]	H18	IO,PU	GPIO	4.7K-10K PD	General purpose IO bit #17 (IO). Must be tied to external 4.7K-10K pulldown resistor in all applications.
GPIO[18]	H19	IO,PU	GPIO	NC	General purpose IO bit #18 (IO)
GPIO[19]	H20	IO,PU	GPIO	NC	General purpose IO bit #19 (IO)
GPIO[20]/MSIO_DO[0]	J17	IO,PU	GPIO	NC	F1: General purpose IO bit #20 (IO); F2: MSIO data output bit #0
GPIO[21]/MSIO_DO[1]	J18	IO,PU	GPIO	NC	F1: General purpose IO bit #21 (IO); F2: MSIO data output bit #1
GPIO[22]/MSIO_DO[2]	J19	IO,PU	GPIO	NC	F1: General purpose IO bit #22 (IO); F2: MSIO data output bit #2
GPIO[23]/MSIO_DO[3]	J20	IO,PU	GPIO	NC	F1: General purpose IO bit #23 (IO); F2: MSIO data output bit #3
GPIO[24]/MSIO_DO[4]	K17	IO,PU	GPIO	NC	F1: General purpose IO bit #24 (IO); F2: MSIO data output bit #4
GPIO[25]/MSIO_DO[5]	K18	IO,PU	GPIO	NC	F1: General purpose IO bit #25 (IO); F2: MSIO data output bit #5
GPIO[26]/MSIO_DI[0]	K19	IO,PU	GPIO	NC	F1: General purpose IO bit #26 (IO); F2: MSIO data input bit #0
GPIO[27]/MSIO_DI[1]	K20	IO,PU	GPIO	NC	F1: General purpose IO bit #27 (IO); F2: MSIO data input bit #1
GPIO[28]/MSIO_DI[2]	L17	IO,PU	GPIO	NC	F1: General purpose IO bit #28 (IO); F2: MSIO data input bit #2

Signal Name	Ball#	Pad Type	I/F category	If Not Used	Functional Description
GPIO[29]/MSIO_DI[3]	L18	IO,PU	GPIO	NC	F1: General purpose IO bit #29 (IO); F2: MSIO data input bit #3
GPIO[30]/MSIO_DI[4]	L19	IO,PU	GPIO	NC	F1: General purpose IO bit #30 (IO); F2: MSIO data input bit #4
GPIO[31]/MSIO_DI[5]	L20	IO,PU	GPIO	NC	F1: General purpose IO bit #31 (IO); F2: MSIO data input bit #5
HDII_AUX_CLOCK	C8	O3State	HDI	NC	HDI auxiliary channel, clock out
HDII_AUX_DAT[0]	C4	O3State	HDI	NC	HDI auxiliary channel, data out 0
HDII_AUX_DAT[1]	D5	O3State	HDI	NC	HDI auxiliary channel, data out 1
HDII_AUX_DAT[2]	D6	O3State	HDI	NC	HDI auxiliary channel, data out 2
HDII_AUX_READY	C5	Input	HDI	GND	HDI auxiliary channel, HDI Rx auxiliary channel ready
HDII_AUX_VALID	C6	O3State	HDI	NC	HDI auxiliary channel, data out valid
HDII_CB_RTT_EXRES	D14	AIO	HDI	Must Use	HDI central bais external resistor; Should be tied to a 1KOhm (1% tolerance) pull down resistor.
HDII_LVDS_CKN	B15	AIO	HDI	NC	* HDI main channel, LVDS clock in (N) * LVCMOS data in, data [0]
HDII_LVDS_CKP	A15	AIO	HDI	NC	* HDI main channel, LVDS clock in (P) * LVCMOS clock in
HDII_LVDSDn[0]	B11	AIO	HDI	NC	* HDI main channel, LVDS data in, lane 0 (N) * LVCMOS data in, data [2]
HDII_LVDSDn[1]	B12	AIO	HDI	NC	* HDI main channel, LVDS data in, lane 1 (N) * LVCMOS data in, data [4]
HDII_LVDSDn[2]	B13	AIO	HDI	NC	* HDI main channel, LVDS data in, lane 2 (N) * LVCMOS data in, data [6]
HDII_LVDSDn[3]	B14	AIO	HDI	NC	* HDI main channel, LVDS data in, lane 3 (N) * LVCMOS data in, data [8]
HDII_LVDSDn[4]	B16	AIO	HDI	NC	* HDI main channel, LVDS data in, lane 4 (N) * LVCMOS data in, data [10]
HDII_LVDSDn[5]	B17	AIO	HDI	NC	* HDI main channel, LVDS data in, lane 5 (N) * LVCMOS data in, data [12]
HDII_LVDSDn[6]	B18	AIO	HDI	NC	* HDI main channel, LVDS data in, lane 6 (N) * LVCMOS data in, data [14]

Signal Name	Ball#	Pad Type	I/F category	If Not Used	Functional Description
HDII_LVDSDn[7]	B19	AIO	HDI	NC	* HDI main channel, LVDS data in, lane 7 (N) * LVCMOS data in, data [16]
HDII_LVDSDp[0]	A11	AIO	HDI	NC	* HDI main channel, LVDS data in, lane 0 (P) * LVCMOS data in, data [1]
HDII_LVDSDp[1]	A12	AIO	HDI	NC	* HDI main channel, LVDS data in, lane 1 (P) * LVCMOS data in, data [3]
HDII_LVDSDp[2]	A13	AIO	HDI	NC	* HDI main channel, LVDS data in, lane 2 (P) * LVCMOS data in, data [5]
HDII_LVDSDp[3]	A14	AIO	HDI	NC	* HDI main channel, LVDS data in, lane 3 (P) * LVCMOS data in, data [7]
HDII_LVDSDp[4]	A16	AIO	HDI	NC	* HDI main channel, LVDS data in, lane 4 (P) * LVCMOS data in, data [9]
HDII_LVDSDp[5]	A17	AIO	HDI	NC	* HDI main channel, LVDS data in, lane 5 (P) * LVCMOS data in, data [11]
HDII_LVDSDp[6]	A18	AIO	HDI	NC	* HDI main channel, LVDS data in, lane 6 (P) * LVCMOS data in, data [13]
HDII_LVDSDp[7]	A19	AIO	HDI	NC	* HDI main channel, LVDS data in, lane 7 (P) * LVCMOS data in, data [15]
HDII_RDY	C7	O3State	HDI	NC	HDI main channel, HDI Rx main channel ready
HDIO_AUX_CLOCK	D12	Input	HDO	GND	HDO auxiliary channel, clock in
HDIO_AUX_DAT[0]	D9	Input	HDO	GND	HDO auxiliary channel, data in 0
HDIO_AUX_DAT[1]	D10	Input	HDO	GND	HDO auxiliary channel, data in 1
HDIO_AUX_DAT[2]	D11	Input	HDO	GND	HDO auxiliary channel, data in 2
HDIO_AUX_READY	D7	O3State	HDO	NC	HDO auxiliary channel, HDI Rx auxiliary channel ready
HDIO_AUX_VALID	D8	Input	HDO	GND	HDO auxiliary channel, data in valid
HDIO_LVDS_CKN	A6	AIO	HDO	NC	HDO main channel, clock out (N)
HDIO_LVDS_CKP	B6	AIO	HDO	NC	HDO main channel, clock out (P)
HDIO_LVDSDn[0]	A10	AIO	HDO	NC	HDO main channel, data out, lane 0 (N)
HDIO_LVDSDn[1]	A9	AIO	HDO	NC	HDO main channel, data out, lane 1 (N)
HDIO_LVDSDn[2]	A8	AIO	HDO	NC	HDO main channel, data out, lane 2 (N)

Signal Name	Ball#	Pad Type	I/F category	If Not Used	Functional Description
HDIO_LVDSDn[3]	A7	AIO	HDO	NC	HDO main channel, data out, lane 3 (N)
HDIO_LVDSDn[4]	A5	AIO	HDO	NC	HDO main channel, data out, lane 4 (N)
HDIO_LVDSDn[5]	A4	AIO	HDO	NC	HDO main channel, data out, lane 5 (N)
HDIO_LVDSDn[6]	A3	AIO	HDO	NC	HDO main channel, data out, lane 6 (N)
HDIO_LVDSDn[7]	A2	AIO	HDO	NC	HDO main channel, data out, lane 7 (N)
HDIO_LVDSDp[0]	B10	AIO	HDO	NC	HDO main channel, data out, lane 0 (P)
HDIO_LVDSDp[1]	B9	AIO	HDO	NC	HDO main channel, data out, lane 1 (P)
HDIO_LVDSDp[2]	B8	AIO	HDO	NC	HDO main channel, data out, lane 2 (P)
HDIO_LVDSDp[3]	B7	AIO	HDO	NC	HDO main channel, data out, lane 3 (P)
HDIO_LVDSDp[4]	B5	AIO	HDO	NC	HDO main channel, data out, lane 4 (P)
HDIO_LVDSDp[5]	B4	AIO	HDO	NC	HDO main channel, data out, lane 5 (P)
HDIO_LVDSDp[6]	B3	AIO	HDO	NC	HDO main channel, data out, lane 6 (P)
HDIO_LVDSDp[7]	B2	AIO	HDO	NC	HDO main channel, data out, lane 7 (P)
HDIO_RDY	C12	Input,PU	HDO	NC	HDO main channel, HDI Rx main channel ready
HDMII_5V	U20	Input	HDMI	GND	HDMI Rx 5V power signal input
HDMII_CEC	U19	IO	HDMI	27K PU	HDMI Rx CEC bus
HDMII_DDC_SCL	U16	IO	HDMI	47K PU	HDMI Rx DDC I2C clock
HDMII_DDC_SDA	U17	IO	HDMI	NC	HDMI Rx DDC I2C data
HDMII_HPD	U18	IO	HDMI	NC	HDMI Rx hot plug detect output
HDMII_RREF	U15	AIO	HDMI	Must Use	HDMI current Source Resistor; Should be tied to a 12 KOhm (1% tolerance) pull up resistor, AVDD33
HDMII_TMDSCLKN	Y13	AI	HDMI	NC	HDMI Rx TMDS clock lane (N)
HDMII_TMDSCLKP	W13	AI	HDMI	NC	HDMI Rx TMDS clock lane (P)
HDMII_TMDSDATAn[0]	Y15	AI	HDMI	NC	HDMI Rx TMDS data lane 0 (N)
HDMII_TMDSDATAn[1]	Y17	AI	HDMI	NC	HDMI Rx TMDS data lane 1 (N)
HDMII_TMDSDATAn[2]	Y19	AI	HDMI	NC	HDMI Rx TMDS data lane 2 (N)
HDMII_TMDSDATAp[0]	W15	AI	HDMI	NC	HDMI Rx TMDS data lane 0 (P)
HDMII_TMDSDATAp[1]	W17	AI	HDMI	NC	HDMI Rx TMDS data lane 1 (P)
HDMII_TMDSDATAp[2]	W19	AI	HDMI	NC	HDMI Rx TMDS data lane 2 (P)
HDSRC_REXT_H	V11	AIO	HDBaseT	Must Use	HDBT current Source Resistor. Should be tied to a 4.53 KOhm (1% tolerance) pull down resistor.
HDSRCn[0]	Y6	AIO	HDBaseT	NC	HDBaseT Transceiver Channel 0 (N)
HDSRCn[1]	Y7	AIO	HDBaseT	NC	HDBaseT Transceiver Channel 1 (N)
HDSRCn[2]	Y9	AIO	HDBaseT	NC	HDBaseT Transceiver Channel 2 (N)

Signal Name	Ball#	Pad Type	I/F category	If Not Used	Functional Description
HDSRCn[3]	Y10	AIO	HDBaseT	NC	HDBaseT Transceiver Channel 3 (N)
HDSRCp[0]	W6	AIO	HDBaseT	NC	HDBaseT Transceiver Channel 0 (P)
HDSRCp[1]	W7	AIO	HDBaseT	NC	HDBaseT Transceiver Channel 1 (P)
HDSRCp[2]	W9	AIO	HDBaseT	NC	HDBaseT Transceiver Channel 2 (P)
HDSRCp[3]	W10	AIO	HDBaseT	NC	HDBaseT Transceiver Channel 3 (P)
I2C_SCL_SLV	U12	IO,PU	I2C	NC	Slave I2C2 interface, clock line, connect to external master
I2C_SDA_SLV	U11	IO,PU	I2C	NC	Slave I2C2 interface, data line, connect to external master
I2C1_SCL_MST	U7	IO,PU	I2C	NC	Master I2C interface 1, clock line, connect to external slave
I2C1_SDA_MST	U6	IO,PU	I2C	NC	Master I2C interface 1, data line, connect to external slave
I2C2_SCL_MST	U14	IO,PU	I2C	NC	Master I2C interface 2, clock line, connect to external slave
I2C2_SDA_MST	U13	IO,PU	I2C	NC	Master I2C interface 2, data line, connect to external slave
MII_COL/GPIO[2]	E4	IO,PU	ETH	NC	F1: MII PHY Collision Detect; F2: General Purpose IO Bit #2
MII_CRS/GPIO[3]	C3	IO,PU	ETH	NC	F1: MII PHY Carrier Sense; F2: General Purpose IO Bit #3
MII_MDC	E3	Input,PU	ETH	NC	MII Slave Management Clock
MII_MDIO	F3	IO,PU	ETH	NC	MII Slave Management Data
MII_RX_CLK	D2	IO	ETH	1K PD	F1: MII PHY Receive Clock; F2: RMII 50MHz output clock
MII_RX_DV_ST4	D4	IO,PU	ETH	1K PD	MII/RMII PHY receive Data Valid; ST: Strap bit #4
MII_RX_ERR_ST5	D3	IO,PD	ETH	1K PD with jumper	MII PHY Receive Error; ST: Strap bit #5
MII_RXD[0]_ST0	C2	IO,PD	ETH	NC	MII/RMII PHY Receive Data Bit 0; ST: Strap bit #0
MII_RXD[1]_ST1	B1	IO,PD	ETH	NC	MII/RMII PHY Receive Data Bit 1; ST: Strap bit #1
MII_RXD[2]_ST2	C1	IO,PD	ETH	NC	MII PHY Receive Data Bit 2; ST: Strap bit #2
MII_RXD[3]_ST3	D1	IO,PU	ETH	1KPD	MII PHY Receive Data Bit 3; ST: Strap bit #3
MII_TX_CLK	H4	IO,PU	ETH	1KPD	F1: MII PHY Transmit Clock; F2: RMII REF_CLK input

Signal Name	Ball#	Pad Type	I/F category	If Not Used	Functional Description
MII_TX_EN	F4	Input	ETH	GND	MII/RMII PHY Transmit Enable
MII_TX_ERR	G3	Input,PU	ETH	GND	MII PHY Transmit Error
MII_TXD[0]	G4	Input,PU	ETH	NC	MII/RMII PHY Transmit Data Bit 0
MII_TXD[1]	H3	Input,PU	ETH	NC	MII/RMII PHY Transmit Data Bit 1
MII_TXD[2]/GPIO[0]	J3	IO,PU	ETH	NC	F1: MII PHY Transmit Data Bit 2 (I); F2: General Purpose IO Bit #0
MII_TXD[3]/GPIO[1]	J4	IO,PU	ETH	NC	F1: MII PHY Transmit Data Bit 3 (I); F2: General Purpose IO Bit #1
ST10	G20	IO	MSIO	1K PU	Strap pin #10
MSIO_DIN[0]/UART_IN/GPIO[4]	D20	IO,PU	MSIO	NC	F1: MSIO data input #0; F2: UART in; F3: General purpose pin #4
MSIO_DIN[1]/I2S_DIN/GPIO[5]	E17	IO,PU	MSIO	NC	F1: MSIO data input #1; F2: I2S data in; F3:General purpose pin #5
MSIO_DIN[2]/I2S_WCLK_IN/GPIO[6]	E18	IO,PU	MSIO	NC	F1: MSIO data input #2; F2: I2S WCLK in; F3:General purpose pin #6
MSIO_DIN[3]/CIR_IN/GPIO[7]	E19	IO,PU	MSIO	NC	F1: MSIO data input #3; F2: CIR in; F3:General purpose pin #7
MSIO_DIN[4]/I2S_BCLK_IN/GPIO[8]	E20	IO,PU	MSIO	NC	F1: MSIO data input #4; F2: I2S BCLK in; f3:General purpose pin #8
MSIO_DIN[5]/SPDIF_IN/GPIO[9]	F20	IO,PU	MSIO	NC	F1: MSIO data input #5; F2: SPDIF in; f3:General purpose pin #9
MSIO_DOUT[0]/UART_OUT/GPIO[10]	F19	IO,PU	MSIO	NC	F1: MSIO data output #0; F2: UART out; F3:General purpose pin #10
MSIO_DOUT[1]/I2S_DOUT/GPIO[11]	F18	IO,PU	MSIO	NC	F1: MSIO data output #1; F2: I2S data out; F3:General purpose pin #11
MSIO_DOUT[2]/I2S_WCLK_OUT/GPIO[12]	F17	IO,PU	MSIO	NC	F1: MSIO data output #2; F2: I2S WCLK out; F3:General purpose pin #12
MSIO_DOUT[3]/CIR_OUT/GPIO[13]	G17	IO,PU	MSIO	NC	F1: MSIO data output #3; F2: CIR out; f3:General purpose pin #13
MSIO_DOUT[4]/I2S_BCLK_OUT/GPIO[14]	G18	IO,PU	MSIO	NC	F1: MSIO data output #4; F2: I2S BCLK out; f3:General purpose pin #14
MSIO_DOUT[5]/SPDIF_OUT/GPIO[15]	G19	IO,PU	MSIO	NC	F1: MSIO data output #5; F2: SPDIF out; f3:General purpose pin #15
POR_BYPASS	C20	Input	MISC	Must use	Power on reset bypass; PD '0'- POR Enabled; PU '1'-POR Disabled
QVDD25	C17	N/A	FU	GND	Reserved. Must be tied to ground

Signal Name	Ball#	Pad Type	I/F category	If Not Used	Functional Description
RCB_REFCLK0_M	W1	AI	MISC	If XO25M_SEL=1 short to VDD18	F1: 125MHz LVDS reference Clock (N); F2: 1.2V dc (see application notes on single ended application for this pin).
RCB_REFCLK0_P	W2	AI	MISC	If XO25M_SEL=1 short to VDD18	F1: 125MHz LVDS reference Clock (P); F2: 125MHz Single-ended reference clock
RESET_IN	B20	Input	MISC	4.7K PU	VS2310 Tx Reset In (Active only when POR_BYPASS=1)
RESET_N	D15	AIO	MISC	WPU	Power on reset bi-directional pin (open drain). 4.7 KOhm PU resistor to AVDD33 and 1nF capacitor to GND close to the pin are needed when active (POR_BYPASS=0)
SGMPHY_CKN	J2	AO	ETH SGMII	NC	SGMII PHY clock (N)
SGMPHY_CKP	J1	AO	ETH SGMII	NC	SGMII PHY clock (P)
SGMPHY_RXN	F2	AI	ETH SGMII	NC	SGMII PHY receive data (N)
SGMPHY_RXP	F1	AI	ETH SGMII	NC	SGMII PHY receive data (P)
SGMPHY_TXN	H2	AO	ETH SGMII	NC	SGMII PHY transmit data (N)
SGMPHY_TXP	H1	AO	ETH SGMII	NC	SGMII PHY transmit data (P)
TCK	M4	Input,PU	JTAG	NC	JTAG
TDI	T4	Input,PU	JTAG	NC	JTAG
TDO	R4	O3State	JTAG	NC	JTAG
TMS	P4	Input,PU	JTAG	NC	JTAG
TRST	N4	Input,PD	JTAG	1KPD	JTAG
USB_DM	R19	AIO	USB	NC	DM pin of the USB connector (IO)
USB_DP	R20	AIO	USB	NC	DP pin of the USB connector (IO)
USB_DRVVBUS	M18	Output	USB	NC	VBUS charge pump control
USB_ID	T17	AIO, PU	USB	NC	Identification (ID) pin of the USB connector. '1' indicates that VS2310 is connected to a host (USBH mode). '0' indicates that VS2310 is connected to a device (USBD mode).

Signal Name	Ball#	Pad Type	I/F category	If Not Used	Functional Description
USB_TXR_RKL	P18	AIO	USB	Must Use	Reference resistor. Should be tied to a 44.2 Ohm (1% tolerance) pull down resistor.
USB_VBUS	R17	AIO	USB	NC	VBUS pin of the USB connector
USB_XI	N20	XTAL	USB	NC	USB 12MHz Crystal clock input
USB_XO	N19	XTAL	USB	NC	USB 12MHz Crystal clock output
WAKEUP_IN	Y3	Input,PU	MISC	NC	Wakeup Input (reserved for future use)
WAKEUP_OUT_ST9	W3	IO	MISC	10K PD	Wakeup Output (reserved for future use);ST: strap pin #9
XO25M_SEL	V3	Input,PD	MISC	1K PD	Reference clock source select: '1' – 25MHz reference clock, crystal or LVCMOS oscillator; '0'- 125MHz reference clock through RCB_REFCLK0_P/M pins **NOTE THAT 25MHz CLOCK IS FUTURE USE ONLY**
XO25MHZ_XIN	Y2	XTAL	MISC	If XO25M_SEL =0 short to GND	25MHz Crystal clock or LVCMOS oscillator input **NOTE THAT 25MHz CLOCK IS FUTURE USE ONLY**
XO25MHZ_XOUT	Y1	XTAL	MISC	NC	25MHz Crystal clock output **NOTE THAT 25MHz CLOCK IS FUTURE USE ONLY**

2.3.1.2 Tx Non-Functional Signals

Table 6: VS2310TX Non-functional Signal Table

Symbol	Type	Description	Ball Numbers
NC	Non-connected balls	Reserved.	M17, V6, V7, U2, U1, U3
FU_C19	Future Use	Reserved. Must be tied to 3.3V external 1K pullup resistor.	C19
FU_V1	JTAG	TEST_MODE_1. Must be tied to external weak pulldown resistor (27.4K).	V1

Symbol	Type	Description	Ball Numbers
FU_V2	JTAG	TEST_MODE_0. Must be tied to external weak pulldown resistor (27.4K).	V2
FU_D19	Future Use	Reserved. Must be tied to external weak pulldown resistor (27.4K).	D19
VDD	1.0 V digital supply	1.0 V Digital supply	F6, F7, F8, F9, F10, F11, F12, F13, F14, F15, G15, H15, J15, K15, L15, M15, N15, P15, R10, R11, R12, R13, R14, R15
VDD33V	3.3 V supply signals	3.3 V digital supply	G6, H6, J6, K6, L6, M6, N6, P6, R6, R7, R8, R9
AVDD10	1.0 V analog supply signals	1.0 V analog supply	C18, D16, D18, M19, N18, P17, R18, T18, V17, V18, V19, V20
AVDD18	1.8 V analog supply signals	1.8 V analog supply	C13, C15, C16, V5, V8, V9, V10
AVDD33	3.3 V analog supply signals	3.3 V analog supply	C9, C11, V12, V13, V15, V16
AVDD33_TERM	3.3 V termination supply	3.3 V termination supply	V14
VSS	Ground signals	Ground	A1, A20, C10, C14, D13, D17, E1, E2, G1, G2, G7, G8, G9, G10, G11, G12, G13, G14, H7, H8, H9, H10, H11, H12, H13, H14, J7, J8, J9, J10, J11, J12, J13, J14, K7, K8, K9, K10, K11, K12, K13, K14, L7, L8, L9, L10, L11, L12, L13, L14, M7, M8, M9, M10, M11, M12, M13, M14, M20, N7, N8, N9, N10, N11, N12, N13, N14, N17, P7, P8, P9, P10, P11, P12, P13, P14, P19, P20, T19, T20, W5, W8, W11, W12, W14, W16, W18, W20, Y5, Y8, Y11, Y12, Y14, Y16, Y18, Y20

2.3.1.3 Tx Bias Resistors

Bias resistors are used to set an internal bias reference current and should be placed as close as possible to their BGA ball.

Table 7: Reference Resistor Values in VS2310TX

Pin Name	Ball #	Resistor Value [ohms]	PU/PD
HDSRC_REXT_H	V11	4.53K	PD to VSS
HDMIDES_RREF	U15	12K	PU to AVDD33
HDII_CB_RTT_EXRES	D14	1K	PD to VSS
USB_TXR_RKL	P18	44.2	PD to VSS

2.3.1.4 VS2310TX Ball Diagram (Top View)

Matrix	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	Matrix
A	VSS	HDIO_LVDSDn[7]	HDIO_LVDSDn[6]	HDIO_LVDSDn[5]	HDIO_LVDSDn[4]	HDIO_LVDS_CKN	HDIO_LVDSDn[3]	HDIO_LVDSDn[2]	HDIO_LVDSDn[1]	HDIO_LVDSDn[0]	HDII_LVDSDp[0]	HDII_LVDSDp[1]	HDII_LVDSDp[2]	HDII_LVDSDp[3]	HDII_LVDS_CKP	HDII_LVDSDp[4]	HDII_LVDSDp[5]	HDII_LVDSDp[6]	HDII_LVDSDp[7]	VSS	A
B	MII_RXD[1]_ST1	HDIO_LVDSDp[7]	HDIO_LVDSDp[6]	HDIO_LVDSDp[5]	HDIO_LVDSDp[4]	HDIO_LVDS_CKP	HDIO_LVDSDp[3]	HDIO_LVDSDp[2]	HDIO_LVDSDp[1]	HDIO_LVDSDp[0]	HDII_LVDSDn[0]	HDII_LVDSDn[1]	HDII_LVDSDn[2]	HDII_LVDSDn[3]	HDII_LVDS_CKN	HDII_LVDSDn[4]	HDII_LVDSDn[5]	HDII_LVDSDn[6]	HDII_LVDSDn[7]	RESET_N	B
C	MII_RXD[2]_ST2	MII_RXD[0]_ST0	MII_CRS/GPIO[3]	HDII_AUX_DAT[0]	HDII_AUX_READY	HDII_AUX_VALID	HDII_RDY	HDII_AUX_CLOCK	AVDD33	VSS	AVDD33	HDIO_RDY	AVDD18	VSS	AVDD18	AVDD18	QVDD25	AVDD10	FU_C19	POR_BYPASS	C
D	MII_RXD[3]_ST3	MII_RX_CLK	MII_RX_ERR_ST5	MII_RX_DV_ST4	HDII_AUX_DAT[3]	HDII_AUX_DAT[2]	HDIO_AUX_READY	HDIO_AUX_VALID	HDIO_AUX_DAT[0]	HDIO_AUX_DAT[1]	HDIO_AUX_DAT[2]	HDIO_AUX_CLOCK	VSS	HDII_CB_RTT_EXRES	RESET_N	AVDD10	VSS	AVDD10	FU_D19	MSIO_DIN[0]/UART_IN/GPIO[4]	D
E	VSS	VSS	MII_MDC	MII_COL/GPIO[2]													MSIO_DIN[1]/I2S_DIN/GPIO[5]	MSIO_DIN[2]/I2S_WCLK_IN/GPIO[6]	MSIO_DIN[3]/CIR_IN/GPIO[7]	MSIO_DIN[4]/I2S_BCLK_IN/GPIO[8]	E
F	SGMPHY_RXP	SGMPHY_RXN	MII_MDIO	MII_TX_EN		VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD		MSIO_DOUT[2]/I2S_WCLK_OUT/GPIO[12]	MSIO_DOUT[1]/I2S_DOUT/GPIO[11]	MSIO_DOUT[0]/UART_OUT/GPIO[10]	MSIO_DIN[5]/SPDIF_IN/GPIO[9]	F
G	VSS	VSS	MII_TX_ERR	MII_TXD[0]		VDD33V	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD		MSIO_DOUT[3]/CIR_OUT/GPIO[13]	MSIO_DOUT[4]/I2S_BCLK_OUT/GPIO[14]	MSIO_DOUT[5]/SPDIF_OUT/GPIO[15]	ST10	G
H	SGMPHY_TXP	SGMPHY_TXN	MII_TXD[1]	MII_TX_CLK		VDD33V	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD		GPIO[16]	GPIO[17]	GPIO[18]	GPIO[19]	H
J	SGMPHY_CKP	SGMPHY_CKN	MII_TXD[2]/GPIO[0]	MII_TXD[3]/GPIO[1]		VDD33V	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD		GPIO[20]/MSIO_DO[0]	GPIO[21]/MSIO_DO[1]	GPIO[22]/MSIO_DO[2]	GPIO[23]/MSIO_DO[3]	J
K	BT1120_D14	BT1120_D16	BT1120_D18	UCC_0		VDD33V	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD		GPIO[24]/MSIO_DO[4]	GPIO[25]/MSIO_DO[5]	GPIO[26]/MSIO_DO[6]	GPIO[27]/MSIO_DI[1]	K
L	BT1120_D12	BT1120_D17	BT1120_D19	UCC_1		VDD33V	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD		GPIO[28]/MSIO_DI[2]	GPIO[29]/MSIO_DI[3]	GPIO[30]/MSIO_DI[4]	GPIO[31]/MSIO_DI[5]	L
M	BT1120_D8	BT1120_D10	BT1120_D15	TCK		VDD33V	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD		NC_M17	USB_DRVVBUS	AVDD10	VSS	M
N	BT1120_D6	BT1120_D11	BT1120_D13	TRST		VDD33V	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD		VSS	AVDD10	USB_XO	USB_XI	N
P	BT1120_D4	BT1120_D7	BT1120_D9	TMS		VDD33V	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD		AVDD10	USB_TXR_RKL	VSS	VSS	P
R	BT1120_D2	BT1120_D3	BT1120_D5	TDO		VDD33V	VDD33V	VDD33V	VDD33V	VDD	VDD	VDD	VDD	VDD	VDD		USB_VBUS	AVDD10	USB_DM	USB_DP	R
T	BT1120_D0	BT1120_D1	BT1120_CLK	TDI													USB_ID	AVDD10	VSS	VSS	T
U	NC_U1	NC_U2	NC_U3	EE_MOST7	DBG_TXD_ST6	I2C1_SDA_MST	I2C1_SCL_MST	DBG_RXD	CFG_SCL	CFG_SDA	I2C_SDA_SLV	I2C_SCL_SLV	I2C2_SDA_MST	I2C2_SCL_MST	HDMII_RREF	HDMII_DDC_SCL	HDMII_DDC_SDA	HDMII_HPD	HDMII_CEC	HDMII_5V	U
V	FU_V1	FU_V2	XO25M_SEL	EE_SCL_SCK	AVDD18	NC_V6	NC_V7	AVDD18	AVDD18	AVDD18	HDSRC_REXT_H	AVDD33	AVDD33	AVDD33_TERM	AVDD33	AVDD33	AVDD10	AVDD10	AVDD10	AVDD10	V
W	RCB_REFCLK0_M	RCB_REFCLK0_P	WAKEUP_OUT_ST9	EE_CS_ST8	VSS	HDSRCp[0]	HDSRCp[1]	VSS	HDSRCp[2]	HDSRCp[3]	VSS	VSS	HDMII_TMDSCLKP	VSS	HDMII_TMDSDATAp[0]	VSS	HDMII_TMDSDATAp[1]	VSS	HDMII_TMDSDATAp[2]	VSS	W
Y	XO25MHZ_XOUT	XO25MHZ_XIN	WAKEUP_IN	EE_SDA_MI	VSS	HDSRCn[0]	HDSRCn[1]	VSS	HDSRCn[2]	HDSRCn[3]	VSS	VSS	HDMII_TMDSCLKN	VSS	HDMII_TMDSDATAn[0]	VSS	HDMII_TMDSDATAn[1]	VSS	HDMII_TMDSDATAn[2]	VSS	Y
Matrix	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	Matrix

Figure 11: VS2310TX Ball Diagram

2.3.2 VS2000TX Signal Description

Table 8 below provides information on each pin of the VS2000TX chip. Pins with more than one function use the following convention:

- F1: <function 1 description>
- F2: <function 2 description>
- ST: <strap function description>

Selecting between functions of multi-functional pins is performed by either using VS2000 chip parameters or asserting strap pins. For more details, refer to the section in Chapter 6 that corresponds with the relevant interface category.

2.3.2.1 Tx Functional Signals

Table 8: VS2000TX Functional Signal Table

Signal Name	Ball#	Pad Type	I/f category	If Not Used	Functional Description
BT1120_D19	L3	Input, PD	BT.1120	NC	BT.1120 – Input Chroma bit 9
BT1120_D18	K3	Input, PD	BT.1120	NC	BT.1120 – Input Chroma bit 8
BT1120_D17	L2	Input, PD	BT.1120	NC	BT.1120 – Input Chroma bit 7
BT1120_D16	K2	Input, PD	BT.1120	NC	BT.1120 – Input Chroma bit 6
BT1120_D15	M3	Input, PD	BT.1120	NC	BT.1120 – Input Chroma bit 5
BT1120_D14	K1	Input, PD	BT.1120	NC	BT.1120 – Input Chroma bit 4
BT1120_D13	N3	Input, PD	BT.1120	NC	BT.1120 – Input Chroma bit 3
BT1120_D12	L1	Input, PD	BT.1120	NC	BT.1120 – Input Chroma bit 2
BT1120_D11	N2	Input, PD	BT.1120	NC	BT.1120 – Input Chroma bit 1
BT1120_D10	M2	Input, PD	BT.1120	NC	BT.1120 – Input Chroma bit 0
BT1120_D9	P3	Input, PD	BT.1120	NC	BT.1120 – Input Luminance bit 9
BT1120_D8	M1	Input, PD	BT.1120	NC	BT.1120 – Input Luminance bit 8
BT1120_D7	P2	Input, PD	BT.1120	NC	BT.1120 – Input Luminance bit 7
BT1120_D6	N1	Input, PD	BT.1120	NC	BT.1120 – Input Luminance bit 6
BT1120_D5	R3	Input, PD	BT.1120	NC	BT.1120 – Input Luminance bit 5
BT1120_D4	P1	Input, PD	BT.1120	NC	BT.1120 – Input Luminance bit 4
BT1120_D3	R2	Input, PD	BT.1120	NC	BT.1120 – Input Luminance bit 3
BT1120_D2	R1	Input, PD	BT.1120	NC	BT.1120 – Input Luminance bit 2
BT1120_D1	T2	Input, PD	BT.1120	NC	BT.1120 – Input Luminance bit 1
BT1120_D0	T1	Input, PD	BT.1120	NC	BT.1120 – Input Luminance bit 0
BT1120_CLK	T3	Input, PD	BT.1120	NC	BT.1120 – Input clock
UCC_0	K4	O3State	BT.1120	NC	BT.1120 – HDcctv Upstream Communication Channel 0
UCC_1	L4	O3State	BT.1120	NC	BT.1120 – HDcctv Upstream Communication Channel 1
CFG_SCL	U9	IO,PU	DEBUG	NC	Host interface I2C clock Signal
CFG_SDA	U10	IO,PU	DEBUG	NC	Host interface I2C data Signal
DBG_RXD	U8	input,PU	DEBUG	NC	Debug Receive Data (I)
DBG_TXD_ST6	U5	IO,PU	DEBUG	1K PD	Debug Transmit Data (O);ST: strap bit #6
EE_CS_ST8	W4	IO,PD	FLASH	Must use	SPI FLASH chip select;ST: strap bit #8
EE_MO_ST7	U4	IO,PD	FLASH	1K PU	SPI FLASH MO (master Out);ST: strap bit #7

Signal Name	Ball#	Pad Type	I/f category	If Not Used	Functional Description
EE_SCL_SCK	V4	IO,PU	FLASH	Must use	Clock for Both I2C and SPI FLASHs (O)
EE_SDA_MI	Y4	IO,PU	FLASH	Must use	I2C FLASH SDA or SPI FLASH MI (Master In)
GPIO[16]	H17	IO,PU	GPIO	4.7K-10K PD	General purpose IO bit #16 (IO). Must be tied to external 4.7K-10K pulldown resistor in all applications.
GPIO[17]	H18	IO,PU	GPIO	4.7K-10K PD	General purpose IO bit #17 (IO). Must be tied to external 4.7K-10K pulldown resistor in all applications.
GPIO[18]	H19	IO,PU	GPIO	NC	General purpose IO bit #18 (IO)
GPIO[19]	H20	IO,PU	GPIO	NC	General purpose IO bit #19 (IO)
GPIO[20]/MSIO_DO[0]	J17	IO,PU	GPIO	NC	F1: General purpose IO bit #20 (IO); F2: MSIO data output bit #0
GPIO[21]/MSIO_DO[1]	J18	IO,PU	GPIO	NC	F1: General purpose IO bit #21 (IO); F2: MSIO data output bit #1
GPIO[22]/MSIO_DO[2]	J19	IO,PU	GPIO	NC	F1: General purpose IO bit #22 (IO); F2: MSIO data output bit #2
GPIO[23]/MSIO_DO[3]	J20	IO,PU	GPIO	NC	F1: General purpose IO bit #23 (IO); F2: MSIO data output bit #3
GPIO[24]/MSIO_DO[4]	K17	IO,PU	GPIO	NC	F1: General purpose IO bit #24 (IO); F2: MSIO data output bit #4
GPIO[25]/MSIO_DO[5]	K18	IO,PU	GPIO	NC	F1: General purpose IO bit #25 (IO); F2: MSIO data output bit #5
GPIO[26]/MSIO_DI[0]	K19	IO,PU	GPIO	NC	F1: General purpose IO bit #26 (IO); F2: MSIO data input bit #0
GPIO[27]/MSIO_DI[1]	K20	IO,PU	GPIO	NC	F1: General purpose IO bit #27 (IO); F2: MSIO data input bit #1
GPIO[28]/MSIO_DI[2]	L17	IO,PU	GPIO	NC	F1: General purpose IO bit #28 (IO); F2: MSIO data input bit #2
GPIO[29]/MSIO_DI[3]	L18	IO,PU	GPIO	NC	F1: General purpose IO bit #29 (IO); F2: MSIO data input bit #3
GPIO[30]/MSIO_DI[4]	L19	IO,PU	GPIO	NC	F1: General purpose IO bit #30 (IO); F2: MSIO data input bit #4
GPIO[31]/MSIO_DI[5]	L20	IO,PU	GPIO	NC	F1: General purpose IO bit #31 (IO); F2: MSIO data input bit #5
HDII_CB_RTT_EXRES	D14	AIO	HDI	Must Use	HDI central bais external resistor; Should be tied to a 1KOhm (1% tolerance) pull down resistor.

Signal Name	Ball#	Pad Type	I/f category	If Not Used	Functional Description
HDMII_5V	U20	Input	HDMI	GND	HDMI Rx 5V power signal input
HDMII_CEC	U19	IO	HDMI	27K PU	HDMI Rx CEC bus
HDMII_DDC_SCL	U16	IO	HDMI	47K PU	HDMI Rx DDC I2C clock
HDMII_DDC_SDA	U17	IO	HDMI	NC	HDMI Rx DDC I2C data
HDMII_HPD	U18	IO	HDMI	WPU	HDMI Rx hot plug detect output
HDMII_RREF	U15	AIO	HDMI	Must Use	HDMI current Source Resistor; Should be tied to a 12 KOhm (1% tolerance) pull up resistor, AVDD33
HDMII_TMDSCLKN	Y13	AI	HDMI	NC	HDMI Rx TMDS clock lane (N)
HDMII_TMDSCLKP	W13	AI	HDMI	NC	HDMI Rx TMDS clock lane (P)
HDMII_TMDSDATAn[0]	Y15	AI	HDMI	NC	HDMI Rx TMDS data lane 0 (N)
HDMII_TMDSDATAn[1]	Y17	AI	HDMI	NC	HDMI Rx TMDS data lane 1 (N)
HDMII_TMDSDATAn[2]	Y19	AI	HDMI	NC	HDMI Rx TMDS data lane 2 (N)
HDMII_TMDSDATAp[0]	W15	AI	HDMI	NC	HDMI Rx TMDS data lane 0 (P)
HDMII_TMDSDATAp[1]	W17	AI	HDMI	NC	HDMI Rx TMDS data lane 1 (P)
HDMII_TMDSDATAp[2]	W19	AI	HDMI	NC	HDMI Rx TMDS data lane 2 (P)
HDSRC_REXT_H	V11	AIO	HDBaseT	Must Use	HDBT current Source Resistor. Should be tied to a 4.53 KOhm (1% tolerance) pull down resistor.
HDSRCn[0]	Y6	AIO	HDBaseT	NC	HDBaseT Transceive Channel 0 (N)
HDSRCn[1]	Y7	AIO	HDBaseT	NC	HDBaseT Transceive Channel 1 (N)
HDSRCn[2]	Y9	AIO	HDBaseT	NC	HDBaseT Transceive Channel 2 (N)
HDSRCn[3]	Y10	AIO	HDBaseT	NC	HDBaseT Transceive Channel 3 (N)
HDSRCp[0]	W6	AIO	HDBaseT	NC	HDBaseT Transceive Channel 0 (P)
HDSRCp[1]	W7	AIO	HDBaseT	NC	HDBaseT Transceive Channel 1 (P)
HDSRCp[2]	W9	AIO	HDBaseT	NC	HDBaseT Transceive Channel 2 (P)
HDSRCp[3]	W10	AIO	HDBaseT	NC	HDBaseT Transceive Channel 3 (P)
I2C_SCL_SLV	U12	IO,PU	I2C	NC	Slave I2C2 interface, clock line, connect to external master
I2C_SDA_SLV	U11	IO,PU	I2C	NC	Slave I2C2 interface, data line, connect to external master
I2C1_SCL_MST	U7	IO,PU	I2C	NC	Master I2C interface 1, clock line, connect to external slave
I2C1_SDA_MST	U6	IO,PU	I2C	NC	Master I2C interface 1, data line, connect to external slave

Signal Name	Ball#	Pad Type	I/f category	If Not Used	Functional Description
I2C2_SCL_MST	U14	IO,PU	I2C	NC	Master I2C interface 2, clock line, connect to external slave
I2C2_SDA_MST	U13	IO,PU	I2C	NC	Master I2C interface 2, data line, connect to external slave
MII_COL/GPIO[2]	E4	IO,PU	ETH	NC	F1: MII PHY Collision Detect; F2: General Purpose IO Bit #2
MII_CRS/GPIO[3]	C3	IO,PU	ETH	NC	F1: MII PHY Carrier Sense ;F2: General Purpose IO Bit #3
MII_MDC	E3	Input,PU	ETH	NC	MII Slave Management Clock
MII_MDIO	F3	IO,PU	ETH	NC	MII Slave Management Data
MII_RX_CLK	D2	IO	ETH	1K PD	F1: MII PHY Receive Clock; F2: RMII 50MHz output clock
MII_RX_DV_ST4	D4	IO,PU	ETH	1K PD	MII/RMII PHY receive Data Valid; ;ST: Strap bit #4
MII_RX_ERR_ST5	D3	IO,PD	ETH	1K PU with jumper	MII PHY Receive Error;ST: Strap bit #5
MII_RXD[0]_ST0	C2	IO,PD	ETH	NC	MII/RMII PHY Receive Data Bit 0; ;ST: Strap bit #0
MII_RXD[1]_ST1	B1	IO,PD	ETH	NC	MII/RMII PHY Receive Data Bit 1; ;ST: Strap bit #1
MII_RXD[2]_ST2	C1	IO,PD	ETH	NC	MII PHY Receive Data Bit 2;ST: Strap bit #2
MII_RXD[3]_ST3	D1	IO,PU	ETH	1KPD	MII PHY Receive Data Bit 3;ST: Strap bit #3
MII_TX_CLK	H4	IO,PU	ETH	1KPD	F1: MII PHY Transmit Clock; F2: RMII REF_CLK input
MII_TX_EN	F4	Input	ETH	GND	MII/RMII PHY Transmit Enable
MII_TX_ERR	G3	Input,PU	ETH	GND	MII PHY Transmit Error
MII_TXD[0]	G4	Input,PU	ETH	NC	MII/RMII PHY Transmit Data Bit 0
MII_TXD[1]	H3	Input,PU	ETH	NC	MII/RMII PHY Transmit Data Bit 1
MII_TXD[2]/GPIO[0]	J3	IO,PU	ETH	NC	F1: MII PHY Transmit Data Bit 2 (I); F2: General Purpose IO Bit #0
MII_TXD[3]/GPIO[1]	J4	IO,PU	ETH	NC	F1: MII PHY Transmit Data Bit 3 (I); F2: General Purpose IO Bit #1
ST10	G20	IO	MSIO	1K PU	Strap pin #10
MSIO_DIN[0]/UART_IN/GPIO[4]	D20	IO,PU	MSIO	NC	F1: MSIO data input #0; F2: UART in ; F3: General purpose pin #4

Signal Name	Ball#	Pad Type	I/f category	If Not Used	Functional Description
MSIO_DIN[1]/I2S_DIN/GPIO[5]	E17	IO,PU	MSIO	NC	F1: MSIO data input #1; F2: I2S data in; F3:General purpose pin #5
MSIO_DIN[2]/I2S_WCLK_IN/GPIO[6]	E18	IO,PU	MSIO	NC	F1: MSIO data input #2; F2: I2S WCLK in; F3:General purpose pin #6
MSIO_DIN[3]/CIR_IN/GPIO[7]	E19	IO,PU	MSIO	NC	F1: MSIO data input #3; F2: CIR in; F3:General purpose pin #7
MSIO_DIN[4]/I2S_BCLK_IN/GPIO[8]	E20	IO,PU	MSIO	NC	F1: MSIO data input #4; F2: I2S BCLK in; f3:General purpose pin #8
MSIO_DIN[5]/SPDIF_IN/GPIO[9]	F20	IO,PU	MSIO	NC	F1: MSIO data input #5; F2: SPDIF in; f3:General purpose pin #9
MSIO_DOUT[0]/UART_OUT/GPIO[10]	F19	IO,PU	MSIO	NC	F1: MSIO data output #0; F2: UART out; F3:General purpose pin #10
MSIO_DOUT[1]/I2S_DOUT/GPIO[11]	F18	IO,PU	MSIO	NC	F1: MSIO data output #1; F2: I2S data out; F3:General purpose pin #11
MSIO_DOUT[2]/I2S_WCLK_OUT/GPIO[12]	F17	IO,PU	MSIO	NC	F1: MSIO data output #2; F2: I2S WCLK out; F3:General purpose pin #12
MSIO_DOUT[3]/CIR_OUT/GPIO[13]	G17	IO,PU	MSIO	NC	F1: MSIO data output #3; F2: CIR out; f3:General purpose pin #13
MSIO_DOUT[4]/I2S_BCLK_OUT/GPIO[14]	G18	IO,PU	MSIO	NC	F1: MSIO data output #4; F2: I2S BCLK out; f3:General purpose pin #14
MSIO_DOUT[5]/SPDIF_OUT/GPIO[15]	G19	IO,PU	MSIO	NC	F1: MSIO data output #5; F2: SPDIF out; f3:General purpose pin #15
POR_BYPASS	C20	Input	MISC	Must use	Power on reset bypass; PD '0'- POR Enabled; PU '1'-POR Disabled
QVDD25	C17	N/A	FU	GND	Reserved. Must be tied to ground
RCB_REFCLK0_M	W1	AI	MISC	If XO25M_SEL=1 short to VDD18	F1: 125MHz LVDS reference Clock (N); F2: 1.2V dc (see application notes on single ended application for this pin).
RCB_REFCLK0_P	W2	AI	MISC	If XO25M_SEL=1 short to VDD18	F1: 125MHz LVDS reference Clock (P); F2: 125MHz Single-ended reference clock
RESET_IN	B20	Input	MISC	4.7K PU	VS2310 Tx Reset In (Active only when POR_BYPASS=1)

Signal Name	Ball#	Pad Type	I/f category	If Not Used	Functional Description
RESET_N	D15	AIO	MISC	WPU	Power on reset bi-directional pin (open drain). 4.7 KOhm PU resistor to AVDD33 and 1nF capacitor to GND close to the pin are needed when active (POR_BYPASS=0)
SGMPHY_CKN	J2	AO	ETH SGMII	NC	SGMII PHY clock (N)
SGMPHY_CKP	J1	AO	ETH SGMII	NC	SGMII PHY clock (P)
SGMPHY_RXN	F2	AI	ETH SGMII	NC	SGMII PHY receive data (N)
SGMPHY_RXP	F1	AI	ETH SGMII	NC	SGMII PHY receive data (P)
SGMPHY_TXN	H2	AO	ETH SGMII	NC	SGMII PHY transmit data (N)
SGMPHY_TXP	H1	AO	ETH SGMII	NC	SGMII PHY transmit data (P)
TCK	M4	Input,PU	FU	NC	Future use.
TDI	T4	Input,PU	FU	NC	Future use.
TDO	R4	O3State	FU	NC	Future use.
TMS	P4	Input,PU	FU	NC	Future use.
TRST	N4	Input,PD	FU	1KPD	Future use.
USB_TXR_RKL	P18	AIO		Must Use	Reference resistor. Should be tied to a 44.2 Ohm (1% tolerance) pull down resistor.
WAKEUP_IN	Y3	Input,PU	MISC	NC	Wakeup Input (reserved for future use)
WAKEUP_OUT_ST9	W3	IO	MISC	10K PD	Wakeup Output (reserved for future use);ST: strap pin #9
XO25M_SEL	V3	Input,PD	MISC	1K PD	Reference clock source select:'1' – 25MHz reference clock, crystal or LVCMOS oscillator; '0'- 125MHz reference clock through RCB_REFCLK0_P/M pins **NOTE THAT 25MHz CLOCK IS FUTURE USE ONLY**
XO25MHZ_XIN	Y2	XTAL	MISC	If XO25M_SEL =0 short to GND	25MHz Crystal clock or LVCMOS oscillator input **NOTE THAT 25MHz CLOCK IS FUTURE USE ONLY**
XO25MHZ_XOUT	Y1	XTAL	MISC	NC	25MHz Crystal clock output **NOTE THAT 25MHz CLOCK IS FUTURE USE ONLY**

2.3.2.2 Tx Non-Functional Signals

Table 9: VS2000TX Non-functional Signal Table

Symbol	Type	Description	Ball Numbers
NC	Non-connected balls	Non-Connected Balls	R19, R20, M18, T17, R17, N20, N19, M17, V6, V7, U2, U1, U3
NS	Not supported	Not Supported	B2, B3, B4, B5, B7, B8, B9, B10, A2, A3, A4, A5, A7, A8, A9, A10, A6, B6, C12, D7, A19, A18, A17, A16, A14, A13, A12, A11, B19, B18, B17, B16, B14, B13, B12, B11, A15, B15, C7, D6, D5, C4, C8, C6
NS	Not supported	Not supported – must be connected to GND	D11, D10, D9, D12, D8, C5
FU_C19	Future Use	Reserved. Must be tied to 3.3V external 1K pullup resistor.	C19
FU_D19	Future Use	Reserved. Must be tied to external weak pull-down resistor (27.4K).	D19
FU_V1	Future Use	Reserved. Must be tied to external weak pull-down resistor (27.4K).	V1
FU_V2	Future Use	Reserved. Must be tied to ground.	V2
VDD	1.0 V digital supply	1.0 V digital supply	F6, F7, F8, F9, F10, F11, F12, F13, F14, F15, G15, H15, J15, K15, L15, M15, N15, P15, R10, R11, R12, R13, R14, R15
VDD33V	3.3 V supply signals	3.3 V supply signal	G6, H6, J6, K6, L6, M6, N6, P6, R6, R7, R8, R9
AVDD10	1.0 V analog supply signals	1.0 V analog supply signal	C18, D16, D18, M19, N18, P17, R18, T18, V17, V18, V19, V20
AVDD18	1.8 V analog supply signals	1.8 V analog supply signal	C13, C15, C16, V5, V8, V9, V10
AVDD33	3.3 V analog supply signals	3.3 V analog supply signal	C9, C11, V12, V13, V15, V16
AVDD33_TERM	3.3 V termination supply	3.3 V termination supply	V14

VSS	Ground signals	Ground signal	A1, A20, C10, C14, D13, D17, E1, E2, G1, G2, G7, G8, G9, G10, G11, G12, G13, G14, H7, H8, H9, H10, H11, H12, H13, H14, J7, J8, J9, J10, J11, J12, J13, J14, K7, K8, K9, K10, K11, K12, K13, K14, L7, L8, L9, L10, L11, L12, L13, L14, M7, M8, M9, M10, M11, M12, M13, M14, M20, N7, N8, N9, N10, N11, N12, N13, N14, N17, P7, P8, P9, P10, P11, P12, P13, P14, P19, P20, T19, T20, W5, W8, W11, W12, W14, W16, W18, W20, Y5, Y8, Y11, Y12, Y14, Y16, Y18, Y20

2.3.2.3 Tx Bias Resistors

Bias resistors are used to set an internal bias reference current and should be placed as close as possible to their BGA ball.

Table 10: Reference Resistor Values in VS2000TX

Pin Name	Ball #	Resistor Value [ohms]	PU/PD
HDSRC_REXT_H	V11	4.53K	PD to VSS
HDMIDES_RREF	U15	12K	PU to AVDD33
HDII_CB_RTT_EXRES	D14	1K	PD to VSS
USB_TXR_RKL	P18	44.2	PD to VSS

2.3.2.4 VS2000TX Ball Diagram (Top View)

Matrix	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	Matrix
A	VSS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	VSS	A
B	MII_RXD[1]_ST1	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	RESET_N	B
C	MII_RXD[2]_ST2	MII_RXD[0]_ST0	MII_CRS/GPIO[3]	NS	NS	NS	NS	NS	AVDD33	VSS	AVDD33	NS	AVDD18	VSS	AVDD18	AVDD18	QVDD25	AVDD10	FU_C19	POR_BYPASS	C
D	MII_RXD[3]_ST3	MII_RX_CLK	MII_RX_ERR_ST5	MII_RX_DV_ST4	NS	NS	NS	NS	NS	NS	NS	NS	VSS	HDII_CB_RTT_EXRES	RESET_N	AVDD10	VSS	AVDD10	FU_D19	MSIO_DIN[0]/UART_IN/GPIO[4]	D
E	VSS	VSS	MII_MDC	MII_COL/GPIO[2]													MSIO_DIN[1]/I2S_DIN/GPIO[5]	MSIO_DIN[2]/I2S_WCLK_IN/GPIO[6]	MSIO_DIN[3]/CIR_IN/GPIO[7]	MSIO_DIN[4]/I2S_BCLK_IN/GPIO[8]	E
F	SGMPHY_RXP	SGMPHY_RXN	MII_MDIO	MII_TX_EN		VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD		MSIO_DOUT[2]/I2S_WCLK_OUT/GPIO[12]	MSIO_DOUT[1]/I2S_DOUT/GPIO[11]	MSIO_DOUT[0]/UART_OUT/GPIO[10]	MSIO_DIN[5]/SPDIF_IN/GPIO[9]	F
G	VSS	VSS	MII_TX_ERR	MII_TXD[0]		VDD33V	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD		MSIO_DOUT[3]/CIR_OUT/GPIO[13]	MSIO_DOUT[4]/I2S_BCLK_OUT/GPIO[14]	MSIO_DOUT[5]/SPDIF_OUT/GPIO[15]	ST10	G
H	SGMPHY_TXP	SGMPHY_TXN	MII_TXD[1]	MII_TX_CLK		VDD33V	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD		GPIO[16]	GPIO[17]	GPIO[18]	GPIO[19]	H
J	SGMPHY_CKP	SGMPHY_CKN	MII_TXD[2]/GPIO[0]	MII_TXD[3]/GPIO[1]		VDD33V	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD		GPIO[20]/MSIO_DO[0]	GPIO[21]/MSIO_DO[1]	GPIO[22]/MSIO_DO[2]	GPIO[23]/MSIO_DO[3]	J
K	BT1120_D14	BT1120_D16	BT1120_D18	UCC_0		VDD33V	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD		GPIO[24]/MSIO_DO[4]	GPIO[25]/MSIO_DO[5]	GPIO[26]/MSIO_DI[0]	GPIO[27]/MSIO_DI[1]	K
L	BT1120_D12	BT1120_D17	BT1120_D19	UCC_1		VDD33V	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD		GPIO[28]/MSIO_DI[2]	GPIO[29]/MSIO_DI[3]	GPIO[30]/MSIO_DI[4]	GPIO[31]/MSIO_DI[5]	L
M	BT1120_D8	BT1120_D10	BT1120_D15	TCK		VDD33V	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD		NC	NC	AVDD10	VSS	M
N	BT1120_D6	BT1120_D11	BT1120_D13	TRST		VDD33V	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD		VSS	AVDD10	NC	NC	N
P	BT1120_D4	BT1120_D7	BT1120_D9	TMS		VDD33V	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD		AVDD10	USB_TXR_RKL	VSS	VSS	P
R	BT1120_D2	BT1120_D3	BT1120_D5	TDO		VDD33V	VDD33V	VDD33V	VDD33V	VDD	VDD	VDD	VDD	VDD	VDD		NC	AVDD10	NC	NC	R
T	BT1120_D0	BT1120_D1	BT1120_CLK	TDI													NC	AVDD10	VSS	VSS	T
U	NC_U1	NC_U2	NC_U3	EE_MOST7	DBG_TXD_ST6	I2C1_SDA_MST	I2C1_SCL_MST	DBG_RXD	CFG_SCL	CFG_SDA	I2C_SDA_SLV	I2C_SCL_SLV	I2C2_SDA_MST	I2C2_SCL_MST	HDMII_RREF	HDMII_DDC_SCL	HDMII_DDC_SDA	HDMII_HPD	HDMII_CEC	HDMII_5V	U
V	FU_V1	FU_V2	XO25M_SEL	EE_SCL_SCK	AVDD18	NC	NC	AVDD18	AVDD18	AVDD18	HDSRC_REXT_H	AVDD33	AVDD33	AVDD33_TERM	AVDD33	AVDD33	AVDD10	AVDD10	AVDD10	AVDD10	V
W	RCB_REFCLK0_M	RCB_REFCLK0_P	WAKEUP_OUT_ST9	EE_CS_ST8	VSS	HDSRCp[0]	HDSRCp[1]	VSS	HDSRCp[2]	HDSRCp[3]	VSS	VSS	HDMII_TMDSCLKP	VSS	HDMII_TMDSDATAp[0]	VSS	HDMII_TMDSDATAp[1]	VSS	HDMII_TMDSDATAp[2]	VSS	W
Y	XO25MHZ_XOUT	XO25MHZ_XIN	WAKEUP_IN	EE_SDA_MI	VSS	HDSRCn[0]	HDSRCn[1]	VSS	HDSRCn[2]	HDSRCn[3]	VSS	VSS	HDMII_TMDSCLKN	VSS	HDMII_TMDSDATAn[0]	VSS	HDMII_TMDSDATAn[1]	VSS	HDMII_TMDSDATAn[2]	VSS	Y
Matrix	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	Matrix

Figure 12: VS2000TX Ball Diagram

2.4 VS2310/VS2000 RX Signal Description

2.4.1 VS2310 RX Signal Description

This section provides information on each pin of the VS2310RX chip. Pins with more than one function use the following convention:

- F1: <function 1 description>
- F2: <function 2 description>
- ST: <strap function description>

Selecting between functions of multi-functional pins is performed by either using VS2310 chip parameters or asserting strap pins. For more details, refer to the section in Chapter 6 that corresponds with the relevant interface category.

2.4.1.1 Rx Functional Signals

Table 11: VS2310RX Functional Signal Table

Signal Name	Ball#	Pad Type	I/F category	If Not Used	Functional Description
BT1120_D19	K22	03State	BT.1120	NC	BT.1120 – Output Chroma bit 9
BT1120_D18	K21	03State	BT.1120	NC	BT.1120 – Output Chroma bit 8
BT1120_D17	K20	03State	BT.1120	NC	BT.1120 – Output Chroma bit 7
BT1120_D16	L22	03State	BT.1120	NC	BT.1120 – Output Chroma bit 6
BT1120_D15	L21	03State	BT.1120	NC	BT.1120 – Output Chroma bit 5
BT1120_D14	L20	03State	BT.1120	NC	BT.1120 – Output Chroma bit 4
BT1120_D13	M22	03State	BT.1120	NC	BT.1120 – Output Chroma bit 3
BT1120_D12	M21	03State	BT.1120	NC	BT.1120 – Output Chroma bit 2
BT1120_D11	M20	03State	BT.1120	NC	BT.1120 – Output Chroma bit 1
BT1120_D10	N22	03State	BT.1120	NC	BT.1120 – Output Chroma bit 0
BT1120_D9	N20	03State	BT.1120	NC	BT.1120 – Output Luminance bit 9
BT1120_D8	P22	03State	BT.1120	NC	BT.1120 – Output Luminance bit 8
BT1120_D7	P21	03State	BT.1120	NC	BT.1120 – Output Luminance bit 7
BT1120_D6	P20	03State	BT.1120	NC	BT.1120 – Output Luminance bit 6
BT1120_D5	R22	03State	BT.1120	NC	BT.1120 – Output Luminance bit 5
BT1120_D4	R21	03State	BT.1120	NC	BT.1120 – Output Luminance bit 4
BT1120_D3	R20	03State	BT.1120	NC	BT.1120 – Output Luminance bit 3
BT1120_D2	T22	03State	BT.1120	NC	BT.1120 – Output Luminance bit 2
BT1120_D1	T21	03State	BT.1120	NC	BT.1120 – Output Luminance bit 1
BT1120_D0	T20	03State	BT.1120	NC	BT.1120 – Output Luminance bit 0
BT1120_CLK	N21	03State	BT.1120	NC	BT.1120 – Output Clock

Signal Name	Ball#	Pad Type	I/F category	If Not Used	Functional Description
UCC_0	V6	Input	BT.1120	GND	HDcctv Upstream Communication Channel 0
UCC_1	V7	Input	BT.1120	GND	HDcctv Upstream Communication Channel 1
CFG_SCL	E3	IO	Debug	1K PD	Host interface I2C clock Signal
CFG_SDA	E4	IO	Debug	NC	Host interface I2C data Signal
DBG_RXD	E1	Input	Debug	3.3V 10K PU	Debug Receive Data (I)
DBG_TXD_ST6	E2	IO,PU	Debug	1K PD	Debug Transmit Data (O); ST: strap pin #6
EE_CS_ST8	G2	IO,PD	FLASH	NC	SPI FLASH chip select; ST: strap pin #8
EE_MO_ST7	G3	IO,PD	FLASH	1K PU	SPI FLASH MO (master Out); ST: strap pin #7
EE_SCL_SCK	F3	IO,PU	FLASH	Must use	Clock for Both I2C and SPI FLASHs (O)
EE_SDA_MI	F2	IO,PU	FLASH	Must use	I2C FLASH SDA or SPI FLASH MI (Master In)
GMII_MDC	K3	O3State	MAC (future use)	NC	MII Master Management Clock
GMII_MDIO	K2	IO	MAC (future use)	4.7K-10K PU	MII Master Management Data
GPIO[16]	J20	IO,PU	GPIO	4.7K-10K PD	General purpose IO bit #16 (IO). Must be tied to external 4.7K-10K pulldown resistor in all applications.
GPIO[17]	J22	IO,PU	GPIO	4.7K-10K PD	General purpose IO bit #17 (IO). Must be tied to external 4.7K-10K pulldown resistor in all applications.
GPIO[18]	J21	IO,PU	GPIO	NC	General purpose IO bit #18 (IO)
GPIO[19]	H20	IO,PU	GPIO	NC	General purpose IO bit #19 (IO)
GPIO[20]/MSIO_DO[0]	H22	IO,PU	GPIO	NC	F1: General purpose IO bit #20;F2: MSIO data out 0
GPIO[21]/MSIO_DO[1]	H21	IO,PU	GPIO	NC	F1: General purpose IO bit #21;F2: MSIO data out 1
GPIO[22]/MSIO_DO[2]	G20	IO,PU	GPIO	NC	F1: General purpose IO bit #22;F2: MSIO data out 2
GPIO[23]/MSIO_DO[3]	G22	IO,PU	GPIO	NC	F1: General purpose IO bit #23;F2: MSIO data out 3
GPIO[24]/MSIO_DO[4]	G21	IO,PU	GPIO	NC	F1: General purpose IO bit #24;F2: MSIO data out 4
GPIO[25]/MSIO_DO[5]	F20	IO,PU	GPIO	NC	F1: General purpose IO bit #25;F2: MSIO data out 5

Signal Name	Ball#	Pad Type	I/F category	If Not Used	Functional Description
GPIO[26]/MSIO_DI[0]	F19	IO,PU	GPIO	NC	F1: General purpose IO bit #26;F2: MSIO data in 0
GPIO[27]/MSIO_DI[1]	F18	IO,PU	GPIO	NC	F1: General purpose IO bit #27;F2: MSIO data in 1
GPIO[28]/MSIO_DI[2]	E19	IO,PU	GPIO	NC	F1: General purpose IO bit #28;F2: MSIO data in 2
GPIO[29]/MSIO_DI[3]	G19	IO,PU	GPIO	NC	F1: General purpose IO bit #29;F2: MSIO data in 3
GPIO[30]/MSIO_DI[4]	H19	IO,PU	GPIO	NC	F1: General purpose IO bit #30;F2: MSIO data in 4
GPIO[31]/MSIO_DI[5]	G18	IO,PU	GPIO	NC	F1: General purpose IO bit #31;F2: MSIO data in 5
HDII_AUX_CLOCK	R18	O3State	HDI	NC	HDI auxiliary channel, clock out
HDII_AUX_DAT[0]	V22	O3State	HDI	NC	HDI auxiliary channel, data out 0
HDII_AUX_DAT[1]	T18	O3State	HDI	NC	HDI auxiliary channel, data out 1
HDII_AUX_DAT[2]	T19	O3State	HDI	NC	HDI auxiliary channel, data out 2
HDII_AUX_READY	V21	input	HDI	GND	HDI auxiliary channel, HDI Rx auxiliary channel ready.
HDII_AUX_VALID	V20	O3State	HDI	NC	HDI auxiliary channel, data out valid
HDII_CB_RTT_EXRES	W11	AIO	HDI	Must Use	HDI central bias external resistor. Should be tied to a 1KOhm 1% pull down resistor
HDII_LVDS_CKN	AA7	AIO	HDI	NC	* HDI main channel, LVDS clock in (N) * LVCMOS data out, data [0]
HDII_LVDS_CKP	AB7	AIO	HDI	NC	* HDI main channel, LVDS clock in (P) * LVCMOS clock out
HDII_LVDSDn[0]	AA11	AIO	HDI	NC	* HDI main channel, LVDS data in, lane 0 (N) * LVCMOS data out, data [2]
HDII_LVDSDn[1]	AA10	AIO	HDI	NC	* HDI main channel, LVDS data in, lane 1 (N) * LVCMOS data out, data [4]
HDII_LVDSDn[2]	AA9	AIO	HDI	NC	* HDI main channel, LVDS data in, lane 2 (N) * LVCMOS data out, data [6]
HDII_LVDSDn[3]	AA8	AIO	HDI	NC	* HDI main channel, LVDS data in, lane 3 (N) * LVCMOS data out, data [8]
HDII_LVDSDn[4]	AA6	AIO	HDI	NC	* HDI main channel, LVDS data in, lane 4 (N) * LVCMOS data out, data [10]

Signal Name	Ball#	Pad Type	I/F category	If Not Used	Functional Description
HDII_LVDSDn[5]	AA5	AIO	HDI	NC	* HDI main channel, LVDS data in, lane 5 (N) * LVCMOS data out, data [12]
HDII_LVDSDn[6]	AA4	AIO	HDI	NC	* HDI main channel, LVDS data in, lane 6 (N) * LVCMOS data out, data [14]
HDII_LVDSDn[7]	AA3	AIO	HDI	NC	* HDI main channel, LVDS data in, lane 7 (N) * LVCMOS data in, data [16]
HDII_LVDSDp[0]	AB11	AIO	HDI	NC	* HDI main channel, LVDS data in, lane 0 (P) * LVCMOS data out, data [1]
HDII_LVDSDp[1]	AB10	AIO	HDI	NC	* HDI main channel, LVDS data in, lane 1 (P) * LVCMOS data out, data [3]
HDII_LVDSDp[2]	AB9	AIO	HDI	NC	* HDI main channel, LVDS data in, lane 2 (P) * LVCMOS data out, data [5]
HDII_LVDSDp[3]	AB8	AIO	HDI	NC	* HDI main channel, LVDS data in, lane 3 (P) * LVCMOS data out, data [7]
HDII_LVDSDp[4]	AB6	AIO	HDI	NC	* HDI main channel, LVDS data in, lane 4 (P) * LVCMOS data out, data [9]
HDII_LVDSDp[5]	AB5	AIO	HDI	NC	* HDI main channel, LVDS data in, lane 5 (P) * LVCMOS data out, data [11]
HDII_LVDSDp[6]	AB4	AIO	HDI	NC	* HDI main channel, LVDS data in, lane 6 (P) * LVCMOS data out, data [13]
HDII_LVDSDp[7]	AB3	AIO	HDI	NC	* HDI main channel, LVDS data in, lane 7 (P) * LVCMOS data out, data [15]
HDII_RDY	W18	O3State	HDI	NC	HDI main channel, HDI Rx main channel ready
HDIO_AUX_CLOCK	V19	Input	HDI	GND	HDO auxiliary channel, clock input.
HDIO_AUX_DAT[0]	W22	Input	HDI	GND	HDO auxiliary channel, data in 0.
HDIO_AUX_DAT[1]	W19	Input	HDI	GND	HDO auxiliary channel, data in 1.
HDIO_AUX_DAT[2]	U19	Input	HDI	GND	HDO auxiliary channel data in 2.
HDIO_AUX_READY	W21	O3State	HDI	NC	HDO auxiliary channel ready
HDIO_AUX_VALID	W20	Input	HDI	GND	HDO auxiliary channel data in valid.

Signal Name	Ball#	Pad Type	I/F category	If Not Used	Functional Description
HDIO_LVDS_CKN	AB16	AIO	HDI	NC	* HDI main channel, LVDS clock out (N) * LVCMOS data out, data [0]
HDIO_LVDS_CKP	AA16	AIO	HDI	NC	* HDI main channel, LVDS clock out (P) * LVCMOS clock out
HDIO_LVDSDn[0]	AB12	AIO	HDI	NC	* HDI main channel, LVDS data out, lane 0 (N) * LVCMOS data out, data [2]
HDIO_LVDSDn[1]	AB13	AIO	HDI	NC	* HDI main channel, LVDS data out, lane 1 (N) * LVCMOS data out, data [4]
HDIO_LVDSDn[2]	AB14	AIO	HDI	NC	* HDI main channel, LVDS data out, lane 2 (N) * LVCMOS data out, data [6]
HDIO_LVDSDn[3]	AB15	AIO	HDI	NC	* HDI main channel, LVDS data out, lane 3 (N) * LVCMOS data out, data [8]
HDIO_LVDSDn[4]	AB17	AIO	HDI	NC	* HDI main channel, LVDS data out, lane 4 (N) * LVCMOS data out, data [10]
HDIO_LVDSDn[5]	AB18	AIO	HDI	NC	* HDI main channel, LVDS data out, lane 5 (N) * LVCMOS data out, data [12]
HDIO_LVDSDn[6]	AB19	AIO	HDI	NC	* HDI main channel, LVDS data out, lane 6 (N) * LVCMOS data out, data [14]
HDIO_LVDSDn[7]	AB20	AIO	HDI	NC	* HDI main channel, LVDS data out, lane 7 (N) * LVCMOS data out, data [16]
HDIO_LVDSDp[0]	AA12	AIO	HDI	NC	* HDI main channel, LVDS data out, lane 0 (P) * LVCMOS data out, data [1]
HDIO_LVDSDp[1]	AA13	AIO	HDI	NC	* HDI main channel, LVDS data out, lane 1 (P) * LVCMOS data out, data [3]
HDIO_LVDSDp[2]	AA14	AIO	HDI	NC	* HDI main channel, LVDS data out, lane 2 (P) * LVCMOS data out, data [5]
HDIO_LVDSDp[3]	AA15	AIO	HDI	NC	* HDI main channel, LVDS data out, lane 3 (P) * LVCMOS data out, data [7]

Signal Name	Ball#	Pad Type	I/F category	If Not Used	Functional Description
HDIO_LVDSDp[4]	AA17	AIO	HDI	NC	* HDI main channel, LVDS data out, lane 4 (P) * LVCMOS data out, data [9]
HDIO_LVDSDp[5]	AA18	AIO	HDI	NC	* HDI main channel, LVDS data out, lane 5 (P) * LVCMOS data out, data [11]
HDIO_LVDSDp[6]	AA19	AIO	HDI	NC	* HDI main channel, LVDS data out, lane 6 (P) * LVCMOS data out, data [13]
HDIO_LVDSDp[7]	AA20	AIO	HDI	NC	* HDI main channel, LVDS data out, lane 7 (P) * LVCMOS data out, data [15]
HDIO_RDY	W17	Input,PU	HDI	NC	HDO main channel, HDI Rx main channel ready
HDMIO_5V	E14	O3State	HDMI	NC	HDMI Tx 5V power signal output enable
HDMIO_CEC	E11	IO	HDMI	27K PU	HDMI Tx CEC bus
HDMIO_DDC_SCL	E12	IO	HDMI	1.5K – 2K PU	HDMI Tx DDC I2C clock
HDMIO_DDC_SDA	E13	IO	HDMI	1.5K – 2K PU	HDMI Tx DDC I2C data
HDMIO_HPD	E15	Input, PD	HDMI	NC	HDMI Tx hot plug detect input
HDMIO_RREF	D9	AIO	HDMI	Must use	HDMI current Source Resistor. Should be tied to a 4.02 KOhm 1% pull down resistor.
HDMIO_TMDSCLKN	A13	AO	HDMI	NC	HDMI Tx TMDS clock lane (N)
HDMIO_TMDSCLKP	B13	AO	HDMI	NC	HDMI Tx TMDS clock lane (P)
HDMIO_TMDSDATAn[0]	A11	AO	HDMI	NC	HDMI Tx TMDS data lane 0 (N)
HDMIO_TMDSDATAn[1]	A9	AO	HDMI	NC	HDMI Tx TMDS data lane 1 (N)
HDMIO_TMDSDATAn[2]	A7	AO	HDMI	NC	HDMI Tx TMDS data lane 2 (N)
HDMIO_TMDSDATAp[0]	B11	AO	HDMI	NC	HDMI Tx TMDS data lane 0 (P)
HDMIO_TMDSDATAp[1]	B9	AO	HDMI	NC	HDMI Tx TMDS data lane 1 (P)
HDMIO_TMDSDATAp[2]	B7	AO	HDMI	NC	HDMI Tx TMDS data lane 2 (P)
HDSNK_REXT_H	C19	AIO	HDBaseT	Must Use	HDBT current Source Resistor. Should be tied to a 4.53 KOhm 1% pull down resistor.
HDSNKn[0]	A21	AIO	HDBaseT	NC	HDBaseT Transceiver Channel 0 (N)
HDSNKn[1]	A20	AIO	HDBaseT	NC	HDBaseT Transceiver Channel 1 (N)
HDSNKn[2]	A17	AIO	HDBaseT	NC	HDBaseT Transceiver Channel 2 (N)
HDSNKn[3]	A16	AIO	HDBaseT	NC	HDBaseT Transceiver Channel 3 (N)

Signal Name	Ball#	Pad Type	I/F category	If Not Used	Functional Description
HDSNKp[0]	B21	AIO	HDBaseT	NC	HDBaseT Transceiver Channel 0 (P)
HDSNKp[1]	B20	AIO	HDBaseT	NC	HDBaseT Transceiver Channel 1 (P)
HDSNKp[2]	B17	AIO	HDBaseT	NC	HDBaseT Transceiver Channel 2 (P)
HDSNKp[3]	B16	AIO	HDBaseT	NC	HDBaseT Transceiver Channel 3 (P)
I2C_SCL_MSTR	F4	IO, PU	I2C	NC	Master I2C interface, clock line, connect to external slave
I2C_SDA_MSTR	F5	IO, PU	I2C	NC	Master I2C interface, data line, connect to external slave
I2C1_SCL_SLAV	H4	IO, PU	I2C	NC	Slave I2C interface 1, clock line, connect to external master
I2C1_SDA_SLAV	H5	IO, PU	I2C	NC	Slave I2C interface 1, data line, connect to external master
I2C2_SCL_SLAV	G4	IO, PU	I2C	NC	Slave I2C interface 2, clock line, connect to external master
I2C2_SDA_SLAV	G5	IO, PU	I2C	NC	Slave I2C interface 2, data line, connect to external master
MAC_RMII_CLK	K4	Input	MAC (future use)	1K PD	RMII MAC clock.
MII_COL/GPIO[2]	N5	IO,PU	ETH	NC	F1:MII PHY Collision Detect; F2:General purpose pin #2
MII_CRS/GPIO[3]	P5	IO,PU	ETH	NC	F1: mii phy carrier sense; F2: general purpose IO bit #3
MII_MDC	R5	IO	ETH	10K PU	PHY MII Slave Management Clock
MII_MDIO	T5	IO	ETH	10K PU	MII Slave Management Data
MII_RX_CLK_ST11	U5	IO	ETH	1K PD	F1: MII PHY Receive Clock; F2: RMII 50MHz output clock; ST: Strap pin #11
MII_RX_DV_ST4	P4	IO,PU	ETH	1K PD	MII/RMII PHY receive Data Valid; ST: Strap pin #4
MII_RX_ERR_ST5	R4	IO,PD	ETH	1K PU with jumper	MII PHY Receive Error.; ST: Strap pin #5
MII_RXD[0]_ST0	V5	IO,PD	ETH	NC	MII/RMII PHY Receive Data Bit 0; ST: strap pin #0
MII_RXD[1]_ST1	V4	IO,PD	ETH	NC	MII/RMII PHY Receive Data Bit 1; ST: strap pin #1
MII_RXD[2]_ST2	U4	IO,PD	ETH	NC	MII PHY Receive Data Bit 2; ST: strap pin #2
MII_RXD[3]_ST3	T4	IO,PU	ETH	1KPD	MII PHY Receive Data Bit 3; ST: strap pin #3

Signal Name	Ball#	Pad Type	I/F category	If Not Used	Functional Description
MII_TX_CLK	M5	IO	ETH	1KPD	F1: MII PHY Transmit Clock; F2: RMII REF_CLK input
MII_TX_EN	L5	Input	ETH	GND	MII/RMII PHY Transmit Enable.
MII_TX_ERR	M4	Input, PU	ETH	GND	MII PHY Transmit Error.
MII_TXD[0]	M3	Input	ETH	GND	MII/RMII PHY Transmit Data Bit 0
MII_TXD[1]	M2	Input	ETH	GND	MII/RMII PHY Transmit Data Bit 1
MII_TXD[2]/GPIO[0]	M1	IO,PU	ETH	NC	F1: MII PHY Transmit Data Bit 2 (I); F2: General purpose pin #0
MII_TXD[3]/GPIO[1]	N4	IO,PU	ETH	NC	F1: MII PHY Transmit Data Bit 3 (I); F2: General purpose pin #1
ST10	K19	IO	MSIO	1K PU	Strap pin #10
MSIO_DIN[0]/UART_IN/GPIO[4]	P18	IO,PU	MSIO	NC	F1: MSIO data in bit 0; F2:UART in; F3: GPIO bit 4
MSIO_DIN[1]/I2S_DIN/GPIO[5]	P19	IO,PU	MSIO	NC	F1: MSIO data in bit 1; F2: I2S data [0] in; F3: GPIO bit #5
MSIO_DIN[2]/I2S_WCLK_IN/GPIO[6]	N19	IO,PU	MSIO	NC	F1: MSIO data in bit 2; F2:I2S WCLK in; F3: General purpose pin #6
MSIO_DIN[3]/CIR_in/GPIO[7]	N18	IO,PU	MSIO	NC	F1: MSIO data in bit 3; F2: CIR in; F3: GPIO bit 7
MSIO_DIN[4]/I2S_BCLK_in/GPIO[8]	M19	IO,PU	MSIO	NC	F1: MSIO data in bit 4; F2: I2S BCLK in; F3: GPIO bit 8
MSIO_DIN[5]/SPDIF_in/GPIO[9]	M18	IO,PU	MSIO	NC	F1: MSIO data in bit 5; F2: SPDIF in; F3: GPIO bit 9
MSIO_DOUT[0]/UART_OUT/GPIO[10]	L19	IO,PU	MSIO	NC	F1: MSIO data out bit 0; F2: UART out; F3: GPIO bit 10
MSIO_DOUT[1]/I2S_DOUT/GPIO[11]	K18	IO,PU	MSIO	NC	F1: MSIO data out bit 1; F2: I2S data [0] out; F3: GPIO bit 11
MSIO_DOUT[2]/I2S_WCLK_OUT/GPIO[12]	L18	IO,PU	MSIO	NC	F1: MSIO data out bit 2; F2: I2S WCLK out; F3: GPIO bit 12
MSIO_DOUT[3]/CIR_OUT/GPIO[13]	J18	IO,PU	MSIO	NC	F1: MSIO data in bit 3; F2: CIR out; F3: GPIO bit 13
MSIO_DOUT[4]/I2S_BCLK_OUT/GPIO[14]	H18	IO,PU	MSIO	NC	F1: MSIO data in bit 4; F2: I2S BCLK out; F3: GPIO bit 14
MSIO_DOUT[5]/SPDIF_OUT/GPIO[15]	J19	IO,PU	MSIO	NC	F1: MSIO data in bit 5; F2: SPDIF out; F3: GPIO bit 15
POR_BYPASS	D2	Input	MISC	Must use	Power on reset select: '0'- POR enabled; '1'-POR disabled
QVDD25	J6	N/A	FU	GND	Reserved. Must be tied to ground

Signal Name	Ball#	Pad Type	I/F category	If Not Used	Functional Description
RCB_REFCLK0_M	E22	AI	MISC	If XO25M_SEL=1 short to VDD18	F1: 125MHz LVDS reference Clock (N); F2: 1.2V dc (see application notes on single ended application for this pin).
RCB_REFCLK0_P	E21	AI	MISC	If XO25M_SEL=1 short to VDD18	F1: 125MHz LVDS reference Clock (P); F2: 125MHz Single-ended reference clock
RESET_IN	E5	Input	MISC	4.7K PU	VS2310 Tx Reset In (Active only when POR_BYPASS=1)
RESET_N	C1	AIO	MISC	WPU	Power on reset bi-directional pin (open drain). 4.7KOhm PU resistor to AVDD33 and 1nF capacitor to GND close to the pin are needed when active (POR_BYPASS=0)
RMII_MAC_RXD[0]	L1	Input	MAC (future use)	GND	RMII MAC Receive Data Bit 0.
RMII_MAC_RXD[1]	K5	Input	MAC (future use)	GND	RMII MAC Receive Data Bit 1
RMII_MAC_RXDV	L2	Input	MAC (future use)	GND	RMII MAC receive Data Valid
RMII_MAC_TXD[0]	L4	O3State	MAC (future use)	NC	RMII MAC Transmit Data Bit 0
RMII_MAC_TXD[1]	L3	O3State	MAC (future use)	NC	RMII MAC Transmit Data Bit 1
RMII_MAC_TXEN	K1	O3State	MAC (future use)	NC	RMII MAC Transmit Enable
SGMAC_CKN	AA1	AO	MAC (future use)	NC	SGMII MAC clock (N)
SGMAC_CKP	AB1	AO	MAC (future use)	NC	SGMII MAC clock (P)
SGMAC_RXN	V2	AI	MAC (future use)	NC	SGMII MAC receive data (N)
SGMAC_RXP	V1	AI	MAC (future use)	NC	SGMII MAC receive data (P)

Signal Name	Ball#	Pad Type	I/F category	If Not Used	Functional Description
SGMAC_TXN	Y2	AO	MAC (future use)	NC	SGMII MAC transmit data (N)
SGMAC_TXP	Y1	AO	MAC (future use)	NC	SGMII MAC transmit data (P)
SGMPHY_CKN	U2	AO	ETH SGMII	NC	SGMII PHY clock (N)
SGMPHY_CKP	U1	AO	ETH SGMII	NC	SGMII PHY clock (P)
SGMPHY_RXN	P2	AI	ETH SGMII	NC	SGMII PHY receive data (N)
SGMPHY_RXP	P1	AI	ETH SGMII	NC	SGMII PHY receive data (P)
SGMPHY_TXN	T2	AO	ETH SGMII	NC	SGMII PHY transmit data (N)
SGMPHY_TXP	T1	AO	ETH SGMII	NC	SGMII PHY transmit data (P)
TCK	H3	Input,PU	JTAG	NC	JTAG
TDI	G1	Input,PU	JTAG	NC	JTAG
TDO	H2	O3State	JTAG	NC	JTAG
TMS	F1	Input,PU	JTAG	NC	JTAG
TRST	H1	Input,PD	JTAG	1KPD	JTAG
USB_DM	B4	AIO	USB	NC	DM pin of the USB connector (IO)
USB_DP	A4	AIO	USB	NC	DP pin of the USB connector (IO)
USB_DRVVBUS	D6	Output	USB	NC	VBUS charge pump control
USB_ID	B5	AIO, PU	USB	NC	Identification (ID) pin of the USB connector. '1' indicates that VS2310 is connected to a host (USBH mode). '0' indicates that VS2310 is connected to a device (USBD mode).
USB_TXR_RKL	C3	AIO	USB	Must Use	Reference resistor. Should be tied to a 44.2 Ohm 1% pull down resistor.
USB_VBUS	C5	AIO	USB	NC	VBUS pin of the USB connector
USB_XI	A2	XTAL	USB	NC	USB 12MHz Crystal clock input
USB_XO	B2	XTAL	USB	NC	USB 12MHz Crystal clock output
WAKEUP_IN	J1	Input, PU	MISC	NC	Wakeup Input (reserved for future use)
WAKEUP_OUT_ST9	J2	IO	MISC	10K PD	Wakeup Output (reserved for future use); ST: Strap pin #9
XO25M_SEL	E20	Input, PD	MISC	1K PD	Reference clock source select: '1'- 25MHz reference clock, crystal or LVCMOS oscillator; '0'- 125MHz reference clock on RCB_REFCLK0_P/M **NOTE THAT 25MHz CLOCK IS FUTURE USE ONLY**

Signal Name	Ball#	Pad Type	I/F category	If Not Used	Functional Description
XO25MHZ_XIN	D21	XTAL	MISC	If XO25M_SEL =0 short to GND	25MHz Crystal clock or LVCMOS oscillator input **NOTE THAT 25MHz CLOCK IS FUTURE USE ONLY**
XO25MHZ_XOUT	D22	XTAL	MISC	If XO25M_SEL =0 NC	25MHz Crystal clock output **NOTE THAT 25MHz CLOCK IS FUTURE USE ONLY**

2.4.1.2 Rx Non-Functional Signals

Table 12: VS2310RX Non-functional Signal Table

Symbol	Type	Description	Ball Numbers
NC	Non-connected balls	Reserved	C14, D13, D16, D17, D7, E6, E9, U21, U20, U22
NC	Non-connected balls	Future use.	
NC	Non-connected balls	Future use. Must be tied to ground.	
FU_D5	Future Use	Reserved. Must be tied to 3.3V external 1K pullup resistor.	D5
FU_J3	JTAG	TEST_MODE_1. Must be tied to external weak pulldown resistor (27.4K).	J3
FU_R19	Future Use	Reserved. Must be tied to external weak pulldown resistor (27K)	R19
FU_J4	JTAG	TEST_MODE_0. Must be tied to external weak pulldown resistor (27.4K).	J4
VDD	1.0 V digital supply	1.0 V Digital supply	D15, D18, E16, E18, F11, F12, F13, F14, F15, F16, K6, L6, M6, N6, P6, R6, T6, U6, U7, U8, U9, U10, U11, U12, U13, U14, U15, U16, U17, V8, V9, V10, V11, V12, V13, V14, V15, V16, V18

Symbol	Type	Description	Ball Numbers
VDD33V	3.3 V supply signals	3.3 V digital supply	E7, F6, F7, F8, F9, F10, F17, G6, G17, H6, H17, J5, J17, K17, L17, M17, N17, P17, R17, T17
AVDD10	1.0 V analog supply signals	1.0 V analog supply	C15, C16, C17, C18, C20, C21, D20, F22, Y13, Y15, Y16, Y17, Y19, Y21, AA21, AA22
AVDD18	1.8 V analog supply signals	1.8 V analog supply	C6, C7, C8, C9, D4, N2, N3, P3, T3, U3, Y3, Y4, Y5, Y6, Y7, AA2
AVDD33	3.3 V analog supply signals	3.3 V analog supply	C10, C11, C12, C13, D8, D10, D12
VSS	Ground signals	Ground	A3, A5, A6, A8, A10, A12, A14, A15, A18, A19, A22, B1, B3, B6, B8, B10, B12, B14, B15, B18, B19, B22, C2, C4, C22, D1, D3, D11, D14, D19, E8, E10, E17, F21, G7, G8, G9, G10, G11, G12, G13, G14, G15, G16, H7, H8, H9, H10, H11, H12, H13, H14, H15, H16, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, K7, K8, K9, K10, K11, K12, K13, K14, K15, K16, L7, L8, L9, L10, L11, L12, L13, L14, L15, W8, AB22, A1, L16, M7, M8, M9, M10, M11, M12, M13, M14, M15, M16, N1, N7, N8, N9, N10, N11, N12, N13, N14, N15, N16, P7, P8, P9, P10, P11, P12, P13, P14, P15, P16, R1, R2, R3, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, T7, T8, T9, T10, T11, T12, T13, T14, T15, T16, U18, V3, V17, W1, W2, W3, W4, W5, W6, W7, W9, W10, W12, W13, W14, W15, W16, Y8, Y9, Y10, Y11, Y12, Y14, Y18, Y20, Y22, AB2, AB21

2.4.1.3 Rx Bias Resistors

Bias resistors are used to set an internal bias reference current and should be placed as close as possible to their BGA ball.

Table 13: Reference Resistor Values in VS2310RX

Pin Name	Pin #	Resistor value (ohms)	PU/PD
HDSNK_REXT_H	C19	4.53K	PD to VSS
HDMISER_RREF	D9	4.02K	PD to VSS
HDII_CB_RTT_EXRES	W11	1K	PD to VSS
USB_TXR_RKL	C3	44.2	PD to VSS

2.4.1.4 VS2310RX Ball Diagram (Top View)

Matrix	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	Matrix
A	VSS	USB_XI	VSS	USB_DP	VSS	VSS	HDMIO_TMDSDATAn[2]	VSS	HDMIO_TMDSDATAn[1]	VSS	HDMIO_TMDSDATAn[0]	VSS	HDMIO_TMDSCLKN	VSS	VSS	HDSNKn[3]	HDSNKn[2]	VSS	VSS	HDSNKn[1]	HDSNKn[0]	VSS	A
B	VSS	USB_XO	VSS	USB_DM	USB_ID	VSS	HDMIO_TMDSDATAp[2]	VSS	HDMIO_TMDSDATAp[1]	VSS	HDMIO_TMDSDATAp[0]	VSS	HDMIO_TMDSCLKP	VSS	VSS	HDSNKp[3]	HDSNKp[2]	VSS	VSS	HDSNKp[1]	HDSNKp[0]	VSS	B
C	RESET_N	VSS	USB_TXR_RKL	VSS	USB_VBUS	AVDD18	AVDD18	AVDD18	AVDD18	AVDD33	AVDD33	AVDD33	AVDD33	NC_C14	AVDD10	AVDD10	AVDD10	AVDD10	HDSNK_REXT_H	AVDD10	AVDD10	VSS	C
D	VSS	POR_BYPASS	VSS	AVDD18	FU_D5	USB_DRVVBUS	NC_D7	AVDD33	HDMIO_RREF	AVDD33	VSS	AVDD33	NC_D13	VSS	VDD	NC_D16	NC_D17	VDD	VSS	AVDD10	XO25MHZ_XIN	XO25MHZ_XOUT	D
E	DBG_RXD	DBG_TXD_ST6	CFG_SCL	CFG_SDA	RESET_IN	NC_E6	VDD33V	VSS	NC_E9	VSS	HDMIO_CEC	HDMIO_DDC_SCL	HDMIO_DDC_SDA	HDMIO_5V	HDMIO_HPD	VDD	VSS	VDD	GPIO[28]/MSIO_D[2]	XO25M_SEL	RCB_REFCLK0_P	RCB_REFCLK0_M	E
F	TMS	EE_SDA_MI	EE_SCL_SCK	I2C_SCL_MSTR	I2C_SDA_MSTR	VDD33V	VDD33V	VDD33V	VDD33V	VDD33V	VDD	VDD	VDD	VDD	VDD	VDD	VDD33V	GPIO[27]/MSIO_D[1]	GPIO[26]/MSIO_D[0]	GPIO[25]/MSIO_DO[5]	VSS	AVDD10	F
G	TDI	EE_CS_ST8	EE_MO_ST7	I2C2_SCL_SLAV	I2C2_SDA_SLAV	VDD33V	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD33V	GPIO[31]/MSIO_D[5]	GPIO[29]/MSIO_D[3]	GPIO[22]/MSIO_DO[2]	GPIO[24]/MSIO_D[4]	GPIO[23]/MSIO_DO[3]	G
H	TRST	TDO	TCK	I2C1_SCL_SLAV	I2C1_SDA_SLAV	VDD33V	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD33V	MSIO_DOUT[4]/I2S_BCLK_OUT/GPIO[14]	GPIO[30]/MSIO_D[4]	GPIO[19]	GPIO[23]/MSIO_D[1]	GPIO[20]/MSIO_DO[0]	H
J	WAKEUP_IN	WAKEUP_OUT_ST9	FU_J3	FU_J4	VDD33V	QVDD25	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD33V	MSIO_DOUT[3]/CIR_OUT/GPIO[13]	MSIO_DOUT[5]/SPDIF_OUT/GPIO[15]	GPIO[16]	GPIO[18]	GPIO[17]	J
K	RMII_MAC_TXEN	GMII_MDIO	GMII_MDC	MAC_RMII_CLK	RMII_MAC_RXD[1]	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD33V	MSIO_DOUT[1]/I2S_DOUT/GPIO[11]	ST10	BT1120_D17	BT1120_D18	BT1120_D19	K
L	RMII_MAC_RXD[0]	RMII_MAC_RXDV	RMII_MAC_TXD[1]	RMII_MAC_TXD[0]	MII_TX_EN	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD33V	MSIO_DOUT[2]/I2S_WCLK_OUT/GPIO[12]	MSIO_DOUT[0]/UART_OUT/GPIO[10]	BT1120_D14	BT1120_D15	BT1120_D16	L
M	MII_TXD[2]/GPIO[0]	MII_TXD[3]	MII_TXD[0]	MII_TX_ERR	MII_TX_CLK	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD33V	MSIO_DIN[5]/SPDIF_in/GPIO[9]	MSIO_DIN[4]/I2S_BCLK_in/GPIO[8]	BT1120_D11	BT1120_D12	BT1120_D13	M
N	VSS	AVDD18	AVDD18	MII_TXD[3]/GPIO[1]	MII_COL/GPIO[2]	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD33V	MSIO_DIN[3]/CIR_in/GPIO[7]	MSIO_DIN[2]/I2S_WCLK_IN/GPIO[6]	BT1120_D9	BT1120_CLK	BT1120_D10	N
P	SGMPHY_RXP	SGMPHY_RXN	AVDD18	MII_RX_DV_ST4	MII_CRS/GPIO[3]	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD33V	MSIO_DIN[0]/UART_IN/GPIO[4]	MSIO_DIN[1]/I2S_DIN/GPIO[5]	BT1120_D6	BT1120_D7	BT1120_D8	P
R	VSS	VSS	VSS	MII_RX_ERR_ST5	MII_MDC	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD33V	HDI_AUX_CLOCK	FU_R19	BT1120_D3	BT1120_D4	BT1120_D5	R
T	SGMPHY_TXP	SGMPHY_TXN	AVDD18	MII_RXD[3]_ST3	MII_MDIO	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD33V	HDI_AUX_DAT[3]	HDI_AUX_DAT[2]	BT1120_D0	BT1120_D1	BT1120_D2	T
U	SGMPHY_CKP	SGMPHY_CKN	AVDD18	MII_RXD[2]_ST2	MII_RX_CLK_ST11	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VSS	HDIO_AUX_DAT[2]	NC_U20	NC_U21	NC_U22	U
V	SGMAC_RXP	SGMAC_RXN	VSS	MII_RXD[1]_ST1	MII_RXD[0]_ST0	UCC_0	UCC_1	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VDD	HDIO_AUX_CLOCK	HDI_AUX_VALID	HDI_AUX_READY	HDI_AUX_DAT[0]	V
W	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	HDI_CB_RTT_EXRES	VSS	VSS	VSS	VSS	VSS	HDIO_RDY	HDI_RDY	HDIO_AUX_DAT[1]	HDIO_AUX_VALID	HDIO_AUX_READY	HDIO_AUX_DAT[0]	W
Y	SGMAC_TXP	SGMAC_TXN	AVDD18	AVDD18	AVDD18	AVDD18	AVDD18	VSS	VSS	VSS	VSS	VSS	AVDD10	VSS	AVDD10	AVDD10	AVDD10	VSS	AVDD10	VSS	AVDD10	VSS	Y
AA	SGMAC_CKN	AVDD18	HDI_LVDSDn[7]	HDI_LVDSDn[6]	HDI_LVDSDn[5]	HDI_LVDSDn[4]	HDI_LVDS_CKN	HDI_LVDSDn[3]	HDI_LVDSDn[2]	HDI_LVDSDn[1]	HDI_LVDSDn[0]	HDIO_LVDSDp[0]	HDIO_LVDSDp[1]	HDIO_LVDSDp[2]	HDIO_LVDSDp[3]	HDIO_LVDS_CKP	HDIO_LVDSDp[4]	HDIO_LVDSDp[5]	HDIO_LVDSDp[6]	HDIO_LVDSDp[7]	AVDD10	AVDD10	AA
AB	SGMAC_CKP	VSS	HDI_LVDSDp[7]	HDI_LVDSDp[6]	HDI_LVDSDp[5]	HDI_LVDSDp[4]	HDI_LVDS_CKP	HDI_LVDSDp[3]	HDI_LVDSDp[2]	HDI_LVDSDp[1]	HDI_LVDSDp[0]	HDIO_LVDSDn[0]	HDIO_LVDSDn[1]	HDIO_LVDSDn[2]	HDIO_LVDSDn[3]	HDIO_LVDS_CKN	HDIO_LVDSDn[4]	HDIO_LVDSDn[5]	HDIO_LVDSDn[6]	HDIO_LVDSDn[7]	VSS	VSS	AB
Matrix	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	Matrix

Figure 13: VS2310RX Ball Diagram

2.4.2 VS2000 RX Signal Description

This section provides information on each pin of the VS2000RX chip. Pins with more than one function use the following convention:

- F1: <function 1 description>
- F2: <function 2 description>
- ST: <strap function description>

Selecting between functions of multi-functional pins is performed by either using VS2000 chip parameters or asserting strap pins. For more details, refer to the section in Chapter 6 that corresponds with the relevant interface category.

2.4.2.1 Rx Functional Signals

Table 14: VS2000RX Functional Signal Table

Signal Name	Ball#	Pad Type	I/F category	If Not Used	Functional Description
BT1120_D19	K22	03State	BT.1120	NC	BT.1120 – Output Chroma bit 9
BT1120_D18	K21	03State	BT.1120	NC	BT.1120 – Output Chroma bit 8
BT1120_D17	K20	03State	BT.1120	NC	BT.1120 – Output Chroma bit 7
BT1120_D16	L22	03State	BT.1120	NC	BT.1120 – Output Chroma bit 6
BT1120_D15	L21	03State	BT.1120	NC	BT.1120 – Output Chroma bit 5
BT1120_D14	L20	03State	BT.1120	NC	BT.1120 – Output Chroma bit 4
BT1120_D13	M22	03State	BT.1120	NC	BT.1120 – Output Chroma bit 3
BT1120_D12	M21	03State	BT.1120	NC	BT.1120 – Output Chroma bit 2
BT1120_D11	M20	03State	BT.1120	NC	BT.1120 – Output Chroma bit 1
BT1120_D10	N22	03State	BT.1120	NC	BT.1120 – Output Chroma bit 0
BT1120_D9	N20	03State	BT.1120	NC	BT.1120 – Output Luminance bit 9
BT1120_D8	P22	03State	BT.1120	NC	BT.1120 – Output Luminance bit 8
BT1120_D7	P21	03State	BT.1120	NC	BT.1120 – Output Luminance bit 7
BT1120_D6	P20	03State	BT.1120	NC	BT.1120 – Output Luminance bit 6
BT1120_D5	R22	03State	BT.1120	NC	BT.1120 – Output Luminance bit 5
BT1120_D4	R21	03State	BT.1120	NC	BT.1120 – Output Luminance bit 4
BT1120_D3	R20	03State	BT.1120	NC	BT.1120 – Output Luminance bit 3
BT1120_D2	T22	03State	BT.1120	NC	BT.1120 – Output Luminance bit 2
BT1120_D1	T21	03State	BT.1120	NC	BT.1120 – Output Luminance bit 1
BT1120_D0	T20	03State	BT.1120	NC	BT.1120 – Output Luminance bit 0
BT1120_CLK	N21	03State	BT.1120	NC	BT.1120 – Output Clock
UCC_0	V6	Input	BT.1120	GND	HDcctv Upstream Communication Channel 0
UCC_1	V7	Input	BT.1120	GND	HDcctv Upstream Communication Channel 1
CFG_SCL	E3	IO	Debug	1K PD	Host interface I2C clock Signal
CFG_SDA	E4	IO	Debug	NC	Host interface I2C data Signal
DBG_RXD	E1	Input	Debug	3.3V 10K PU	Debug Receive Data (I)
DBG_TXD_ST6	E2	IO,PU	Debug	1K PD	Debug Transmit Data (O); ST: strap pin #6
EE_CS_ST8	G2	IO,PD	FLASH	NC	SPI FLASH chip select; ST: strap pin #8
EE_MO_ST7	G3	IO,PD	FLASH	1K PU	SPI FLASH MO (master Out); ST: strap pin #7

Signal Name	Ball#	Pad Type	I/F category	If Not Used	Functional Description
EE_SCL_SCK	F3	IO,PU	FLASH	Must use	Clock for Both I2C and SPI FLASHs (O)
EE_SDA_MI	F2	IO,PU	FLASH	Must use	I2C FLASH SDA or SPI FLASH MI (Master In)
GMII_MDC	K3	O3State	MAC (future use)	NC	MII Master Management Clock
GMII_MDIO	K2	IO	MAC (future use)	4.7K – 10K PU	MII Master Management Data
GPIO[16]	J20	IO,PU	GPIO	4.7K-10K PD	General purpose IO bit #16 (IO). Must be tied to external 4.7K-10K pulldown resistor in all applications.
GPIO[17]	J22	IO,PU	GPIO	4.7K-10K PD	General purpose IO bit #16 (IO). Must be tied to external 4.7K-10K pulldown resistor in all applications.
GPIO[18]	J21	IO,PU	GPIO	NC	General purpose IO bit #18 (IO)
GPIO[19]	H20	IO,PU	GPIO	NC	General purpose IO bit #19 (IO)
GPIO[20]/MSIO_DO[0]	H22	IO,PU	GPIO	NC	F1: General purpose IO bit #20;F2: MSIO data out 0
GPIO[21]/MSIO_DO[1]	H21	IO,PU	GPIO	NC	F1: General purpose IO bit #21;F2: MSIO data out 1
GPIO[22]/MSIO_DO[2]	G20	IO,PU	GPIO	NC	F1: General purpose IO bit #22;F2: MSIO data out 2
GPIO[23]/MSIO_DO[3]	G22	IO,PU	GPIO	NC	F1: General purpose IO bit #23;F2: MSIO data out 3
GPIO[24]/MSIO_DO[4]	G21	IO,PU	GPIO	NC	F1: General purpose IO bit #24;F2: MSIO data out 4
GPIO[25]/MSIO_DO[5]	F20	IO,PU	GPIO	NC	F1: General purpose IO bit #25;F2: MSIO data out 5
GPIO[26]/MSIO_DI[0]	F19	IO,PU	GPIO	NC	F1: General purpose IO bit #26;F2: MSIO data in 0
GPIO[27]/MSIO_DI[1]	F18	IO,PU	GPIO	NC	F1: General purpose IO bit #27;F2: MSIO data in 1
GPIO[28]/MSIO_DI[2]	E19	IO,PU	GPIO	NC	F1: General purpose IO bit #28;F2: MSIO data in 2
GPIO[29]/MSIO_DI[3]	G19	IO,PU	GPIO	NC	F1: General purpose IO bit #29;F2: MSIO data in 3
GPIO[30]/MSIO_DI[4]	H19	IO,PU	GPIO	NC	F1: General purpose IO bit #30;F2: MSIO data in 4

Signal Name	Ball#	Pad Type	I/F category	If Not Used	Functional Description
GPIO[31]/MSIO_DI[5]	G18	IO,PU	GPIO	NC	F1: General purpose IO bit #31;F2: MSIO data in 5
HDII_CB_RTT_EXRES	W11	AIO	HDI	Must Use	HDI central bias external resistor. Should be tied to a 1KOhm 1% pull down resistor
HDMIO_5V	E14	O3State	HDMI	NC	HDMI Tx 5V power signal output enable
HDMIO_CEC	E11	IO	HDMI	27K PU	HDMI Tx CEC bus
HDMIO_DDC_SCL	E12	IO	HDMI	1.5K – 2K PU	HDMI Tx DDC I2C clock
HDMIO_DDC_SDA	E13	IO	HDMI	1.5K – 2K PU	HDMI Tx DDC I2C data
HDMIO_HPD	E15	Input, PD	HDMI	NC	HDMI Tx hot plug detect input
HDMIO_RREF	D9	AIO	HDMI	Must use	HDMI current Source Resistor. Should be tied to a 4.02 KOhm 1% pull down resistor.
HDMIO_TMDSCLKN	A13	AO	HDMI	NC	HDMI Tx TMDS clock lane (N)
HDMIO_TMDSCLKP	B13	AO	HDMI	NC	HDMI Tx TMDS clock lane (P)
HDMIO_TMDSDATAn[0]	A11	AO	HDMI	NC	HDMI Tx TMDS data lane 0 (N)
HDMIO_TMDSDATAn[1]	A9	AO	HDMI	NC	HDMI Tx TMDS data lane 1 (N)
HDMIO_TMDSDATAn[2]	A7	AO	HDMI	NC	HDMI Tx TMDS data lane 2 (N)
HDMIO_TMDSDATAp[0]	B11	AO	HDMI	NC	HDMI Tx TMDS data lane 0 (P)
HDMIO_TMDSDATAp[1]	B9	AO	HDMI	NC	HDMI Tx TMDS data lane 1 (P)
HDMIO_TMDSDATAp[2]	B7	AO	HDMI	NC	HDMI Tx TMDS data lane 2 (P)
HDSNK_REXT_H	C19	AIO	HDBaseT	Must Use	HDBT current Source Resistor. Should be tied to a 4.53 KOhm 1% pull down resistor.
HDSNKn[0]	A21	AIO	HDBaseT	NC	HDBaseT Tranceive Channel 0 (N)
HDSNKn[1]	A20	AIO	HDBaseT	NC	HDBaseT Tranceive Channel 1 (N)
HDSNKn[2]	A17	AIO	HDBaseT	NC	HDBaseT Tranceive Channel 2 (N)
HDSNKn[3]	A16	AIO	HDBaseT	NC	HDBaseT Tranceive Channel 3 (N)
HDSNKp[0]	B21	AIO	HDBaseT	NC	HDBaseT Tranceive Channel 0 (P)
HDSNKp[1]	B20	AIO	HDBaseT	NC	HDBaseT Tranceive Channel 1 (P)
HDSNKp[2]	B17	AIO	HDBaseT	NC	HDBaseT Tranceive Channel 2 (P)
HDSNKp[3]	B16	AIO	HDBaseT	NC	HDBaseT Tranceive Channel 3 (P)
I2C_SCL_MSTR	F4	IO, PU	I2C	NC	Master I2C interface, clock line, connect to external slave
I2C_SDA_MSTR	F5	IO, PU	I2C	NC	Master I2C interface, data line, connect to external slave

Signal Name	Ball#	Pad Type	I/F category	If Not Used	Functional Description
I2C1_SCL_SLAV	H4	IO, PU	I2C	NC	Slave I2C interface 1, clock line, connect to external master
I2C1_SDA_SLAV	H5	IO, PU	I2C	NC	Slave I2C interface 1, data line, connect to external master
I2C2_SCL_SLAV	G4	IO, PU	I2C	NC	Slave I2C interface 2, clock line, connect to external master
I2C2_SDA_SLAV	G5	IO, PU	I2C	NC	Slave I2C interface 2, data line, connect to external master
MAC_RMII_CLK	K4	Input	MAC (future use)	1K PD	RMII MAC clock.
MII_COL/GPIO[2]	N5	IO,PU	ETH	NC	F1:MII PHY Collision Detect; F2:General purpose pin #2
MII_CRS/GPIO[3]	P5	IO,PU	ETH	NC	F1: mii phy carrier sense; F2: general purpose IO bit #3
MII_MDC	R5	IO	ETH	10K PU	PHY MII Slave Management Clock
MII_MDIO	T5	IO	ETH	10K PU	MII Slave Management Data
MII_RX_CLK_ST11	U5	IO	ETH	1K PD	F1: MII PHY Receive Clock; F2: RMII 50MHz output clock; ST: Strap pin #11
MII_RX_DV_ST4	P4	IO,PU	ETH	1K PD	MII/RMII PHY receive Data Valid; ST: Strap pin #4
MII_RX_ERR_ST5	R4	IO,PD	ETH	1K PU with jumper	MII PHY Receive Error.; ST: Strap pin #5
MII_RXD[0]_ST0	V5	IO,PD	ETH	NC	MII/RMII PHY Receive Data Bit 0; ST: strap pin #0
MII_RXD[1]_ST1	V4	IO,PD	ETH	NC	MII/RMII PHY Receive Data Bit 1; ST: strap pin #1
MII_RXD[2]_ST2	U4	IO,PD	ETH	NC	MII PHY Receive Data Bit 2; ST: strap pin #2
MII_RXD[3]_ST3	T4	IO,PU	ETH	1KPD	MII PHY Receive Data Bit 3; ST: strap pin #3
MII_TX_CLK	M5	IO	ETH	1KPD	F1: MII PHY Transmit Clock; F2: RMII REF_CLK input
MII_TX_EN	L5	Input	ETH	GND	MII/RMII PHY Transmit Enable.
MII_TX_ERR	M4	Input, PU	ETH	GND	MII PHY Transmit Error.
MII_TXD[0]	M3	Input	ETH	GND	MII/RMII PHY Transmit Data Bit 0
MII_TXD[1]	M2	Input	ETH	GND	MII/RMII PHY Transmit Data Bit 1

Signal Name	Ball#	Pad Type	I/F category	If Not Used	Functional Description
MII_TXD[2]/GPIO[0]	M1	IO,PU	ETH	NC	F1: MII PHY Transmit Data Bit 2 (I); F2:General purpose pin #0
MII_TXD[3]/GPIO[1]	N4	IO,PU	ETH	NC	F1: MII PHY Transmit Data Bit 3 (I); F2:General purpose pin #1
ST10	K19	IO	MSIO	1K PU	Strap pin #10
MSIO_DIN[0]/UART_IN/GPIO[4]	P18	IO,PU	MSIO	NC	F1: MSIO data in bit 0; F2:UART in; F3: GPIO bit 4
MSIO_DIN[1]/I2S_DIN/GPIO[5]	P19	IO,PU	MSIO	NC	F1: MSIO data in bit 1; F2: I2S data [0] in; F3: GPIO bit #5
MSIO_DIN[2]/I2S_WCLK_IN/GPIO[6]	N19	IO,PU	MSIO	NC	F1: MSIO data in bit 2; F2:I2S WCLK in; f3: General purpose pin #6
MSIO_DIN[3]/CIR_in/GPIO[7]	N18	IO,PU	MSIO	NC	F1: MSIO data in bit 3; F2: CIR in ; f3: GPIO bit 7
MSIO_DIN[4]/I2S_BCLK_in/GPIO[8]	M19	IO,PU	MSIO	NC	F1: MSIO data in bit 4; F2: I2S BCLK in ; f3: GPIO bit 8
MSIO_DIN[5]/SPDIF_in/GPIO[9]	M18	IO,PU	MSIO	NC	F1: MSIO data in bit 5; F2: SPDIF in ; f3: GPIO bit 9
MSIO_DOUT[0]/UART_OUT/GPIO[10]	L19	IO,PU	MSIO	NC	F1: MSIO data out bit 0; F2: UART out ; F3: GPIO bit 10
MSIO_DOUT[1]/I2S_DOUT/GPIO[11]	K18	IO,PU	MSIO	NC	F1: MSIO data out bit 1;F2: I2S data [0] out; f3: GPIO bit 11
MSIO_DOUT[2]/I2S_WCLK_OUT/GPIO[12]	L18	IO,PU	MSIO	NC	F1: MSIO data out bit 2; F2: I2S WCLK out; F3: GPIO bit 12
MSIO_DOUT[3]/CIR_OUT/GPIO[13]	J18	IO,PU	MSIO	NC	F1: MSIO data in bit 3; F2: CIR out ;f3: GPIO bit 13
MSIO_DOUT[4]/I2S_BCLK_OUT/GPIO[14]	H18	IO,PU	MSIO	NC	F1: MSIO data in bit 4; F2: I2S BCLK out; f3: GPIO bit 14
MSIO_DOUT[5]/SPDIF_OUT/GPIO[15]	J19	IO,PU	MSIO	NC	F1: MSIO data in bit 5; F2: SPDIF out; f3: GPIO bit 15
POR_BYPASS	D2	Input	MISC	Must use	Power on reset select: '0'- POR enabled; '1'-POR disabled
QVDD25	J6	N/A	FU	GND	Reserved. Must be tied to ground
RCB_REFCLK0_M	E22	AI	MISC	If XO25M_SEL=1 short to VDD18	F1: 125MHz LVDS reference Clock (N); F2: 1.2V dc (see application notes on single ended application for this pin).

Signal Name	Ball#	Pad Type	I/F category	If Not Used	Functional Description
RCB_REFCLK0_P	E21	AI	MISC	If XO25M_SEL=1 short to VDD18	F1: 125MHz LVDS reference Clock (P); F2: 125MHz Single-ended reference clock
RESET_IN	E5	Input	MISC	4.7K PU	VS2310 Tx Reset In (Active only when POR_BYPASS=1)
RESET_N	C1	AIO	MISC	WPU	Power on reset bi-directional pin (open drain). 4.7KOhm PU resistor to AVDD33 and 1nF capacitor to GND close to the pin are needed when active (POR_BYPASS=0)
RMII_MAC_RXD[0]	L1	Input	MAC (future use)	GND	RMII MAC Receive Data Bit 0.
RMII_MAC_RXD[1]	K5	Input	MAC (future use)	GND	RMII MAC Receive Data Bit 1
RMII_MAC_RXDV	L2	Input	MAC (future use)	GND	RMII MAC receive Data Valid
RMII_MAC_TXD[0]	L4	O3State	MAC (future use)	NC	RMII MAC Transmit Data Bit 0
RMII_MAC_TXD[1]	L3	O3State	MAC (future use)	NC	RMII MAC Transmit Data Bit 1
RMII_MAC_TXEN	K1	O3State	MAC (future use)	NC	RMII MAC Transmit Enable
SGMAC_CKN	AA1	AO	MAC (future use)	NC	SGMII MAC clock (N)
SGMAC_CKP	AB1	AO	MAC (future use)	NC	SGMII MAC clock (P)
SGMAC_RXN	V2	AI	MAC (future use)	NC	SGMII MAC receive data (N)

Signal Name	Ball#	Pad Type	I/F category	If Not Used	Functional Description
SGMAC_RXP	V1	AI	MAC (future use)	NC	SGMII MAC receive data (P)
SGMAC_TXN	Y2	AO	MAC (future use)	NC	SGMII MAC transmit data (N)
SGMAC_TXP	Y1	AO	MAC (future use)	NC	SGMII MAC transmit data (P)
SGMPHY_CKN	U2	AO	ETH SGMII	NC	SGMII PHY clock (N)
SGMPHY_CKP	U1	AO	ETH SGMII	NC	SGMII PHY clock (P)
SGMPHY_RXN	P2	AI	ETH SGMII	NC	SGMII PHY receive data (N)
SGMPHY_RXP	P1	AI	ETH SGMII	NC	SGMII PHY receive data (P)
SGMPHY_TXN	T2	AO	ETH SGMII	NC	SGMII PHY transmit data (N)
SGMPHY_TXP	T1	AO	ETH SGMII	NC	SGMII PHY transmit data (P)
TCK	H3	Input,PU	FU	NC	Future use.
TDI	G1	Input,PU	FU	NC	Future use.
TDO	H2	O3State	FU	NC	Future use.
TMS	F1	Input,PU	FU	NC	Future use.
TRST	H1	Input,PD	FU	1KPD	Future use. Must be tied to external 1Kohm pulldown resistor
USB_TXR_RKL	C3	AIO		Must Use	Reference resistor. Should be tied to a 44.2 Ohm 1% pull down resistor.
WAKEUP_IN	J1	Input, PU	MISC	NC	Wakeup Input (reserved for future use)
WAKEUP_OUT_ST9	J2	IO	MISC	10K PD	Wakeup Output (reserved for future use); ST: Strap pin #9
XO25M_SEL	E20	Input, PD	MISC	1K PD	Reference clock source select: '1'- 25MHz reference clock, crystal or LVCMOS oscillator; '0'- 125MHz reference clock on RCB_REFCLK0_P/M **NOTE THAT 25MHz CLOCK IS FUTURE USE ONLY**
XO25MHZ_XIN	D21	XTAL	MISC	If XO25M_SEL=0 short to GND	25MHz Crystal clock or LVCMOS oscillator input **NOTE THAT 25MHz CLOCK IS FUTURE USE ONLY**

Signal Name	Ball#	Pad Type	I/F category	If Not Used	Functional Description
XO25MHZ_XOUT	D22	XTAL	MISC	If XO25M_SEL=0 NC	25MHz Crystal clock output **NOTE THAT 25MHz CLOCK IS FUTURE USE ONLY**

2.4.2.2 Rx Non-Functional Signals

Table 15: VS2000RX Non-functional Signal Table

Symbol	Type	Description	Ball Numbers
NC	Non-connected balls	Non-connected balls	B4, A4, D6, B5, C5, A2, B2, C14, D13, D16, D17, D7, E6, E9, U21, U20, U22
NC	Non-connected balls	Future use. Must be tied to ground.	
NS	Not supported	Not supported	AA20, AA19, AA18, AA17, AA15, AA14, AA13, AA12, AB20, AB19, AB18, AB17, AB15, AB14, AB13, AB12, AA16, AB16, W17, W21, AB3, AB4, AB5, AB6, AB8, AB9, AB10, AB11, AA3, AA4, AA5, AA6, AA8, AA9, AA10, AA11, AB7, AA7, W18, T19, T18, V22, R18, V20
NS	Not supported	Not supported – must be connected to GND	U19, W19, W22, V19, W20, V21
FU_D5	Future Use	Reserved. Must be tied to 3.3V external 1K pullup resistor.	D5
FU_J3	Future Use	Reserved. Must be tied to external weak pull-down resistor (27K)	J3
FU_R19	Future Use	Reserved. Must be tied to external weak pull-down resistor (27K)	R19
FU_J4	Future Use	Reserved. Must be tied to ground.	J4
VDD	1.0 V digital supply	1.0 V digital supply	D15, D18, E16, E18, F11, F12, F13, F14, F15, F16, K6, L6, M6, N6, P6, R6, T6, U6, U7, U8, U9, U10, U11, U12, U13, U14, U15, U16, U17, V8, V9, V10, V11, V12, V13, V14, V15, V16, V18

VDD33V	3.3 V supply signals	3.3 V supply signal	E7, F6, F7, F8, F9, F10, F17, G6, G17, H6, H17, J5, J17, K17, L17, M17, N17, P17, R17, T17
AVDD10	1.0 V analog supply signals	1.0 V analog supply signal	C15, C16, C17, C18, C20, C21, D20, F22, Y13, Y15, Y16, Y17, Y19, Y21, AA21, AA22
AVDD18	1.8 V analog supply signals	1.8 V analog supply signal	C6, C7, C8, C9, D4, N2, N3, P3, T3, U3, Y3, Y4, Y5, Y6, Y7, AA2
AVDD33	3.3 V analog supply signals	3.3 V analog supply signal	C10, C11, C12, C13, D8, D10, D12
VSS	Ground signals	Ground signal	A3, A5, A6, A8, A10, A12, A14, A15, A18, A19, A22, B1, B3, B6, B8, B10, B12, B14, B15, B18, B19, B22, C2, C4, C22, D1, D3, D11, D14, D19, E8, E10, E17, F21, G7, G8, G9, G10, G11, G12, G13, G14, G15, G16, H7, H8, H9, H10, H11, H12, H13, H14, H15, H16, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, K7, K8, K9, K10, K11, K12, K13, K14, K15, K16, L7, L8, L9, L10, L11, L12, L13, L14, L15, W8, AB22, A1, L16, M7, M8, M9, M10, M11, M12, M13, M14, M15, M16, N1, N7, N8, N9, N10, N11, N12, N13, N14, N15, N16, P7, P8, P9, P10, P11, P12, P13, P14, P15, P16, R1, R2, R3, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, T7, T8, T9, T10, T11, T12, T13, T14, T15, T16, U18, V3, V17, W1, W2, W3, W4, W5, W6, W7, W9, W10, W12, W13, W14, W15, W16, Y8, Y9, Y10, Y11, Y12, Y14, Y18, Y20, Y22, AB2, AB21

2.4.2.3 Rx Bias Resistors

Bias resistors are used to set an internal bias reference current and should be placed as close as possible to their BGA ball.

Table 16: Reference Resistor Values in VS2000RX

Pin Name	Pin #	Resistor value (ohms)	PU/PD
HDSNK_REXT_H	C19	4.53K	P.D to VSS
HDMISER_RREF	D9	4.02K	P.D to VSS
HDII_CB_RTT_EXRES	W11	1K	P.D to VSS
USB_TXR_RKL	C3	44.2	P.D to VSS

2.4.2.4 VS2000RX Ball Diagram (Top View)

Matrix	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	Matrix
A	VSS	NC	VSS	NC	VSS	VSS	HDMIO_TMDSDATAn[2]	VSS	HDMIO_TMDSDATAn[1]	VSS	HDMIO_TMDSDATAn[0]	VSS	HDMIO_TMDSCLKN	VSS	VSS	HDSNKn[3]	HDSNKn[2]	VSS	VSS	HDSNKn[1]	HDSNKn[0]	VSS	A
B	VSS	NC	VSS	NC	NC	VSS	HDMIO_TMDSDATAp[2]	VSS	HDMIO_TMDSDATAp[1]	VSS	HDMIO_TMDSDATAp[0]	VSS	HDMIO_TMDSCLKP	VSS	VSS	HDSNKp[3]	HDSNKp[2]	VSS	VSS	HDSNKp[1]	HDSNKp[0]	VSS	B
C	RESET_N	VSS	USB_TXR_RKL	VSS	NC	AVDD18	AVDD18	AVDD18	AVDD18	AVDD33	AVDD33	AVDD33	AVDD33	NC	AVDD10	AVDD10	AVDD10	AVDD10	HDSNK_REXT_H	AVDD10	AVDD10	VSS	C
D	VSS	POR_BYPASS	VSS	AVDD18	FU_D5	NC	NC	AVDD33	HDMIO_RREF	AVDD33	VSS	AVDD33	NC	VSS	VDD	NC	NC	VDD	VSS	AVDD10	XO25MHZ_XIN	XO25MHZ_XOUT	D
E	DBG_RXD	DBG_TXD_ST6	CFG_SCL	CFG_SDA	RESET_IN	NC	VDD33V	VSS	NC	VSS	HDMIO_CEC	HDMIO_DDC_SCL	HDMIO_DDC_SDA	HDMIO_5V	HDMIO_HPD	VDD	VSS	VDD	GPIO[28]/MSIO_D[2]	XO25M_SEL	RCB_REFCLK0_P	RCB_REFCLK0_M	E
F	TMS	EE_SDA_MI	EE_SCL_SCK	I2C_SCL_MSTR	I2C_SDA_MSTR	VDD33V	VDD33V	VDD33V	VDD33V	VDD33V	VDD	VDD	VDD	VDD	VDD	VDD	VDD33V	GPIO[27]/MSIO_D[3]	GPIO[26]/MSIO_D[0]	GPIO[25]/MSIO_DO[5]	VSS	AVDD10	F
G	TDI	EE_CS_ST8	EE_MO_ST7	I2C2_SCL_SLAV	I2C2_SDA_SLAV	VDD33V	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD33V	GPIO[31]/MSIO_D[5]	GPIO[29]/MSIO_D[3]	GPIO[22]/MSIO_DO[2]	GPIO[24]/MSIO_DO[4]	GPIO[23]/MSIO_DO[3]	G
H	TRST	TDO	TCK	I2C1_SCL_SLAV	I2C1_SDA_SLAV	VDD33V	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD33V	MSIO_DOUT[4]/I2S_BCLK_OUT/GPIO[14]	GPIO[30]/MSIO_D[4]	GPIO[19]	GPIO[23]/MSIO_D[1]	GPIO[20]/MSIO_DO[0]	H
J	WAKEUP_IN	WAKEUP_OUT_ST9	FU_J3	FU_J4	VDD33V	QVDD25	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD33V	MSIO_DOUT[3]/CIR_OUT/GPIO[13]	MSIO_DOUT[5]/SPDIF_OUT/GPIO[15]	GPIO[16]	GPIO[18]	GPIO[17]	J
K	RMII_MAC_TXEN	GMII_MDIO	GMII_MDC	MAC_RMII_CLK	RMII_MAC_RXD[1]	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD33V	MSIO_DOUT[1]/I2S_DOUT/GPIO[11]	ST10	BT1120_D17	BT1120_D18	BT1120_D19	K
L	RMII_MAC_RXD[0]	RMII_MAC_RXDV	RMII_MAC_TXD[1]	RMII_MAC_TXD[0]	MII_TX_EN	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD33V	MSIO_DOUT[2]/I2S_WCLK_OUT/GPIO[12]	MSIO_DOUT[0]/UART_OUT/GPIO[10]	BT1120_D14	BT1120_D15	BT1120_D16	L
M	MII_TXD[2]/GPIO[0]	MII_TXD[3]	MII_TXD[0]	MII_TX_ERR	MII_TX_CLK	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD33V	MSIO_DIN[5]/SPDIF_in/GPIO[9]	MSIO_DIN[4]/I2S_BCLK_in/GPIO[8]	BT1120_D11	BT1120_D12	BT1120_D13	M
N	VSS	AVDD18	AVDD18	MII_TXD[3]/GPIO[1]	MII_COL/GPIO[2]	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD33V	MSIO_DIN[3]/CIR_in/GPIO[7]	MSIO_DIN[2]/I2S_WCLK_IN/GPIO[6]	BT1120_D9	BT1120_CLK	BT1120_D10	N
P	SGMPHY_RXP	SGMPHY_RXN	AVDD18	MII_RX_DV_ST4	MII_CRS/GPIO[3]	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD33V	MSIO_DIN[0]/UART_IN/GPIO[4]	MSIO_DIN[1]/I2S_DIN/GPIO[5]	BT1120_D6	BT1120_D7	BT1120_D8	P
R	VSS	VSS	VSS	MII_RX_ERR_ST5	MII_MDC	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD33V	NS	FU_R19	BT1120_D3	BT1120_D4	BT1120_D5	R
T	SGMPHY_TXP	SGMPHY_TXN	AVDD18	MII_RXD[3]_ST3	MII_MDIO	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD33V	NS	NS	BT1120_D0	BT1120_D1	BT1120_D2	T
U	SGMPHY_CKP	SGMPHY_CKN	AVDD18	MII_RXD[2]_ST2	MII_RX_CLK_ST11	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VSS	NS	NC_U20	NC_U21	NC_U22	U
V	SGMAC_RXP	SGMAC_RXN	VSS	MII_RXD[1]_ST1	MII_RXD[0]_ST0	UCC_0	UCC_1	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VDD	NS	NS	NS	NS	V
W	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	HDII_CB_RTT_EXRES	VSS	VSS	VSS	VSS	VSS	NS	NS	NS	NS	NS	NS	W
Y	SGMAC_TXP	SGMAC_TXN	AVDD18	AVDD18	AVDD18	AVDD18	AVDD18	VSS	VSS	VSS	VSS	VSS	AVDD10	VSS	AVDD10	AVDD10	AVDD10	VSS	AVDD10	VSS	AVDD10	VSS	Y
AA	SGMAC_CKN	AVDD18	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	AVDD10	AVDD10	AA
AB	SGMAC_CKP	VSS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	VSS	VSS	AB
Matrix	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	Matrix

Figure 14: VS2000RX Ball Diagram

3 Functional Description

3.1 HDMI Interface

The VS2310/VS2000 chip family includes an HDMI 2.0-compatible interface. The VS2310TX/VS2000TX receives HDMI traffic from a source, converts the traffic into HDBaseT packets (T-packets) and forwards them to the link. On the VS2310RX/VS2000RX side, the HDMI interface extracts T-packets with HDMI traffic from the HDBaseT link, converts them back to HDMI and transmits them via the HDMI port.

There are two types of HDMI signals:

- TMDS Signals – includes differential data signals and the differential clock signal.
- HDMI Control Signals – includes all control signals defined in the HDMI 2.0 standard (DDC, 5V, HPD, and CEC).

3.1.1 TMDS Signals

This group contains four pairs of unidirectional differential signals:

- Three differential pairs are used for the HDMI serial data transfer. The data is driven by a TMDS transmit PHY on the VS2310RX/VS2000RX chip or received by the VS2310TX/VS2000TX chip. The data rate on the TMDS data line can reach up to 3.4 GHz.
- The fourth differential pair is the TMDS clock that is generated by the HDMI transmitter. The frequency of the clock signal is one tenth of the actual serial data rate. The HDMI PHY receiver uses this clock signal to generate the serial clock used for HDMI data recovery.

The VS2310/VS2000 HDMI transmitters incorporate specialized capabilities suited to dealing with the broad bandwidth of TMDS signals and varying HDMI cable lengths in order to maintain signal quality. For example:

- A TMDS driver with configurable signal pre-emphasis capabilities.
- The VS2310/VS2000 transmitter supports a double termination feature.
- The VS2310TX/VS2000TX HDMI receiver uses an internal adaptive equalizer to improve its signal detection capabilities. The adaptive equalization process is done automatically after the receiver powers up and the optimal equalizer (in terms of BER) is selected.
- The receiver handles two termination types – AC and DC termination.
- The 3 HDMI data lanes in the VS2310TX/VS2000TX are swappable.

3.1.2 HDMI Control Signals

This group contains the following signals:

- **HPD** – This signal is an HDMI Rx device output (VS2310RX/VS2000RX input and VS2310TX/VS2000TX output) that is sent towards the source HDMI equipment, indicating that the sink E-EDID memory is available for reading. The Hot Plug Detect pin can be asserted only when the +5V Power signal from the source is detected.
- **5V** – This signal is output from the source HDMI device (VS2310TX/VS2000TX input and VS2310RX/VS2000RX output). The HDMI 5V signal is pass-through (by default) – that is, it is only shown on the VS2310RX/VS2000RX output when an HDBaseT link is established and the HDMI Source is connected and outputting its 5V control signal.
- **CEC** – The CEC line is used for high-level user control of HDMI-connected devices.
- **DDC** – This is a two-wire bidirectional I2C interface used for HDMI control. Any HDMI device connected to a VS2310/VS2000 device must support the I2C clock stretching mechanism.

Note that the HDMI specification requires special treatment for these signals such as pull-up or pull-down resistors. You must utilize these requirements on your board according to the HDMI specification.

3.2 Ethernet System

3.2.1 General

The VS2310/VS2000 functions as a 100BaseTX PHY device. The figure below shows two Ethernet systems on both sides of an HDBaseT link. Both the display system and the source system are network enabled devices and embed MAC devices. The system is connected to the home network over an HDBaseT connection. In this case, the display system side is connected to the home switch or router. A switch / router may be connected on either side of the HDBaseT link.

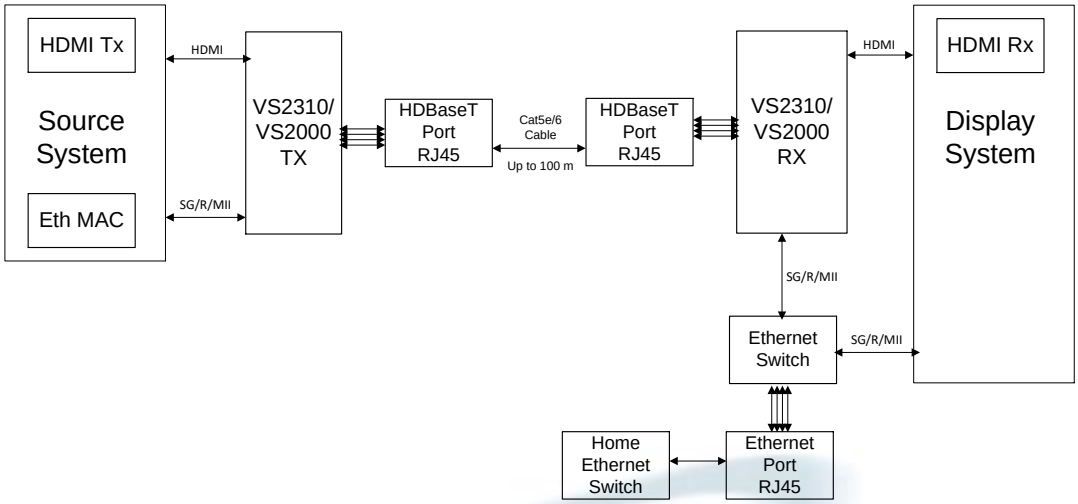


Figure 15: VS2310/VS2000 Ethernet System

The VS2310/VS2000 devices support three possible Ethernet interfaces: MII, RMII and SGMII. Selecting the preferred interface is done by asserting the strap pins #3 and #8 during chip reset. Refer to section 6.1 for more on MII/RMII/SGMII Interface Selection.

3.2.1.1 MII

The VS2310/VS2000 devices use the standard MII interface (IEEE802.3u) to transfer 100BaseTX Ethernet data over the HDBaseT link or in Ethernet fallback mode. Both VS2310 devices behave as Ethernet PHY devices and, as such, should be connected to an Ethernet MAC device in order to transfer bidirectional full duplex data.

The MII interface defines a 4-bit wide data path for transmitting and receiving data that is clocked at 25 MHz to provide the required 100 Mbps transfer speed. The MII interface output two clock signals as reference clocks: *MII_RX_CLK* and *MII_TX_CLK*.

Valens recommends *not* to use these clock signals for other system purposes because in some cases this clock is disabled (e.g. when the VS2310/VS2000 operational mode is LFFP1). For more information, refer to the IEEE802.3u standard.

IMPORTANT

When Ethernet functionality is not required, set the Ethernet interface to **MII** in order to ensure correct operation of the HDBaseT link.

For new designs requiring Ethernet functionality, it is strongly recommended to use the RMII or SGMII interface rather than the MII interface.

3.2.1.2 RMII

RMII uses independent 2-bit wide transmit *MII_TXD[0:1]* and receive *MII_RXD[0:1]* data buses synchronized to a common 50MHz reference clock. The RMII reference clock is input to the VS2310/VS2000 on pin *MII_TX_CLK*, and may be sourced by the MAC or from an external source (such as an oscillator).

When working in RMII mode, the MII_RX_CLK output is not supported and should not be fedback to the MII_TX_CLK nor provided to any other devices on the board. In order to provide a 50MHz clock, the designer must use an external clock (e.g. Oscillator) to drive the MII_TX_CLK input.

NOTE

When RMII is selected, pins *MII_TXD[2:3]* are allocated as GPIO and are not used for Ethernet connectivity.

Table 17: RMIIClkOutputEn Configuration – Reserved for Future Use Only

Parameter Value	Definition
System.Ethernet.RMIIClkOutputEn = 0	50MHz RMII clock is not output on pin MII_RX_CLK
System.Ethernet.RMIIClkOutputEn = 1	(default) 50MHz RMII clock is output on pin MII_RX_CLK and can be used on the board to drive MII_TX_CLK input on VS2310/VS2000.

3.2.1.3 SGMII

The Serial Gigabit Media Independent Interface is supported. This interface includes three differential pairs of signals: a clock pair (typically left unconnected), receive data pair and a transmit data pair. The 625 MHz clock pair is an output of the VS2310/VS2000.

NOTES

Although originally designed to support up to 1Gbps rates, when using SGMII over HDBaseT, only 100Mbps rates are supported – that is, a x10 data repetition is performed.

A MAC device must be present on both sides of each HDBaseT link segment. In other words, there must be Ethernet termination next to each HDBaseT port since HDBaseT networking does not handle Ethernet packet routing and switching.

3.2.2 Serial Management IF (MDIO)

Both VS2310/VS2000 chipsets support the MII management interface over the MII_MDIO and MII_MDC pins. This is a two-bit interface (a bidirectional serial data bit and a clock signal) that allows addressing the PHY management registers by a MAC device. Only the MAC can initiate MDIO transactions, which can be either write (to control registers) or read (from status registers).

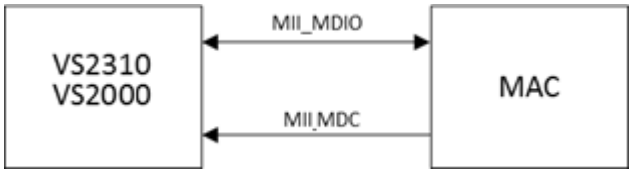


Figure 16: MDIO Topology

The IEEE 802.3 standard defines three different register groups:

- Basic (addresses 0 – 1)
- Extended (addresses 2 – 15)
- Vendor Specific (addresses 16 – 31)

The VS2310/VS2000 supports SMI registers 0 through 6 as required by Clause 22 of the IEEE 802.3 standard. Non-supported Extended registers and Vendor Specific registers will be read as hexadecimal “FFFF”.

The device’s MDIO/MDC PHY Address default value is '00000'. It may be configured using the parameter System.Ethernet.MIIPhyAddress.

MDC/MDIO timing, frame structure and a full registers description is as defined by clause 22 of the IEEE 802.3 standard.

3.2.3 Ethernet Fallback

When the VS2310/VS2000 HDBaseT port is connected to a standard Ethernet device, it automatically reverts to operation as a 100BaseTX Ethernet port, according to the IEEE 802.3u specification (that is, the VS2310/VS2000 chip functions as a 100BaseTX PHY).

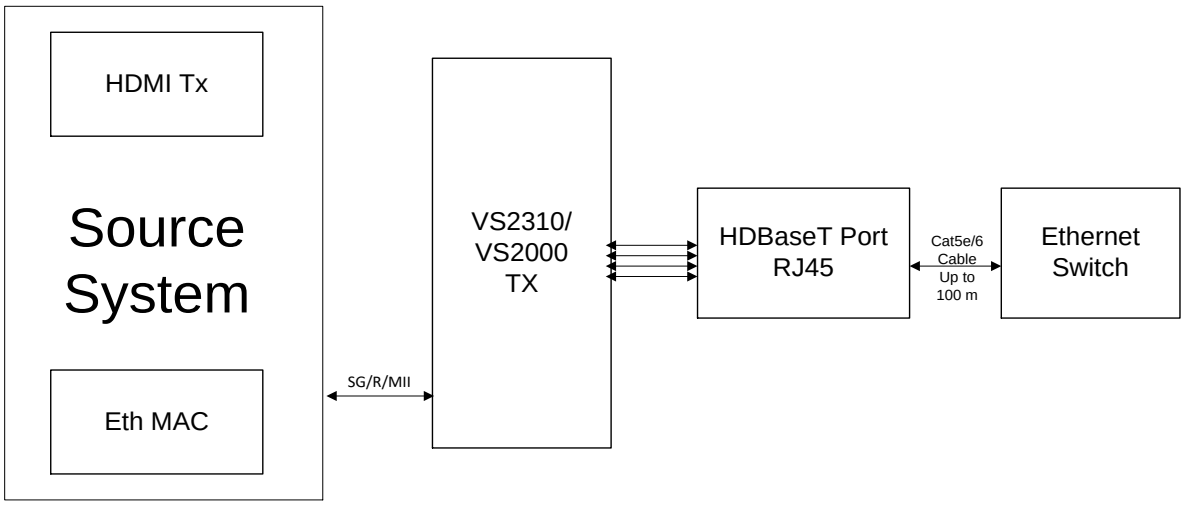


Figure 17: VS2310TX/VS2000TX in Ethernet Fallback Mode

3.3 HDBaseT Interface

VS2310/VS2000 chips use a four-pair STP/UTP cable to transfer AV data over a CATx cable. Figure 18 illustrates conceptual schematics of how the VS2310/VS2000 RX and TX devices should be connected to the UTP cable when the link is not used to transfer power.

The four-differential HDBaseT pairs in the VS2310/VS2000 are connected to a transformer and to pull-up resistors. The transformer is connected to the STP/UTP cable via an RJ45 connector.

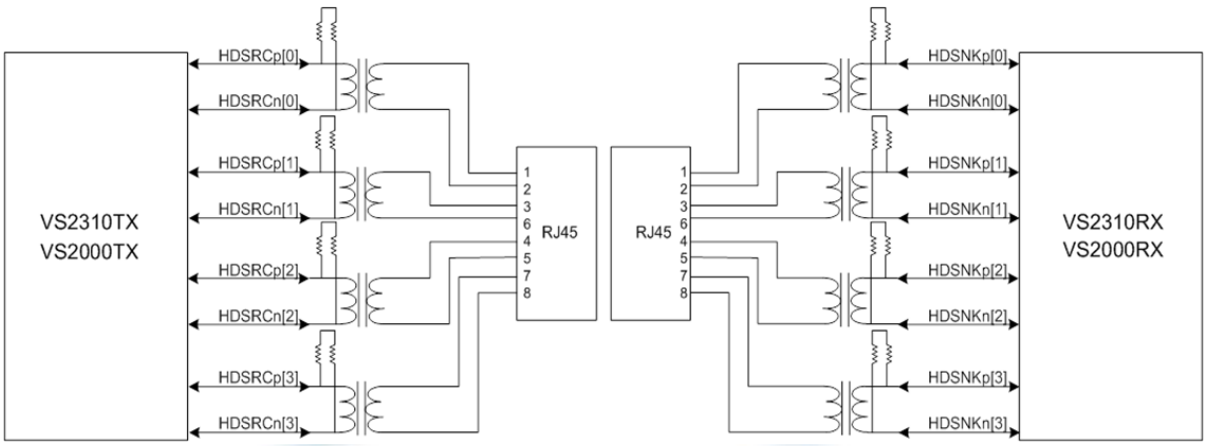


Figure 18: VS2310TX/VS2000TX and VS2310RX/VS2000RX Link Connection Example

The pair order in the VS2310/VS2000 HDBaseT interface may be swapped. The HDBaseT PHY automatically detects pairs coupling. Three different configurations are supported: straight, crossover and semi-crossover as shown below:

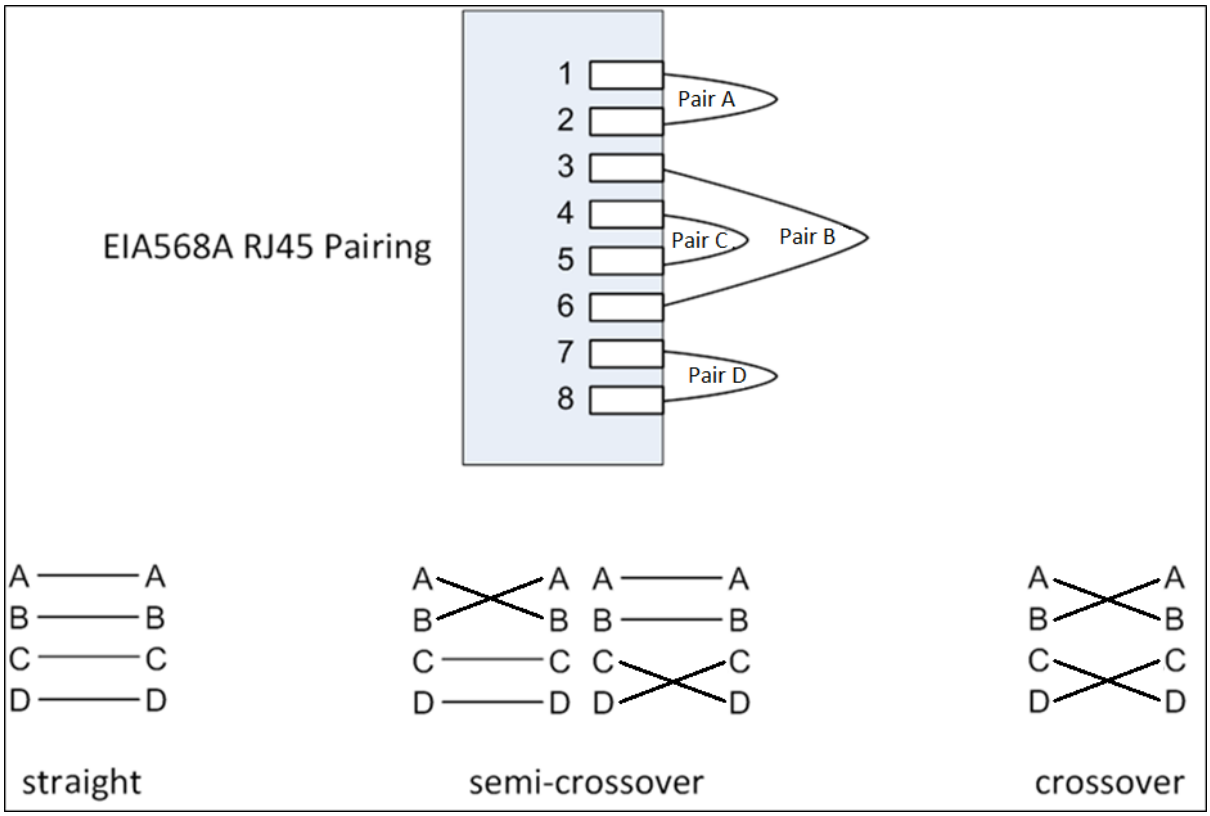


Figure 19: VS2310/VS2000 RX and TX Pair Coupling

3.4 USB Functionality

The VS2310TX and VS2310RX chips include USB2.0 support for seamlessly extending USB2.0 traffic over the HDBaseT link. These components include:

- Embedded USB2.0 PHY transceiver
- A serial interface engine
- Two types of USB interfaces: USBD and USBH

Both VS2310RX and VS2310TX chips include a USB2.0 T-Adaptor block. The T-adaptors are responsible for converting USB2.0 traffic into T-packets for transfer over the HDBaseT link. This block may be configured by SW parameter to function as either a USBH T-Adaptor or a USBD T-Adaptor and connect either a host or a device respectively. An HDBaseT link with a USBH T-adaptor on one end and a USBD T-adaptor on the other end may be considered a USB2.0 HUB with the upstream port and downstream port. This is shown in the figure below:

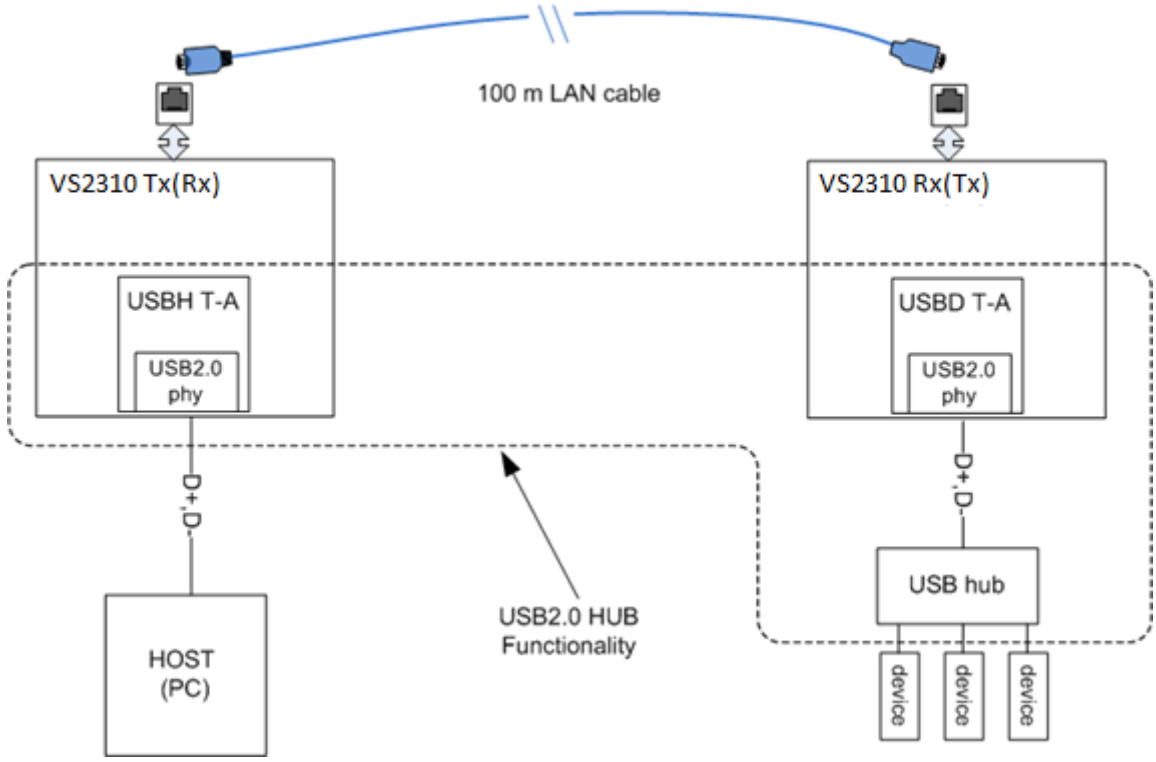


Figure 20: USB2.0 Extension Over HDBaseT Link

Note that the USBD T-adaptor performs an enumeration process with all devices and hubs connected to it. This means that the host sees a flattened tree that includes all devices without cascaded hubs (if present).

Up to 7 USB devices are supported by the USB hub.

The VS2310 chipset supports isochronous transfers for USB webcams, microphones, and speakers.

Refer to the Firmware Release Note for additional information on supported USB functionality.

NOTE

The state of the USB D+ and D- pins is not defined during the Colligo reset state. For some Colligo devices, while the device is in reset state and Vbus is active, USB pins D+ and/or D- may be in a High state. Refer to Application Notes AN2001 (Hardware Design Guidelines) and AN2050 (USB Interface) for additional information and system considerations.

3.5 External Boot Memory I/F

VS2310/VS2000 chips can be connected to an external SPI Flash memory for storage of software and important system parameters. An SPI interface is used for CPU access to the memory.

NOTE

It is also possible to utilize the SPI interface to update the firmware, although this requires special handling. Refer to the *Hardware Design Guideline Application Note* for additional information.

3.6 UART T-Adaptor Functionality

The UART T-adaptor converts native UART traffic from the UART interface (*MSIO_DI0 / UART_TX, MSIO_DO0 / UART_RX*) into HDBaseT packets. UART HDBaseT packets may be transmitted over the link to the partner device. The UART T-adaptor may be configured to two modes of operation:

- Pre-configured
- Oversampled

3.6.1 Working in Pre-configured mode

In this mode, the UART baud rate is known a priori to both partners. This mode is more efficient with respect to data rate consumption. It is recommended to use this mode when high UART rates are required in LPPF1/2 HDBaseT modes. The table below illustrates how to configure a system to preconfigured UART mode:

Table 18: UART Pre-configured Parameter Settings

Parameter Name	Description
TAConf.UART.Mode	Pre-configured
TAConf.UART.BaudRate	The required discrete baud rate (maximum 115.2 Kbps currently supported)
TAConf.UART.CharLen	The required character length (5,6,7 or 8 bits)
TAConf.UART.OversampleRate	Don’t care (leave as default)
TAConf.UART.ParityBit	The required parity true/false
TAConf.UART.StopBit	The required number of stop bits (none, one or two bits)

3.6.2 Working in Oversampled Mode

In this mode, the UART baud rate is unknown a priori. This mode is typically used when a PC with DTE client is connected and the baud rate depends on the managed equipment which may change between setups. In oversampled mode, the UART TX and RX lines are sampled using a 1.5MHz sampling clock on one side and recovered using a recovery clock on the partner's side.

The table below illustrates how to configure a system to oversampled UART mode:

Table 19: UART Oversampled Parameter Settings

Parameter Name	Value
TAConf.UART.Mode	Oversampled
TAConf.UART.BaudRate	Don't care (leave as default)
TAConf.UART.CharLen	Don't care (leave as default)
TAConf.UART.OversampleRate	Fixed, read only field
TAConf.UART.ParityBit	Don't care (leave as default)
TAConf.UART.StopBit	Don't care (leave as default)

NOTE

When using oversampled UART in LPPF mode, the maximum supported baud rate is 115.2 Kbps.

3.7 IR T-Adaptor Functionality

Two IR T-adaptors are available on both VS2310/VS2000 RX and TX chips.
These T-adaptors convert native infrared traffic from the CIR interface (*MSIO_DI3/CIR_IN, MSIO_DO3/CIR_OUT*) into HDBaseT packets. CIR HDBaseT packets may be transmitted over the link to the partner device.

The IR signal input from the *CIR_IN* signal is oversampled by the CIR-Tx T-adaptor and transferred over the link in an HDBaseT packet format. The CIR-Rx T-adaptor receives the CIR T-packets and recovers the original IR wave over the *CIR_OUT* signal. On each side, the user assigns the attributes of its received/transmitted CIR signal using the CIR T-adaptor info parameters.

3.8 I²S T-Adaptor Functionality

Two I²S audio T-adaptors are available on both VS2310/VS2000 RX and TX chips.
These T-adaptors convert native I²S audio traffic from the I²S input interface into HDBaseT packets:

- MSIO_DIN[1]/I2S_DIN/GPIO[5]
- MSIO_DIN[2]/I2S_WCLK_IN/GPIO[6]
- MSIO_DIN[4]/I2S_BCLK_IN/GPIO[8]

On the other side of the link, the native I²S signals are recovered via the pins:

- MSIO_DOUT[1]/I2S_DOUT/GPIO[11]
- MSIO_DOUT[2]/I2S_WCLK_OUT/GPIO[12]

- MSIO_DOUT[4]/I2S_BCLK_OUT/GPIO[14]

The maximum I2S BCLK rate currently supported is 5MHz.

NOTE

Special care should be taken when selecting an audio DAC device. The designer should be aware that the Audio DAC device must include an integrated PLL. Using an audio DAC without an integrated PLL may result in audio corruption.

3.9 SPDIF Functionality

Two SPDIF audio T-adaptors are available on both VS2310/VS2000 RX and TX chips. These T-adaptors convert native SPDIF audio traffic from the SPDIF input interface (*MSIO_DIN[5]/SPDIF_in/GPIO[9]* pin) into HDBaseT packets. On the other side of the link, the SPDIF output signal is recovered via the pins: *MSIO_DOUT[5]/SPDIF_OUT/GPIO[15]*.

The configuration of the SPDIF T-Adaptor is fixed. The maximum allowed audio frame rate for this interface is 192K frames per seconds.

3.10 I²C T-Adaptor Functionality

Valens Colligo VS2310 and VS2000 devices have the ability to extend native I²C data across the HDBaseT link through the I²C T-Adaptors. This is in addition to the I²C interfaces provided for the HDMI DDC control bus and the external SPI Flash.

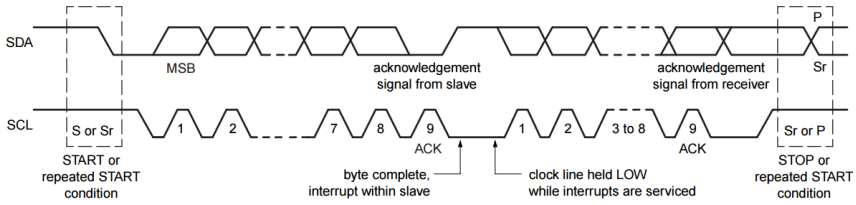


Figure 21: Native I²C Data Transfer (Ref: I2C-Bus Specification, Rev.6)

The number and type of native I²C ports depends on the device:

- VS2310/VS2000 TX 2 Master ports, 1 Slave port
- VS2310/VS2000 RX 1 Master port, 2 Slave ports

A Colligo Master port should be connected to an external Slave, whilst a Colligo Slave port should be connected to an external Master.

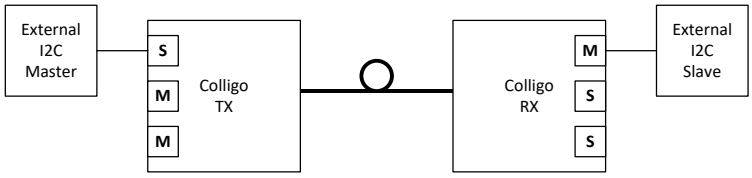


Figure 22: Valens Colligo I²C T-Adaptors and Connectivity

The external Master can work at data rates up to 100Kb/s. Data is transferred across the HDBaseT link bit-by-bit at the rate set by the external Master's SCL clock, and output at the far-end of the link on the Colligo's Master port.

For Read transactions (external I²C Master reads data from the external I²C Slave), the Colligo I²C Master "understands" that it must reply back to the Colligo I²C Slave with valid data from the external Slave. Therefore, the Colligo I²C Master does not need to wait for bits to arrive from the external I2C Slave (which would reduce the transaction baud rate), and the transaction with the external Slave occurs at the full 100KHz speed.

For Write transactions (external I²C Master writes data to the external I²C Slave), should the data rate be less than 100Kb/s, the Colligo Master port outputs the SCL clock with a pulse width of 5µs (equivalent to 50% of a 100KHz period), but with a duty cycle which matches the external Master's clock rate. Note that the Colligo Master port only works at 100KHz clock rate, but support slower data rates using this method.

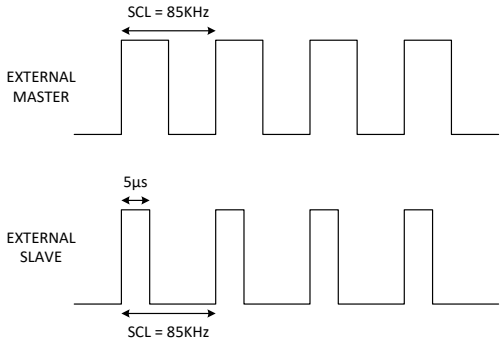


Figure 23: I²C Interface Timing Representation (Example)

Note that the Valens Colligo I²C T-Adaptors support stretching of up to 250µS by an I²C external Slave.

3.11 HDI Interface

The VS2310 RX and TX chips support the proprietary HDI input and output digital interfaces. The HDI bus enables the transfer of HDBaseT packets (at speeds of 8 Gbps) directly between the VS2310 and another device that supports the HDI interface.

As with all HDBaseT interfaces, the HDI comprises a main channel (downstream) and an auxiliary return channel (upstream), meaning that all HDBaseT traffic types can be supported.

Both HDI input and output interfaces comprise an 8-bit differential LVDS main channel bus, 3-bit auxiliary channel bus, and the various clock and control signals required for both buses. (See the interface diagrams in section 2.1).

The HDI interface is used to connect VS2310 with VS2311, creating an HDBaseT fiber application as well as HDI connectivity to a second VS2310, creating applications such as switching and daisy-chaining. HDI output data from one source can be seamlessly merged with data from a local T-adaptor (such as an HDMI source) and transmitted over a single HDBaseT link to multiple daisy-chained displays. Refer to Figure 2 to see a sample application diagram.

3.12 LVDS Interface

The VS2310 chipset includes an LVDS-compatible interface. The VS2310TX receives LVDS traffic from a source, converts the traffic into HDBaseT packets (T-packets) and forwards them to the link. On the VS2310RX side, the T-packets containing LVDS traffic are extracted from the HDBaseT link, converted back to native LVDS and then output as LVDS traffic within the sink.

The LVDS interface is arranged into two discrete buses (LVDS0 and LVDS1), each of which comprises a Main Channel. Both input and output interfaces comprise an 8-bit differential LVDS main data channel bus plus differential clock (LVDS group). There is no support for Auxiliary Channel over the LVDS interface.

The VS2310 devices support standard 7:1 LVDS (7 data bits per clock cycle), bit exact with no parsing mode.

When configured to work as LVDS, both buses in the VS2310TX become inputs and both buses in the VS2310RX become outputs.

The LVDS interface can operate in 3 possible modes: single, dual and twin (please refer to Valens Application Note *AN2051 – HDI / LVDS / DigIF Interface* for further information). The maximum throughput in all modes is 7.2 Gb of data, so the number of lanes, ports and the clock frequencies need to be calculated carefully per application.

In dual mode, there is a 2UI offset between LVDS0 and LVDS1. Note that when working in LVDS dual mode with 4 data lanes per port and LVDS clock greater than 80MHz, a skew greater than 2UI may on occasion occur between the ports.

NOTE

The LVDS interfaces is supported over Cat5e cables up to 90m (295ft) in length or Cat6 cables up to 100m (328ft) in length.

3.13 DigIF Interface – Supported in Future Release

The VS2310 chipset includes an DigIF LVDS-compatible interface that enables RGB data (or other formats) to be extended over an HDBaseT link.

The DigIF interface in the VS2310 comprises up to 34 bits of data (two 17-bit physical ports that combine to create a 34-bit logical port) and 2 clocks. For RGB traffic, for example, the 30 data bits are allocated as follows:

- Red: 10 bits
- Green: 10 bits
- Blue: 10

The DigIF bus requires a 3.3V to 1.8V level shifter (or vice versa) in order to interface with standard RGB devices.

For further information, refer to Valens Application Note *AN2051 – HDI / LVDS / DigIF Interface.*

3.14 BT.1120 Interface

BT.1120 is an internal interface widely used in camera and DVR applications. The VS2310 and VS2000 chipsets provide the ability to extend this interface over an HDBaseT link for enhanced range.

The VS2310 and VS2000 have a 21-bit BT.1120 interface comprising:

- 20-bit video data (10b Chroma and 10b Luminance) + embedded controls
- Clock

The supported formats for the BT-1120 interface are 720p and 1080p/60/4:2:2, which use clock speeds 74.25MHz and 148.5MHz respectively. In both cases, the parallel data input width is 20-bit.

NOTE

The BT-1120 interface supports embedded controls only. H:V:F timing must be provided as embedded TRS ID words in the parallel data. It is not possible to use external H_Blanking, V_Blanking, and F_Digital signals.

3.15 Multistreaming Support

The VS2310 chipset supports simultaneous use of HDMI and LVDS/DigIF interfaces, in which the two dedicated physical ports are used for two separate streams, while sharing the available bandwidth:

- HDMI
- LVDS or DigIF (DigIF will be support in a future release)

NOTE

System developers should take care not to exceed the total available bandwidth.

4 Traffic Rate Specification

The auxiliary channel has an aggregated traffic budget of 300 Mbps. For T-Adaptors, the budget is 280 Mbps (due to additional overhead) that is shared between the T-adaptors that are enabled by the application. Enabling or disabling T-adaptors is possible using *system.FeatureList.<T-adaptor name>.class of parameters*.

When a T-adaptor is enabled, its native data packets consume traffic rate budget according to the values specified in Table 20 below.

Table 20: T-Adaptor Auxiliary Channel Traffic Consumption

	Consumed bit rate (Mbps)	
Feature	**Active (Double-Aux)**	**Long Reach Mode**
Aggregated budget	280	130
Ethernet	100	100
SPDIF	18	18
I2S	12	12
UART (oversampled @115200 baud)	3	3
MSIO	6	6
CIR (oversampled, pass-through)	0.5	0.5
HDMI controls (DDC, 5V,HPD)	3.3	3.3
I2C (all 3 user channels)	10	10
Total Excluding USB	152.8	152.8 – not possible!
USB	Best Effort - utilizes remaining available bandwidth. For example, in Active mode when all the features above are active, USB can utilize 280 – 152.8 = 127.2 Mbps. In Long Reach mode, there will be bandwidth exhaustion if all T-Adaptors are enabled.	

5 HDBaseT Operational Modes

5.1 Overview

The VS2310/VS2000 runs in the following HDBaseT operation modes:

- Low Power Partial Functionality (LPPF), with 2 sub-modes of operation:
  - LPPF1
  - LPPF2
- Active HDBaseT (ACTIVE)
- Ethernet Fallback (FB)
- Long Reach (LR)

During transitions between HDBaseT Operation Modes, there is no signal continuity on the chip interfaces.

5.2 Modes

5.2.1 Ethernet Fallback (FB)

Ethernet Fallback (FB) mode is entered when the link partner is identified as a non-HDBaseT legacy partner (e.g. Ethernet). In this mode a standard legacy link is established between the link partners.

5.2.2 Low Power Partial Functionality (LPPF)

In Low Power Partial Functionality (LPPF) mode, a low-power communication link is established between two HDBaseT devices:

- LPPF1 – without Ethernet connectivity. The following modules are powered down: HDMI Data stream, I2S Interface, SPDIF Interface, I2C Interface, MSIO Interface, DSP Phy, Ethernet (Fallback) Phy
- LPPF2 – with Ethernet connectivity. The following modules are powered down: HDMI Data stream, I2S Interface, SPDIF Interface, I2C Interface, MSIO Interface, DSP Phy

If Ethernet is enabled in the “feature list” parameter, the LPPF2 mode is entered. If Ethernet is disabled, the LPPF1 mode is entered.

5.2.3 Active HDBaseT (ACTIVE)

In Active HDBaseT (ACTIVE) mode, the HDBaseT port establishes a high throughput link with its link partner using downstream/upstream sub-links.

5.2.4 Long Reach (LR)

Long Reach (LR) mode enables operation over longer cable runs (up to 150m/492ft) through the reduction of the symbol rate over the HDBaseT link.

5.2.4.1 Limitations of Long Reach Mode

When running in LR mode, the maximum HDMI pixel clock supported is 148.5MHz (equivalent 1080p/60 video format). When using the LVDS interface, only 3.6Gb/s of video bandwidth is available which (for example) is suitable for 6 LVDS lanes running at 65MHz LVDS clock speed (refer to Valens Application Note AN2051 for details on how to calculate the LVDS bandwidth consumption).

Due to the bandwidth reduction of the Auxiliary channel when operating in LR mode, contentions may occur between Ethernet and other native interfaces. In Long Reach mode, there is approximately 130Mb/s of Auxiliary channel bandwidth available, shared among all non-video interfaces. Ethernet consumes 100Mb/s, meaning that all other interfaces share approximately 30Mb/s.

Running Ethernet and MSIO interfaces simultaneously may result in the loss of MSIO packets. With Ethernet operating at 100% utilization, MSIO packet loss will occur if the MSIO configuration is as follows:

- 1 or more MSIO channels with 1.5MHz sampling rate
- 2 or more MSIO channels with 1.0MHz sampling rate
- 3 or more MSIO channels with 0.5MHz sampling rate

Further, in Long Reach mode only USB HID devices (keyboard, mouse, touch-screen, etc) should be used with Ethernet disabled. If Ethernet is enabled, it is recommended to check HID functionality to ensure bandwidth limitations are not exceeded.

The performance of other T-Adaptors may also be affected if Ethernet is enabled in LR mode. Table 20 lists the approximate bandwidth consumption per T-Adaptor, and should be used when considering using LR mode.

Table 21 presents the system state with regard to mode selection behavior for all possible combinations at both ends of the link. The white cells indicate the state of the system. Note that the far-end of the link can be any Valens device.

Table 21: System State per Selection Mode on Local and Remote Sides

		Mode Selected on Remote Side			
		LPPF1	LPPF2	Long Reach	HDBaseT
Mode Selected on Local Side (VS2310/VS2000)	HDBaseT	LPPF1	LPPF2	Long Reach	HDBaseT
	Long Reach	LPPF1	LPPF2	Long Reach	Long Reach
	LPPF2	LPPF1	LPPF2	LPPF2	LPPF2
	LPPF1	LPPF1	LPPF1	LPPF1	LPPF1

5.3 Events

The table below describes the events leading to Operating Mode changes.

Table 22: Operating Mode Events

Event Name	Description
Link Loss	Any event that causes a link loss
Operation Change Mode Request	As defined in the HDBaseT Specification
Wakeup	Event causing a transition from LPPF to ACTIVE
Standby	Event causing a transition from ACTIVE to LPPF

5.3.1 Auto-LPPF Functionality

Mode transitions between Active and Low-Power modes are possible through different mechanisms:

- Manual control using Host Interface parameters to specify the required operating mode. Mismatches between the requested operating modes of the link partners are resolved according to table 22 above.
- Automatic mode transitions based on certain events (“Auto-LPPF”)

Auto-LPPF allows for Colligo devices to enter and exit LPPF mode without the intervention of any external control element (such as an on-board controller). Trigger events can be defined, the presence - or absence - of which result in the mode transition. These triggers are as follows:

- HDMI video (TMDS clock)
- USB traffic

The triggers are configurable via boot-time (bring-up) parameters, which in turn defines the exact behavior of the Auto-LPPF mechanism. Auto-LPPF can interoperate with VS100/VS010 link partners, as well as with link partners operating in manual mode.

Refer to Valens Application Note AN2015 – Firmware Parameter Descriptions for information on the Auto-LPPF configuration settings.

6 Configuration and Management

Configuring the VS2310/VS2000 chip can be achieved by the following methods:

- HW Strap Pins – Values are latched upon exiting reset
- Soft straps (GPIOs) – Asserting GPIO inputs during application bring-up
- Parameters – Configuring VS2310/VS2000 parameter values in the external FLASH memory
- Host Interface – Configuring VS2310/VS2000 parameters during run time or immediately after reset and before link establishment.

A VS2310/VS2000 device is capable of managing its remote link partner using the host interface commands. Management messages are transferred over the main and auxiliary HDBaseT channels.

6.1 HW Strap Pins

Hardware strap pins are used to configure the chip's operational mode. These pins are sampled at the rise of the reset signal. After they are sampled, these pins regain their default run-time functionality.

Table 23: VS2310/VS2000 RX/TX HW Strap Pin Description

STRAP Pin	Pin Name	Default (Internal PU/PD)	Strap Functionality
Strap[0]	MII_RXD[0]_ST0	PD	Strap bits 0-2 define the 3 LSB bits of the VS2310/VS2000 configuration I2C slave device address. The 7 bit I2C address of VS2310/VS2000 is set as follows: I2C address = {4'b0101, A2, A1, A0} Where A2, A1 and A0 are the values of MII_RXD[2]_ST2, MII_RxD[1]_ST1 and MII_RXD[0]_ST0 during reset respectively.
Strap[1]	MII_RxD[1]_ST1	PD	
Strap[2]	MII_RXD[2]_ST2	PD	
Strap[3]	MII_RXD[3]_ST3	PU	This strap bit, together with strap bit #8 defines the mode of the Ethernet PHY interface: {Strap #8, strap #3} = '00': MII interface mode. This mode **must** be used when Ethernet functionaitly is not required. '01': RMII interface mode '10' :SGMII interface mode '11': Illegal selection
Strap[4]	MII_RX_DV_ST4	PU	Defines the type of interface for the external FLASH device: '0' -SPI '1' - Reserved

STRAP Pin	Pin Name	Default (Internal PU/PD)	Strap Functionality
Strap[5]	MII_RX_ERR_ST5	PD	Defines if the VS2310/VS2000 boots from internal or external memory: '0' - Internal '1' - External
Strap[6]	DBG_TXD_ST6	PU	This strap bit, together with strap bit #7 and strap bit #10 define the external FLASH memory size as follows: [strap#10, strap#7, strap#6] = [110] - 2MB (16Mbits) All other bit combinations are illegal.
Strap[7]	EE_MO_ST7	PD	This strap bit, together with strap bit #6 and strap bit #10 define the external FLASH memory size. See strap #6 above for a full description.
Strap[8]	EE_CS_ST8	PD	Ethernet PHY interface mode select. See description above in strap[3]
Strap[9]	WAKEUP_OUT_ST9	None*	This strap bit selects one of two options for the page bit location (address bit 16) in an I2C FLASH memory '0' -Page/block bit is in Bit[16] of the I2C command '1'- Page/block bit is in Bit[18] of the I2C command If your memory device uses SPI interface, the value of this strap is ignored.
Strap[10]	ST10	None*	This strap bit, together with strap bit #6 and strap bit #7 define the external FLASH memory size. See strap #6 above for a full description.
Strap[11]	MII_RX_CLK_ST11	None*	Selects the MAC interface type: '0' – RMII '1' - SGMII

** IMPORTANT: The strap pins MII_RX_CLK_ST11, ST10 and WAKEUP_OUT_ST9 do not have internal default pullup/pulldown resistors. They must be tied to a weak pullup/pulldown resistor on the board.*

6.2 SW Strap Pins

The pins listed in Table 24 are used to configure firmware behavior. These pins may be left unconnected if the default internal pad resistor value is suitable for the application. You can assert these pins on your board (typically using dip-switch buttons or using external pullup/pulldown) to change the FW default configuration. These SW strap pins are only sampled upon reset.

Table 24: SW Strap Pin Description

Pin Name	Soft Strap Functionality	Default (by internal pad pullup/down value)
MII_COL/GPIO[2]	Long reach (LR) mode request: '0' – Activate the link in HDBaseT mode '1' – Activate the link in long reach mode Must be deactivated using Update Parameters (LR function is currently enabled by default)	1
MII_CRS/GPIO[3]	WaitForHost_n soft strap: '0' – The FW will pause its boot session, allowing a host to configure the VS2310 with HIF set/get commands. '1' – The FW loads the parameters from the external memory update parameter section and resumes boot as usual.	1
GPIO[20]/MSIO_DO[0]	Fiber-or-copper selection soft strap (VS2310 only): Set “Fiber Enable” parameter (0.3.0.0) to ‘2’ – selection by external input (GPIO[20]). ‘0’ – Copper ‘1’ – Fiber	1
GPIO[22]	EDID Source Selection soft strap: ‘0’ – The EDID from the HDMI Sink is presented to the HDMI Source ‘1’ – The static EDID defined in Host Interface parameter 0.1.5.9 is presented to the HDMI Source This soft strap is enabled by setting Host Interface parameter 0.1.5.10 to ‘1’	1

IMPORTANT

Additional soft strap pins are reserved for future purposes and do not have any attached functionality. To make sure your design is future compatible, soft straps pins must not be tied to external pullup or pulldown resistors.

6.3 GPIO Functionality

VS2310/VS2000 GPIO pins are used by the FW for various input indications and status outputs. These GPIO functions are pre-assigned and detailed in this section.

6.3.1 FW LED (pin GPIO[24]/MSIO_DO[4])

This GPIO function indicates FW operation status as follows:

- 1 (high – LED off): Indicates no FW operation.
- 0.5Hz blink (1 second on, 1 second off): Indicates that the Full firmware is loaded and running
- 2.5Hz blink (0.2 seconds on, 0.2 seconds off): Indicates that the Internal Boot firmware is running. This should only be used during first-time programming of an empty external Flash memory.
- 5Hz blink (0.1 seconds on, 0.1 seconds off): Indicates that the device is running from the Basic firmware bank. The Basic firmware does not provide full functionality, and running from the Basic bank usually indicates a failure in the system.

6.3.2 Link LED (pin GPIO[27]/MSIO_DI[1])

This GPIO function reports the link status as follows:

- 0 (low – LED on): HDBaseT Link.
- 6.25Hz blink (0.08 seconds on, 0.08 seconds off): Ethernet Fallback mode.
- 2.5Hz blink (0.2 seconds on, 0.2 seconds off): Low Power mode without Ethernet (LPPF1).
- 0.5Hz - blink (1 second on, 1 second off): Low Power mode with Ethernet (LPPF2).
- 1 (high – LED off): No link

6.3.3 HDMI LED (pin GPIO[28]/MSIO_DI[2])

This GPIO function reports the HDMI status as follows:

- 0 (low – LED on): HDMI/DVI Content exists – with HDCP encryption.
- 2.5Hz blink (0.2 seconds on, 0.2 seconds off): HDMI/DVI Content exists – without HDCP encryption
- 1 (high – LED off): No HDMI/DVI video.

6.3.4 CIR Type In (pin GPIO[21]/MSIO_DOUT[1])

This GPIO function is an input from the CIR circuit indicating the type of CIR message received and send over the HDBaseT link.

- 0 (low): indicates that the CIR T-Adaptor input signal (MSIO_DIN[3]/CIR_in/GPIO[7] pin) carries a modulated CIR signal.

- 1 (high): indicates that the CIR T-Adaptor input signal (MSIO_DIN[3]/CIR_in/GPIO[7] pin) carries a baseband CIR signal.

The polarity of this GPIO function may be inverted using the parameter system.CIR.CIRTypeInPolarity. When the polarity is set to 0 (system.CIR.CIRTypeInPolarity = 0), the encoding above applies. By default, system.CIR.CIRTypeInPolarity = 1 and the inverted encoding applies:

- 1 (High): indicates that the CIR T-Adaptor input signal (MSIO_DIN[3]/CIR_in/GPIO[7] pin) carries a modulated CIR signal.
- 0 (low): indicates that the CIR T-Adaptor input signal (MSIO_DIN[3]/CIR_in/GPIO[7] pin) carries a baseband CIR signal.

If your CIR circuit supports only one type of CIR message (modulated only or baseband only), you can leave this pin unconnected. The CIR message type attribute must be correctly defined using the TAInfo.CIRTx table of parameters.

For more information about CIR circuit implementation, refer to *Application Note AN2050*.

6.3.5 CIR Type Out (pin GPIO[17])

This GPIO function is an output from chip to the CIR circuit indicating the type of CIR message output over the MSIO_DO3/CIR_OUT pin.

- 0 (low): indicates that the CIR output signal carries a baseband CIR signal.
- 1 (high): indicates that the CIR output signal carries a modulated CIR signal.

The polarity of this GPIO function may be inverted using the parameter system.CIR.CIRTypeOutPolarity. When the default polarity is set (system.CIR.CIRTypeInPolarity = 0), the encoding above applies. When system.CIR.CIRTypeInPolarity = 1, the inverted encoding applies:

- 1 (high): indicates that the CIR output signal carries a baseband CIR signal.
- 0 (low): indicates that the CIR output signal carries a modulated CIR signal.

If your CIR circuit applies only one CIR message type (modulated only or baseband only), you can leave this pin unconnected.

6.3.6 RX Detect Circuit (pin GPIO[31]/MSIO_D[5])

This function is used as input for the external RX detect circuit. The RX-detect circuit output feeds GPIO31 on the VS2xxxRX device. The function needs to be enabled in the firmware parameter configuration. The RX device firmware samples GPIO31, and digitally forwards it over HDBaseT to the VS2xxxTX device for regeneration on the source device interface. This method of transmission eliminates degradation of the analog signal over the CATx HDBaseT link.

6.4 MSIO Functionality

MSIO (Multi-Serial Input Output) channels allow for any low-speed data to be transferred across the HDBaseT link. Up to 6 MSIO channels may be used simultaneously. Data is transferred asynchronously through oversampling of the input data – the sample rate is set by configuration to either 0.5MHz, 1.0MHz or 1.5MHz. It is recommended to use a sampling rate of 10:1, meaning that (for example) with a sample rate of 1.5MHz the maximum native data rate should not exceed 150Kb/s.

For additional information, refer to Valens application note AN2052 – MSIO Functionality.

6.4.1 MSIO Compatibility with VS100 PDIF

In the event of V2000 Series – VS100 Series interoperation, the following general-purpose pins are connected over the HDBaseT link.

- VS2000 Series: MSIO[5:0] – Multi-Serial Input Output
- VS100 Series: PDIF[5:0] – Programmable Data Interface

NOTE

Not all of the pin connections are interoperable, please see the below table for details.

Table 25: PDIF-MSIO Compatibiity

VS010/VS100	VS2000 Series	Interoperability
PDIF[0] **(UART function)**	MSIO[0]	MSIO_DIN[0]/UART_IN/GPIO[4] MSIO_DOUT[0]/UART_OUT/GPIO[10]
PDIF[1]	MSIO[1]	Interoperability not supported
PDIF[2]	MSIO[2]	Interoperability not supported
PDIF[3] **(CIR function)**	MSIO[3]	MSIO_DIN[3]/CIR_IN/GPIO[7] MSIO_DOUT[3]/CIR_OUT/GPIO[13]
PDIF[4]	MSIO[4]	MSIO_DIN[4]/I2S_BCLK_IN/GPIO[8] MSIO_DOUT[4]/I2S_BCLK_OUT/GPIO[14]
PDIF[5]	MSIO[5]	MSIO_DIN[5]/SPDIF_IN/GPIO[9] MSIO_DOUT[5]/SPDIF_OUT/GPIO[15]

6.5 Debug Port

The UART-based Debug port is used to enable first-time flash memory programming. The port is *always* available – even if no firmware is programmed in flash memory.

The following pins serve as the UART interface to the Debug port

- DBG_RXD
- DBG_TXD_ST6

The UART interface operates at the TTL level. Therefore, an external TTL-to-RS232 level shifter is required in order to connect to a PC and download firmware into the device.

6.6 VS2310/VS2000 Parameters

VS2310/VS2000 parameters are used to configure and monitor the chip's functionality during runtime and bring up. Each parameter has a default value and a set of attributes defining the method of updating the parameter. Parameter attributes are explained below.

BU (Bring-up Parameter) Attribute

A parameter with a BU attribute attains its value once only during the boot session. There are two methods for setting BU parameters:

1. By pre-programming the external memory (FLASH) parameter section. This is done using the update parameter tool. The FW loads the parameter values from the external memory parameter section as part of the boot session.
2. By HIF (Host Interface) commands during WaitForHost_n soft strap. This option is described in detail in *Application Note AN2004 – Host Interface*.

All BU parameters may be read using GET HIF commands at any time.

RT (Run-time Parameter) Attribute

Parameters with RT attribute (on local or remote devices) may be accessed anytime during runtime using SET and GET HIF commands. These parameters may only be modified using HIF commands.

- RO – read only (can be accessed using HIF GET commands)
- RW – read write (can be accessed using HIF GET and SET commands)
- W – write only (can be accessed using HIF SET commands)

6.6.1 VS2310/VS2000 Initialization Flow

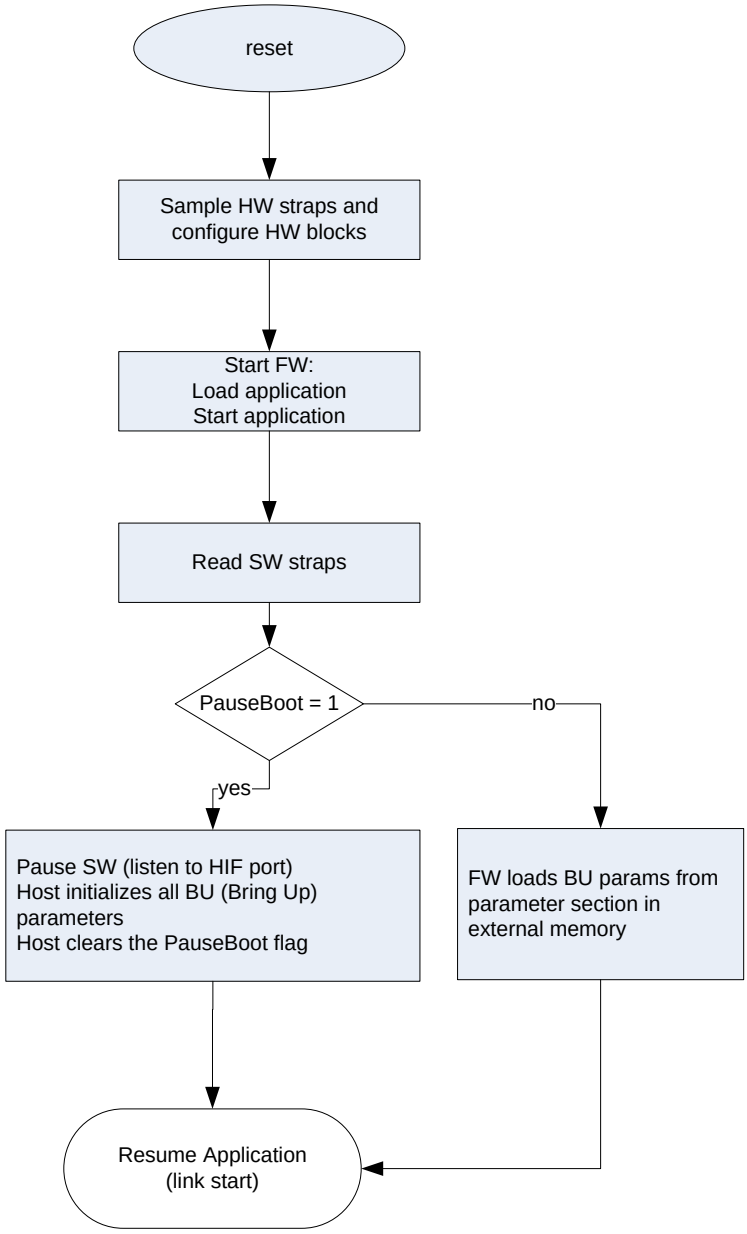


Figure 24: VS2310/VS2000 Initialization Flow

6.6.2 Parameter List

For a complete guide to configuration of firmware parameters, refer to *Application Note AN2015 – Firmware Parameter Descriptions*.

6.7 Host Interface (HIF)

The Host Interface provides a channel for exchanging information between a VS2310/VS2000 family chip and a host system used to control, configure, and monitor the chip.

For a complete description of the HIF and its operations, refer to the following Valens Application Notes:

- *AN2004 – Host Interface*
- *AN2015 – Firmware Parameter Descriptions*

6.8 JTAG Interface

The JTAG interface includes the signals: TEST_MODE_0; TEST_MODE; TCK; TDI; TDO; TMS; TRST.

The following signals are used to switch to the JTAG mode of operation:

Table 26: JTAG Mode

TEST_MODE_0	TEST_MODE_1	Chip Operation mode
0	0	Normal Mode
1	1	JTAG Mode

To enter JTAG mode follow these steps:

1. RESET the device.
2. Assert TEST_MODE_0 to ‘1’ and TEST_MODE_1 to ‘1’.
3. Release device from RESET.

To return to normal operation mode follow the steps:

1. RESET the device.
2. Assert TEST_MODE_0 to ‘0’ and TEST_MODE_1 to ‘0’.
3. Release device from RESET.

Note: for BSDL files please contact Valens customer support.

7 Electrical Specifications

This chapter contains electrical specifications for the Valens VS2310/VS2000 TX and RX chips.

NOTE

The ratings appearing in this section are preliminary and based on tests performed under lab conditions.

7.1 Absolute Maximum Rating

Table 27: VS2310TX/VS2000TX Absolute Maximum Rating

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VI	Digital Inputs voltage		0		5.5	V
Tj	Junction Temperature range		-40		125	°C
TSTG	Storage Temperature range				150	°C
VDD	VDD		-0.2		1.1	V
VDDA10	AVDD10		-0.2		1.1	V
VDDA18	AVDD18		-0.2		1.98	V
VDDIO	VDD33V		-0.2		3.6	V
VDDA33	AVDD33		-0.2		3.6	V
VTERM33	AVDD33_TERM		-0.2		3.6	V

Table 28: VS2310RX/VS2000RX Absolute Maximum Rating

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Vi	Digital Inputs voltage		0		5.5	V
Tj	Junction Temperature range		-40		125	°C
TSTG	Storage Temperature range				150	°C
VDD	VDD		-0.2		1.1	V
VDDA10	AVDD10		-0.2		1.1	V
VDDA18	AVDD18		-0.2		1.98	V
VDDIO	VDD33V		-0.2		3.6	V
VDDA33	AVDD33		-0.2		3.6	V

NOTE

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only - functional operation of the device under these or any other conditions above those indicated in the operational section of this datasheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 Power Supplies

7.2.1 Tx Power Supplies

Table 29: VS2310TX/VS2000TX Power Supply

Symbol	Parameter	Min	Typ	Max	Unit
VDD	1.0V digital voltage	Typ-5%	1.0	Typ+5%	V
AVDD10	1.0V analog voltage	Typ-5%	1.0	Typ+5%	V
AVDD18	1.8V analog voltage	Typ-5%	1.8	Typ+5%	V
AVDD33	3.3V analog voltage	Typ-5%	3.3	Typ+5%	V
VDD33V	3.3V IO voltage	Typ-5%	3.3	Typ+5%	V
AVDD33_TERM	3.3V analog termination voltage	Typ-5%	3.3	Typ+5%	V
VSS	Ground		0		V

7.2.2 Rx Power Supplies

Table 30: VS2310RX/VS2000RX Power Supply

Symbol	Parameter	Min	Typ	Max	Unit
VDD	1.0V digital voltage	Typ-5%	1.0	Typ+5%	V
AVDD10	1.0V analog voltage	Typ-5%	1.0	Typ+5%	V
AVDD18	1.8V analog voltage	Typ-5%	1.8	Typ+5%	V
AVDD33	3.3V analog voltage	Typ-5%	3.3	Typ+5%	V
VDD33V	3.3V IO voltage	Typ-5%	3.3	Typ+5%	V
VSS	Ground		0		V

7.3 Power Consumption Ratings

7.3.1 Tx Power Consumption

Table 31: Typical* VS2310TX/VS2000TX Power Consumption Ratings

Symbol	Parameter	Conditions	Typ	Unit
IVDD33	3.3V Supply Current (AVDD33, AVDD33_TERM, VDD33V)	LPPF1	15	mA
IVDD18	1.8V Supply Current (AVDD18)		17	mA
IVDD10	1.0V Supply Current (AVDD10, VDD)		167	mA
PSUPP	**Total Power Consumption**		**248**	**mW**
IVDD33	3.3V Supply Current (AVDD33, AVDD33_TERM, VDD33V)	LPPF1 in Auto-LPPF Mode with USB Trigger	30	mA
IVDD18	1.8V Supply Current (AVDD18)		17	mA
IVDD10	1.0V Supply Current (AVDD10, VDD)		219	mA
PSUPP	**Total Power Consumption**		**349**	**mW**
IVDD33	3.3V Supply Current (AVDD33, AVDD33_TERM, VDD33V)	LPPF2	36	mA
IVDD18	1.8V Supply Current (AVDD18)		93	mA
IVDD10	1.0V Supply Current (AVDD10, VDD)		350	mA
PSUPP	**Total Power Consumption**		**637**	**mW**
IVDD33	3.3V Supply Current (AVDD33, AVDD33_TERM, VDD33V)	Fallback (RMII interface)	30	mA
IVDD18	1.8V Supply Current (AVDD18)		115	mA
IVDD10	1.0V Supply Current (AVDD10, VDD)		480	mA
PSUPP	**Total Power Consumption**		**786**	**mW**
IVDD33	3.3V Supply Current (AVDD33, AVDD33_TERM, VDD33V)	HDBaseT (Long Reach) HDMI 1080P/24bpp/60Hz Ethernet 100BTx	130	mA
IVDD18	1.8V Supply Current (AVDD18)		270	mA
IVDD10	1.0V Supply Current (AVDD10, VDD)		937	mA
PSUPP	**Total Power Consumption**		**1852**	**mW**
IVDD33	3.3V Supply Current (AVDD33, AVDD33_TERM, VDD33V)	HDBaseT single channel HDMI 720P/24bpp/60Hz Ethernet 100BTx	TBD	mA
IVDD18	1.8V Supply Current (AVDD18)		TBD	mA
IVDD10	1.0V Supply Current (AVDD10, VDD)		TBD	mA
PSUPP	**Total Power Consumption**		**TBD**	**mW**

IVDD33	3.3V Supply Current (AVDD33, AVDD33_TERM, VDD33V)	HDBaseT dual channel HDMI 1080P/24bpp/60Hz Ethernet 100BTx	TBD	mA
IVDD18	1.8V Supply Current (AVDD18)		TBD	mA
IVDD10	1.0V Supply Current (AVDD10, VDD)		TBD	mA
PSUPP	**Total Power Consumption**		**TBD**	**mW**
IVDD33	3.3V Supply Current (AVDD33, AVDD33_TERM, VDD33V)	HDBaseT HDMI 4k2k/24bpp/30Hz Ethernet 100BTx	140	mA
IVDD18	1.8V Supply Current (AVDD18)		270	mA
IVDD10	1.0V Supply Current (AVDD10, VDD)		1116	mA
PSUPP	**Total Power Consumption**		**2064**	**mW**
IVDD33	3.3V Supply Current (AVDD33, AVDD33_TERM, VDD33V)	HDBaseT HDMI 4k2k/24bpp/30Hz Ethernet 100BTx USB **(VS2310 only)**	140	mA
IVDD18	1.8V Supply Current (AVDD18)		279	mA
IVDD10	1.0V Supply Current (AVDD10, VDD)		1248	mA
PSUPP	**Total Power Consumption**		**2213**	**mW**
IVDD33	3.3V Supply Current (AVDD33, AVDD33_TERM, VDD33V)	VS100/VS010 compatability mode HDBaseT HDMI 4k2k/24bpp/30Hz Ethernet 100BTx	140	mA
IVDD18	1.8V Supply Current (AVDD18)		270	mA
IVDD10	1.0V Supply Current (AVDD10, VDD)		1073	mA
PSUPP	**Total Power Consumption**		**2021**	**mW**
IVDD33	3.3V Supply Current (AVDD33, AVDD33_TERM, VDD33V)	HDBaseT HDMI 4k2k/24bpp/30Hz HDI/HDO for fiber, Ethernet 100BTx **(VS2310 only)**	155	mA
IVDD18	1.8V Supply Current (AVDD18)		336	mA
IVDD10	1.0V Supply Current (AVDD10, VDD)		1281	mA
PSUPP	**Total Power Consumption**		**2400**	**mW**
IVDD33	3.3V Supply Current (AVDD33, AVDD33_TERM, VDD33V)	HDBaseT LVDS Single mode (6 data lanes), 90MHz clock **(VS2310 only)**	7	mA
IVDD18	1.8V Supply Current (AVDD18)		267	mA
IVDD10	1.0V Supply Current (AVDD10, VDD)		874	mA
PSUPP	**Total Power Consumption**		**1378**	**mW**
IVDD33	3.3V Supply Current (AVDD33, AVDD33_TERM, VDD33V)	HDBaseT LVDS Dual mode (2x6 data lanes), 83MHz clock **(VS2310 only)**	9	mA
IVDD18	1.8V Supply Current (AVDD18)		270	mA
IVDD10	1.0V Supply Current (AVDD10, VDD)		931	mA
PSUPP	**Total Power Consumption**		**1447**	**mW**

IVDD33	3.3V Supply Current (AVDD33, AVDD33_TERM, VDD33V)	HDBaseT HDMI_4K2K/24bpp/30Hz HDI/HDO, UART, Ethernet 100BTx **(VS2310 only)**	208	mA
IVDD18	1.8V Supply Current (AVDD18)		240	mA
IVDD10	1.0V Supply Current (AVDD10, VDD)		1130	mA
PSUPP	**Total Power Consumption**		**1767**	**mW**

** Maximum power consumption ratings are estimated as follows: <Typical>+20%*

7.3.2 Rx Power Consumption

Table 32: Typical* VS2310RX/VS2000RX Power Consumption Ratings

Symbol	Parameter	Conditions	Typ	Unit
IVDD33	3.3V Supply Current (AVDD33, AVDD33_TERM, VDD33V)	LPPF1	10	mA
IVDD18	1.8V Supply Current (AVDD18)		30	mA
IVDD10	1.0V Supply Current (AVDD10, VDD)		223	mA
PSUPP	**Total Power Consumption**		**310**	**mW**
IVDD33	3.3V Supply Current (AVDD33, AVDD33_TERM, VDD33V)	LPPF1 in Auto-LPPF Mode with USB Trigger	19	mA
IVDD18	1.8V Supply Current (AVDD18)		30	mA
IVDD10	1.0V Supply Current (AVDD10, VDD)		278	mA
PSUPP	**Total Power Consumption**		**395**	**mW**
IVDD33	3.3V Supply Current (AVDD33, AVDD33_TERM, VDD33V)	LPPF2	31	mA
IVDD18	1.8V Supply Current (AVDD18)		165	mA
IVDD10	1.0V Supply Current (AVDD10, VDD)		449	mA
PSUPP	**Total Power Consumption**		**849**	**mW**
IVDD33	3.3V Supply Current (AVDD33, AVDD33_TERM, VDD33V)	Fallback (RMII Interface)	18	mA
IVDD18	1.8V Supply Current (AVDD18)		281	mA
IVDD10	1.0V Supply Current (AVDD10, VDD)		710	mA
PSUPP	**Total Power Consumption**		**1275**	**mW**
IVDD33	3.3V Supply Current (AVDD33, AVDD33_TERM, VDD33V)	HDBaseT (Long Reach) HDMI 1080P/24bpp/60Hz Ethernet 100BTx	52	mA
IVDD18	1.8V Supply Current (AVDD18)		371	mA
IVDD10	1.0V Supply Current (AVDD10, VDD)		1577	mA
PSUPP	**Total Power Consumption**		**2417**	**mW**
IVDD33	3.3V Supply Current (AVDD33, AVDD33_TERM, VDD33V)	HDBaseT single channel HDMI 720P/24bpp/60Hz Ethernet 100BTx	TBD	mA
IVDD18	1.8V Supply Current (AVDD18)		TBD	mA
IVDD10	1.0V Supply Current (AVDD10, VDD)		TBD	mA
PSUPP	**Total Power Consumption**		**TBD**	**mW**
IVDD33	3.3V Supply Current (AVDD33, AVDD33_TERM, VDD33V)	HDBaseT dual channel HDMI 1080P/24bpp/60Hz Ethernet 100BTx	TBD	mA
IVDD18	1.8V Supply Current (AVDD18)		TBD	mA
IVDD10	1.0V Supply Current (AVDD10, VDD)		TBD	mA
PSUPP	**Total Power Consumption**		**TBD**	**mW**

IVDD33	3.3V Supply Current (AVDD33, AVDD33_TERM, VDD33V)	HDBaseT HDMI 4k2k/24bpp/30Hz Ethernet 100BTx	68	mA
IVDD18	1.8V Supply Current (AVDD18)		398	mA
IVDD10	1.0V Supply Current (AVDD10, VDD)		2441	mA
PSUPP	**Total Power Consumption**		**3382**	**mW**
IVDD33	3.3V Supply Current (AVDD33, AVDD33_TERM, VDD33V)	HDBaseT HDMI 4k2k/24bpp/30Hz Ethernet 100BTx USB **(VS2310 only)**	77	mA
IVDD18	1.8V Supply Current (AVDD18)		407	mA
IVDD10	1.0V Supply Current (AVDD10, VDD)		2546	mA
PSUPP	**Total Power Consumption**		**3533**	**mW**
IVDD33	3.3V Supply Current (AVDD33, AVDD33_TERM, VDD33V)	VS100/VS010 compatability mode HDBaseT HDMI 4k2k/24bpp/30Hz Ethernet 100BTx	68	mA
IVDD18	1.8V Supply Current (AVDD18)		371	mA
IVDD10	1.0V Supply Current (AVDD10, VDD)		2326	mA
PSUPP	**Total Power Consumption**		**3219**	**mW**
IVDD33	3.3V Supply Current (AVDD33, AVDD33_TERM, VDD33V)	HDBaseT HDMI 4k2k/24bpp/30Hz HDI,HDO for fiber Ethernet 100BTx **(VS2310 only)**	97	mA
IVDD18	1.8V Supply Current (AVDD18)		472	mA
IVDD10	1.0V Supply Current (AVDD10, VDD)		2661	mA
PSUPP	**Total Power Consumption**		**3833**	**mW**
IVDD33	3.3V Supply Current (AVDD33, AVDD33_TERM, VDD33V)	HDBaseT LVDS Single mode (6 data lanes), 90MHz clock **(VS2310 only)**	8	mA
IVDD18	1.8V Supply Current (AVDD18)		413	mA
IVDD10	1.0V Supply Current (AVDD10, VDD)		2246	mA
PSUPP	**Total Power Consumption**		**3016**	**mW**
IVDD33	3.3V Supply Current (AVDD33, AVDD33_TERM, VDD33V)	HDBaseT HDMI_4K2K/24bpp/30Hz HDI/HDO, UART Ethernet 100BTx **(VS2310 only)**	146	mA
IVDD18	1.8V Supply Current (AVDD18)		448	mA
IVDD10	1.0V Supply Current (AVDD10, VDD)		2270	mA
PSUPP	**Total Power Consumption**		**3220**	**mW**

**Maximum power consumption ratings are estimated as follows: <Typical>+20%*

7.4 Reference Clock Requirements

7.4.1 CMOS Oscillator Requirements

NOTE

Implementation of the CMOS oscillator requires the use of an analog CMOS-to-LVDS conversion circuit. Refer to *Application Note 2001 – Hardware Design Guidelines* for further details.

The CMOS oscillator should comply with the following requirements:

- Frequency: 125 MHz
- Accuracy: ±100 ppm (±0.01%)
- Phase Noise must be kept below the phase noise mask specified in Table 33 below.

Table 33: CMOS Oscillator Phase Noise Mask

Frequency	Phase Noise (dBc/Hz)
1 Hz	-30
10 Hz	-60
100 Hz	-90
1 KHz	-127
10 KHz	-148
100 KHz	-150
10 GHz	-150

7.4.2 LVDS Oscillator Requirements

An LVDS oscillator may be used to generate a 125 MHz reference clock input. The LVDS oscillator should comply with the following requirements:

Table 34: LVDS Oscillator Requirements

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Note
F_{CLK}	Reference clock frequency			125		MHz	
F_{TOL}	Input clock frequency tolerance	includes aging, temperature change and supply voltage swing	-100		+100	PPM	
F_{DCD}	Reference clock duty cycle		40	50	60	%	
$T_{FALL/RISE}$	Rise / Fall Time	20% - 80% differential	260		2400	pSec	
V_I	Single-ended Input Voltage Range		0		1.89	V	
$\|V_{ID}\|$	Differential input voltage range		100		600	mV	Fig2
V_{CM}	Common-mode input range		600	1200	1800	mV	
R_{IN}	Input differential resistance		80		120	Ω	

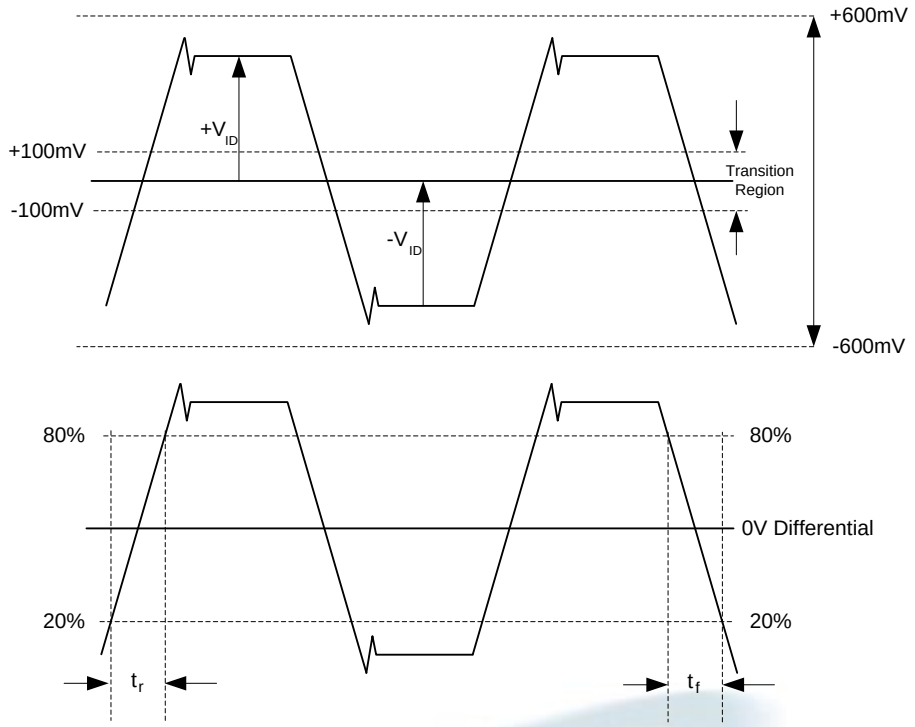


Figure 25: Input Reference Clock Wave Diagram

7.5 Recommended Operating Conditions

7.5.1 Electrical Characteristics (DC Specifications)

Table 35: VS2310TX/VS2000TX Electrical Specification

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Digital pads						
VIH	Input voltage high	Digital pads	2.0		5.5	V
VIL	Input voltage low		-0.3		0.8	V
CIN	Input capacitance				2	pF
RPU	Pull-up resistor		65	93	141	KΩ
RPD	Pull-down resistor		60	90	163	KΩ
VOH	Output voltage High		2.4			V
VOL	Output voltage Low				0.4	V
LVDS/HDI Transmit Mode - DC specifications						
Vo_se	Single ended Voltage range that can be observed on LVDS IOs.	Standard LVDS levels	0		1.98	V
Vcmout_lvds	Output Common mode range (LVDS mode)		1.125	1.2	1.375	V
Vod_lvds	Output differential voltage peak, VCM = 1.2V		0.25	0.33	0.4	V
Vcmout_sub_lvds	Output Common mode range (sub LVDS mode)		0.8	0.9	1	V
Vod_sub_lvds	Output differential voltage peak, VCM = 0.9V		0.125	0.165	0.2	V
LVDS/HDI Receive Mode - DC specifications						
Vi_se	Single ended Voltage range that can be tolerable on LVDS IO without damage induced to DUT nor open any clamping device.		0		1.98	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Vid	Differential input voltage range that should be supported by LVDS receiver over all common mode range defined as Vcmin below.		0.1		0.6	V
Vcmin	Input Common mode range		0.07	1.2	(AVDD18 -0.1)	V
RIN(DIFF)	Receiver differential input impedance		90	100	110	Ω
TMDS Receivers DC specification						
VTH	Differential Input Threshold (+)				+75	mV
VTL	Differential Input Threshold (-)		-75			mV
|VID|	Differential Input Voltage (pk-pk)	Refer to HDMI specification 1.4 for further details.	150		1560	mV
VICM1	Input common mode		-400		37.5	mV
VICM2	Input common mode		-10		10	mV
RIN(SE)	Single ended input impedance			50		Ω
SPI Interface DC Specification						
VOH	Output voltage High		2.4			V
VOL	Output voltage Low				0.4	V
IOH	Output current High		13.2	25.5	42.2	mA
IOL	Output current Low		10	15.7	21.1	mA

Table 36: VS2310RX/VS2000RX Electrical Specification

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Digital pads						
VIH	Input voltage high	Digital pads	2.0		5.5	V
VIL	Input voltage low		-0.3		0.8	V
CIN	Input capacitance				2	pF
RPU	Pull-up resistor		65	93	141	KΩ
RPD	Pull-down resistor		60	90	163	KΩ
VOH	Output voltage High		2.4			V
VOL	Output voltage Low				0.4	V

LVDS/HDI Transmit Mode DC specifications						
Vo_se	Single ended Voltage range that can be observed on LVDS IOs.	standard LVDS levels	0		1.98	V
Vcmout_lvds	Output Common mode range (LVDS mode)		1.125	1.2	1.375	V
Vod_lvds	Output differential voltage peak, VCM = 1.2V		0.25	0.33	0.4	V
Vcmout_sub_lvds	Output Common mode range (sub LVDS mode)		0.8	0.9	1	V
Vod_sub_lvds	Output differential voltage peak, VCM = 0.9V		0.125	0.165	0.2	V
LVDS/HDI Receive Mode - DC specifications						
Vi_se	Single ended Voltage range that can be tolerable on LVDS IO without damage induced to DUT nor open any clamping device.		0		1.98	V
Vid	Differential input voltage range that should be supported by LVDS receiver over all common mode range defined as Vcmin below.		0.1		0.6	V
Vcmin	Input Common mode range		0.07	1.2	(AVDD18 -0.1)	V
RIN(DIFF)	Receiver differential input impedance		90	100	110	Ω
TMDS Drivers DC specification						
VSWING	Single-ended output swing voltage	Compliance point TP1 as defined in Section 4.2.4 of HDMI Specification V1.4.	400		600	mV
VH	Single-ended high level output voltage	if attached Sink supports TMDSCLK<= 165Mhz	Typ - 5%	AVCC	Typ + 5%	V
		if attached Sink supports	Typ - 200mV	AVCC	Typ + 10mV	V

		TMDSCLK > 165Mhz				
VL	Single-ended low level output voltage	if attached Sink supports TMDSCLK<= 165Mhz	Typ - 600mV	AVCC	Typ - 400mV	V
		if attached Sink supports TMDSCLK > 165Mhz	Typ - 700mV	AVCC	Typ - 400mV	V
RLOAD	50 ohm resistor loads Source Termination		45	50	55	Ω
SPI Interface DC Specification						
VOH	Output voltage High		2.4			V
VOL	Output voltage Low				0.4	V
IOH	Output current High		13.2	25.5	42.2	mA
IOL	Output current Low		10	15.7	21.1	mA

7.5.2 Timing (AC specifications)

Table 37: VS2310TX/VS2000TX AC Specification

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Reference clock						
Frefclk_lvds	Reference clock frequency	LVDS levels on RCB_REFCLK_P/M pins		125		MHz
Frefclk_xtal	Reference clock frequency	XTAL		25		MHz
	Input clock frequency tolerance		-50		+50	PPM
	Reference clock duty cycle		40	50	60	%
Frefclk_usb (VS2310 only)	USB2_0 Reference clock frequency	XTAL		12		MHz
	USB2_0 reference clock frequency tolerance		-50		+50	PPM
Digital pads MII						
TMII_FS	MII_Tx_CLK, MII_RX_CLK frequency			25		MHz
TMII_DC	MII_Tx_CLK, MII_RX_CLK duty cycle		35		65	%

TMII_DLY	MII_RX_DV, MII_RXD[3:0], MII_Rx_ERR output delay	relative to RX_CLK	10		30	ns
TMII_SU	MII_TX_EN, MII_TXD[1:0], MII_TXD[3:2]_GPIO, MII_TX_ERR_GPIO setup	relative to TX_CLK	10			ns
TMII_HD	MII_TX_EN, MII_TXD[1:0], MII_TXD[3:2]_GPIO, MII_TX_ERR_GPIO hold	relative to TX_CLK	0			ns
TMDIO_TC	MII_MDC period		400			ns
TMDIO_SU	MII_MDIO setup	MDIO sourced by MAC	10			ns
TMDIO_HD	MII_MDIO hold	MDIO sourced by MAC	10			ns
TMDIO_DY	MII_MDIO delay	MDIO source by PHY	0		300	ns
RMII mode						
TRMII_FS	MII_Tx_CLK frequency			50		MHz
TRMII_DC	MII_Tx_CLK duty cycle		35		65	%
TRMII_SU	MII_TXD[1:0], MII_TX_EN, MII_RXD[1:0], MII_Rx_DV, MII_RX_ERR data setup	relative to MII_Tx_CLK rising edge	4			ns
TRMII_HD	MII_TXD[1:0], MII_TX_EN, MII_RXD[1:0], MII_Rx_DV, MII_RX_ERR data hold	relative to MII_Tx_CLK rising edge	2			ns
Digital Pads BT.1120						
1120_SU	BT1120_D[19:0] data setup	Relative to BT1120_CLK rising edge	3			ns
1120_HD	BT1120_D[19:0] data hold	Relative to BT1120_CLK rising edge	2			ns
FLASH (I2C)						
Same as the Host interface (I2C), see below						
FLASH SPI						

Supports all standard devices, maximum clock rate = 20 MHz						
Host Interface (I2C)						
		Standard Mode		Fast Mode		
		Min	Max	Min	Max	Units
fSCL	SCL clock frequency	0	100	0	400	KHz
tHD;STA	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0		0.6		us
tLOW	LOW period of the SCL clock	4.7		1.3		us
tHIGH	HIGH period of the SCL clock	4.0		0.6		us
tSU;STA	Set-up time for a repeated START condition	4.7		0.6		us
tHD;DAT	Data hold time	0	3.45	0	0.9	us
tSU;DAT	Data set-up time	250		100(1*)		ns
tr	Rise time of both SDA and SCL signals		1000	20+0.1Cb (2*)	300	ns
tf	Fall time of both SDA and SCL signals		300	20+0.1Cb (2*)	300	ns
tSU;STO	Set-up time for STOP condition	4.0		0.6		us
tBUF	Bus free time between a STOP and START condition	4.7		1.3		us
Cb	Capacitive load for each bus line		400		400	pF
(1*) A Fast-mode I2C-bus device can be used in a Standard-mode I2C -bus system, but the requirement tSU;DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr max + tSU;DAT = 1000 + 250 = 1250 ns (according to the Standard-mode I2C -bus specification) before the SCL line is released. (2*) Cb = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall-times are allowed.						
LVDS Tranceive pads AC specifications (VS2310 only)						
FHDI_phy	LVDS TX output frequency on HDI_PHY lanes				560	MHz
FSGMII	LVDS TX output frequency on SGMPHY_TXP/TXN lanes @ SGMII mode	SGMII Standard			625	MHz
Tintra_skew_tx	Output intra pair skew		-25		+25	ps
Tinter_skew_tx	Output inter pair skew between every two pairs		-50		+50	ps
CL	Total Output load				5	pF
Tintra_skew_rx	input intra pair skew tolerance		-100		+100	ps

Tc2d_skew_hdi_rx (VS2310 only)	Clock to data skew tolerance on HDI_PHY receiver		-0.2		+0.2	UI
CLinput	Input capacitance on each LVDS receiver line.				2.5	pF
TMDS Receivers specification						
-	Maximum serial data rate				3.4	Gbps
FPCLK	TMDS Input clock frequency	On HDMIDES_TMDSCLKP/N	25		340	MHz
Intra-pair skew tolerance		FPCLK ≤ 225MHz			0.4	UI
		FPCLK > 225MHz			0.15UI + 112ps	mixed
Inter per skew					2UI + 1.78ns	mixed
	Input Clock Jitter Tolerance	Relative to Ideal Recovered Clock as defined in HDMI specification 1.4			0.30	UI

Table 38: VS2310RX/VS2000RX AC specification

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
General						
Frefclk_lvds	Reference clock frequency	LVDS levels on RCB_REFCLK_P/M pins		125		MHz
Frefclk_xtal	Reference clock frequency	XTAL		25		MHz
	Input clock frequency tolerance		-50		+50	PPM
	Reference clock duty cycle		40	50	60	%
Frefclk_usb (VS2310 only)	USB2_0 Reference clock frequency	XTAL		12		MHz
	USB2_0 reference clock frequency tolerance		-50		+50	PPM

Digital pads MII						
TMII_FS	MII_Tx_CLK, MII_RX_CLK frequency			25		MHz
TMII_DC	MII_Tx_CLK, MII_RX_CLK duty cycle		35		65	%
TMII_DLY	MII_RX_DV, MII_RXD[3:0], MII_Rx_ERR output delay	relative to RX_CLK	10		30	ns
TMII_SU	MII_TX_EN, MII_TXD[1:0], MII_TXD[3:2]_GPIO, MII_TX_ERR_GPIO setup	relative to TX_CLK	10			ns
TMII_HD	MII_TX_EN, MII_TXD[1:0], MII_TXD[3:2]_GPIO, MII_TX_ERR_GPIO hold	relative to TX_CLK	0			ns
TMDIO_TC	MII_MDC period		400			ns
TMDIO_SU	MII_MDIO setup	MDIO sourced by MAC	10			ns
TMDIO_HD	MII_MDIO hold	MDIO sourced by MAC	10			ns
TMDIO_DY	MII_MDIO delay	MDIO source by PHY	0		300	ns
RMII mode						
TRMII_FS	MII_Tx_CLK frequency			50		MHz
TRMII_DC	MII_Tx_CLK duty cycle		35		65	%
TRMII_SU	MII_TXD[1:0], MII_TX_EN, MII_RXD[1:0], MII_Rx_DV, MII_RX_ERR data setup	relative to MII_Tx_CLK rising edge	4			ns
TRMII_HD	MII_TXD[1:0], MII_TX_EN, MII_RXD[1:0], MII_Rx_DV, MII_RX_ERR data hold	relative to MII_Tx_CLK rising edge	2			ns
Digital Pads BT.1120						
1120_SU	BT1120_D[19:0] data setup	Relative to BT1120_CLK rising edge	4			ns
1120_HD	BT1120_D[19:0] data hold	Relative to BT1120_CLK rising edge	1			ns
FLASH (I2C)						
Same as the Host interface (I2C), see below						
FLASH SPI						
Support all standard devices, maximum clock rate = 20 MHz						
Host interface (I2C)						

		Standard Mode		Fast Mode		
		Min	Max	Min	Max	
fSCL	SCL clock frequency	0	100	0	400	KHz

tHD;STA	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0		0.6		us
tLOW	LOW period of the SCL clock	4.7		1.3		us
tHIGH	HIGH period of the SCL clock	4.0		0.6		us
tSU;STA	Set-up time for a repeated START condition	4.7		0.6		us
tHD;DAT	Data hold time	0	3.45	0	0.9	us
tSU;DAT	Data set-up time	250		100(1*)		ns
tr	Rise time of both SDA and SCL signals		1000	20+0.1Cb (2*)	300	ns
tf	Fall time of both SDA and SCL signals		300	20+0.1Cb (2*)	300	ns
tSU;STO	Set-up time for STOP condition	4.0		0.6		us
tBUF	Bus free time between a STOP and START condition	4.7		1.3		us
Cb	Capacitive load for each bus line		400		400	pF
(1*) A Fast-mode I2C-bus device can be used in a Standard-mode I2C -bus system, but the requirement tSU;DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr max + tSU;DAT = 1000 + 250 = 1250 ns (according to the Standard-mode I2C -bus specification) before the SCL line is released. (2*) Cb = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall-times are allowed.						
LVDS Tranceive pads AC specifications (VS2310 only)						
FHDI_phy	LVDS TX output frequency on HDI_PHY lanes				560	MHz
FSGMII	LVDS TX output frequency on SGMPHY_TXP/TXN or SGMAC_TXP/TXN lanes @ SGMII mode	SGMII Standard			625	MHz
Tintra_skew_tx	Output intra pair skew		-25		+25	ps
Tinter_skew_tx	Output inter pair skew between every two pairs		-50		+50	ps
CL	Total Output load				5	pF
Tintra_skew_rx	input intra pair skew tolerance		-100		+100	ps
Tc2d_skew_hdi_rx	Clock to data skew tolerance on HDI_PHY receiver		-0.2		+0.2	UI
CLinput	Input capacitance on each LVDS receiver line.				2.5	pF
TMDS Drivers specification						

-	Maximum serial data rate				3.4	Gbps
FTMDSCLK	TMDS output clock frequency	On HDMISER_TMDSCLKP/N outputs	25		340	MHz
PTMDSCLK	TMDSCLK period	RL=50Ω ±10%	2.94		40	ns
tCDC	TMDSCLK duty cycle	tCDC = tCPH / PTMDSCLK RL=50Ω ±10%	40	50	60	%
tCPH	TMDSCLK high time	RL=50Ω ±10%	4	5	6	UI
tCPL	TMDSCLK low time	RL=50Ω ±10%	4	5	6	UI
	TMDSCLK jitter 1	RL=50Ω ±10%			0.25	UI
tSK(P)	Intra-Pair (Pulse) skew. (between a pair lanes)	RL=50Ω ±10%			0.15	UI
tSK(PP)	Inter-Pair (Pulse) skew (between different pairs).	RL=50Ω ±10%			2	UI
tr	Differential output signal rise time	20% to 80%, RL = 50±10%	75			ps
tf	Differential output signal fall time	20% to 80%, RL = 50±10%	75			ps

7.5.3 Clock Oscillator Requirements

Table 39 provides the clocking requirement specification for *XO25MHZ_XIN* clock input of the VS2310/VS2000 chip. **NOTE THAT 25MHz CLOCK IS FOR FUTURE USE ONLY.**

Table 39: VS2310/VS2000 RX/TX Oscillator Requirements

Parameter	System Crystal Value	USB Crystal Value
Nominal Frequency	25MHz	12MHz
Frequency Tolerance @ 25oC	±50 PPM	±50 PPM
Frequency Stability, ref @ 25oC over operating temp. range	±50 PPM	±50 PPM
Load Capacitance (CL)	18.0pF	15.0pF
Drive Level	0.5 mW	0.5 mW
Aging per year	±5 PPM / year Max.	±5 PPM / year Max.
Max. ESR	30 ohm	60 ohm

7.5.3.1 Power on Reset Signal Timing

Option 1 : Using Internal POR (POR_BYPASS = 0. Pin RESET_N is the system reset)

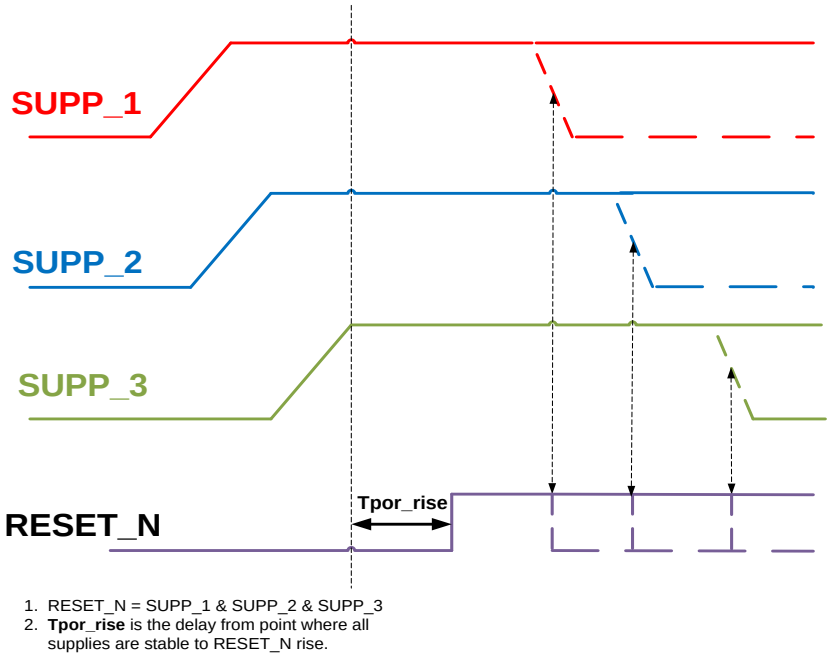


Figure 26: Internal Power on Reset Timing

Table 40: Internal Power on Reset Timing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
25MHz XTAL – **FUTURE USE ONLY**						
Tpor_rise	Reset pulse width on RESET_N				170	mS
125MHz reference						
Tpor_rise	Reset pulse width on RESET_N				135	mS

NOTE

For the internal POR system to be valid, the following supplies should ramp up together as a group (generated from same regulator):
* VDD and AVDD10
* VDD33V and AVDD33

Option 2: Using External POR (POR_BYPASS = 1. Pin RESET_IN is the system reset)

The RESET_IN signal must be held active at least 1ms after all chip supply voltages (VDD, VDD33V, AVDD10, AVDD18 and AVDD33).

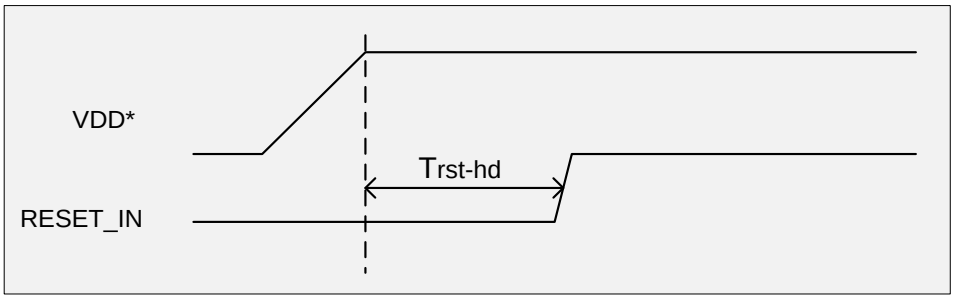


Figure 27: Reset Signal Timing

Table 41: External Power on Reset Timing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Trst_hd	Reset pulse width on RESET_IN after all 3 supplies are stable		1		80	mS

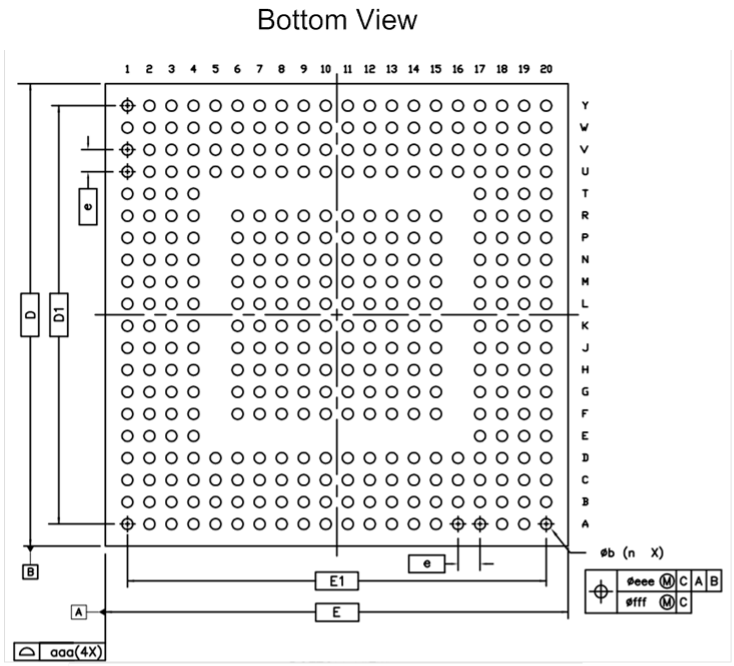
7.6 ESD Ratings

Table 42: ESD Ratings

Test	Value	Unit
HBM (per JEDEC JS-001)	± 2000	V
CDM (per JEDEC JESD22-C101)	± 500	
Latch Up (per JEDEC JESD78)	± 100	mA
	Over-voltage: 1.5x supply at 85°C	

8 Package Mechanical Data

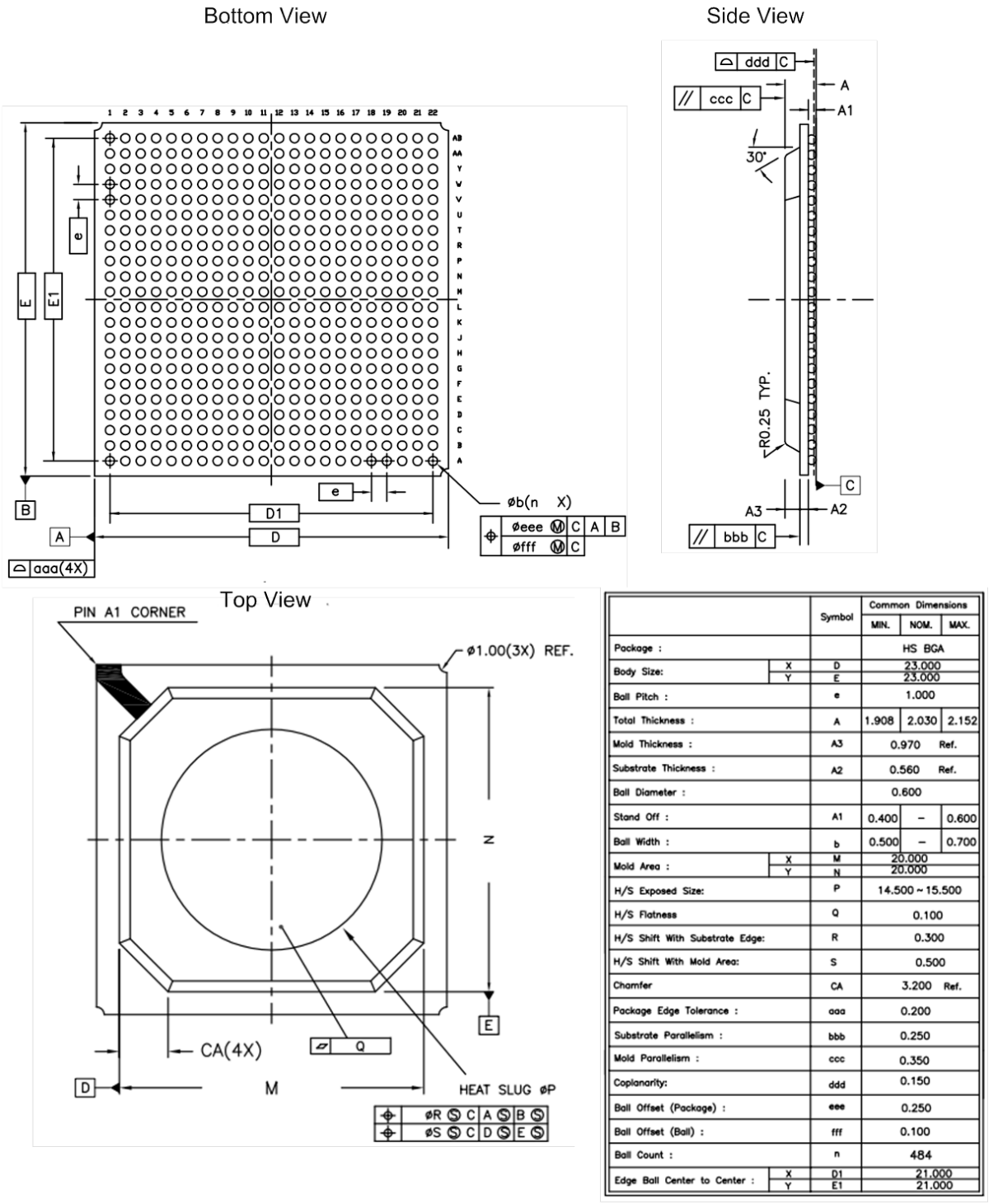
8.1 VS2310TX/VS2000TX Package Mechanical Data



		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package :			LBGA		
Body Size:	X	E		21.000	
	Y	D		21.000	
Ball Pitch :		e		1.000	
Total Thickness :		A			1.700
Mold Thickness :		M		0.700 Ref.	
Substrate Thickness :		S		0.360 Ref.	
Ball Diameter :				0.500	
Stand Off :		A1	0.360	–	0.460
Ball Width :		b	0.440	–	0.640
Package Edge Tolerance :		aaa		0.200	
Mold Parallelism :		bbb		0.250	
Coplanarity:		ddd		0.200	
Ball Offset (Package) :		eee		0.250	
Ball Offset (Ball) :		fff		0.100	
Ball Count :		n		356	
Edge Ball Center to Center :	X	E1		19.000	
	Y	D1		19.000	

Figure 28: VS2310TX/VS2000Tx Mechanical Information (all dimensions in mm)

8.2 VS2310RX/VS2000RX Package Mechanical Data



		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package :			HS BGA		
Body Size:	X	D		23.000	
	Y	E		23.000	
Ball Pitch :		e		1.000	
Total Thickness :		A	1.908	2.030	2.152
Mold Thickness :		A3		0.970 Ref.	
Substrate Thickness :		A2		0.560 Ref.	
Ball Diameter :				0.600	
Stand Off :		A1	0.400	–	0.600
Ball Width :		b	0.500	–	0.700
Mold Area :	X	M		20.000	
	Y	N		20.000	
H/S Exposed Size:		P		14.500 ~ 15.500	
H/S Flatness		Q		0.100	
H/S Shift With Substrate Edge:		R		0.300	
H/S Shift With Mold Area:		S		0.500	
Chamfer		CA		3.200 Ref.	
Package Edge Tolerance :		aaa		0.200	
Substrate Parallelism :		bbb		0.250	
Mold Parallelism :		ccc		0.350	
Coplanarity:		ddd		0.150	
Ball Offset (Package) :		eee		0.250	
Ball Offset (Ball) :		fff		0.100	
Ball Count :		n		484	
Edge Ball Center to Center :	X	D1		21.000	
	Y	E1		21.000	

Figure 29: VS2310RX/VS2000RX Mechanical Information (all dimensions in mm)

NOTE

The integrated Heat Slug in the RX device is connected to package GND (digital GND). To prevent possible shorting between the package GND and the chassis GND when using a heatsink, it is recommended to add an isolation sticker between the heatsink and the chassis cover.

8.3 VS2310/VS2000 Marking Information

For the VS2310/VS2000 TX and RX markings depicted below, the following information applies:

Table 43: VS2310/VS2000 Marking Schema

Marking Schema	
a	Pin A1 corner
b	Valens logo
c	Valens part number
d	Valens Lot #
Valens Lot # Schema	
First Line	Fab lot # XXXXXX.ZZ
Second Line	YYWW (assembly year and week number) ABC (Valens production lot)

8.3.1 VS2310TX

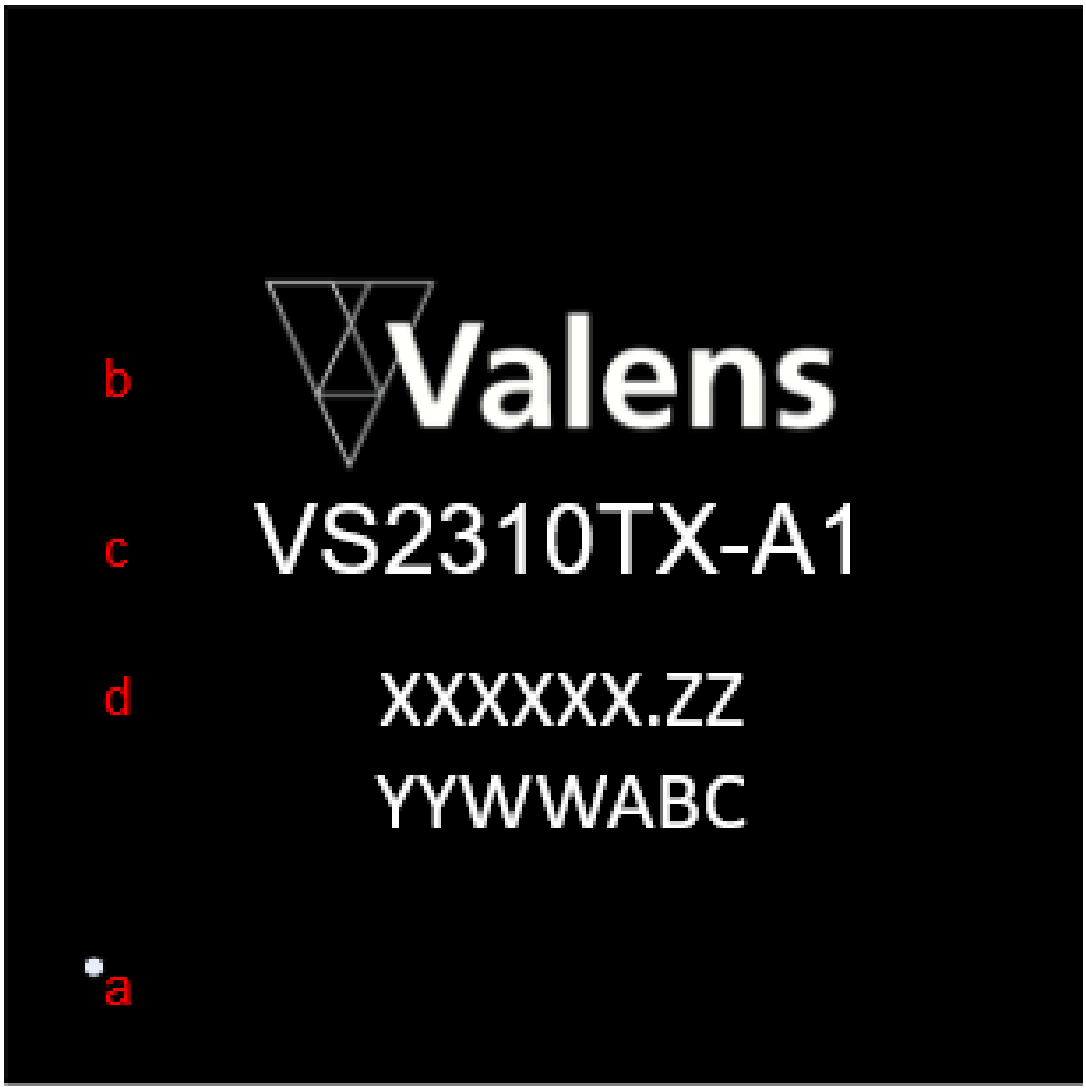


Figure 30: VS2310TX Marking

8.3.2 VS2310RX

Figure 31: VS2310RX Marking

8.3.3 VS2000TX

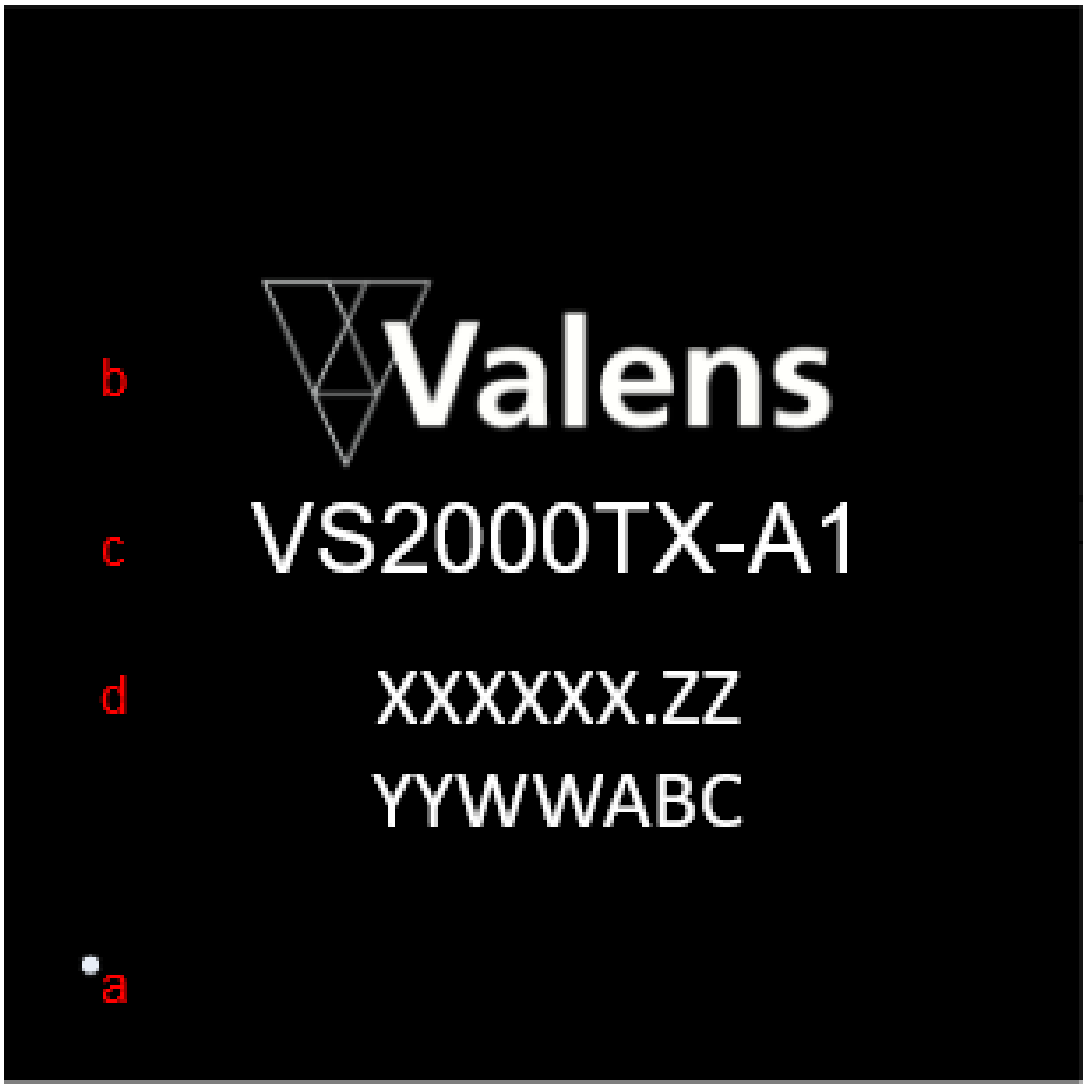


Figure 32: VS2000TX Marking

8.3.4 VS2000RX

Figure 33: VS2000RX Marking

8.4 Ordering Codes

Table 44: Ordering Codes

Ordering Code	Item Description
VS2310TX-A1	Valens HDBaseT 2310 Transmitter
VS2310RX-A1	Valens HDBaseT 2310 Receiver
VS2000TX-A1	Valens HDBaseT 2000 Transmitter
VS2000RX-A1	Valens HDBaseT 2000 Receiver

9 Thermal Parameters

9.1 Terminology

- θ_{JA} - Junction-to-ambient thermal resistance (EIA/JESD51-2 and EIA/JESD51-6):

  $\theta_{JA} = (T_J - T_A) / P_H$
  where T_J = junction temperature
  T_A = ambient temperature
  P_H = power dissipation

  θ_{JA} represents the resistance to the heat flows from the chip to ambient air. It is an indicator of package heat dissipation capability. Lower θ_{JA} means better overall thermal performance.

- Ψ_{JT} - Junction-to-top-center thermal characterization parameter (EIA/JESD51-2 and EIA/JESD51-6):

  $\Psi_{JT} = (T_J - T_T) / P_H$
  where T_T = temperature at the top-center of the package

  Ψ_{JT} is used for estimating the junction temperature by measuring T_T in an actual environment.

- Ψ_{JB} - Junction-to-board thermal characterization parameter (EIA/JESD51-2 and EIA/JESD51-6):

  $\Psi_{JB} = (T_J - T_B) / P_H$
  where T_B = board temperature

  Ψ_{JB} is a useful indicator of the thermal resistance between the junction and PCB if the package is not attached with an external heat sink.

- θ_{JB} - Junction-to-board thermal resistance (EIA/JESD51-8):

  $\theta_{JB} = (T_J - T_B) / P_H$
  where T_B = board temperature with ring cold plate fixture applied

  θ_{JB} represents the resistance to the heat flows from the chip to PCB. θ_{JB} is used in compact thermal models for system-level thermal simulation.

- θ_{JC} - Junction-to-case thermal resistance:

  $\theta_{JC} = (T_J - T_C) / P_H$
  where T_C = case temperature attached with a cold plate

  θ_{JC} represents the resistance to the heat flows from the chip to package top case. θ_{JC} is important when external heat sink is attached on package top.

9.2 TX Devices

Table 45: TX Thermal Data

Ambient Temperature	VAIR (m/s)	θJA (°C/W)	ΨJT (°C/W)	ΨJB (°C/W)	TJ (°C)	TT (°C)	θJC (°C/W)	θJB (°C/W)
70°C	0	16.37	0.13	8.33	119.10	118.72	3.01	8.47
	1	14.31	0.31	8.22	112.93	112.01		
	2	13.53	0.39	8.14	110.60	109.43		
85°C	0	16.01	0.13	8.33	133.03	132.63		
	1	14.16	0.30	8.22	127.48	126.57		
	2	13.41	0.39	8.14	125.22	124.07		

Table 46: TX PCB Constructions

Contstruction	Dimensions
PCB Layers	4-layer
PCB dimensions	101.5 x 114.3 x 1.6 mm
Core thickness	0.60 mm
Prepreg thickness	0.375 mm
Trace thickness	0.07 mm
Inner plane thickness	0.035 mm
Solder mask thickness	0.02 mm
Diameter of PCB vias	0.20 mm
Number of PCB via	64
Top / bottom copper coverage (%)	20
Inner copper coverage (%)	90

9.3 RX Devices

Table 47: RX Thermal Data

Ambient Temperature	V_{AIR} (m/s)	θ_{JA} (°C/W)	Ψ_{JT} (°C/W)	Ψ_{JB} (°C/W)	T_J (°C)	T_T (°C)	θ_{JC} (°C/W)	θ_{JB} (°C/W)
70°C	0	12.96	1.75	5.10	133.45	124.67	3.00	5.18
	1	10.78	1.80	5.00	123.88	114.90		
	2	10.02	1.82	4.94	120.08	110.99		
85°C	0	12.39	1.76	5.10	146.94	138.12		
	1	10.65	1.81	5.01	138.24	129.22		
	2	9.94	1.83	4.94	134.69	125.55		

Table 48: RX PCB Constructions

Contstruction	Dimensions
PCB Layers	4-layer
PCB dimensions	101.5 x 114.3 x 1.6 mm
Core thickness	0.60 mm
Prepreg thickness	0.375 mm
Trace thickness	0.07 mm
Inner plane thickness	0.035 mm
Solder mask thickness	0.02 mm
Diameter of PCB vias	0.20 mm
Number of PCB via	100
Top / bottom copper coverage (%)	20
Inner copper coverage (%)	90

10 Quality and Environmental Policy

Valens is committed to delivering the highest quality cutting-edge products to our customers, on time, every time.

Valens' management and employees are fully engaged in a culture of continuous improvement, and constructive partnerships with suppliers, customers and stakeholders.

Valens consistently monitors and strives to minimize the environmental impact of our activities, by implementing sustainable business practices across our operations, infrastructure and products.

We are committed to meeting or exceeding our customers' highest level of expectations, complying with all applicable environmental, health and safety requirements, and acting in accordance with the relevant laws and regulations.

ISO 9001:2008

ISO 14001:2004

RoHS – Restriction of Hazardous Substances

REACH SVHC – Substances of Very High Concern

Conflict Minerals Sourcing Policy

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