Valens

VS2010
Data Sheet

Version 2.5

Valens First in HDBaseT

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Revision History

Revision	Date	Author	Description
0.1	August 2015	Daniel Shwartzberg	First Draft
1.0	September 2015	Daniel Shwartzberg	Internal Revisions
1.1	October 2015	Daniel Shwartzberg	
1.2		Daniel Shwartzberg	
1.3	November 2015	Daniel Shwartzberg	
1.4	December 2015	Daniel Shwartzberg	
1.5	February 2016	Daniel Shwartzberg	
1.6	March 2016	Daniel Shwartzberg	Formal Release version
1.7		Daniel Shwartzberg	MSIO maximum speed of 1.5MHz
1.8		Daniel Shwartzberg	• Added thermal parameters (section 9) • Added note on heatsink isolation sticker for RX (Section 8.2)
1.9	May 2016	Daniel Shwartzberg	• Removed HDI power consumption from section 7.3 (HDI interface is not supported in VS2010) • Added Operating Mode table (Table 12) • 25MHz crystal oscillator is reserved for future use • Added that 4K video is supported over 90m of Cat5e cable

2.0	July 2016	Daniel Shwartzberg	• Corrected typo in Table 15 – polarity of MII_COL/GPIO[2] reversed • Corrected typo in heading 6.3.1 (MSIO_DO[4]) • Corrected typo in table 14, Strap[6] (setting must be [110]) • Added auto-LPPF mode (section 5.3.1) • Added "LPPF1 in Auto-LPPF Mode with USB Trigger" to power consumption tables
2.1	January 2017	Daniel Shwartzberg	• Corrected "If Not Used" connectivity for GPIO[16] and GPIO[17] in tables 3 and 6 • Added new soft strap functionality on GPIO[22] • Updated Quality and Environmental policy (Section 10) • Removed obsolete MSIO_CLKOUT functionality • Additional information on MSIO functionality (including use of 10:1 oversampling ratio) • Added LED blink rates • Added ESD ratings
2.2	June 2017	Daniel Shwartzberg	• Added SPI interface DC characteristics (tables 25 and 26) • Added note on I^2S DAC • Corrected CIRTypeInPolarity default typo in section 6.3.4
2.3	September 2017	Yaki Sfadya	• Updated marking information and ordering codes
2.4	July 2018	Yaki Sfadya	• Corrected typo in table 27; was 165Mhz -> 340Mhz and 1.65G -> 3.4G
2.5	February 2019	Yaki Sfadya	• Added JTAG interface and updated pin out

Glossary

Term	Definition
ARC	Audio Return Channel
AFE	Analog Front End
AV	Audio Video / Audio-Visual
CE	Consumer Electronics
CEC	Consumer Electronic Control
CIR	Consumer Infrared
EVK	Evaluation Kit
CTS	Compliance Test Specification
DDC	Display Data Channel
DVI	Digital Visual Interface
EEPROM	Electronically Erasable Programmable Read-Only Memory
GPIO	General Purpose Input Output
HD	High Definition
HDBT	HDBaseT
HDCD	HDBaseT Configuration Database
HDCP	High-Bandwidth Digital Content Protection
HDMI	High Definition Multimedia Interface
HIF	Host Interface
HLIC	HDBaseT Link Internal Controls
HPD	Hot Plug Detect
I/F	Interface
IC	Integrated Circuit
I^2C	Inter IC
I^2S	Inter IC Sound
KVM	Keyboard / Video / Mouse
LPPF	Low Power Partial Functionality
LSB	Least Significant Bit
LVDS	Low-Voltage Differential Signaling
MSIO	Multi Serial Input Output
MAC	Media Access Control Layer
MCU	Microcontroller Unit
MIB	Management Information Base
MSB	Most Significant Bit
OM	Operation Mode
PHY	Physical Layer

Term	Definition
PoE	Power Over Ethernet
PRBS	Pseudo Random Bit Stream
RIF	Register Interface
RoHS	Restriction of Hazardous Substances
SERDES	SERializer DESerializer
SNR	Signal-to-Noise Ratio
SPI	Serial Peripheral Interface
STB	Set-Top Box
UART	Universal Asynchronous Receive Transmit
USB	Universal Serial Bus

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1 Introduction

This datasheet provides a detailed description of the Valens VS2010 chipset, which includes an HDBaseT transmitter chip and an HDBaseT receiver chip. The datasheet provides essential information required for designing a VS2010 embedded application.

1.1 About the VS2010 Chipset

Valens Semiconductor developed the VS2010 chipset to enable high-quality transmission of uncompressed, high-definition HDMI 2.0-compatible, multimedia content (audio and video), together with USB 2.0 data – using HDBaseT™ technology – over a single, 100 meter (328 foot) Cat6-standard cable. The VS2010 does not support transmission of HDCP-encrypted video.

The VS2010 family consists of the following devices:

- **VS2010TX:** A source-side implementation designed for use inside high-definition source equipment or extenders.
- **VS2010RX:** A sink-side implementation designed for use inside high-definition display equipment or extenders.

1.2 Features

The VS2010 chipset offers the following features:

- Enables up to 7.2 Gbps of HDMI video traffic (without HDCP encryption), together with USB 2.0 data and other native interfaces, simultaneously over a single 100 meter (328 foot) Cat6 cable (4K video supported up to 90 meter/295 feet over Cat5e cable).
- Support for up to 297MHz pixel clock over HDMI to support 4K/30Hz/4:4:4 and 4K/60Hz/4:2:0 resolutions.
- Support for up to 150 meters in long-reach mode:
  - Up to 4 Gbps HDBaseT Traffic rate
  - HDMI Pixel Frequency 148.5Mhz
- Video Format 1080p / 60Hz / 24bpp
- Native T-adaptor support for various data formats and interfaces, including USB 2.0, CIR, I^2S and UART.
- USB 2.0 support
  - Configurable either as Host or as a Device USB port
  - Up to 7 USB devices supported

- Supports isochronous transfers for USB webcams, microphones, and speakers
- Support for three RJ45 pair arrangements: straight, crossover and semi-crossover
- Traffic latency of less than 10 usec over a 100-meter Cat6 cable.
- Coexistence with PoE (802.3af), PoE+ (802.3at) and PoH
- RoHS compliance.
- Package Dimensions:
  - VS2010TX: LFBGA 21mm x 21mm, 356-ball grid
  - VS2010RX: HSBGA 23 mm x 23 mm, 484-ball grid
  - Ball pitch 1 mm
- Absolute maximum rated junction temperature: minimum -40°C, maximum +125°C

1.3 Main Applications

The VS2010 chipset is ideal for the following applications:

- Internet Café PC extension
- Industrial PC extension

1.4 Application Example

1.4.1 Typical System Connection

Figure 1 displays a typical system application, employing source and sink equipment connected over an HDBaseT link to Rx and Tx boards with embedded VS2010 chips.

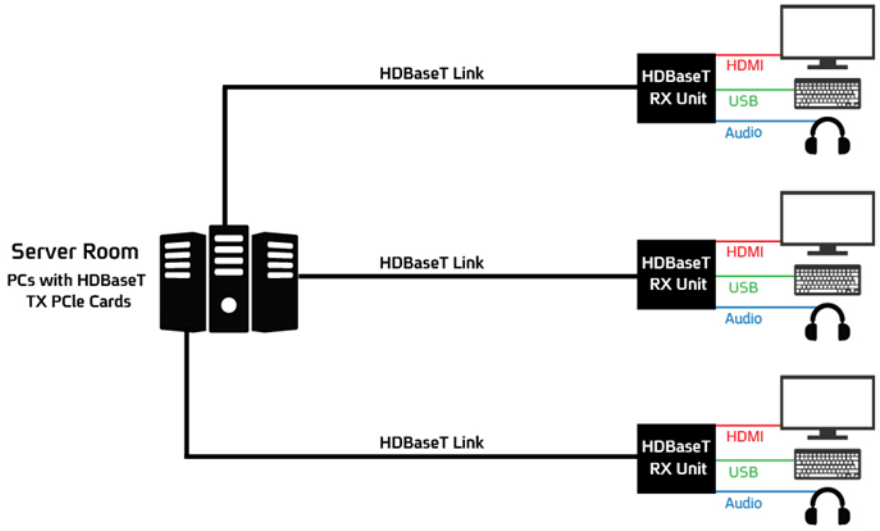


Figure 1: Typical System Connection – Internet Café Application

In Figure 1, the following sources for each signal type are connected to the Tx VS2010 device:

- Non-HDCP video via the HDMI interface
- Audio via the I2S analog interface
- USB 2.0 data via the USB interface
- Control information via the UART interface

The video, audio, USB and control data are all sent to the HDBaseT Rx board over the HDBaseT link using a Cat6 cable with a length of up to 100 meters. The HDBaseT Rx unit converts the HDBaseT stream back to HDMI video, audio and USB streams, which are sent to the display HDMI input, to/from the audio devices (headphones / loudspeakers and microphone) and to / from the mouse and keyboard USB devices via the USB connectors.

1.5 HDBaseT Technology Overview

Valens HDBaseT™ technology empowers **5Play™** digital connectivity between high-definition video sources and remote displays. HDBaseT™ enables plug-and-play delivery of multimedia traffic over a single 100 meter (328 foot) CATx cable:

- Video – Uncompressed high-definition/3D video in up to 4K resolution
- Audio – Any standard digital audio format
- Ethernet – 100BaseTX Ethernet (not supported in VS2010 devices)
- Control – Various control signals including CEC, RS-232, and IR
- Power – Up to 100W using Power-over-Cable (PoH) technology

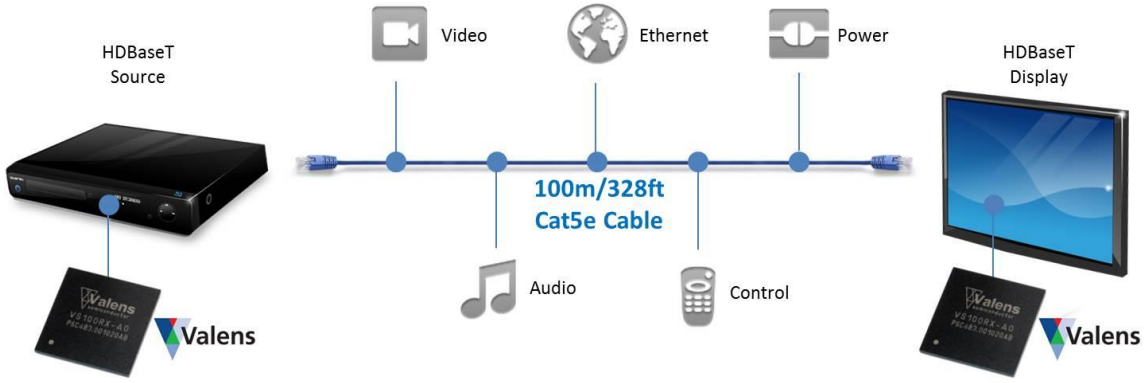


Figure 2: HDBaseT Technology

Video

HDBaseT™ delivers Ultra HD (4K2K@30Hz with YCbCr 4:4:4 and 4K2K@60Hz with YCbCr 4:2:0) formats of up to 1080p@60Hz@48 b/pixel, and 3D – to a network of devices, or over a point-to-point connection. HDBaseT™ provides a transparent transport mechanism for HDMI chipsets, thus supporting all key features of HDMI 2.0, including HPD, 5V, CEC, EDID and HDCP. Valens' proprietary video coding scheme ensures the highest video quality with zero latency.

Note

VS2010 devices do not support transmission of HDCP-encrypted video.

Audio

As with video, HDBaseT™ Audio is transparently transported directly from the HDMI chipset, thus supporting all standard formats, such as Dolby Digital, DTS, Dolby TrueHD, DTS HD-Master Audio and more.

Ethernet – not supported in VS2010 devices

HDBaseT™ supports 100 Mbps Ethernet capabilities, enabling televisions, hi-fi equipment, computers, and other consumer electronic devices to communicate with each other and access stored multimedia content, including video streaming, images and music. Relying on the same physical infrastructure, HDBaseT™ also supports Ethernet Fallback Mode. In this mode, if you plug an HDBaseT device into an Ethernet-only infrastructure, the device will automatically "realize" it and will enable only the Ethernet capabilities of the connection.

Controls

HDBaseT™ delivers a variety of multipurpose control signals, including Consumer Electronic Controls (CEC), RS-232, USB, and infrared. Since HDBaseT™ also supports an Ethernet channel, IP-based control can be employed as well. This opens up endless possibilities for equipment manufacturers, from remote device control to fully managed networks.

The control plane supports additional bandwidth of up to 250 Mbps for applications requiring extra capacity.

Power

As part of its 5Play™ feature-set, HDBaseT™ supports transmission of up to 100W of DC power over the same CATx cable. Now, you can provide power without requiring access to an electic outlet – enhancing device mobility.

1.6 HDBaseT Channel Terminology

The HDBaseT channel consists of two distinct asymmetric unidirectional channels:

- *Main Channel* – Directed downstream from the HDBaseT transmitter to the HDBaseT receiver, carrying uncompressed multimedia content (HDMI, USB, GP MSIO, UART, CIR, I2S) and multimedia controls.
- *Auxiliary Return Channel* – Directed upstream from the HDBaseT receiver to the HDBaseT transmitter, carrying the return channel controls and the receiver to transmitter portion of the data content.

The HDBaseT Transmitter and Receiver chips are labeled VS2010TX and VS2010RX, respectively. The HDBaseT transmitter is used to connect the HD source equipment (STBs, Blu-ray / DVD players, etc.) while the HDBaseT receiver is used to connect the sink equipment (monitors, TVs, projectors, etc.).

1.7 VS2010 Chipset Overview

The figure below is a block diagram illustrating the main functional blocks of the VS2010TX and VS2010RX devices:

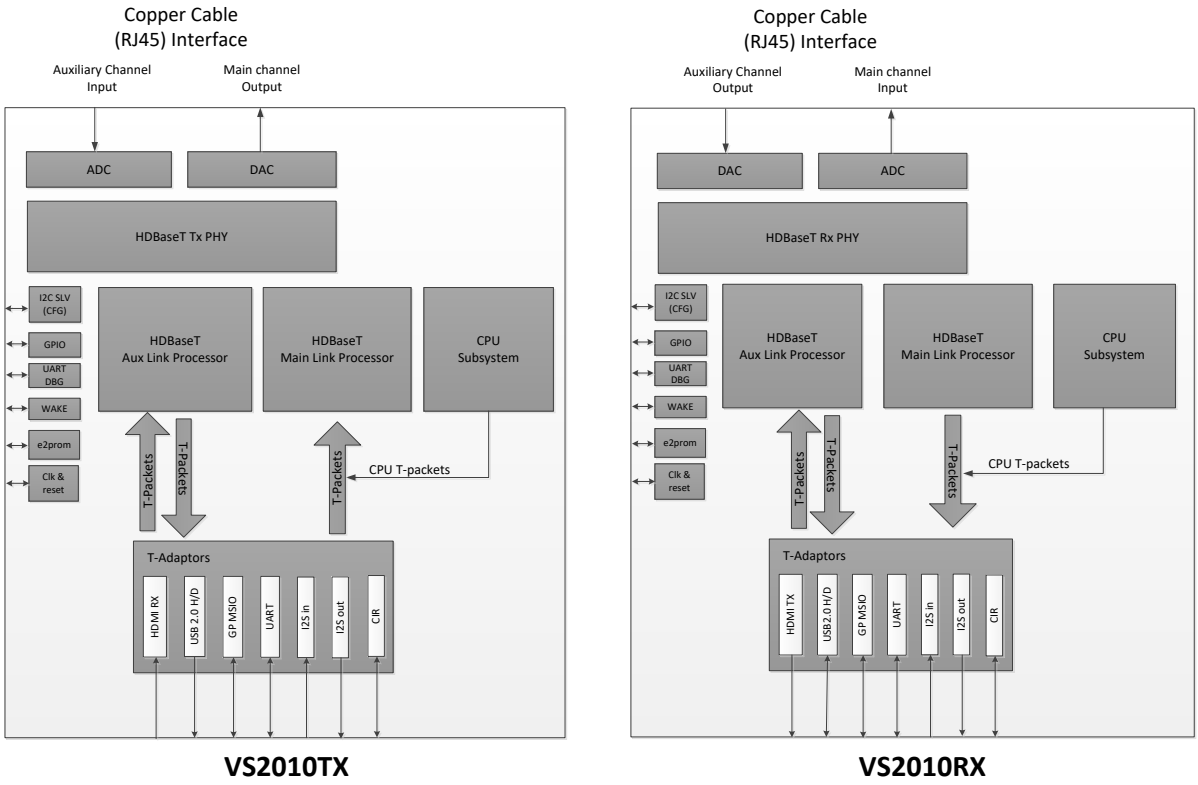


Figure 3: VS2010TX and VS2010RX Block Diagrams

2 Pin Configuration and Ball Diagram

2.1 Interface Diagrams

The interface diagrams in the following sections details the signal groups of the various interfaces. The brackets below each interface group indicate for which part the interface is available.

2.1.1 VS2010TX Interface Diagram

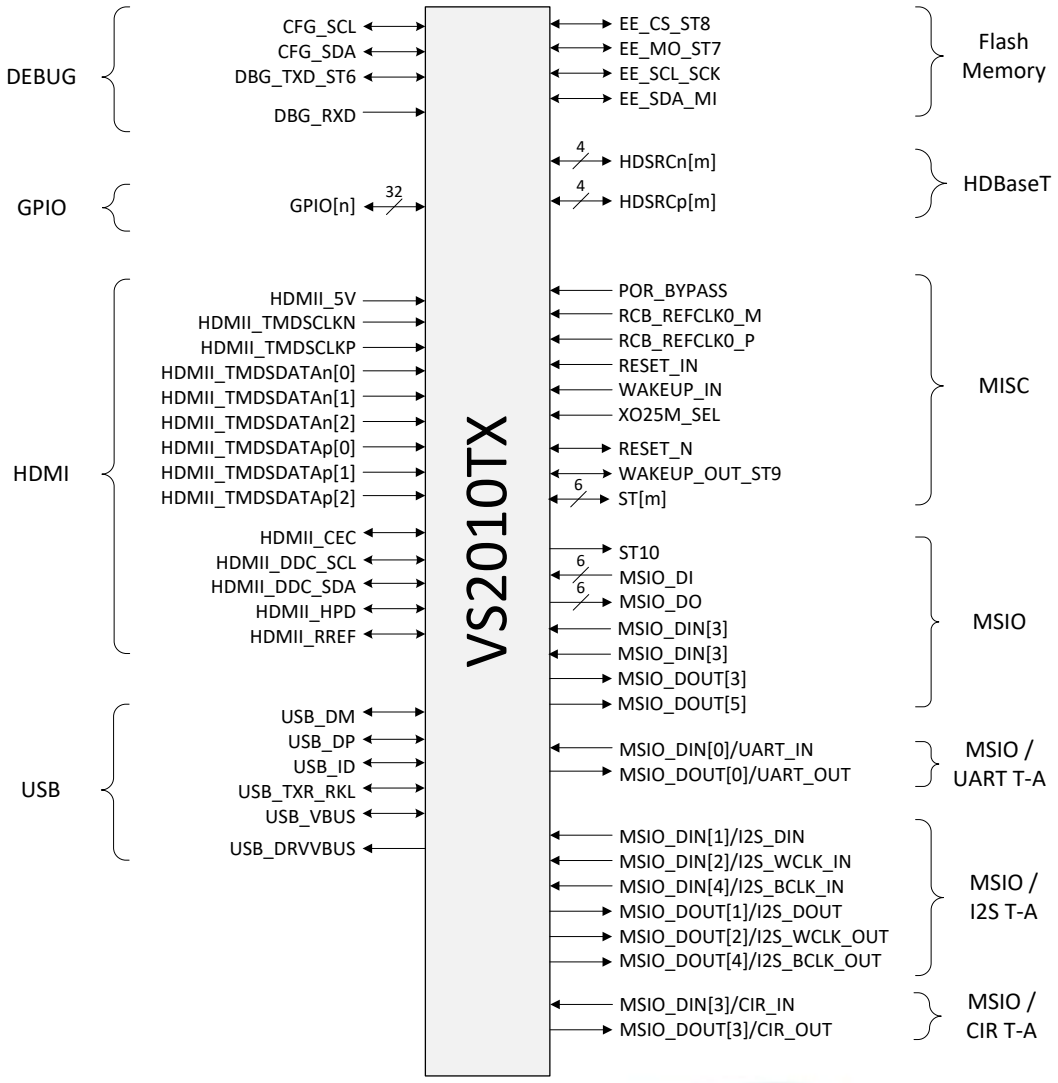


Figure 4: VS2010TX I/F Signal Block Diagram

2.1.2 VS2010RX Interface Diagram

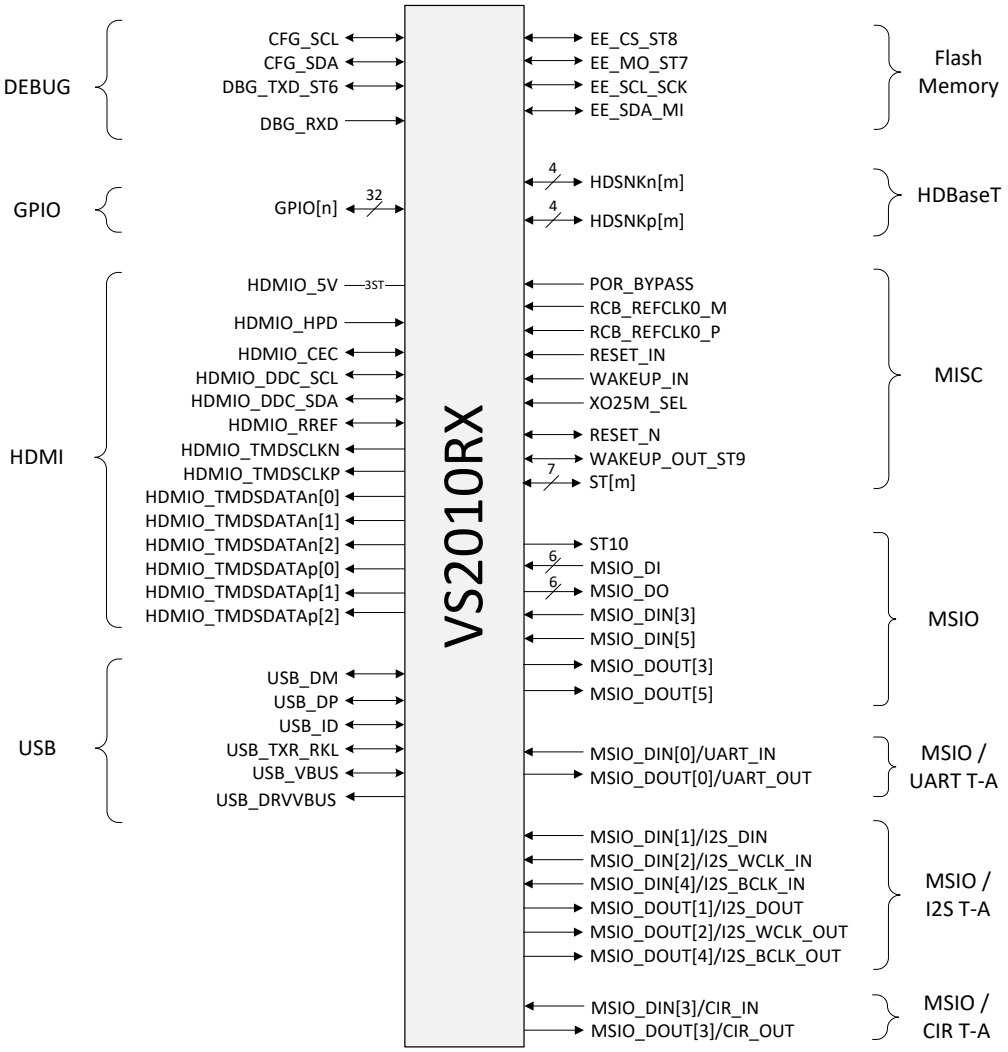


Figure 5: VS2010RX I/F Signal Block Diagram

2.2 Pin Type Convention

2.2.1 IO Pad Types

The VS2010 pin types and their descriptions are listed below:

Table 1: VS2010 Pin Types

Pin Type	Description
Input	Digital input pad
Output	Digital output pad
IO	Bidirectional IO digital pad
Input [PU/PD]	Digital input pad [with integrated pull-up/pull-down resistor]
Output [PU/PD]	Digital output pad [with integrated pull-up/pull-down resistor]
IO, PU	Bidirectional IO digital pad with integrated pull-up resistor
IO, PD	Bidirectional IO digital pad with integrated pull-down resistor
AIO	Analog bidirectional pad
AI	Analog input pad
AO	Analog output pad
03State	Digital output pad with tri-state buffer
XTAL	Crystal I/O pad

2.2.2 Unused Pins

If your application does not use one or more interfaces, you should implement the connectivity of the interface's balls according to the *If Not Used* column in Table 3 for the TX chip and Table 6 for the RX chip.

The following conventions are used to connect unused pins:

Table 2: VS2010 Unused Pin Types

Category	Connection Requirement
NC	Safe to leave unconnected (floating)
GND	Must be connected to a ground
WPD	Must be connected to a ground via a weak pull-down resistor
WPU	Must be connected to 3.3V supply via a weak pull-up resistor
1KPD	Must be connected to a ground via 1Kohm resistor
1KPU	Must be connected to a 3.3V supply via 1Kohm resistor

2.3 VS2010TX Signal Description

Table 3 below provides information on each pin of the VS2010TX chip. Pins with more than one function use the following convention:

- F1: <function 1 description>
- F2: <function 2 description>
- ST: <strap function description>

Selecting between functions of multi-functional pins is performed by either using VS2010 chip parameters or asserting strap pins. For more details, refer to the section in Chapter 6 that corresponds with the relevant interface category.

2.3.1 Tx Functional Signals

Table 3: VS2010TX Functional Signal Table

Signal Name	Ball#	Pad Type	I/f category	If Not Used	Functional Description
CFG_SCL	U9	IO,PU	DEBUG	NC	Host interface I2C clock Signal
CFG_SDA	U10	IO,PU	DEBUG	NC	Host interface I2C data Signal
DBG_RXD	U8	input, PU	DEBUG	NC	Debug Receive Data (I)
DBG_TXD_ST6	U5	IO,PU	DEBUG	NC	Debug Transmit Data (O);ST: strap bit #6
EE_CS_ST8	W4	IO,PD	EEPROM	NC	SPI EEPROM chip select;ST: strap bit #8
EE_MO_ST7	U4	IO,PD	EEPROM	NC	SPI EEPROM MO (master Out);ST: strap bit #7
EE_SCL_SCK	V4	IO,PU	EEPROM	NC	Clock for Both I2C and SPI EEPROMs (O)
EE_SDA_MI	Y4	IO,PU	EEPROM	NC	I2C EEPROM SDA or SPI EEPROM MI (Master In)
GPIO[0]	J3	IO,PU	GPIO	NC	General Purpose IO Bit #0
GPIO[1]	J4	IO,PU	GPIO	NC	General Purpose IO Bit #1
GPIO[16]	H17	IO,PU	GPIO	4.7K-10K PD	General purpose IO bit #16 (IO). Must be tied to external 4.7K-10K pulldown resistor in all applications.
GPIO[17]	H18	IO,PU	GPIO	4.7K-10K PD	General purpose IO bit #17 (IO). Must be tied to external 4.7K-10K pulldown resistor in all applications.
GPIO[18]	H19	IO,PU	GPIO	NC	General purpose IO bit #18 (IO)
GPIO[19]	H20	IO,PU	GPIO	NC	General purpose IO bit #19 (IO)
GPIO[2]	E4	IO,PU	GPIO	NC	General Purpose IO Bit #2
GPIO[20]/MSIO_DO[0]	J17	IO,PU	GPIO	NC	F1: General purpose IO bit #20 (IO); F2: MSIO data output bit #0

Signal Name	Ball#	Pad Type	I/f category	If Not Used	Functional Description
GPIO[21]/MSIO_DO[1]	J18	IO,PU	GPIO	NC	F1: General purpose IO bit #21 (IO); F2: MSIO data output bit #1
GPIO[22]/MSIO_DO[2]	J19	IO,PU	GPIO	NC	F1: General purpose IO bit #22 (IO); F2: MSIO data output bit #2
GPIO[23]/MSIO_DO[3]	J20	IO,PU	GPIO	NC	F1: General purpose IO bit #23 (IO); F2: MSIO data output bit #3
GPIO[24]/MSIO_DO[4]	K17	IO,PU	GPIO	NC	F1: General purpose IO bit #24 (IO); F2: MSIO data output bit #4
GPIO[25]/MSIO_DO[5]	K18	IO,PU	GPIO	NC	F1: General purpose IO bit #25 (IO); F2: MSIO data output bit #5
GPIO[26]/MSIO_DI[0]	K19	IO,PU	GPIO	NC	F1: General purpose IO bit #26 (IO); F2: MSIO data input bit #0 (future use)
GPIO[27]/MSIO_DI[1]	K20	IO,PU	GPIO	NC	F1: General purpose IO bit #27 (IO); F2: MSIO data input bit #1
GPIO[28]/MSIO_DI[2]	L17	IO,PU	GPIO	NC	F1: General purpose IO bit #28 (IO); F2: MSIO data input bit #2
GPIO[29]/MSIO_DI[3]	L18	IO,PU	GPIO	NC	F1: General purpose IO bit #29 (IO); F2: MSIO data input bit #3
GPIO[3]	C3	IO,PU	GPIO	NC	General Purpose IO Bit #3
GPIO[30]/MSIO_DI[4]	L19	IO,PU	GPIO	NC	F1: General purpose IO bit #30 (IO); F2: MSIO data input bit #4
GPIO[31]/MSIO_DI[5]	L20	IO,PU	GPIO	NC	F1: General purpose IO bit #31 (IO); F2: MSIO data input bit #5
HDII_CB_RTT_EXRES	D14	AIO	HDI	Must Use	HDI central bais external resistor; Should be tied to a 1KOhm (1% tolerance) pull down resistor.
HDMII_5V	U20	Input	HDMI	GND	HDMI Rx 5V power signal input
HDMII_CEC	U19	IO	HDMI	WPU	HDMI Rx CEC bus
HDMII_DDC_SCL	U16	IO	HDMI	WPU	HDMI Rx DDC I2C clock
HDMII_DDC_SDA	U17	IO	HDMI	WPU	HDMI Rx DDC I2C data
HDMII_HPD	U18	IO	HDMI	WPU	HDMI Rx hot plug detect output
HDMII_RREF	U15	AIO	HDMI	Must Use	HDMI current Source Resistor; Should be tied to a 12 KOhm (1% tolerance) pull up resistor, AVDD33
HDMII_TMDSCLKN	Y13	AI	HDMI	NC	HDMI Rx TMDS clock lane (N)
HDMII_TMDSCLKP	W13	AI	HDMI	NC	HDMI Rx TMDS clock lane (P)
HDMII_TMDSDATAn[0]	Y15	AI	HDMI	NC	HDMI Rx TMDS data lane 0 (N)
HDMII_TMDSDATAn[1]	Y17	AI	HDMI	NC	HDMI Rx TMDS data lane 1 (N)

Signal Name	Ball#	Pad Type	I/f category	If Not Used	Functional Description
HDMII_TMDSDATAn[2]	Y19	AI	HDMI	NC	HDMI Rx TMDS data lane 2 (N)
HDMII_TMDSDATAp[0]	W15	AI	HDMI	NC	HDMI Rx TMDS data lane 0 (P)
HDMII_TMDSDATAp[1]	W17	AI	HDMI	NC	HDMI Rx TMDS data lane 1 (P)
HDMII_TMDSDATAp[2]	W19	AI	HDMI	NC	HDMI Rx TMDS data lane 2 (P)
HDSRC_REXT_H	V11	AIO	HDBaseT	Must Use	HDBT current Source Resistor. Should be tied to a 4.53 KOhm (1% tolerance) pull down resistor.
HDSRCn[0]	Y6	AIO	HDBaseT	NC	HDBaseT Transceive Channel 0 (N)
HDSRCn[1]	Y7	AIO	HDBaseT	NC	HDBaseT Transceive Channel 1 (N)
HDSRCn[2]	Y9	AIO	HDBaseT	NC	HDBaseT Transceive Channel 2 (N)
HDSRCn[3]	Y10	AIO	HDBaseT	NC	HDBaseT Transceive Channel 3 (N)
HDSRCp[0]	W6	AIO	HDBaseT	NC	HDBaseT Transceive Channel 0 (P)
HDSRCp[1]	W7	AIO	HDBaseT	NC	HDBaseT Transceive Channel 1 (P)
HDSRCp[2]	W9	AIO	HDBaseT	NC	HDBaseT Transceive Channel 2 (P)
HDSRCp[3]	W10	AIO	HDBaseT	NC	HDBaseT Transceive Channel 3 (P)
ST10	G20	IO	MSIO	WPU	Strap pin #10
MSIO_DIN[0]/UART_IN/ GPIO[4]	D20	IO,PU	MSIO	NC	F1: MSIO data input #0; F2: UART in ; F3: General purpose pin #4
MSIO_DIN[1]/I2S_DIN/ GPIO[5]	E17	IO,PU	MSIO	NC	F1: MSIO data input #1; F2: I2S data in; F3:General purpose pin #5
MSIO_DIN[2]/I2S_WCLK _IN/GPIO[6]	E18	IO,PU	MSIO	NC	F1: MSIO data input #2; F2: I2S WCLK in; F3:General purpose pin #6
MSIO_DIN[3]/CIR_IN/ GPIO[7]	E19	IO,PU	MSIO	NC	F1: MSIO data input #3; F2: CIR In; F3:General purpose pin #7
MSIO_DIN[4]/I2S_BCLK _IN/GPIO[8]	E20	IO,PU	MSIO	NC	F1: MSIO data input #4; F2: I2S BCLK in; f3:General purpose pin #8
MSIO_DIN[5]/GPIO[9]	F20	IO,PU	MSIO	NC	F1: MSIO data input #5; F2:General purpose pin #9
MSIO_DOUT[0]/UART_ OUT/GPIO[10]	F19	IO,PU	MSIO	NC	F1: MSIO data output #0; F2: UART out; F3:General purpose pin #10
MSIO_DOUT[1]/I2S_DO UT/GPIO[11]	F18	IO,PU	MSIO	NC	F1: MSIO data output #1; F2: I2S data out; F3:General purpose pin #11
MSIO_DOUT[2]/I2S_WC LK_OUT/GPIO[12]	F17	IO,PU	MSIO	NC	F1: MSIO data output #2; F2: I2S WCLK out; F3:General purpose pin #12
MSIO_DOUT[3]/ CIR_OUT/GPIO[13]	G17	IO,PU	MSIO	NC	F1: MSIO data output #3; F2: CIR Out; F3:General purpose pin #13

MSIO_DOUT[4]/I2S_BCLK_OUT/GPIO[14]	G18	IO,PU	MSIO	NC	F1: MSIO data output #4; F2: I2S BCLK out; f3:General purpose pin #14
MSIO_DOUT[5]/GPIO[15]	G19	IO,PU	MSIO	NC	F1: MSIO data output #5; F2:General purpose pin #15
POR_BYPASS	C20	Input	MISC	Must use	Power on reset bypass; PD '0'- POR Enabled; PU '1'-POR Disabled
QVDD25	C17	N/A	FU	GND	Reserved. Must be tied to ground
RCB_REFCLK0_M	W1	AI	MISC	If XO25M_SEL=1 short to VDD18	F1: 125MHz LVDS reference Clock (N); F2: 1.2V dc (see application notes on single ended application for this pin).
RCB_REFCLK0_P	W2	AI	MISC	If XO25M_SEL=1 short to VDD18	F1: 125MHz LVDS reference Clock (P); F2: 125MHz Single-ended reference clock
RESET_IN	B20	Input	MISC	WPU	VS2310 Tx Reset In (Active only when POR_BYPASS=1)
RESET_N	D15	AIO	MISC	WPU	Power on reset bi-directional pin (open drain). 4.7 KOhm PU resistor to AVDD33 and 1nF capacitor to GND close to the pin are needed when active (POR_BYPASS=0)
ST0	C2	IO,PD	MISC	Must Use	Strap bit #0
ST1	B1	IO,PD	MISC	Must Use	Strap bit #1
ST2	C1	IO,PD	MISC	Must Use	Strap bit #2
ST3	D1	IO,PU	MISC	Must Use	Strap bit #3.Must be connected to 1k pulldown in all applications.
ST4	D4	IO,PU	MISC	Must Use	Strap bit #4
ST5	D3	IO,PD	MISC	Must Use	Strap bit #5
TCK	M4	Input,PU	JTAG	NC	JTAG
TDI	T4	Input,PU	JTAG	NC	JTAG
TDO	R4	O3State	JTAG	NC	JTAG
TMS	P4	Input,PU	JTAG	NC	JTAG
TRST	N4	Input,PD	JTAG	1KPD	JTAG
USB_DM	R19	AIO	USB	NC	DM pin of the USB connector (IO)
USB_DP	R20	AIO	USB	NC	DP pin of the USB connector (IO)
USB_DRVVBUS	M18	Output	USB	NC	VBUS charge pump control

USB_ID	T17	AIO, PU	USB	NC	Identification (ID) pin of the USB connector. '1' indicates that VS2010 is connected to a host (USBH mode). '0' indicates that VS2010 is connected to a device (USBD mode).
USB_TXR_RKL	P18	AIO	USB	Must Use	Reference resistor. Should be tied to a 44.2 Ohm (1% tolerance) pull down resistor.
USB_VBUS	R17	AIO	USB	NC	VBUS pin of the USB connector
USB_XI	N20	XTAL	USB	NC	USB 12MHz Crystal clock input
USB_XO	N19	XTAL	USB	NC	USB 12MHz Crystal clock output
WAKEUP_IN	Y3	Input,PU	MISC	NC	Wakeup Input
WAKEUP_OUT_ST9	W3	IO	MISC	WPD	Wakeup Output;ST: strap pin #9
XO25M_SEL	V3	Input,PD	MISC	NC	Reference clock source select:'1' – 25MHz reference clock, crystal or LVCMOS oscillator; '0'- 125MHz reference clock through RCB_REFCLK0_P/M pins **NOTE THAT 25MHz CRYSTAL IS FOR FUTURE USE ONLY**
XO25MHZ_XIN	Y2	XTAL	MISC	If XO25M_SEL=0 short to GND	25MHz Crystal clock or LVCMOS oscillator input **NOTE THAT 25MHz CRYSTAL IS FOR FUTURE USE ONLY**
XO25MHZ_XOUT	Y1	XTAL	MISC	NC	25MHz Crystal clock output **NOTE THAT 25MHz CRYSTAL IS FOR FUTURE USE ONLY**

2.3.2 Tx Non-Functional Signals

Table 4: VS2010TX Non-functional Signal Table

Symbol	Type	Description	Ball Numbers
NC	Non-connected balls	Non-Connected Balls	M3, K1, L3, R1, T2, T1, L4, K4, R3, P1, R2, M1, P2, N1, M2, T3, P3, N3, L1, N2, K2, L2, U2, U1, U3, K3, M17, V6, V7
FU	Future Use	Reserved. Must be tied to 3.3V external 1K pull-up resistor.	C19
FU	Future Use	Reserved. Must be tied to external weak pull-down resistor.	D19
FU_V1	JTAG	TEST_MODE_1. Must be tied to external weak pulldown resistor (27.4K)	V1

Symbol	Type	Description	Ball Numbers
FU_V2	JTAG	TEST_MODE_0. Must be tied to external weak pulldown resistor (27.4K).	V2
NS	Not Supported	Not supported	E3, F3, D2, G4, H3, J2, J1, F2, F1, H2, H1, U7, U6, U12, U14, U11, U13, B2, B3, B4, B5, B7, B8, B9, B10, A2, A3, A4, A5, A7, A8, A9, A10, A6, B6, C12, D7, A19, A18, A17, A16, A14, A13, A12, A11, B19, B18, B17, B16, B14, B13, B12, B11, A15, B15, C7, D6, D5, C4, C8, C6
NS	Not Supported	Not supported – Must be tied to external 1K pulldown resistor	H4
NS	Not Supported	Not supported – must be connected to GND	F4, G3, D11, D10, D9, D12, D8, C5
VDD	1.0 V digital supply	1.0 V digital supply	F6, F7, F8, F9, F10, F11, F12, F13, F14, F15, G15, H15, J15, K15, L15, M15, N15, P15, R10, R11, R12, R13, R14, R15
VDD33V	3.3 V supply signals	3.3 V supply signal	G6, H6, J6, K6, L6, M6, N6, P6, R6, R7, R8, R9
AVDD10	1.0 V analog supply signals	1.0 V analog supply signal	C18, D16, D18, M19, N18, P17, R18, T18, V17, V18, V19, V20
AVDD18	1.8 V analog supply signals	1.8 V analog supply signal	C13, C15, C16, V5, V8, V9, V10
AVDD33	3.3 V analog supply signals	3.3 V analog supply signal	C9, C11, V12, V13, V15, V16
AVDD33_TERM	3.3 V termination supply	3.3 V termination supply	V14
VSS	Ground signals	Ground signal	A1, A20, C10, C14, D13, D17, E1, E2, G1, G2, G7, G8, G9, G10, G11, G12, G13, G14, H7, H8, H9, H10, H11, H12, H13, H14, J7, J8, J9, J10, J11, J12, J13, J14, K7, K8, K9, K10, K11, K12, K13, K14, L7, L8, L9, L10, L11, L12, L13, L14, M7, M8, M9, M10, M11, M12, M13, M14, M20, N7, N8, N9, N10, N11, N12, N13, N14, N17, P7, P8, P9, P10, P11, P12, P13, P14, P19, P20, T19, T20, W5, W8, W11, W12, W14, W16, W18, W20, Y5, Y8, Y11, Y12, Y14, Y16, Y18, Y20

2.3.3 Tx Bias Resistors

Bias resistors are used to set an internal bias reference current and should be placed as close as possible to their BGA ball.

Table 5: Reference Resistor Values in VS2010TX

Pin Name	Ball #	Resistor Value [ohms]	PU/PD
HDSRC_REXT_H	V11	4.53K	PD to VSS
HDMIDES_RREF	U15	12K	PU to AVDD33
HDII_CB_RTT_EXRES	D14	1K	PD to VSS
USB_TXR_RKL	P18	44.2	PD to VSS

2.3.4 VS2010TX Ball Diagram (Top View)

Matrix	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	Matrix
A	VSS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	VSS	A
B	ST1	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	RESET_IN	B
C	ST2	ST0	GPIO[3]	NS	NS	NS	NS	NS	AVDD33	VSS	AVDD33	NS	AVDD18	VSS	AVDD18	AVDD18	QVDD25	AVDD10	FU_C19	POR_BYPASS	C
D	ST3	NS	ST5	ST4	NS	NS	NS	NS	NS	NS	NS	NS	VSS	HDII_CB_RTT_EXRES	RESET_N	AVDD10	VSS	AVDD10	FU_D19	MSIO_DIN[0]/UART_IN/GPIO[4]	D
E	VSS	VSS	NS	GPIO[2]													MSIO_DIN[1]/I2S_DIN/GPIO[5]	MSIO_DIN[2]/I2S_WCLK_IN/GPIO[6]	MSIO_DIN[3]/GPIO[7]	MSIO_DIN[4]/I2S_BCLK_IN/GPIO[8]	E
F	NS	NS	NS	NS		VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD		MSIO_DOUT[2]/I2S_WCLK_OUT/GPIO[12]	MSIO_DOUT[1]/I2S_DOUT/GPIO[11]	MSIO_DOUT[0]/UART_OUT/GPIO[10]	MSIO_DIN[5]/GPIO[9]	F
G	VSS	VSS	NS	NS		VDD33V	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD		MSIO_DOUT[3]/GPIO[13]	MSIO_DOUT[4]/I2S_BCLK_OUT/GPIO[14]	MSIO_DOUT[5]/GPIO[15]	ST10	G
H	NS	NS	NS	NS		VDD33V	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD		GPIO[16]	GPIO[17]	GPIO[18]	GPIO[19]	H
J	NS	NS	GPIO[0]	GPIO[1]		VDD33V	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD		GPIO[20]/MSIO_DO[0]	GPIO[21]/MSIO_DO[1]	GPIO[22]/MSIO_DO[2]	GPIO[23]/MSIO_DO[3]	J
K	NC	NC	NC	NC		VDD33V	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD		GPIO[24]/MSIO_DO[4]	GPIO[25]/MSIO_DO[5]	GPIO[26]/MSIO_DI[0]	GPIO[27]/MSIO_DI[1]	K
L	NC	NC	NC	NC		VDD33V	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD		GPIO[28]/MSIO_DI[2]	GPIO[29]/MSIO_DI[3]	GPIO[30]/MSIO_DI[4]	GPIO[31]/MSIO_DI[5]	L
M	NC	NC	NC	TCK		VDD33V	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD		NC	USB_DRVVBUS	AVDD10	VSS	M
N	NC	NC	NC	TRST		VDD33V	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD		VSS	AVDD10	USB_XO	USB_XI	N
P	NC	NC	NC	TMS		VDD33V	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD		AVDD10	USB_TXR_RKL	VSS	VSS	P
R	NC	NC	NC	TDO		VDD33V	VDD33V	VDD33V	VDD33V	VDD	VDD	VDD	VDD	VDD	VDD		USB_VBUS	AVDD10	USB_DM	USB_DP	R
T	NC	NC	NC	TDI													USB_ID	AVDD10	VSS	VSS	T
U	NC	NC	NC	EE_MOSI_ST7	DBG_TXD_ST6	NS	NS	DBG_RXD	CFG_SCL	CFG_SDA	NS	NS	NS	NS	HDMII_RREF	HDMII_DDC_SCL	HDMII_DDC_SDA	HDMII_HPD	HDMII_CEC	HDMII_5V	U
V	FU_V1	FU_V2	XO2SM_SEL	EE_SCL_SCK	AVDD18	NC	NC	AVDD18	AVDD18	AVDD18	HDSRC_REXT_H	AVDD33	AVDD33	AVDD33_TERM	AVDD33	AVDD33	AVDD10	AVDD10	AVDD10	AVDD10	V
W	RCB_REFCLK0_M	RCB_REFCLK0_P	WAKEUP_OUT_ST9	EE_CS_ST8	VSS	HDSRCp[0]	HDSRCp[1]	VSS	HDSRCp[2]	HDSRCp[3]	VSS	VSS	HDMII_TMDSCLKP	VSS	HDMII_TMDSDATAp[0]	VSS	HDMII_TMDSDATAp[1]	VSS	HDMII_TMDSDATAp[2]	VSS	W
Y	XO2SMHZ_XOUT	XO2SMHZ_XIN	WAKEUP_IN	EE_SDA_MI	VSS	HDSRCn[0]	HDSRCn[1]	VSS	HDSRCn[2]	HDSRCn[3]	VSS	VSS	HDMII_TMDSCLKN	VSS	HDMII_TMDSDATAn[0]	VSS	HDMII_TMDSDATAn[1]	VSS	HDMII_TMDSDATAn[2]	VSS	Y
Matrix	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	Matrix

Figure 6: VS2010TX Ball Diagram

2.4 VS2010 RX Signal Description

This section provides information on each pin of the VS2010RX chip. Pins with more than one function use the following convention:

- F1: <function 1 description>
- F2: <function 2 description>
- ST: <strap function description>

Selecting between functions of multi-functional pins is performed by either using VS2010 chip parameters or asserting strap pins. For more details, refer to the section in Chapter 6 that corresponds with the relevant interface category.

2.4.1 Rx Functional Signals

Table 6: VS2010RX Functional Signal Table

Signal Name	Ball #	Pad Type	I/f category	If Not Used	Functional Description
CFG_SCL	E3	IO	Debug	WPD	Host interface I2C clock Signal
CFG_SDA	E4	IO	Debug	NC	Host interface I2C data Signal
DBG_RXD	E1	Input	Debug	3.3V WPU	Debug Receive Data (I)
DBG_TXD_ST6	E2	IO,PU	Debug	NC	Debug Transmit Data (O); ST: strap pin #6
EE_CS_ST8	G2	IO,PD	EEPROM	NC	SPI EEPROM chip select; ST: strap pin #8
EE_MO_ST7	G3	IO,PD	EEPROM	NC	SPI EEPROM MO (master Out); ST: strap pin #7
EE_SCL_SCK	F3	IO,PU	EEPROM	NC	Clock for Both I2C and SPI EEPROMs (O)
EE_SDA_MI	F2	IO,PU	EEPROM	NC	I2C EEPROM SDA or SPI EEPROM MI (Master In)
GPIO[0]	M1	IO,PU	GPIO	NC	General Purpose IO Bit #0
GPIO[1]	N4	IO,PU	GPIO	NC	General Purpose IO Bit #1
GPIO[16]	J20	IO,PU	GPIO	4.7K-10K PD	General purpose IO bit #16 (IO).Must be tied to external 4.7K-10K pulldown resistor in all applications.
GPIO[17]	J22	IO,PU	GPIO	4.7K-10K PD	General purpose IO bit #17 (IO)).Must be tied to external 4.7K-10K pulldown resistor in all applications.
GPIO[18]	J21	IO,PU	GPIO	NC	General purpose IO bit #18 (IO)
GPIO[19]	H20	IO,PU	GPIO	NC	General purpose IO bit #19 (IO)
GPIO[2]	N5	IO,PU	GPIO	NC	General Purpose IO Bit #2
GPIO[20]/MSIO_DO[0]	H22	IO,PU	GPIO	NC	F1: General purpose IO bit #20;F2: MSIO data out 0
GPIO[21]/MSIO_DO[1]	H21	IO,PU	GPIO	NC	F1: General purpose IO bit #21;F2: MSIO data

Signal Name	Ball #	Pad Type	I/f category	If Not Used	Functional Description
					out 1
GPIO[22]/MSIO_DO[2]	G20	IO,PU	GPIO	NC	F1: General purpose IO bit #22;F2: MSIO data out 2
GPIO[23]/MSIO_DO[3]	G22	IO,PU	GPIO	NC	F1: General purpose IO bit #23;F2: MSIO data out 3
GPIO[24]/MSIO_DO[4]	G21	IO,PU	GPIO	NC	F1: General purpose IO bit #24;F2: MSIO data out 4
GPIO[25]/MSIO_DO[5]	F20	IO,PU	GPIO	NC	F1: General purpose IO bit #25;F2: MSIO data out 5
GPIO[26]/MSIO_DI[0]	F19	IO,PU	GPIO	NC	F1: General purpose IO bit #26;F2: MSIO data in 0
GPIO[27]/MSIO_DI[1]	F18	IO,PU	GPIO	NC	F1: General purpose IO bit #27;F2: MSIO data in 1
GPIO[28]/MSIO_DI[2]	E19	IO,PU	GPIO	NC	F1: General purpose IO bit #28;F2: MSIO data in 2
GPIO[29]/MSIO_DI[3]	G19	IO,PU	GPIO	NC	F1: General purpose IO bit #29;F2: MSIO data in 3
GPIO[3]	P5	IO,PU	GPIO	NC	General Purpose IO Bit #3
GPIO[30]/MSIO_DI[4]	H19	IO,PU	GPIO	NC	F1: General purpose IO bit #30;F2: MSIO data in 4
GPIO[31]/MSIO_DI[5]	G18	IO,PU	GPIO	NC	F1: General purpose IO bit #31;F2: MSIO data in 5
HDII_CB_RTT_EXRES	W11	AIO	HDI	Must Use	HDI central bias external resistor. Should be tied to a 1KOhm 1% pull down resistor
HDMIO_5V	E14	O3State	HDMI	NC	HDMI Tx 5V power signal output enable
HDMIO_CEC	E11	IO	HDMI	WPU	HDMI Tx CEC bus
HDMIO_DDC_SCL	E12	IO	HDMI	WPU	HDMI Tx DDC I2C clock
HDMIO_DDC_SDA	E13	IO	HDMI	WPU	HDMI Tx DDC I2C data
HDMIO_HPD	E15	Input, PD	HDMI	NC	HDMI Tx hot plug detect input
HDMIO_RREF	D9	AIO	HDMI	Must use	HDMI current Source Resistor. Should be tied to a 4.02 KOhm 1% pull down resistor.
HDMIO_TMDSCLKN	A13	AO	HDMI	NC	HDMI Tx TMDS clock lane (N)
HDMIO_TMDSCLKP	B13	AO	HDMI	NC	HDMI Tx TMDS clock lane (P)
HDMIO_TMDSDATAn[0]	A11	AO	HDMI	NC	HDMI Tx TMDS data lane 0 (N)
HDMIO_TMDSDATAn[1	A9	AO	HDMI	NC	HDMI Tx TMDS data lane 1 (N)

Signal Name	Ball #	Pad Type	I/f category	If Not Used	Functional Description
]					
HDMIO_TMDSDATAn[2]	A7	AO	HDMI	NC	HDMI Tx TMDS data lane 2 (N)
HDMIO_TMDSDATAp[0]	B11	AO	HDMI	NC	HDMI Tx TMDS data lane 0 (P)
HDMIO_TMDSDATAp[1]	B9	AO	HDMI	NC	HDMI Tx TMDS data lane 1 (P)
HDMIO_TMDSDATAp[2]	B7	AO	HDMI	NC	HDMI Tx TMDS data lane 2 (P)
HDSNK_REXT_H	C19	AIO	HDBaseT	Must Use	HDBT current Source Resistor. Should be tied to a 4.53 KOhm 1% pull down resistor.
HDSNKn[0]	A21	AIO	HDBaseT	NC	HDBaseT Tranceive Channel 0 (N)
HDSNKn[1]	A20	AIO	HDBaseT	NC	HDBaseT Tranceive Channel 1 (N)
HDSNKn[2]	A17	AIO	HDBaseT	NC	HDBaseT Tranceive Channel 2 (N)
HDSNKn[3]	A16	AIO	HDBaseT	NC	HDBaseT Tranceive Channel 3 (N)
HDSNKp[0]	B21	AIO	HDBaseT	NC	HDBaseT Tranceive Channel 0 (P)
HDSNKp[1]	B20	AIO	HDBaseT	NC	HDBaseT Tranceive Channel 1 (P)
HDSNKp[2]	B17	AIO	HDBaseT	NC	HDBaseT Tranceive Channel 2 (P)
HDSNKp[3]	B16	AIO	HDBaseT	NC	HDBaseT Tranceive Channel 3 (P)
ST10	K19	IO	MSIO	WPU	Strap pin #10
MSIO_DIN[0]/UART_IN/ GPIO[4]	P18	IO,PU	MSIO	NC	F1: MSIO data in bit 0; F2:UART in; F3: GPIO bit 4
MSIO_DIN[1]/I2S_DIN/ GPIO[5]	P19	IO,PU	MSIO	NC	F1: MSIO data in bit 1; F2: I2S data [0] in; F3: GPIO bit #5
MSIO_DIN[2]/I2S_WCLK_IN/GPIO[6]	N19	IO,PU	MSIO	NC	F1: MSIO data in bit 2; F2:I2S WCLK in; f3: General purpose pin #6
MSIO_DIN[3]/CIR_IN/ GPIO[7]	N18	IO,PU	MSIO	NC	F1: MSIO data in bit 3; F2: CIR in; F3: GPIO bit 7
MSIO_DIN[4]/I2S_BCLK_in/GPIO[8]	M19	IO,PU	MSIO	NC	F1: MSIO data in bit 4; F2: I2S BCLK in ; f3: GPIO bit 8
MSIO_DIN[5]/GPIO[9]	M18	IO,PU	MSIO	NC	F1: MSIO data in bit 5; F2: GPIO bit 9
MSIO_DOUT[0]/UART_OUT/GPIO[10]	L19	IO,PU	MSIO	NC	F1: MSIO data out bit 0; F2: UART out ; F3: GPIO bit 10
MSIO_DOUT[1]/I2S_DOUT/GPIO[11]	K18	IO,PU	MSIO	NC	F1: MSIO data out bit 1;F2: I2S data [0] out; f3: GPIO bit 11
MSIO_DOUT[2]/I2S_WCLK_OUT/GPIO[12]	L18	IO,PU	MSIO	NC	F1: MSIO data out bit 2; F2: I2S WCLK out; F3: GPIO bit 12
MSIO_DOUT[3]/	J18	IO,PU	MSIO	NC	F1: MSIO data in bit 3; F2: CIR Out; F3: GPIO

Signal Name	Ball #	Pad Type	I/f category	If Not Used	Functional Description
CIR_OUT/GPIO[13]					bit 13
MSIO_DOUT[4]/I2S_BCLK_OUT/GPIO[14]	H18	IO,PU	MSIO	NC	F1: MSIO data in bit 4; F2: I2S BCLK out; f3: GPIO bit 14
MSIO_DOUT[5]/GPIO[15]	J19	IO,PU	MSIO	NC	F1: MSIO data in bit 5; F2: GPIO bit 15
POR_BYPASS	D2	Input	MISC	Must use	Power on reset select: '0'- POR enabled; '1'- POR disabled
QVDD25	J6	N/A	FU	GND	Reserved. Must be tied to ground
RCB_REFCLK0_M	E22	AI	MISC	If XO25M_SEL=1 short to VDD18	F1: 125MHz LVDS reference Clock (N); F2: 1.2V dc (see application notes on single ended application for this pin).
RCB_REFCLK0_P	E21	AI	MISC	If XO25M_SEL=1 short to VDD18	F1: 125MHz LVDS reference Clock (P); F2: 125MHz Single-ended reference clock
RESET_IN	E5	Input	MISC	WPU	VS2310 Tx Reset In (Active only when POR_BYPASS=1)
RESET_N	C1	AIO	MISC	WPU	Power on reset bi-directional pin (open drain). 4.7KOhm PU resistor to AVDD33 and 1nF capacitor to GND close to the pin are needed when active (POR_BYPASS=0)
ST0	V5	IO,PD	MISC	Must Use	Strap pin #0
ST1	V4	IO,PD	MISC	Must Use	Strap pin #1
ST11	U5	IO	MISC	Must Use	Strap pin #11. Must be tied to external weak pulldown resistor in all applications.
ST2	U4	IO,PD	MISC	Must Use	Strap pin #2
ST3	T4	IO,PU	MISC	Must Use	Strap pin #3. Must be connected to 1k pulldown in all applications.
ST4	P4	IO,PU	MISC	Must Use	Strap pin #4
ST5	R4	IO,PD	MISC	Must Use	Strap pin #5
TCK	H3	Input, PU	JTAG	NC	JTAG
TDI	G1	Input, PU	JTAG	NC	JTAG
TDO	H2	O3State	JTAG	NC	JTAG
TMS	F1	Input, PU	JTAG	NC	JTAG

Signal Name	Ball #	Pad Type	I/f category	If Not Used	Functional Description
TRST	H1	Input, PD	JTAG	1KPD	JTAG
USB_DM	B4	AIO	USB	NC	DM pin of the USB connector (IO)
USB_DP	A4	AIO	USB	NC	DP pin of the USB connector (IO)
USB_DRVVBUS	D6	Output	USB	NC	VBUS charge pump control
USB_ID	B5	AIO, PU	USB	NC	Identification (ID) pin of the USB connector. '1' indicates that VS2010 is connected to a host (USBH mode). '0' indicates that VS2010 is connected to a device (USBD mode).
USB_TXR_RKL	C3	AIO	USB	Must Use	Reference resistor. Should be tied to a 44.2 Ohm 1% pull down resistor.
USB_VBUS	C5	AIO	USB	NC	VBUS pin of the USB connector
USB_XI	A2	XTAL	USB	NC	USB 12MHz Crystal clock input
USB_XO	B2	XTAL	USB	NC	USB 12MHz Crystal clock output
WAKEUP_IN	J1	Input, PU	MISC	NC	Wakeup Input
WAKEUP_OUT_ST9	J2	IO	MISC	WPD	Wakeup Output; ST: Strap pin #9
XO25M_SEL	E20	Input, PD	MISC	NC	Reference clock source select: ‘1’- 25MHz reference clock, crystal or LVCMOS oscillator; ‘0’- 125MHz reference clock on RCB_REFCLK0_P/M **NOTE THAT 25MHz CRYSTAL IS FOR FUTURE USE ONLY**
XO25MHZ_XIN	D21	XTAL	MISC	If XO25M_SEL=0 short to GND	25MHz Crystal clock or LVCMOS oscillator input **NOTE THAT 25MHz CRYSTAL IS FOR FUTURE USE ONLY**
XO25MHZ_XOUT	D22	XTAL	MISC	If XO25M_SEL=0 NC	25MHz Crystal clock output **NOTE THAT 25MHz CRYSTAL IS FOR FUTURE USE ONLY**

2.4.2 Rx Non-Functional Signals

Table 7: VS2010RX Non-functional Signal Table

Symbol	Type	Description	Ball Numbers
NC	Non-connected balls	Non-connected ball	C14, D13, D16, D17, D7, E6, E9, K20, K21, K22, L20, L21, L22, M20, M21, M22, N20, N21, N22, P20, P21, P22, R20, R21, R22, T20, T21, T22, U20, U21, U22, V6, V7
FU	Future Use	Reserved. Must be tied to 3.3V external 1K pull-up resistor.	D5
FU	Future Use	Reserved. Must be tied to external weak pull-down resistor	R19
FU_J3	JTAG	TEST_MODE_1. Must be tied to external weak pulldown resistor (27.4K).	J3
FU_J4	JTAG	TEST_MODE_0. Must be tied to external weak pulldown resistor (27.4K).	J4
NS	Not Supported	Not supported	K3, F4, F5, H4, H5, G4, G5, AA20, AA19, AA18, AA17, AA15, AA14, AA13, AA12, AB20, AB19, AB18, AB17, AB15, AB14, AB13, AB12, AA16, AB16, W17, W21, AB3, AB4, AB5, AB6, AB8, AB9, AB10, AB11, AA3, AA4, AA5, AA6, AA8, AA9, AA10, AA11, AB7, AA7, W18, T19, T18, V22, R18, V20, L4, L3, K1, AA1, AB1, V2, V1, Y2, Y1, U2, U1, P2, P1, T2, T1
NS	Not Supported	Not supported – Must be tied to external weak pullup resistor	K2, R5, T5
NS	Not Supported	Not supported – Must be tied to external weak pulldown resistor	K4, M5
NS	Not Supported	Not supported – must be connected to GND	L5, M4, M3, M2, U19, W19, W22, V19, W20, V21, L1, K5, L2
VDD	1.0 V digital supply	1.0 V digital supply	D15, D18, E16, E18, F11, F12, F13, F14, F15, F16, K6, L6, M6, N6, P6, R6, T6, U6, U7, U8, U9, U10, U11, U12, U13, U14, U15, U16, U17, V8, V9, V10, V11, V12, V13, V14, V15, V16, V18
VDD33V	3.3 V supply signals	3.3 V supply signal	E7, F6, F7, F8, F9, F10, F17, G6, G17, H6, H17, J5, J17, K17, L17, M17, N17, P17,

			R17, T17
AVDD10	1.0 V analog supply signals	1.0 V analog supply signal	C15, C16, C17, C18, C20, C21, D20, F22, Y13, Y15, Y16, Y17, Y19, Y21, AA21, AA22
AVDD18	1.8 V analog supply signals	1.8 V analog supply signal	C6, C7, C8, C9, D4, N2, N3, P3, T3, U3, Y3, Y4, Y5, Y6, Y7, AA2
AVDD33	3.3 V analog supply signals	3.3 V analog supply signal	C10, C11, C12, C13, D8, D10, D12
VSS	Ground signals	Ground signal	A3, A5, A6, A8, A10, A12, A14, A15, A18, A19, A22, B1, B3, B6, B8, B10, B12, B14, B15, B18, B19, B22, C2, C4, C22, D1, D3, D11, D14, D19, E8, E10, E17, F21, G7, G8, G9, G10, G11, G12, G13, G14, G15, G16, H7, H8, H9, H10, H11, H12, H13, H14, H15, H16, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, K7, K8, K9, K10, K11, K12, K13, K14, K15, K16, L7, L8, L9, L10, L11, L12, L13, L14, L15, W8, AB22, A1, L16, M7, M8, M9, M10, M11, M12, M13, M14, M15, M16, N1, N7, N8, N9, N10, N11, N12, N13, N14, N15, N16, P7, P8, P9, P10, P11, P12, P13, P14, P15, P16, R1, R2, R3, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, T7, T8, T9, T10, T11, T12, T13, T14, T15, T16, U18, V3, V17, W1, W2, W3, W4, W5, W6, W7, W9, W10, W12, W13, W14, W15, W16, Y8, Y9, Y10, Y11, Y12, Y14, Y18, Y20, Y22, AB2, AB21

2.4.3 Rx Bias Resistors

Bias resistors are used to set an internal bias reference current and should be placed as close as possible to their BGA ball.

Table 8: Reference Resistor Values in VS2010RX

Pin Name	Pin #	Resistor value (ohms)	PU/PD
HDSNK_REXT_H	C19	4.53K	P.D to VSS
HDMISER_RREF	D9	4.02K	P.D to VSS
HDII_CB_RTT_EXRES	W11	1K	P.D to VSS
USB_TXR_RKL	C3	44.2	P.D to VSS

2.4.4 VS2010RX Ball Diagram (Top View)

Matrix	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	Matrix
A	VSS	USB_XI	VSS	USB_DP	VSS	VSS	HDMIO_TMDSDATAn[2]	VSS	HDMIO_TMDSDATAn[1]	VSS	HDMIO_TMDSDATAn[0]	VSS	HDMIO_TMDSCLKN	VSS	VSS	HDSNKn[3]	HDSNKn[2]	VSS	VSS	HDSNKn[1]	HDSNKn[0]	VSS	A
B	VSS	USB_XO	VSS	USB_DM	USB_ID	VSS	HDMIO_TMDSDATAp[2]	VSS	HDMIO_TMDSDATAp[1]	VSS	HDMIO_TMDSDATAp[0]	VSS	HDMIO_TMDSCLKP	VSS	VSS	HDSNKp[3]	HDSNKp[2]	VSS	VSS	HDSNKp[1]	HDSNKp[0]	VSS	B
C	RESET_N	VSS	USB_TXR_RKL	VSS	USB_VBUS	AVDD18	AVDD18	AVDD18	AVDD18	AVDD33	AVDD33	AVDD33	AVDD33	NC	AVDD10	AVDD10	AVDD10	AVDD10	HDSNK_REXT_H	AVDD10	AVDD10	VSS	C
D	VSS	POR_BYPASS	VSS	AVDD18	FU_D5	USB_DRVVBUS	NC	AVDD33	HDMIO_RREF	AVDD33	VSS	AVDD33	NC	VSS	VDD	NC	NC	VDD	VSS	AVDD10	XO25MHZ_XIN	XO25MHZ_XOUT	D
E	DBG_RXD	DBG_TXD_ST6	CFG_SCL	CFG_SDA	RESET_IN	NC	VDD33V	VSS	NC	VSS	HDMIO_CEC	HDMIO_DDC_SCL	HDMIO_DDC_SDA	HDMIO_5V	HDMIO_HPD	VDD	VSS	VDD	GPIO[28]/MSIO_D[2]	XO25M_SEL	RCB_REFCLK0_P	RCB_REFCLK0_M	E
F	TMS	EE_SDA_MI	EE_SCL_SCK	NS	NS	VDD33V	VDD33V	VDD33V	VDD33V	VDD33V	VDD	VDD	VDD	VDD	VDD	VDD	VDD33V	GPIO[27]/MSIO_D[3]	GPIO[26]/MSIO_D[0]	GPIO[25]/MSIO_DO[5]	VSS	AVDD10	F
G	TDI	EE_CS_ST8	EE_MO_ST7	NS	NS	VDD33V	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD33V	GPIO[31]/MSIO_D[5]	GPIO[29]/MSIO_D[3]	GPIO[22]/MSIO_DO[2]	GPIO[24]/MSIO_DO[4]	GPIO[23]/MSIO_DO[3]	G
H	TRST	TDO	TCK	NS	NS	VDD33V	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD33V	MSIO_DOUT[4]/I2S_BCLK_OUT/GPIO[14]	GPIO[30]/MSIO_D[4]	GPIO[18]	GPIO[21]/MSIO_DO[1]	GPIO[20]/MSIO_DO[0]	H
J	WAKEUP_IN	WAKEUP_OUT_ST9	FU_J3	FU_J4	VDD33V	QVDD25	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD33V	MSIO_DOUT[3]/GPIO[13]	MSIO_DOUT[5]/GPIO[15]	GPIO[16]	GPIO[18]	GPIO[17]	J
K	NS	NS	NS	NS	NS	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD33V	MSIO_DOUT[1]/I2S_DOUT/GPIO[11]	ST10	NC	NC	NC	K
L	NS	NS	NS	NS	NS	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD33V	MSIO_DOUT[2]/I2S_WCLK_OUT/GPIO[12]	MSIO_DOUT[0]/UART_OUT/GPIO[10]	NC	NC	NC	L
M	GPIO[0]	NS	NS	NS	NS	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD33V	MSIO_DIN[5]/GPIO[9]	MSIO_DIN[4]/I2S_BCLK_IN/GPIO[8]	NC	NC	NC	M
N	VSS	AVDD18	AVDD18	GPIO[1]	GPIO[2]	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD33V	MSIO_DIN[3]/GPIO[7]	MSIO_DIN[2]/I2S_WCLK_IN/GPIO[6]	NC	NC	NC	N
P	NS	NS	AVDD18	ST4	GPIO[3]	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD33V	MSIO_DIN[0]/UART_IN/GPIO[4]	MSIO_DIN[1]/I2S_DIN/GPIO[5]	NC	NC	NC	P
R	VSS	VSS	VSS	ST5	NS	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD33V	NS	FU_R19	NC	NC	NC	R
T	NS	NS	AVDD18	ST3	NS	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD33V	NS	NS	NC	NC	NC	T
U	NS	NS	AVDD18	ST2	ST11	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VSS	NS	NC	NC	NC	U
V	NS	NS	VSS	ST1	ST0	NC	NC	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VDD	NS	NS	NS	NS	V
W	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	HDI_CB_RTT_EXRES	VSS	VSS	VSS	VSS	VSS	NS	NS	NS	NS	NS	NS	W
Y	NS	NS	AVDD18	AVDD18	AVDD18	AVDD18	AVDD18	VSS	VSS	VSS	VSS	VSS	AVDD10	VSS	AVDD10	AVDD10	AVDD10	VSS	AVDD10	VSS	AVDD10	VSS	Y
AA	NS	AVDD18	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	AVDD10	AVDD10	AA
AB	NS	VSS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	NS	VSS	VSS	AB
Matrix	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	Matrix

Figure 7: VS2010RX Ball Diagram

3 Functional Description

3.1 HDMI Interface

The VS2010 chipset supports an HDMI-compatible interface. The VS2010TX receives non HDCP-encrypted HDMI traffic from a source, converts the traffic into HDBaseT packets (T-packets) and forwards them to the link. On the VS2010RX side, the HDMI interface extracts T-packets with HDMI traffic from the HDBaseT link, converts them back to HDMI and transmits them via the HDMI port.

There are two types of HDMI signals:

- TMDS Signals – includes differential data signals and the differential clock signal.
- HDMI Control Signals – includes all control signals defined in the HDMI 2.0 standard (DDC, 5V, HPD, and CEC).

3.1.1 TMDS Signals

This group contains four pairs of unidirectional differential signals:

- Three differential pairs are used for the HDMI serial data transfer. The data is driven by a TMDS transmit PHY on the VS2010RX chip or received by the VS2010TX chip. The data rate on the TMDS data line can reach up to 3.4 GHz.
- The fourth differential pair is the TMDS clock that is generated by the HDMI transmitter. The frequency of the clock signal is one tenth of the actual serial data rate. The HDMI PHY receiver uses this clock signal to generate the serial clock used for HDMI data recovery.

The VS2010 HDMI transmitters incorporate specialized capabilities suited to dealing with the broad bandwidth of TMDS signals and varying HDMI cable lengths in order to maintain signal quality. For example:

- A TMDS driver with configurable signal pre-emphasis capabilities.
- The VS2010 transmitter supports a double termination feature.
- The VS2010TX HDMI receiver uses an internal adaptive equalizer to improve its signal detection capabilities. The adaptive equalization process is done automatically after the receiver powers up and the optimal equalizer (in terms of BER) is selected.
- The receiver handles two termination types – AC and DC termination.
- The 3 HDMI data lanes in the VS2010TX are swappable.

3.1.2 HDMI Control Signals

This group contains the following signals:

- *HPD* – This signal is an HDMI Rx device output (VS2010RX input and VS2010TX output) that is sent towards the source HDMI equipment, indicating that the sink E-EDID memory is available for reading. The Hot Plug Detect pin can be asserted only when the +5V Power signal from the source is detected.
- *5V* – This signal is output from the source HDMI device (VS2010TX input and VS2010RX output). The HDMI 5V signal is pass-through (by default) – that is, it is only shown on the VS2310RX/VS2000RX output when an HDBaseT link is established and the HDMI Source is connected and outputting its 5V control signal.
- *CEC* – The CEC line is used for high-level user control of HDMI-connected devices.
- *DDC* – This is a two-wire bidirectional I2C interface used for HDMI control. Any HDMI device connected to a VS2010 device must support the I2C clock stretching mechanism.

Note that the HDMI specification requires special treatment for these signals such as pull-up or pull-down resistors. You must utilize these requirements on your board according to the HDMI specification.

3.2 HDBaseT Interface

VS2010 chips use a four-pair STP/UTP cable to transfer AV data over a CATx cable. Figure 8 illustrates conceptual schematics of how the VS2010 RX and TX devices should be connected to the UTP cable when the link is not used to transfer power.

The four-differential HDBaseT pairs in the VS2010 are connected to a transformer and to pull-up resistors. The transformer is connected to the STP/UTP cable via an RJ45 connector.

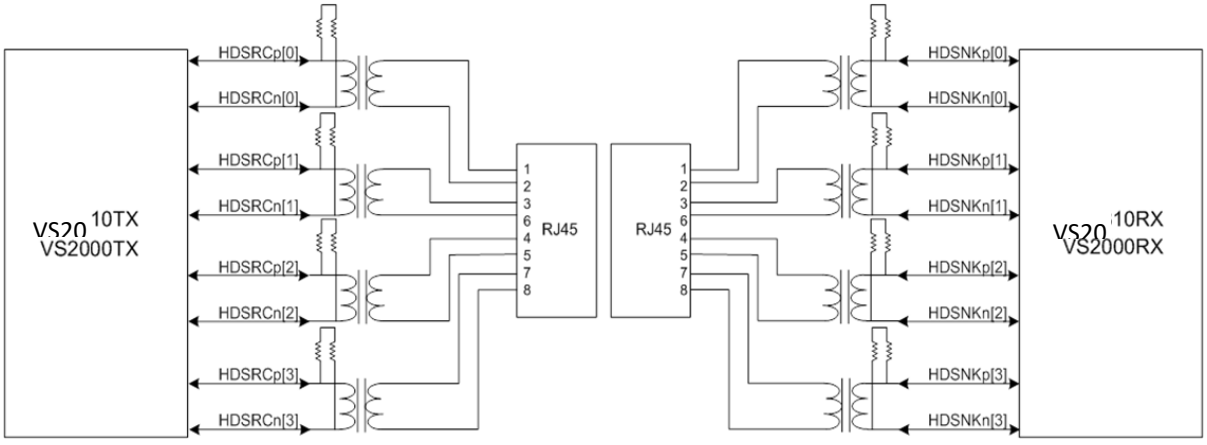


Figure 8: VS2010TX and VS2010RX Link Connection Example

The pair order in the VS2010 HDBaseT interface may be swapped. The HDBaseT PHY automatically detects pairs coupling. Three different configurations are supported: straight, crossover and semi-crossover as shown below:

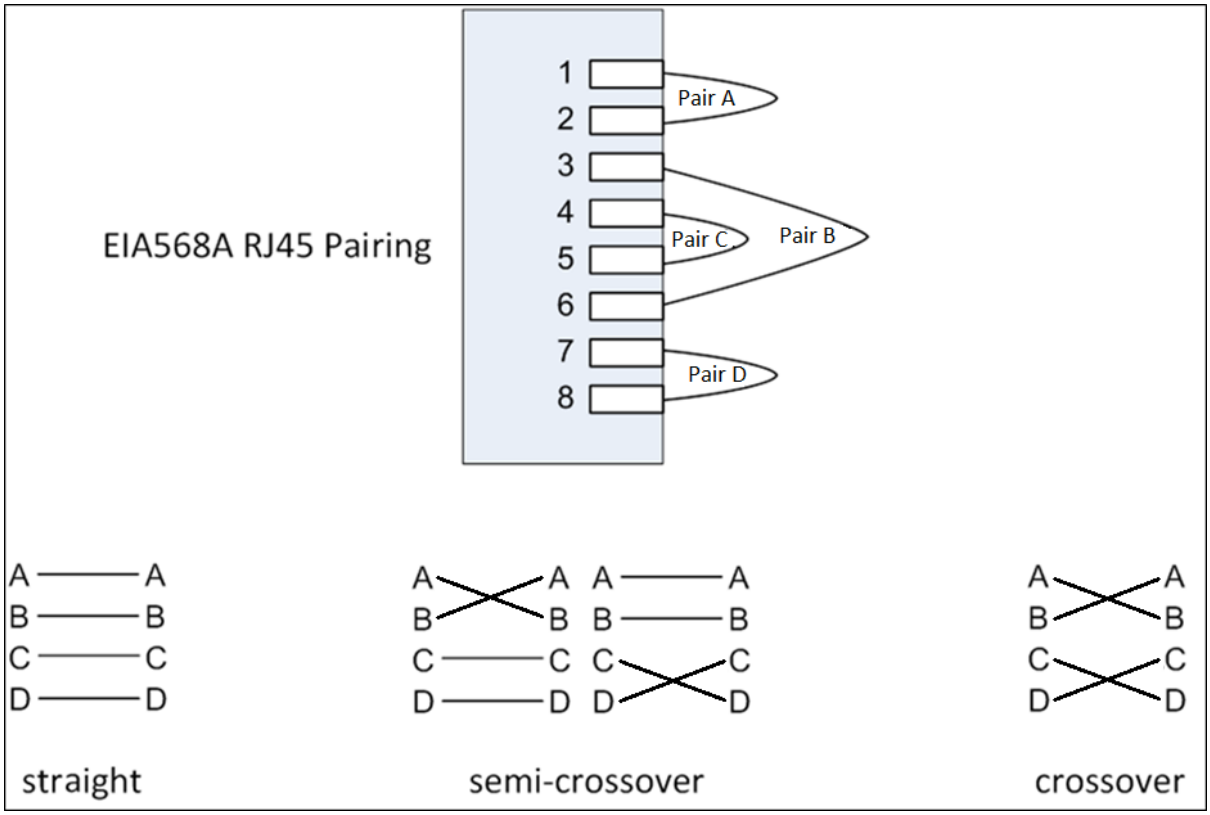


Figure 9: VS2010 RX and TX Pair Coupling

3.3 USB Functionality

The VS2010TX and VS2010RX chips include USB2.0 support for seamlessly extending USB2.0 traffic over the HDBaseT link. These components include:

- Embedded USB2.0 PHY transceiver
- A serial interface engine
- Two types of USB interfaces: USBD and USBH

Both VS2010RX and VS2010TX chips include a USB2.0 T-Adaptor block. The T-adaptors are responsible for converting USB2.0 traffic into T-packets for transfer over the HDBaseT link. This block may be configured by SW parameter to function as either a USBH T-Adaptor or a USBD T-Adaptor and connect either a host or a device respectively. An HDBaseT link with a USBH T-adaptor on one end and a USBD T-adaptor on the other end may be considered a USB2.0 HUB with the upstream port and downstream port. This is shown in the figure below:

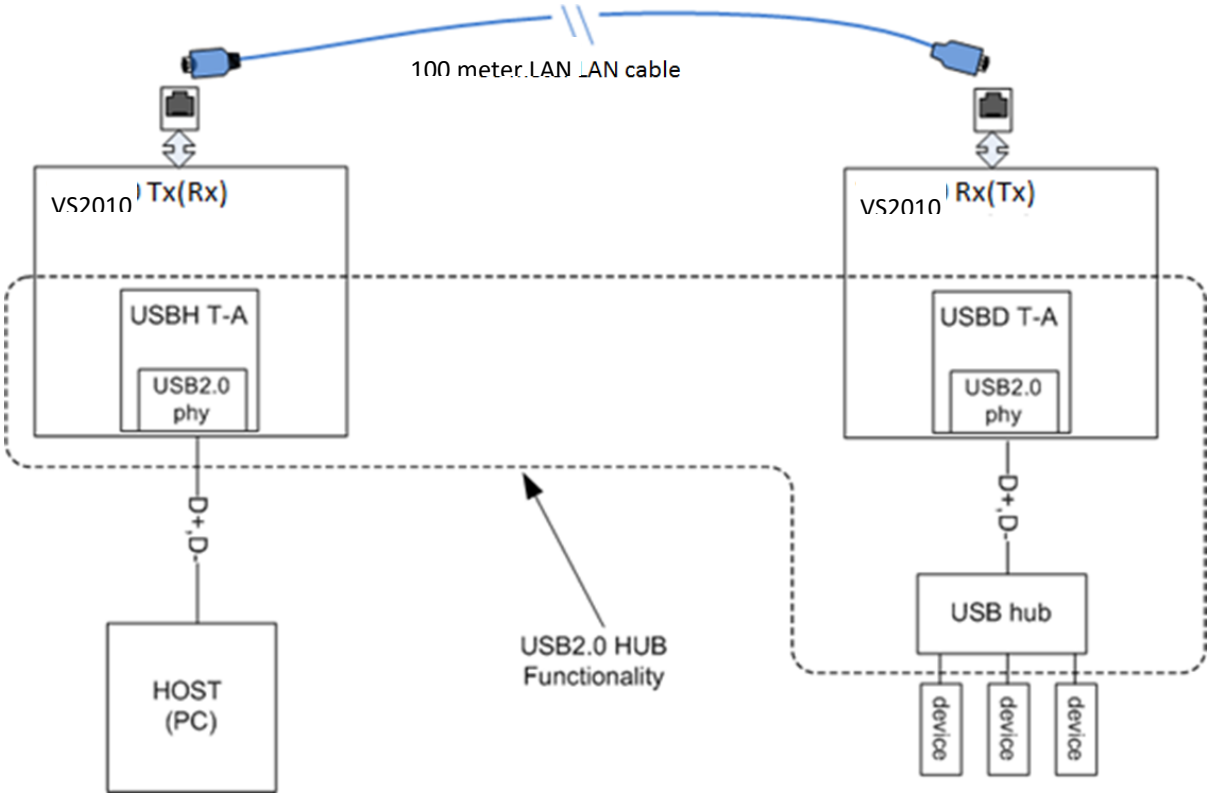


Figure 10: USB2.0 Extension Over HDBaseT Link

Note that the USBD T-adaptor performs an enumeration process with all devices and hubs connected to it. This means that the host sees a flattened tree that includes all devices without cascaded hubs (if present).

Up to 7 USB devices are supported by the USB hub.

The VS2010 chipset supports isochronous transfers for USB webcams, microphones, and speakers.

Refer to the Firmware Release Note for additional information on supported USB functionality.

NOTE

The state of the USB D+ and D- pins is not defined during the Colligo reset state. For some Colligo devices, while the device is in reset state and Vbus is active, USB pins D+ and/or D- may be in a High state. Refer to Application Notes AN2001 (Hardware Design Guidelines) and AN2050 (USB Interface) for additional information and system considerations.

3.4 External Boot Memory I/F

VS2010 chips can be connected to an external SPI Flash memory for storage of software and important system parameters. An SPI interface is used to give the CPU access to the memory.

NOTE

It is also possible to utilize the SPI interface to update the firmware, although this requires special handling. Refer to the *Hardware Design Guideline Application Note* for additional information.

3.5 UART T-Adaptor Functionality

The UART T-adaptor converts native UART traffic from the UART interface (*MSIO_DI0 / UART_TX, MSIO_DO0 / UART_RX*) into HDBaseT packets. UART HDBaseT packets may be transmitted over the link to the partner device. The UART T-adaptor may be configured to two modes of operation:

- Pre-configured
- Oversampled

3.5.1 Working in Pre-configured mode

In this mode, the UART baud rate is known a priori to both partners. This mode is more efficient with respect to data rate consumption. It is recommended to use this mode when high UART rates are required in LPPF1/2 HDBaseT modes. The table below illustrates how to configure a system to preconfigured UART mode:

Table 9: UART Pre-configured Parameter Settings

Parameter Name	Description
TAConf.UART.Mode	Pre-configured
TAConf.UART.BaudRate	The required discrete baud rate
TAConf.UART.CharLen	The required character length (5,6,7 or 8 bits)
TAConf.UART.OversampleRate	Don’t care (leave as default)
TAConf.UART.ParityBit	The required parity true/false
TAConf.UART.StopBit	The required number of stop bits (none, one or two bits)

3.5.2 Working in Oversampled Mode

In this mode, the UART baud rate is unknown a priori. This mode is typically used when a PC with DTE client is connected and the baud rate depends on the managed equipment which may change between setups. In oversampled mode, the UART TX and RX lines are sampled using a 1.5MHz sampling clock on one side and recovered using a recovery clock on the partner's side.

The table below illustrates how to configure a system to oversampled UART mode:

Table 10: UART Oversampled Parameter Settings

Parameter Name	Value
TAConf.UART.Mode	Oversampled
TAConf.UART.BaudRate	Don't care (leave as default)
TAConf.UART.CharLen	Don't care (leave as default)
TAConf.UART.OversampleRate	Fixed, read only field
TAConf.UART.ParityBit	Don't care (leave as default)
TAConf.UART.StopBit	Don't care (leave as default)

NOTE

When using oversampled UART in LPPF mode, the maximum supported baud rate is 115200 Kbps.

3.6 IR T-Adaptor Functionality

Two IR T-adaptors are available on both VS2010 RX and TX chips.

These T-adaptors convert native infrared traffic from the CIR interface (*MSIO_DI3/CIR_IN, MSIO_DO3/CIR_OUT*) into HDBaseT packets. CIR HDBaseT packets may be transmitted over the link to the partner device.

The IR signal input from the *CIR_IN* signal is oversampled by the CIR-Tx T-adaptor and transferred over the link in an HDBaseT packet format. The CIR-Rx T-adaptor receives the CIR T-packets and recovers the original IR wave over the *CIR_OUT* signal. On each side, the user assigns the attributes of its received/transmitted CIR signal using the CIR T-adaptor info parameters.

3.7 I^2S T-Adaptor Functionality

Two I^2S audio T-adaptors are available on VS2010 RX and TX chips.
These T-adaptors convert native I^2S audio traffic from the I^2S input interface into HDBaseT packets:

- MSIO_DIN[1]/I2S_DIN/GPIO[5]
- MSIO_DIN[2]/I2S_WCLK_IN/GPIO[6]
- MSIO_DIN[4]/I2S_BCLK_IN/GPIO[8]

On the other side of the link, the native I^2S signals are recovered via the pins:

- MSIO_DOUT[1]/I2S_DOUT/GPIO[11]
- MSIO_DOUT[2]/I2S_WCLK_OUT/GPIO[12]
- MSIO_DOUT[4]/I2S_BCLK_OUT/GPIO[14]

The maximum I2S BCLK rate currently supported is 5MHz.

NOTE

Special care should be taken when selecting an audio DAC device. The designer should be aware that the Audio DAC device must include an integrated PLL. Using an audio DAC without an integrated PLL may result in audio corruption.

4 Traffic Rate Specification

The auxiliary channel has an aggregated traffic budget of 300 Mbps. For T-Adaptors, the budget is 280 Mbps (due to additional overhead) that is shared between the T-adaptors that are enabled by the application. Enabling or disabling T-adaptors is possible using *system.FeatureList.<T-adaptor name>.class of parameters*.

When a T-adaptor is enabled, its native data packets consume traffic rate budget according to the values specified in Table 11 below.

Table 11: T-Adaptor Auxiliary Channel Traffic Consumption

Feature	Active (Double-Aux) Consumed bit rate (Mbps)
Aggregated budget	280
I2S	12
UART (oversampled @115200 baud)	3
MSIO	6
CIR (oversampled, pass-through)	0.5
HDMI controls (DDC, 5V,HPD)	3.3
Total Excluding USB	24.8
USB	Best Effort - utilizes remaining available bandwidth. For example, when all the features above are active, USB can utilize 280 – 24.8 = 255.2 Mbps.

5 HDBaseT Operational Modes

5.1 Overview

The VS2010 runs in the following HDBaseT operation modes:

- Low Power Partial Functionality (LPPF1)
- Active HDBaseT (ACTIVE)
- Long-Reach (LR)

During transitions between HDBaseT Operation Modes, there is no signal continuity on the chip interfaces.

5.2 Modes

5.2.1 Low Power Partial Functionality (LPPF1)

In Low Power Partial Functionality (LPPF1) mode, a low-power communication link is established between two HDBaseT devices.

5.2.2 Active HDBaseT (ACTIVE)

In Active HDBaseT (ACTIVE) mode, the HDBaseT port establishes a high throughput link with its link partner using downstream/upstream sub-links.

5.2.3 Long Reach (LR)

Long Reach (LR) mode enables operation over longer cable runs (up to 150m/492ft) through the reduction of the symbol rate over the HDBaseT link. Note that the far-end of the link can be any Valens device.

Table 12: System State per Selection Mode on Local and Remote Sides

		Mode Selected on Remote Side			
		LPPF1	LPPF2	Long Reach	HDBaseT
Mode Selected on Local Side (VS2010)	HDBaseT	LPPF1	LPPF1	Long Reach	HDBaseT
	Long Reach	LPPF1	LPPF1	Long Reach	Long Reach
	LPPF1	LPPF1	LPPF1	LPPF1	LPPF1

5.3 Events

The table below describes the events leading to Operating Mode changes.

Table 13: Operating Mode Events

Event Name	Description
Link Loss	Any event that causes a link loss
Operation Mode Change Request	As defined in the HDBaseT Specification
Wakeup	Event causing a transition from LPPF to ACTIVE – for future support
Standby	Event causing a transition from ACTIVE to LPPF – for future support

5.3.1 Auto-LPPF Functionality

Mode transitions between Active and Low-Power modes are possible through different mechanisms:

- Manual control using Host Interface parameters to specify the required operating mode. Mismatches between the requested operating modes of the link partners are resolved according to table 22 above.
- Automatic mode transitions based on certain events (“Auto-LPPF”)

Auto-LPPF allows for Colligo devices to enter and exit LPPF mode without the intervention of any external control element (such as an on-board controller). Trigger events can be defined, the presence - or absence - of which result in the mode transition. These triggers are as follows:

- HDMI video (TMDS clock)
- USB traffic

The triggers are configurable via boot-time (bring-up) parameters, which in turn defines the exact behavior of the Auto-LPPF mechanism. Auto-LPPF can interoperate with VS100/VS010 link partners, as well as with link partners operating in manual mode.

Refer to Valens Application Note AN2015 – Firmware Parameter Descriptions for information on the Auto-LPPF configuration settings.

6 Configuration and Management

Configuring the VS2010 chip can be achieved by the following methods:

- HW Strap Pins – Values are latched upon exiting reset
- Soft straps (GPIOs) – Asserting GPIO inputs during application bring-up
- Parameters – Configuring VS2010 parameter values in the external FLASH memory
- Host Interface – Configuring VS2010 parameters during run time or immediately after reset and before link establishment.

A VS2010 device is capable of managing its remote link partner using the host interface commands. Management messages are transferred over the main and auxiliary HDBaseT channels.

6.1 HW Strap Pins

Hardware strap pins are used to configure the chip's operational mode. These pins are sampled at the rise of the reset signal. After they are sampled, these pins regain their default run-time functionality.

Table 14: VS2010 RX/TX HW Strap Pin Description

STRAP Pin	Pin Name	Default (Internal PU/PD)	Strap Functionality
Strap[0]	ST0	PD	Strap bits 0-2 define the 3 LSB bits of the VS2010 configuration I2C slave device address. The 7 bit I2C address of VS2010 is set as follows: I2C address = {4'b0101, A2, A1, A0} Where A2, A1 and A0 are the values of ST2, ST1 and ST0 during reset respectively.
Strap[1]	ST1	PD	
Strap[2]	ST2	PD	
Strap[3]	ST3	PU	Strap bit #3. Must be connected to 1k pull down in all applications.
Strap[4]	ST4	PU	Defines the type of interface for the external FLASH device: '0' -SPI '1' - Reserved
Strap[5]	ST5	PD	Defines if the VS2010 boots from internal or external memory: '0' - Internal '1' - External
Strap[6]	DBG_TXD_ST6	PU	This strap bit, together with strap bit #7 and strap bit #10 define the external FLASH memory size as follows: [strap#10, strap#7, strap#6] = [110] - 2MB (16Mbits)

STRAP Pin	Pin Name	Default (Internal PU/PD)	Strap Functionality
			All other bit combinations are illegal.
Strap[7]	EE_MO_ST7	PD	This strap bit, together with strap bit #6 and strap bit #10 define the external FLASH memory size. See strap #6 above for a full description.
Strap[8]	EE_CS_ST8	PD	For Valens internal use only
Strap[9]	WAKEUP_OUT_ST9	None*	This strap bit selects one of two options for the page bit location (address bit 16) in an I2C FLASH memory '0' -Page/block bit is in Bit[16] of the I2C command '1'- Page/block bit is in Bit[18] of the I2C command If your memory device uses SPI interface, the value of this strap is ignored.
Strap [10]	ST10	None*	This strap bit, together with strap bit #6 and strap bit #7 define the external FLASH memory size. See strap #6 above for a full description.
Strap [11]	ST11	None*	For Valens internal use only

** IMPORTANT: The strap pins ST11, ST10 and WAKEUP_OUT_ST9 do not have internal default pullup/pulldown resistors. They must be tied to a weak pullup/pulldown resistor on the board.*

6.2 SW Strap Pins

The pins listed in Table 15 are used to configure the FW behavior. These pins may be left unconnected if the default internal pad resistor value is suitable for the application. You can assert these pins on your board (typically using dip-switch buttons or using external pullup/pulldown) to change the FW default configuration.

Table 15: SW Strap Pin Description

Pin Name	Soft Strap Functionality	Default (by internal pad pullup/down value)
GPIO[2]	Long reach (LR) mode request: '0' – Activate the link in HDBaseT mode '1' – Activate the link in long reach mode Must be deactivated using Update Parameters (LR function is currently enabled by default)	1
GPIO[3]	WaitForHost_n soft strap: '0' – The FW will pause its boot session, allowing a host to	1

	configure the VS2010 with HIF set/get commands. '1' – The FW loads the parameters from the external memory update parameter section and resumes boot as usual.	
GPIO[22]	EDID Source Selection soft strap: '0' – The EDID from the HDMI Sink is presented to the HDMI Source '1' – The static EDID defined in Host Interface parameter 0.1.5.9 is presented to the HDMI Source This soft strap is enabled by setting Host Interface parameter 0.1.5.10 to '1'	1

IMPORTANT

Additional soft strap pins are reserved for future purposes and do not have any attached functionality. To make sure your design is future compatible, soft strap pins must not be tied to external pullup or pulldown resistors.

6.3 GPIO Functionality

VS2010 GPIO pins are used by the firmware for various indication inputs and status outputs, known as GPIO functions. These GPIO functions are pre-assigned and detailed this section.

6.3.1 FW LED (pin GPIO[24]/MSIO_DO[4])

This GPIO function indicates FW operation status as follows:

- 1 (high – LED off): Indicates no FW operation.
- 0.5Hz blink (1 second on, 1 second off): Indicates that the Full firmware is loaded and running
- 2.5Hz blink (0.2 seconds on, 0.2 seconds off): Indicates that the Internal Boot firmware is running. This should only be used during first-time programming of an empty external Flash memory.
- 5Hz blink (0.1 seconds on, 0.1 seconds off): Indicates that the device is running from the Basic firmware bank. The Basic firmware does not provide full functionality, and running from the Basic bank usually indicates a failure in the system.

6.3.2 Link LED (pin GPIO[27]/MSIO_DI[1])

This GPIO function reports the link status as follows:

- 0 (low – LED on): HDBaseT Link.
- 6.25Hz blink (0.08 seconds on, 0.08 seconds off): Ethernet Fallback mode.
- 2.5Hz blink (0.2 seconds on, 0.2 seconds off): Low Power mode without Ethernet (LPPF1).
- 0.5Hz - blink (1 second on, 1 second off): Low Power mode with Ethernet (LPPF2).

- 1 (high – LED off): No link

6.3.3 HDMI LED (pin GPIO[28]/MSIO_DI[2])

This GPIO function reports the HDMI status as follows:

- 0 (low – LED on): HDMI/DVI video exists with HDCP encryption. **Not supported in VS2010.**
- 2.5Hz blink (0.2 seconds on, 0.2 seconds off): HDMI/DVI Content exists – without HDCP encryption
- 1 (high – LED off): No HDMI/DVI video.

6.3.4 CIR Type In (pin GPIO[21]/MSIO_DOUT[1])

This GPIO function is an input from the CIR circuit indicating the type of CIR message received and send over the HDBaseT link.

- 0 (low): indicates that the CIR T-Adaptor input signal (MSIO_DIN[3]/CIR_in/GPIO[7] pin) carries a modulated CIR signal.
- 1 (high): indicates that the CIR T-Adaptor input signal (MSIO_DIN[3]/CIR_in/GPIO[7] pin) carries a baseband CIR signal.

The polarity of this GPIO function may be inverted using the parameter system.CIR.CIRTypeInPolarity. When the polarity is set to 0 (system.CIR.CIRTypeInPolarity = 0), the encoding above applies. By default, system.CIR.CIRTypeInPolarity = 1 and the inverted encoding applies:

- 1 (High): indicates that the CIR T-Adaptor input signal (MSIO_DIN[3]/CIR_in/GPIO[7] pin) carries a modulated CIR signal.
- 0 (low): indicates that the CIR T-Adaptor input signal (MSIO_DIN[3]/CIR_in/GPIO[7] pin) carries a baseband CIR signal.

If your CIR circuit supports only one type of CIR message (modulated only or baseband only), you can leave this pin unconnected. The CIR message type attribute must be correctly defined using the TAInfo.CIRTx table of parameters.

For more information about CIR circuit implementation, refer to *Application Note AN2001*.

6.3.5 CIR Type Out (pin GPIO[17])

This GPIO function is an output from chip to the CIR circuit indicating the type of CIR message output over the MSIO_DO3/CIR_OUT pin.

- 0 (low): indicates that the CIR output signal carries a baseband CIR signal.
- 1 (high): indicates that the CIR output signal carries a modulated CIR signal.

The polarity of this GPIO function may be inverted using the parameter system.CIR.CIRTypeOutPolarity. When the default polarity is set

(system.CIR.CIRTypeInPolarity = 0), the encoding above applies. When system.CIR.CIRTypeInPolarity = 1, the inverted encoding applies:

- 1 (high): indicates that the CIR output signal carries a baseband CIR signal.
- 0 (low): indicates that the CIR output signal carries a modulated CIR signal.

If your CIR circuit applies only one CIR message type (modulated only or baseband only), you can leave this pin unconnected.

6.3.6 RX Detect Circuit (pin GPIO[31]/MSIO_D[5])

This function is used as input for the external RX detect circuit. The RX-detect circuit output feeds GPIO31 on the VS2xxxRX device. The function needs to be enabled in the firmware parameter configuration. The RX device firmware samples GPIO31, and digitally forwards it over HDBaseT to the VS2xxxTX device for regeneration on the source device interface. This method of transmission eliminates degradation of the analog signal over the CATx HDBaseT link.

6.4 MSIO Functionality

MSIO (Multi Serial Input Output) channels enable low-speed transfer of data over an HDBaseT link. They can be used to forward low-speed information (such as proprietary control signals) between source and sink devices. Up to 6 MSIO channels may be used simultaneously. Data is transferred asynchronously through oversampling of the input data – the sample rate is set by configuration to either 0.5MHz, 1.0MHz or 1.5MHz. It is recommended to use a sampling rate of 10:1, meaning that (for example) with a sample rate of 1.5MHz the maximum native data rate should not exceed 150Kb/s.

For additional information, refer to Valens application note AN2052 – MSIO Functionality.

6.4.1 MSIO Compatibility with VS100 PDIF

In the event of V2000 Series – VS100 Series interoperation, the following general-purpose pins are connected over the HDBaseT link.

- VS2000 Series: MSIO[5:0] – Multi-Serial Input Output
- VS100 Series: PDIF[5:0] – Programmable Data Interface

NOTE

Not all of the pin connections are interoperable, please see the below table for details.

Table 16: PDIF-MSIO Compatibiity

VS010/VS100	VS2000 Series	Interoperability
PDIF[0] **(UART function)**	MSIO[0]	MSIO_DIN[0]/UART_IN/GPIO[4] MSIO_DOUT[0]/UART_OUT/GPIO[10]
PDIF[1]	MSIO[1]	Interoperability not supported
PDIF[2]	MSIO[2]	Interoperability not supported
PDIF[3] **(CIR function)**	MSIO[3]	MSIO_DIN[3]/CIR_IN/GPIO[7] MSIO_DOUT[3]/CIR_OUT/GPIO[13]
PDIF[4]	MSIO[4]	MSIO_DIN[4]/I2S_BCLK_IN/GPIO[8] MSIO_DOUT[4]/I2S_BCLK_OUT/GPIO[14]
PDIF[5]	MSIO[5]	MSIO_DIN[5]/GPIO[9] MSIO_DOUT[5]/GPIO[15]

6.5 Debug Port

The UART-based Debug port is used to enable first-time flash memory programming. The port is *always* available – even if no firmware is programmed in flash memory.

The following pins serve as the UART interface to the Debug port

- DBG_RXD
- DBG_TXD_ST6

The UART interface operates at the TTL level. Therefore, an external TTL-to-RS232 level shifter is required in order to connect to a PC and download firmware into the device.

6.6 VS2010 Parameters

VS2010 parameters are used to configure and monitor the chip's functionality during runtime and bring up. Each parameter has a default value and a set of attributes defining the method of updating the parameter. Parameter attributes are explained below.

BU (Bring-up Parameter) Attribute

A parameter with a BU attribute attains its value once only during the boot session. There are two methods for setting BU parameters:

1. By pre-programming the external memory (FLASH) parameter section. This is done using the update parameter tool. The FW loads the parameter values from the external memory parameter section as part of the boot session.
2. By HIF (Host Interface) commands during WaitForHost_n soft strap. This option is described in detail in *Application Note AN2004 – Host Interface*.

All BU parameters may be read using GET HIF commands at any time.

RT (Run-time Parameter) Attribute

Parameters with RT attribute (on local or remote devices) may be accessed anytime during runtime using SET and GET HIF commands. These parameters may only be modified using HIF commands.

- RO – read only (can be accessed using HIF GET commands)
- RW – read write (can be accessed using HIF GET and SET commands)
- W – write only (can be accessed using HIF SET commands)

6.6.1 VS2010 Initialization Flow

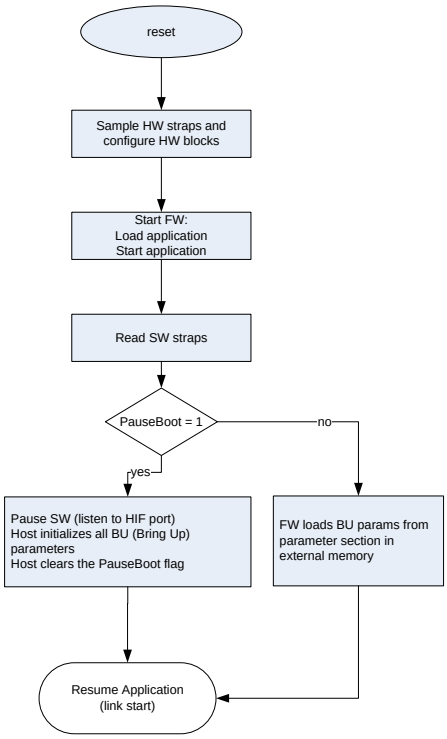


Figure 11: VS2010 Initialization Flow

6.6.2 Parameter List

For a complete guide to configuration of firmware parameters, refer to *Application Note AN2015 – Firmware Parameter Descriptions*.

6.7 Host Interface (HIF)

The Host Interface provides a channel for exchanging information between a VS2010 family chip and a host system used to control, configure, and monitor the chip.

For a complete description of the HIF and its operations, refer to the following Valens Application Notes:

- *AN2004 – Host Interface*
- *AN2015 – Firmware Parameter Descriptions*

6.8 JTAG Interface

The JTAG interface includes the signals: TEST_MODE_0; TEST_MODE; TCK; TDI; TDO; TMS; TRST.

The following signals are used to switch to the JTAG mode of operation:

Table 17: JTAG Mode

TEST_MODE_0	TEST_MODE_1	Chip Operation mode
0	0	Normal Mode
1	1	JTAG Mode

To enter JTAG mode follow these steps:

1. RESET the device.
2. Assert TEST_MODE_0 to ‘1’ and TEST_MODE_1 to ‘1’.
3. Release device from RESET.

To return to normal operation mode follow the steps:

1. RESET the device.
2. Assert TEST_MODE_0 to ‘0’ and TEST_MODE_1 to ‘0’.
3. Release device from RESET.

Note: for BSDL files please contact Valens customer support.

7 Electrical Specifications

This chapter contains electrical specifications for the Valens VS2010TX and VS2010RX chips.

NOTE

The ratings appearing in this section are preliminary and based on tests performed under lab conditions.

7.1 Absolute Maximum Rating

Table 18: VS2010TX Absolute Maximum Rating

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VI	Digital Inputs voltage		0		5.5	V
Tj	Junction Temperature range		-40		125	°C
TSTG	Storage Temperature range				150	°C
VDD	VDD		-0.2		1.1	V
VDDA10	AVDD10		-0.2		1.1	V
VDDA18	AVDD18		-0.2		1.98	V
VDDIO	VDD33V		-0.2		3.6	V
VDDA33	AVDD33		-0.2		3.6	V
VTERM33	AVDD33_TERM		-0.2		3.6	V

Table 19: VS2010RX Absolute Maximum Rating

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Vi	Digital Inputs voltage		0		5.5	V
Tj	Junction Temperature range		-40		125	°C
TSTG	Storage Temperature range				150	°C
VDD	VDD		-0.2		1.1	V
VDDA10	AVDD10		-0.2		1.1	V
VDDA18	AVDD18		-0.2		1.98	V
VDDIO	VDD33V		-0.2		3.6	V
VDDA33	AVDD33		-0.2		3.6	V

NOTE

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only - functional operation of the device under these or any other conditions above those indicated in the operational section of this datasheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 Power Supplies

7.2.1 Tx Power Supplies

Table 20: VS2010TX Power Supply

Symbol	Parameter	Min	Typ	Max	Unit
VDD	1.0V digital voltage	Typ-5%	1.0	Typ+5%	V
AVDD10	1.0V analog voltage	Typ-5%	1.0	Typ+5%	V
AVDD18	1.8V analog voltage	Typ-5%	1.8	Typ+5%	V
AVDD33	3.3V analog voltage	Typ-5%	3.3	Typ+5%	V
VDD33V	3.3V IO voltage	Typ-5%	3.3	Typ+5%	V
AVDD33_TERM	3.3V analog termination voltage	Typ-5%	3.3	Typ+5%	V
VSS	Ground		0		V

7.2.2 Rx Power Supplies

Table 21: VS2010RX Power Supply

Symbol	Parameter	Min	Typ	Max	Unit
VDD	1.0V digital voltage	Typ-5%	1.0	Typ+5%	V
AVDD10	1.0V analog voltage	Typ-5%	1.0	Typ+5%	V
AVDD18	1.8V analog voltage	Typ-5%	1.8	Typ+5%	V
AVDD33	3.3V analog voltage	Typ-5%	3.3	Typ+5%	V
VDD33V	3.3V IO voltage	Typ-5%	3.3	Typ+5%	V
VSS	Ground		0		V

7.3 Power Consumption Ratings

7.3.1 Tx Power Consumption

Table 22: Typical* VS2010TX Power Consumption Ratings

Symbol	Parameter	Conditions	Typ	Unit
IVDD33	3.3V Supply Current (AVDD33, AVDD33_TERM, VDD33V)	LPPF1	15	mA
IVDD18	1.8V Supply Current (AVDD18)		17	mA
IVDD10	1.0V Supply Current (AVDD10, VDD)		167	mA
PSUPP	**Total Power Consumption**		**248**	**mW**
IVDD33	3.3V Supply Current (AVDD33, AVDD33_TERM, VDD33V)	LPPF1 in Auto-LPPF Mode with USB Trigger	30	mA
IVDD18	1.8V Supply Current (AVDD18)		17	mA
IVDD10	1.0V Supply Current (AVDD10, VDD)		219	mA
PSUPP	**Total Power Consumption**		**349**	**mW**
IVDD33	3.3V Supply Current (AVDD33, AVDD33_TERM, VDD33V)	HDBaseT HDMI 4k2k/24bpp/30Hz	140	mA
IVDD18	1.8V Supply Current (AVDD18)		270	mA
IVDD10	1.0V Supply Current (AVDD10, VDD)		1116	mA
PSUPP	**Total Power Consumption**		**2064**	**mW**
IVDD33	3.3V Supply Current (AVDD33, AVDD33_TERM, VDD33V)	HDBaseT HDMI 4k2k/24bpp/30Hz USB	140	mA
IVDD18	1.8V Supply Current (AVDD18)		279	mA
IVDD10	1.0V Supply Current (AVDD10, VDD)		1248	mA
PSUPP	**Total Power Consumption**		**2213**	**mW**

** Maximum power consumption ratings are estimated as follows: <Typical>+20%*

7.3.2 Rx Power Consumption

Table 23: Typical* VS2010RX Power Consumption Ratings

Symbol	Parameter	Conditions	Typ	Unit
IVDD33	3.3V Supply Current (AVDD33, AVDD33_TERM, VDD33V)	LPPF1	10	mA
IVDD18	1.8V Supply Current (AVDD18)		30	mA
IVDD10	1.0V Supply Current (AVDD10, VDD)		223	mA
PSUPP	**Total Power Consumption**		**310**	**mW**
IVDD33	3.3V Supply Current (AVDD33, AVDD33_TERM, VDD33V)	LPPF1 in Auto-LPPF Mode with USB Trigger	19	mA
IVDD18	1.8V Supply Current (AVDD18)		30	mA
IVDD10	1.0V Supply Current (AVDD10, VDD)		278	mA
PSUPP	**Total Power Consumption**		**395**	**mW**
IVDD33	3.3V Supply Current (AVDD33, AVDD33_TERM, VDD33V)	HDBaseT HDMI 4k2k/24bpp/30Hz	68	mA
IVDD18	1.8V Supply Current (AVDD18)		398	mA
IVDD10	1.0V Supply Current (AVDD10, VDD)		2441	mA
PSUPP	**Total Power Consumption**		**3382**	**mW**
IVDD33	3.3V Supply Current (AVDD33, AVDD33_TERM, VDD33V)	HDBaseT HDMI 4k2k/24bpp/30Hz USB	77	mA
IVDD18	1.8V Supply Current (AVDD18)		407	mA
IVDD10	1.0V Supply Current (AVDD10, VDD)		2546	mA
PSUPP	**Total Power Consumption**		**3533**	**mW**

**Maximum power consumption ratings are estimated as follows: <Typical>+20%*

7.4 Reference Clock Requirements

7.4.1 CMOS Oscillator Requirements

NOTE

Implementation of the CMOS oscillator requires the use of an analog CMOS-to-LVDS conversion circuit. Refer to *Application Note 2001 – Hardware Design Guidelines* for further details.

The CMOS oscillator should comply with the following requirements:

- Frequency: 125 MHz
- Accuracy: ±100 ppm (±0.01%)
- Phase Noise must be kept below the phase noise mask specified in Table 24 below.

Table 24: CMOS Oscillator Phase Noise Mask

Frequency	Phase Noise (dBc/Hz)
1 Hz	-30
10 Hz	-60
100 Hz	-90
1 KHz	-127
10 KHz	-148
100 KHz	-150
10 GHz	-150

7.4.2 LVDS Oscillator Requirements

An LVDS oscillator may be used to generate a 125 MHz reference clock input. The LVDS oscillator should comply with the following requirements:

Table 25: LVDS Oscillator Requirements

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Note
F_{CLK}	Reference clock frequency			125		MHz	
F_{TOL}	Input clock frequency tolerance	includes aging, temperature change and supply voltage swing	-100		+100	PPM	
F_{DCD}	Reference clock duty cycle		40	50	60	%	
$T_{FALL/RISE}$	Rise / Fall Time	20% - 80% differential	260		2400	pSec	
V_I	Single-ended Input Voltage Range		0		1.89	V	
$\|V_{ID}\|$	Differential input voltage range		100		600	mV	Fig2
V_{CM}	Common-mode input range		600	1200	1800	mV	
R_{IN}	Input differential resistance		80		120	Ω	

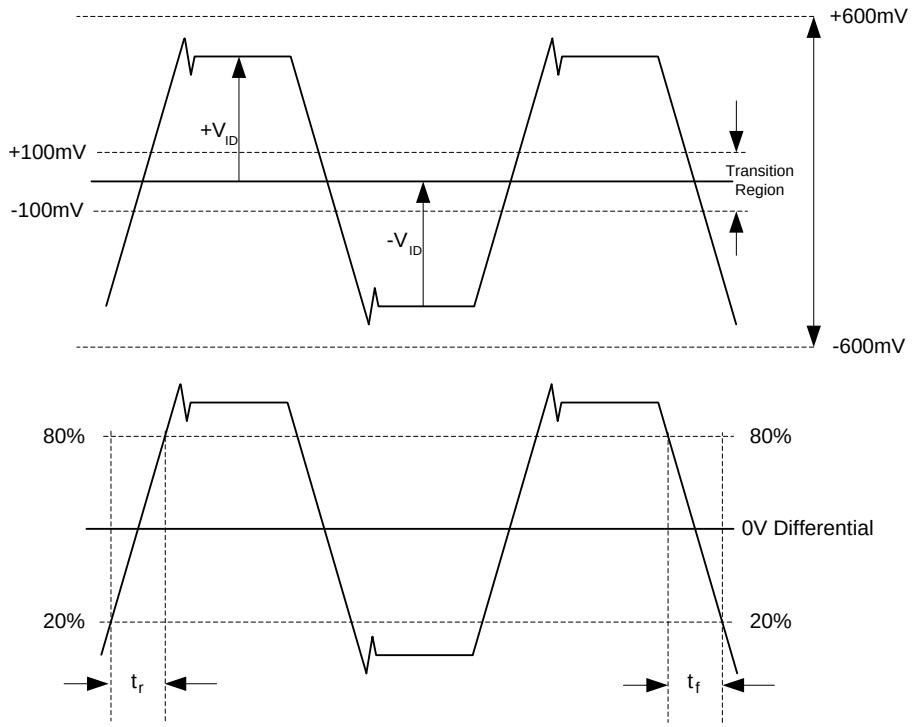


Figure 12: Input Reference Clock Wave Diagram

7.5 Recommended Operating Conditions

7.5.1 Electrical Characteristics (DC Specifications)

Table 26: VS2010TX Electrical Specification

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Digital pads						
VIH	Input voltage high	Digital pads	2.0		5.5	V
VIL	Input voltage low		-0.3		0.8	V
CIN	Input capacitance				2	pF
RPU	Pull-up resistor		65	93	141	KΩ
RPD	Pull-down resistor		60	90	163	KΩ
VOH	Output voltage High		2.4			V
VOL	Output voltage Low				0.4	V
TMDS Receivers DC specification						
VTH	Differential Input Threshold (+)				+75	mV
VTL	Differential Input Threshold (-)		-75			mV
|VID|	Differential Input Voltage (pk-pk)	Refer tp HDMI specification 1.4 for further details.	150		1560	mV
VICM1	Input common mode		-400		37.5	mV
VICM2	Input common mode		-10		10	mV
RIN(SE)	Single ended input impedance			50		Ω
SPI Interface DC Specification						
VOH	Output voltage High		2.4			V
VOL	Output voltage Low				0.4	V
IOH	Output current High		13.2	25.5	42.2	mA
IOL	Output current Low		10	15.7	21.1	mA

Table 27: VS2010RX Electrical Specification

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Digital pads						
VIH	Input voltage high	Digital pads	2.0		5.5	V
VIL	Input voltage low		-0.3		0.8	V
CIN	Input capacitance				2	pF
RPU	Pull-up resistor		65	93	141	KΩ

RPD	Pull-down resistor		60	90	163	KΩ
VOH	Output voltage High		2.4			V
VOL	Output voltage Low				0.4	V
TMDS Drivers DC specification						
VSWING	Single-ended output swing voltage	Compliance point TP1 as defined in Section 4.2.4 of HDMI Specification V1.4.	400		600	mV
VH	Single-ended high level output voltage	if attached Sink supports TMDSCLK<= 165Mhz	Typ - 5%	AVCC	Typ + 5%	V
		if attached Sink supports TMDSCLK > 165Mhz	Typ - 200mV	AVCC	Typ + 10mV	V
VL	Single-ended low level output voltage	if attached Sink supports TMDSCLK<= 165Mhz	Typ - 600mV	AVCC	Typ - 400mV	V
		if attached Sink supports TMDSCLK > 165Mhz	Typ - 700mV	AVCC	Typ - 400mV	V
RLOAD	50 ohm resistor loads Source Termination		45	50	55	Ω
SPI Interface DC Specification						
VOH	Output voltage High		2.4			V
VOL	Output voltage Low				0.4	V
IOH	Output current High		13.2	25.5	42.2	mA
IOL	Output current Low		10	15.7	21.1	mA

7.5.2 Timing (AC specifications)

Table 28: VS2010TX AC Specification

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Reference clock						
Frefclk_lvds	Reference clock frequency	LVDS levels on RCB_REFCLK_P/M pins		125		MHz
Frefclk_xtal	Reference clock frequency	XTAL		25		MHz
	Input clock frequency tolerance		-50		+50	PPM
	Reference clock duty cycle		40	50	60	%
Frefclk_usb	USB2_0 Reference clock frequency	XTAL		12		MHz
	USB2_0 reference clock frequency tolerance		-50		+50	PPM
FLASH (I2C)						
Same as the Host interface (I2C), see below						
FLASH SPI						
Supports all standard devices, maximum clock rate = 20 MHz						
Host Interface (I2C)						

		Standard Mode		Fast Mode		
		Min	Max	Min	Max	Units
fSCL	SCL clock frequency	0	100	0	400	KHz
tHD;STA	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0		0.6		us
tLOW	LOW period of the SCL clock	4.7		1.3		us
tHIGH	HIGH period of the SCL clock	4.0		0.6		us
tSU;STA	Set-up time for a repeated START condition	4.7		0.6		us
tHD;DAT	Data hold time	0	3.45	0	0.9	us
tSU;DAT	Data set-up time	250		100(1*)		ns
tr	Rise time of both SDA and SCL signals		1000	20+0.1Cb (2*)	300	ns
tf	Fall time of both SDA and SCL signals		300	20+0.1Cb (2*)	300	ns
tSU;STO	Set-up time for STOP condition	4.0		0.6		us

tBUF	Bus free time between a STOP and START condition	4.7		1.3		us
Cb	Capacitive load for each bus line		400		400	pF
(1*) A Fast-mode I2C-bus device can be used in a Standard-mode I2C -bus system, but the requirement tSU;DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr max + tSU;DAT = 1000 + 250 = 1250 ns (according to the Standard-mode I2C -bus specification) before the SCL line is released. (2*) Cb = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall-times are allowed.						
TMDS Receivers specification						
-	Maximum serial data rate				3.4	Gbps
FPCLK	TMDS Input clock frequency	On HDMIDES_TMDSCLKP/N	25		340	MHz
Intra-pair skew tolerance		FPCLK ≤ 225MHz			0.4	UI
		FPCLK > 225MHz			0.15UI + 112ps	mixed
Inter per skew					2UI + 1.78ns	mixed
	Input Clock Jitter Tolerance	Relative to Ideal Recovered Clock as defined in HDMI specification 1.4			0.30	UI

Table 29: VS2010RX AC specification

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
General						
Frefclk_lvds	Reference clock frequency	LVDS levels on RCB_REFCLK_P/M pins		125		MHz
Frefclk_xtal	Reference clock frequency	XTAL		25		MHz
	Input clock frequency tolerance		-50		+50	PPM
	Reference clock duty cycle		40	50	60	%

Frefclk_usb	USB2_0 Reference clock frequency	XTAL		12		MHz
	USB2_0 reference clock frequency tolerance		-50		+50	PPM

FLASH (I2C)
Same as the Host interface (I2C), see below
FLASH SPI
Support all standard devices, maximum clock rate = 20 MHz
Host interface (I2C)

		Standard Mode		Fast Mode		
		Min	Max	Min	Max	
fSCL	SCL clock frequency	0	100	0	400	KHz
tHD;STA	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0		0.6		us
tLOW	LOW period of the SCL clock	4.7		1.3		us
tHIGH	HIGH period of the SCL clock	4.0		0.6		us
tSU;STA	Set-up time for a repeated START condition	4.7		0.6		us
tHD;DAT	Data hold time	0	3.45	0	0.9	us
tSU;DAT	Data set-up time	250		100(1*)		ns
tr	Rise time of both SDA and SCL signals		1000	20+0.1Cb (2*)	300	ns
tf	Fall time of both SDA and SCL signals		300	20+0.1Cb (2*)	300	ns
tSU;STO	Set-up time for STOP condition	4.0		0.6		us
tBUF	Bus free time between a STOP and START condition	4.7		1.3		us
Cb	Capacitive load for each bus line		400		400	pF

(1*) A Fast-mode I2C-bus device can be used in a Standard-mode I2C -bus system, but the requirement tSU;DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr max + tSU;DAT = 1000 + 250 = 1250 ns (according to the Standard-mode I2C -bus specification) before the SCL line is released.

(2*) Cb = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall-times are allowed.

TMDS Drivers specification						
-	Maximum serial data rate				3.4	Gbps
FTMDSCLK	TMDS output clock frequency	On HDMISER_TMDSCLKP/N outputs	25		340	MHz

PTMDSCLK	TMDSCLK period	RL=50Ω ±10%	2.94		40	ns
tCDC	TMDSCLK duty cycle	tCDC = tCPH / PTMDSCLK RL=50Ω ±10%	40	50	60	%
tCPH	TMDSCLK high time	RL=50Ω ±10%	4	5	6	UI
tCPL	TMDSCLK low time	RL=50Ω ±10%	4	5	6	UI
	TMDSCLK jitter 1	RL=50Ω ±10%			0.25	UI
tSK(P)	Intra-Pair (Pulse) skew. (between a pair lanes)	RL=50Ω ±10%			0.15	UI
tSK(PP)	Inter-Pair (Pulse) skew (between different pairs).	RL=50Ω ±10%			2	UI
tr	Differential output signal rise time	20% to 80%, RL = 50±10%	75			ps
tf	Differential output signal fall time	20% to 80%, RL = 50±10%	75			ps

7.5.3 Clock Oscillator Requirements

Table 30 provides the clocking requirement specification for *XO25MHZ_XIN* clock input of the VS2010 chip. **NOTE THAT 25MHz CRYSTAL IS FOR FUTURE USE ONLY**

Table 30: VS2010 RX/TX Oscillator Requirements

Parameter	System Crystal Value	USB Crystal Value
Nominal Frequency	25MHz	12MHz
Frequency Tolerance @ 25oC	±50 PPM	±50 PPM
Frequency Stability, ref @ 25oC over operating temp. range	±50 PPM	±50 PPM
Load Capacitance (CL)	18.0pF	15.0pF
Drive Level	0.5 mW	0.5 mW
Aging per year	±5 PPM / year Max.	±5 PPM / year Max.
Max. ESR	30 ohm	60 ohm

7.5.3.1 Power on Reset Signal Timing

Option 1 : Using Internal POR (POR_BYPASS = 1'b0. Pin RESET_N is the system reset)

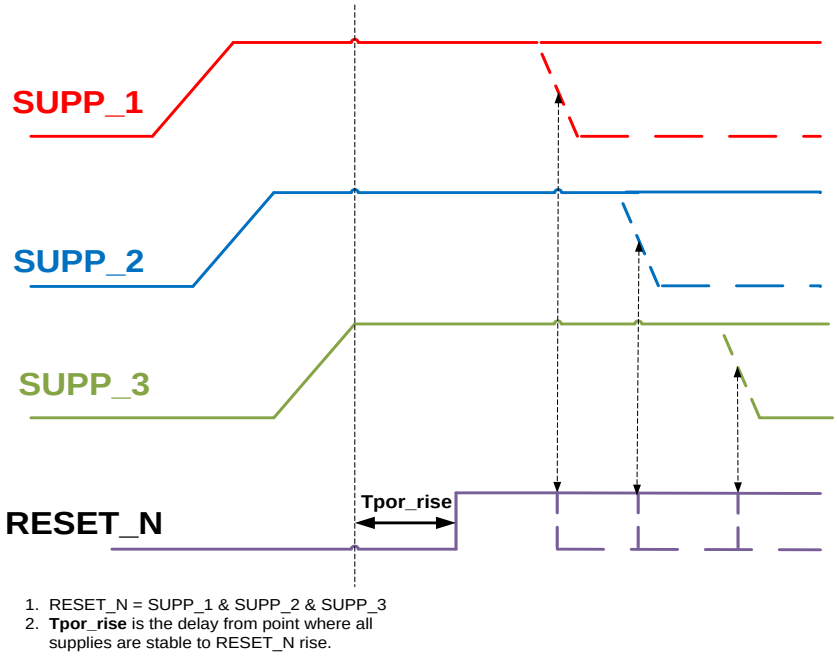


Figure 13: Internal Power on Reset Timing

Table 31: Internal Power on Reset Timing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
25MHz XTAL – **FOR FUTURE USE ONLY**						
Tpor_rise	Reset pulse width on RESET_N				170	mS
125MHz reference						
Tpor_rise	Reset pulse width on RESET_N				135	mS

NOTE

For the internal POR system to be valid, the following supplies should ramp up together as a group (generated from same regulator):
* VDD and AVDD10
* VDD33V and AVDD33

Option 2: Using External POR (POR_BYPASS = 1'b1. Pin RESET_IN is the system reset)

The RESET_IN signal must be held active at least 1ms after all chip supply voltages (VDD, VDD33V, AVDD10, AVDD18 and AVDD33).

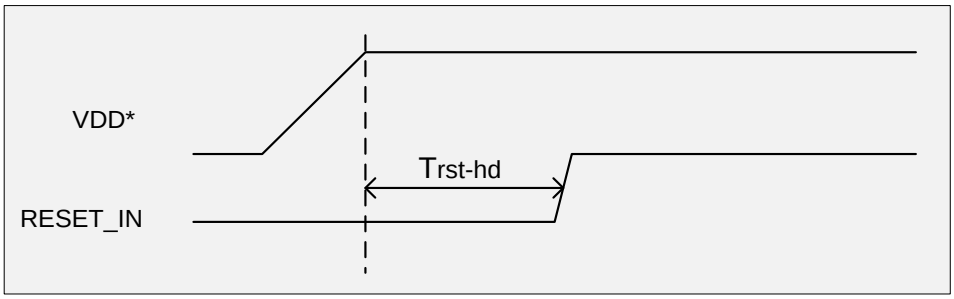


Figure 14: Reset Signal Timing

Table 32: External Power on Reset Timing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Trst_hd	Reset pulse width on RESET_IN after all 3 supplies are stable		1		80	mS

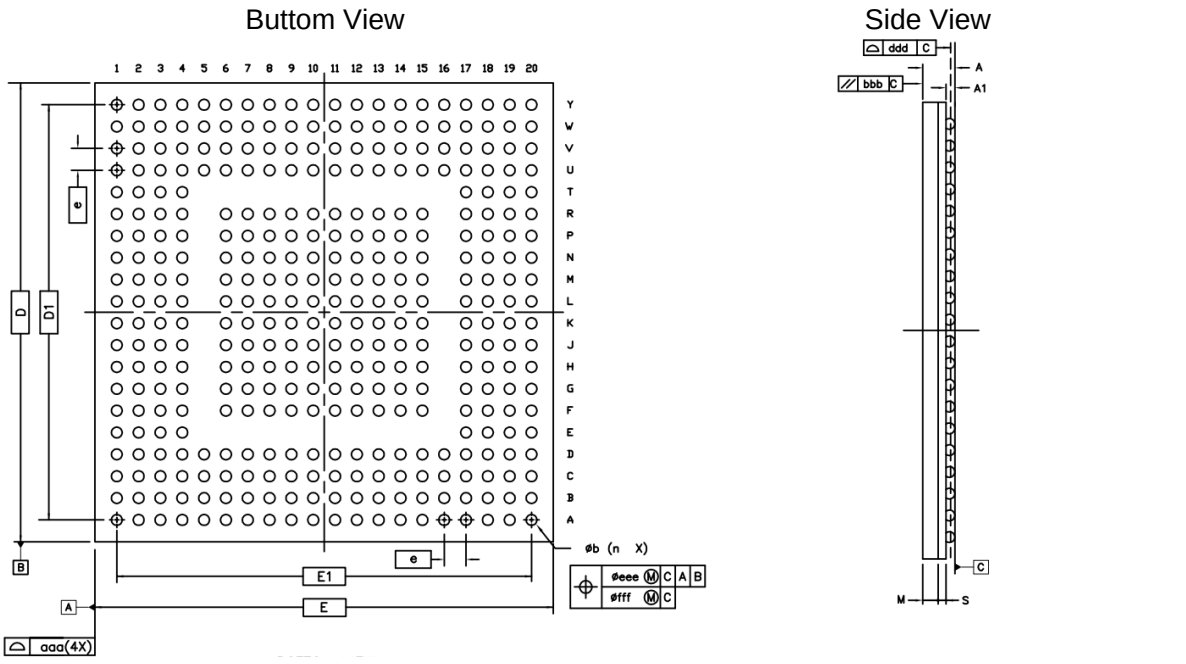
7.6 ESD Ratings

Table 33: ESD Ratings

Test	Value	Unit
HBM (per JEDEC JS-001)	± 2000	V
CDM (per JEDEC JESD22-C101)	± 500	
Latch Up (per JEDEC JESD78)	± 100	mA
	Over-voltage: 1.5x supply at 85°C	

8 Package Mechanical Data

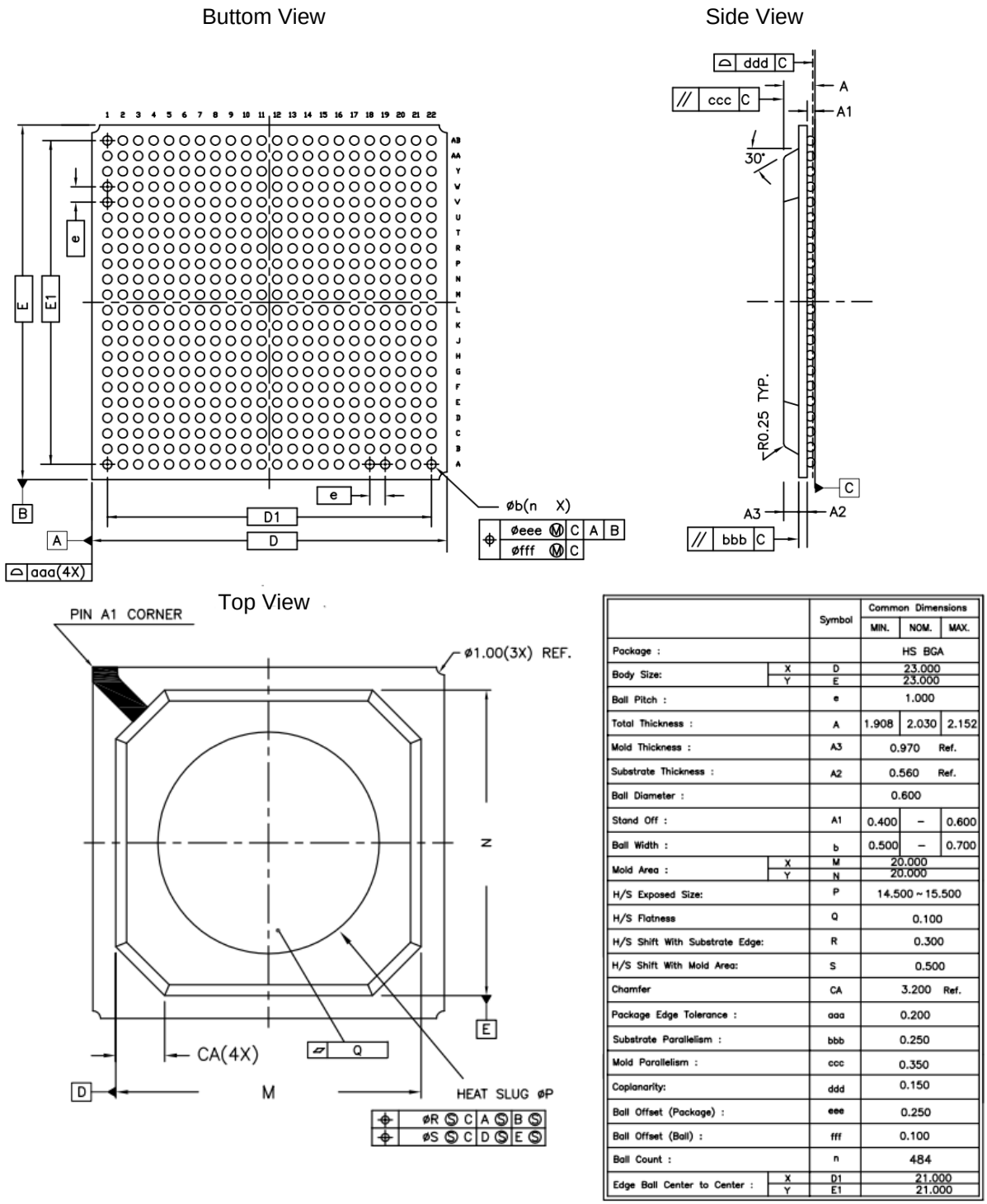
8.1 VS2010TX Package Mechanical Data



		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package :			LBGA		
Body Size:	X	E	21.000		
	Y	D	21.000		
Ball Pitch :		e	1.000		
Total Thickness :		A			1.700
Mold Thickness :		M	0.700		Ref.
Substrate Thickness :		S	0.360		Ref.
Ball Diameter :			0.500		
Stand Off :		A1	0.360	–	0.460
Ball Width :		b	0.440	–	0.640
Package Edge Tolerance :		aaa	0.200		
Mold Parallelism :		bbb	0.250		
Coplanarity:		ddd	0.200		
Ball Offset (Package) :		eee	0.250		
Ball Offset (Ball) :		fff	0.100		
Ball Count :		n	356		
Edge Ball Center to Center :	X	E1	19.000		
	Y	D1	19.000		

Figure 15: VS2010TX Mechanical Information (all dimensions in mm)

8.2 VS2010RX Package Mechanical Data



		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package :				HS BGA	
Body Size:	X	D		23.000	
	Y	E		23.000	
Ball Pitch :		e		1.000	
Total Thickness :		A	1.908	2.030	2.152
Mold Thickness :		A3		0.970 Ref.	
Substrate Thickness :		A2		0.560 Ref.	
Ball Diameter :				0.600	
Stand Off :		A1	0.400	–	0.600
Ball Width :		b	0.500	–	0.700
Mold Area :	X	M		20.000	
	Y	N		20.000	
H/S Exposed Size:		P		14.500 ~ 15.500	
H/S Flatness		Q		0.100	
H/S Shift With Substrate Edge:		R		0.300	
H/S Shift With Mold Area:		S		0.500	
Chamfer		CA		3.200 Ref.	
Package Edge Tolerance :		aaa		0.200	
Substrate Parallelism :		bbb		0.250	
Mold Parallelism :		ccc		0.350	
Coplanarity:		ddd		0.150	
Ball Offset (Package) :		eee		0.250	
Ball Offset (Ball) :		fff		0.100	
Ball Count :		n		484	
Edge Ball Center to Center :	X	D1		21.000	
	Y	E1		21.000	

Figure 16: VS2010RX Mechanical Information (all dimensions in mm)

NOTE

The integrated Heat Slug in the RX device is connected to package GND (digital GND). To prevent possible shorting between the package GND and the chassis GND when using a heatsink, it is recommended to add an isolation sticker between the heatsink and the chassis cover.

8.3 VS2010 Marking Information

For the VS2010 TX and RX markings depicted below, the following information applies:

Table 34: VS2010 Marking Schema

Marking Schema	
a	Pin A1 corner
b	Valens logo
c	Valens part number
d	Valens Lot #
Valens Lot # Schema	
First Line	Fab lot # XXXXXX.ZZ
Second Line	YYWW (assembly year and week number) ABC (Valens production lot)

8.3.1 VS2010TX Marking Information

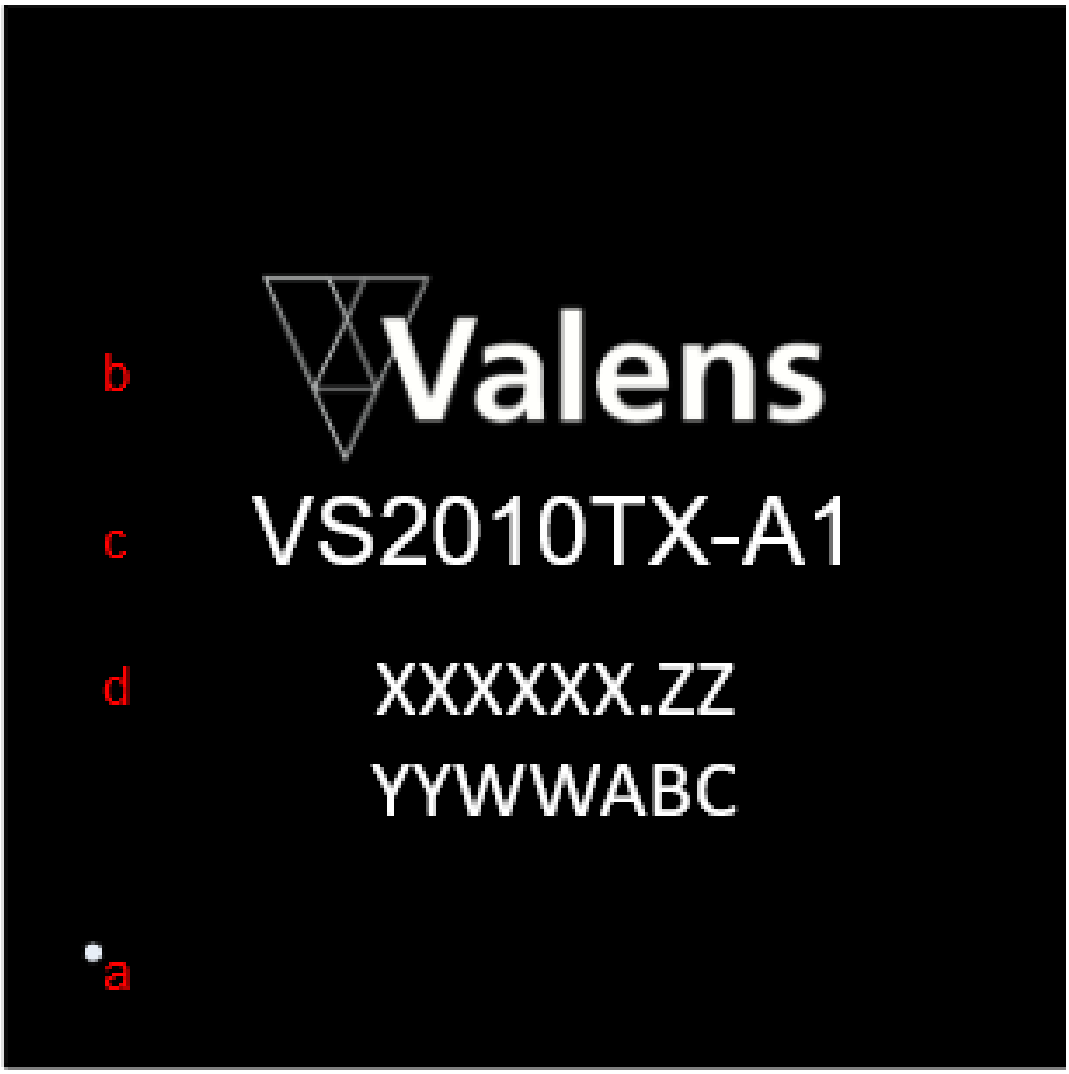


Figure 17: VS2010TX Marking

8.3.2 VS2010RX Marking Information

Figure 18: VS2010RX Marking

8.4 Ordering Codes

Table 35: Ordering Codes

Ordering Code	Item Description
VS2010TX-A1	Valens HDBaseT 2010 Transmitter
VS2010RX-A1	Valens HDBaseT 2010 Receiver

9 Thermal Parameters

9.1 Terminology

- θ_{JA} - Junction-to-ambient thermal resistance (EIA/JESD51-2 and EIA/JESD51-6):

  $\theta_{JA} = (T_J - T_A) / P_H$
  where T_J = junction temperature
  T_A = ambient temperature
  P_H = power dissipation

  θ_{JA} represents the resistance to the heat flows from the chip to ambient air. It is an indicator of package heat dissipation capability. Lower θ_{JA} means better overall thermal performance.

- Ψ_{JT} - Junction-to-top-center thermal characterization parameter (EIA/JESD51-2 and EIA/JESD51-6):

  $\Psi_{JT} = (T_J - T_T) / P_H$
  where T_T = temperature at the top-center of the package

  Ψ_{JT} is used for estimating the junction temperature by measuring T_T in an actual environment.

- Ψ_{JB} - Junction-to-board thermal characterization parameter (EIA/JESD51-2 and EIA/JESD51-6):

  $\Psi_{JB} = (T_J - T_B) / P_H$
  where T_B = board temperature

  Ψ_{JB} is a useful indicator of the thermal resistance between the junction and PCB if the package is not attached with an external heat sink.

- θ_{JB} - Junction-to-board thermal resistance (EIA/JESD51-8):

  $\theta_{JB} = (T_J - T_B) / P_H$
  where T_B = board temperature with ring cold plate fixture applied

  θ_{JB} represents the resistance to the heat flows from the chip to PCB. θ_{JB} is used in compact thermal models for system-level thermal simulation.

- θ_{JC} - Junction-to-case thermal resistance:

  $\theta_{JC} = (T_J - T_C) / P_H$
  where T_C = case temperature attached with a cold plate

  θ_{JC} represents the resistance to the heat flows from the chip to package top case. θ_{JC} is important when external heat sink is attached on package top.

9.2 TX Devices

Table 36: TX Thermal Data

Ambient Temperature	VAIR (m/s)	θJA (°C/W)	ΨJT (°C/W)	ΨJB (°C/W)	TJ (°C)	TT (°C)	θJC (°C/W)	θJB (°C/W)
70°C	0	16.37	0.13	8.33	119.10	118.72	3.01	8.47
	1	14.31	0.31	8.22	112.93	112.01		
	2	13.53	0.39	8.14	110.60	109.43		
85°C	0	16.01	0.13	8.33	133.03	132.63		
	1	14.16	0.30	8.22	127.48	126.57		
	2	13.41	0.39	8.14	125.22	124.07		

Table 37: TX PCB Constructions

Contstruction	Dimensions
PCB Layers	4-layer
PCB dimensions	101.5 x 114.3 x 1.6 mm
Core thickness	0.60 mm
Prepreg thickness	0.375 mm
Trace thickness	0.07 mm
Inner plane thickness	0.035 mm
Solder mask thickness	0.02 mm
Diameter of PCB vias	0.20 mm
Number of PCB via	64
Top / bottom copper coverage (%)	20
Inner copper coverage (%)	90

9.3 RX Devices

Table 38: RX Thermal Data

Ambient Temperature	V_{AIR} (m/s)	θ_{JA} (°C/W)	Ψ_{JT} (°C/W)	Ψ_{JB} (°C/W)	T_J (°C)	T_T (°C)	θ_{JC} (°C/W)	θ_{JB} (°C/W)
70°C	0	12.96	1.75	5.10	133.45	124.67	3.00	5.18
	1	10.78	1.80	5.00	123.88	114.90		
	2	10.02	1.82	4.94	120.08	110.99		
85°C	0	12.39	1.76	5.10	146.94	138.12		
	1	10.65	1.81	5.01	138.24	129.22		
	2	9.94	1.83	4.94	134.69	125.55		

Table 39: RX PCB Constructions

Contstruction	Dimensions
PCB Layers	4-layer
PCB dimensions	101.5 x 114.3 x 1.6 mm
Core thickness	0.60 mm
Prepreg thickness	0.375 mm
Trace thickness	0.07 mm
Inner plane thickness	0.035 mm
Solder mask thickness	0.02 mm
Diameter of PCB vias	0.20 mm
Number of PCB via	100
Top / bottom copper coverage (%)	20
Inner copper coverage (%)	90

10 Quality and Environmental Policy

Valens is committed to delivering the highest quality cutting-edge products to our customers, on time, every time.

Valens' management and employees are fully engaged in a culture of continuous improvement, and constructive partnerships with suppliers, customers and stakeholders.

Valens consistently monitors and strives to minimize the environmental impact of our activities, by implementing sustainable business practices across our operations, infrastructure and products.

We are committed to meeting or exceeding our customers' highest level of expectations, complying with all applicable environmental, health and safety requirements, and acting in accordance with the relevant laws and regulations.

ISO 9001:2008

ISO 14001:2004

RoHS – Restriction of Hazardous Substances

REACH SVHC – Substances of Very High Concern

Conflict Minerals Sourcing Policy

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