

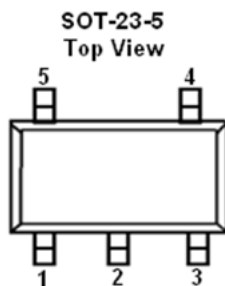


CJ9221

■ INTRODUCTION:

The CJ9221 is a high efficiency, DC to DC step down switching regulator, capable of delivering up to 2A of output current. The input and output range of CJ9221 is from 2.7V to 5.5V and 0.6V to V_{IN} , making it suitable for low voltage power conversion. Running at a fixed frequency of 1.5MHz allows the use of small inductance value and low DCR inductors, thereby achieving higher efficiencies. Other external components, such as ceramic input and output caps, can also be small due to higher switching frequency, while maintaining exceptional low noise output voltages. Internal soft start control circuit reduces inrush current.

■ PIN CONFIGURATION:



■ FEATURES:

- Wide Input Voltage Range: 2.7 ~ 5.5V
- up to 2A max Output Current
- Light Load Operation
- 1.5MHz Frequency
- 100% Duty Operation
- Internal Compensation
- SOT-23-5L Package

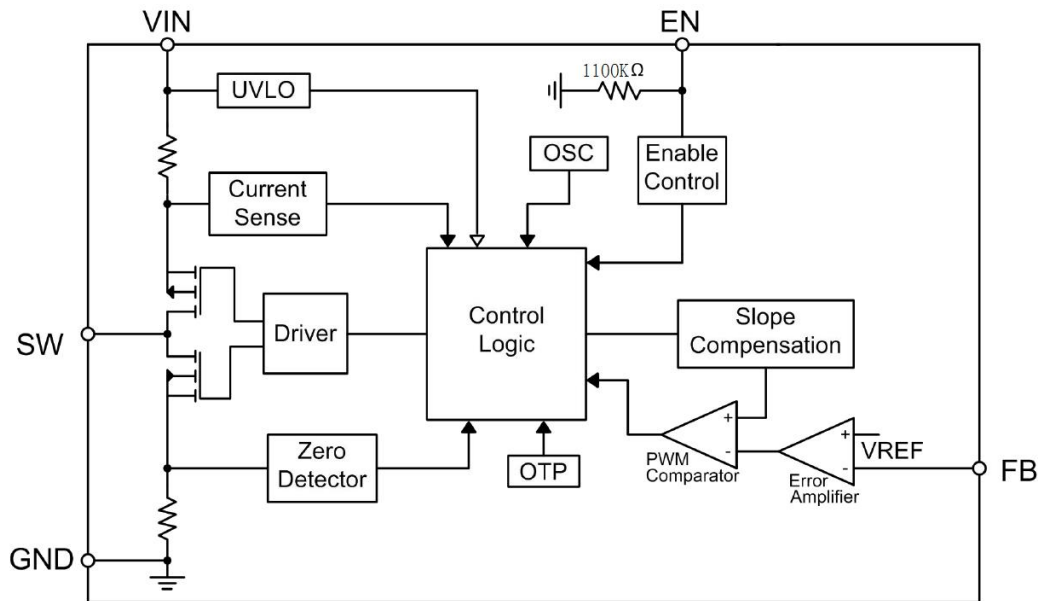
■ APPLICATION:

- USB ports / Hubs
- Portable Devices
- Cellphones
- Tablet PC
- Set Top Boxes

■ DEVICE INFORMATION:

PART NUMBER	PACKAGE
CJ9221T5	SOT-23-5L

■ BLOCK DIAGRAM



■ PIN CONFIGURATION

PIN NUMBER	PIN NAME	FUNCTION
1	EN	Enable pin for the IC. Drive this pin to high to enable the part, low to disable.
2	GND	Analog Ground pin
3	SW	Inductor Connection. Connect an inductor Between SW and the regulator output.
4	V _{IN}	Supply Voltage pin. Bypass with a 10μF ceramic capacitor to GND
5	FB	Feedback Input. Connect external resistors divider from the output to FB and GND to set the output to a voltage between 0.6V and VIN

Electrical Characteristics

■ ABSOLUTE MAXIMUM RATINGS⁽¹⁾ (Unless otherwise specified, $T_A = 25^\circ\text{C}$)

PARAMETER	SYMBOL	RATINGS	UNITS
Input Voltage ⁽²⁾	V_{IN}	-0.3~ 6.5	V
SW(DC) FB Voltage ⁽²⁾		$V_{SS}-0.3 \sim V_{IN}$	V
SW(AC, less than 10ns) Voltage ⁽²⁾		$V_{SS}-0.3 \sim$ $V_{OUT}+6.5$	V
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$	250	$^\circ\text{C/W}$
Power Dissipation SOT23-5L	P_D	400	mW
Operating Junction Temperature Range	T_J	-40~+150	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-55~+150	$^\circ\text{C}$
Lead Temperature (Soldering, 10 sec)	T_{solder}	260	$^\circ\text{C}$
ESD rating ⁽³⁾	Human Body Model (HBM)	2000	V
	Machine Model (MM)	200	V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to network ground terminal.

(3) ESD testing is performed according to the respective JEDEC standard. The human body model is a 100pF capacitor discharged through a 1.5k Ω resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN.	NOM.	MAX.	UNITS
Supply voltage at V_{IN}	-0.3	-	5.5	V
Output voltage at V_{OUT}	-0.3	-	5.5	V
Operating free air temperature range, T_A	-40	-	85	$^\circ\text{C}$

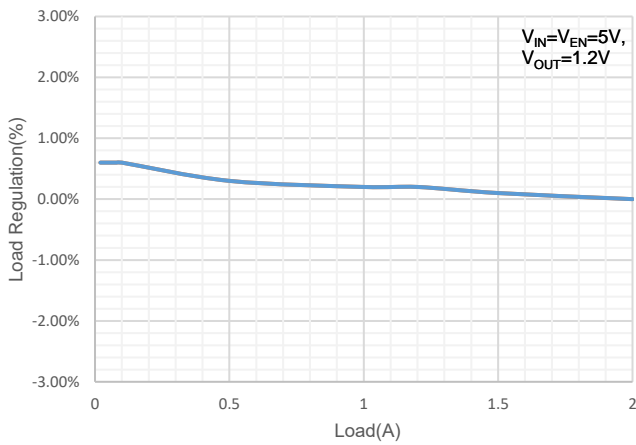
■ ELECTRICAL CHARACTERISTICS

CJ9221 ($V_{IN} = 5V$, $T_A = 25^{\circ}C$, unless otherwise specified)

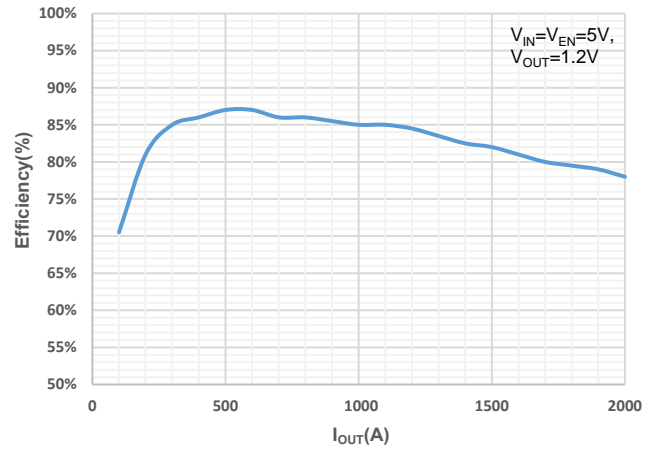
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Range		2.7		5.5	V
Shutdown Supply Current	$V_{EN}=0V$		0.1	1	μA
Quiescent Current	$V_{FB}=0.7V$		40		μA
Feedbackk Voltage	$V_{IN}=2.7$ to $5.5V$	0.588	0.600	0.612	V
Feedbackk Current			0.01		μA
UVLO Hysteresis			0.15		V
UVLO Threshold			2.5		V
EN in Pull-Low Resistance			1100		$k\Omega$
EN in Input Low Voltage				0.4	V
EN in Input High Voltage		1.5			V
NMOS Switch On Resistance			110		$m\Omega$
PMOS Switch On Resistance			90		$m\Omega$
NMOS Current LLimit			4		A
Output Discharge Switch On Resistance	$V_{EN}=0V$		60		Ω
NMOS Leakage Current	$V_{IN}=5V$, $V_{FB}=0.7V$			10	μA
Maximum Duty		100			%
Internal Soft-Start Time			1		ms
Switching Frequency			1.5		MHz
Short Switching Frequency			380		kHz
Thermal Shutdown Temperature			160		$^{\circ}C$

Typical Characteristics

CJ9221 ($V_{IN} = 5V$, $V_{OUT} = 1.2V$, $L = 2.2\mu H$, $T_A = 25^\circ C$, unless otherwise specified)



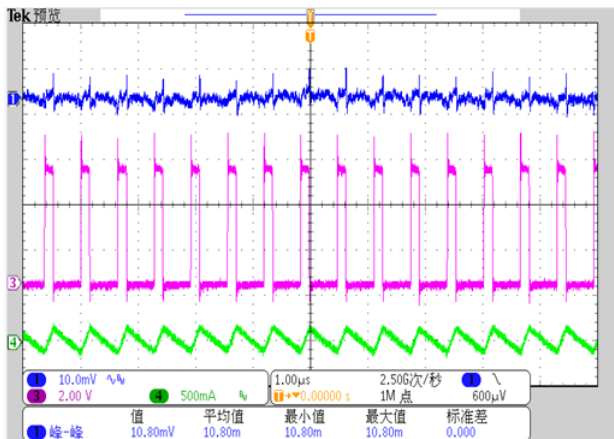
$V_{IN} = 5V$, $V_{OUT} = 1.2V$
Fig. 1 Load Regulation



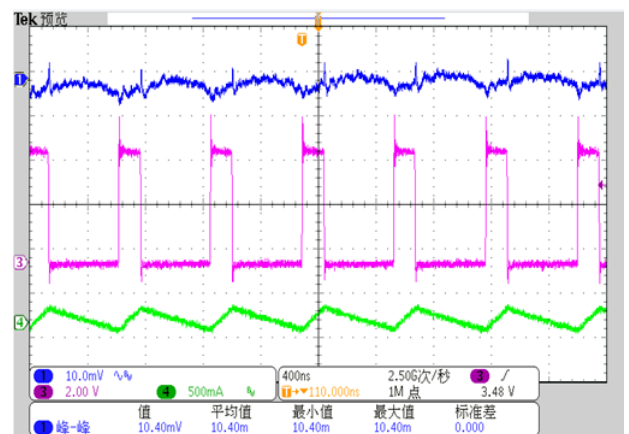
$V_{IN} = 5V$, $V_{OUT} = 1.2V$
Fig. 2 Efficiency

Steady State Waveform

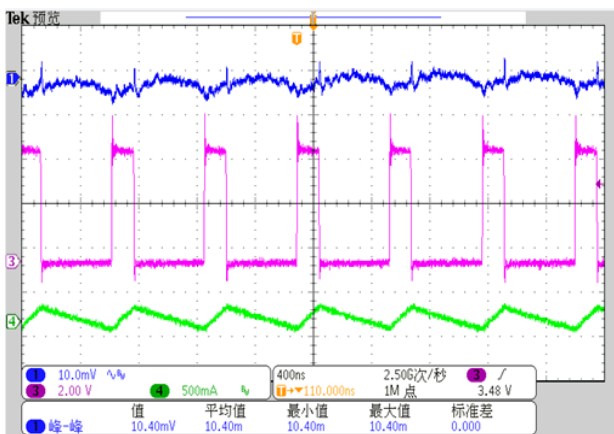
CH1: V_{SW} CH2: V_{OUT} CH4: I_{LOAD}



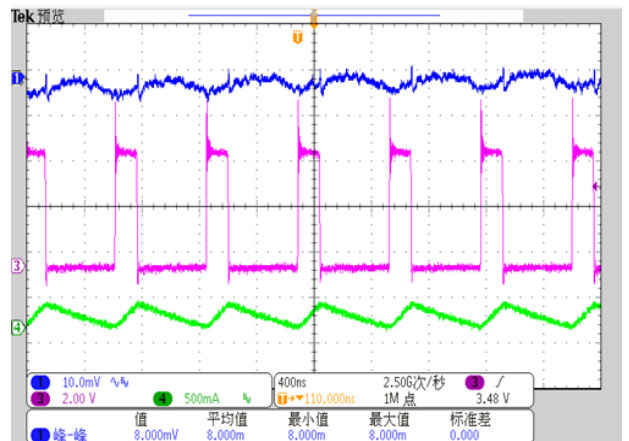
$V_{IN} = 5V$, $V_{OUT} = 1.2V$, $I_{LOAD} = 0A$
Fig. 3 Steady State Waveform



$V_{IN} = 5V$, $V_{OUT} = 1.2V$, $I_{LOAD} = 0.01A$
Fig. 4 Steady State Waveform

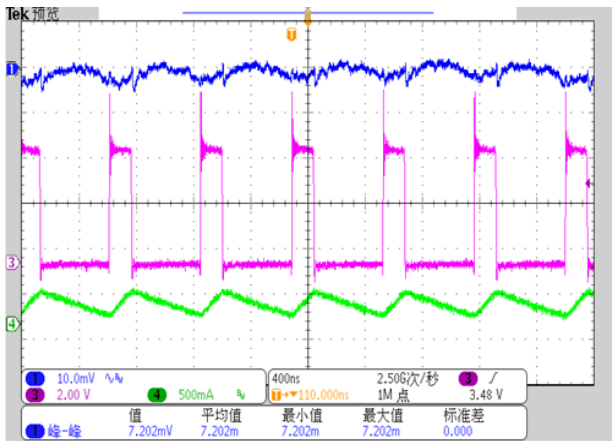


$V_{IN} = 5V$, $V_{OUT} = 1.2V$, $I_{LOAD} = 0.05A$
Fig. 5 Steady State Waveform

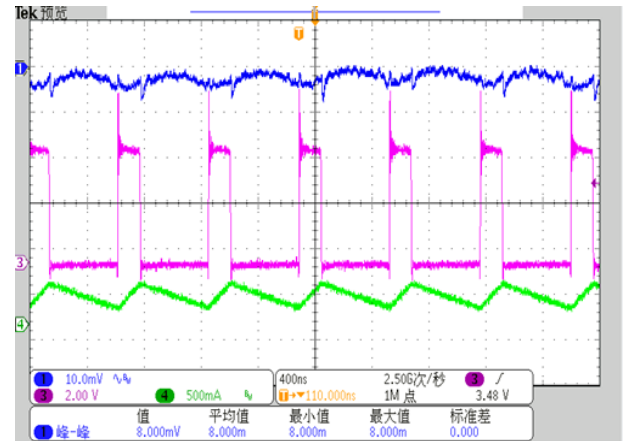


$V_{IN} = 5V$, $V_{OUT} = 1.2V$, $I_{LOAD} = 0.1A$
Fig. 6 Steady State Waveform

Typical Characteristics



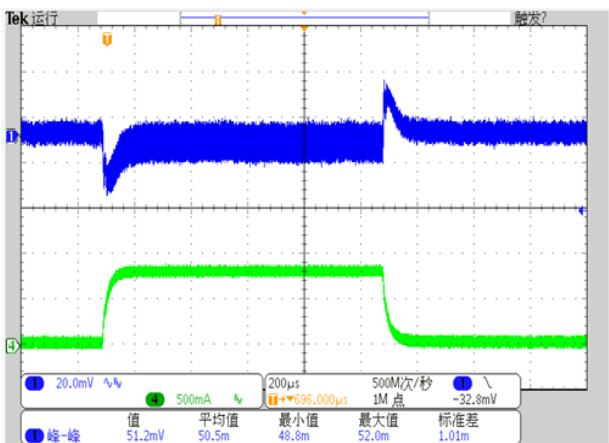
$V_{IN} = 5V, V_{OUT} = 1.2V, I_{LOAD} = 0.2A$
Fig. 7 Steady State Waveform



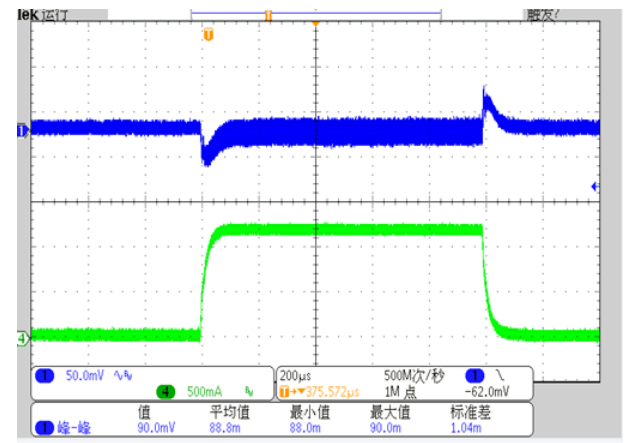
$V_{IN} = 5V, V_{OUT} = 1.2V, I_{LOAD} = 0.3A$
Fig. 8 Steady State Waveform

Transient Waveform

CH1:V_{OUT} CH4:I_{LOAD}



$V_{IN} = 5V, V_{OUT} = 1.2V, I_{LOAD} = 0.01A \text{ to } 0.8A$
Fig. 9 Transient Waveform



$V_{IN} = 5V, V_{OUT} = 1.2V, I_{LOAD} = 0.01A \text{ to } 1.2A$
Fig. 10 Transient Waveform

■ FUNCTION DESCRIPTION

● General Description

CJ9221 high efficiency switching regulator is a small, simple, DC-to-DC step-down converter capable of delivering up to 1A of output current. The device operates in pulse-width modulation (PWM) at 1.5MHz from 2.7V to 5.5V input voltage and provides an output voltage from 0.6V to V_{IN} , making the IC ideal for on-board post-regulation applications. An internal synchronous rectifier improves efficiency and eliminates the typical Schottky free-wheeling diode. Using the on resistance of the internal high-side MOSFET to sense switching currents eliminates current-sense resistors, further improving efficiency and reducing cost.

● Loop Operation

The IC uses a PWM current-mode control scheme. An open-loop comparator compares the integrated voltage-feedback signal against the sum of the amplified current-sense signal and the slope compensation ramp. At each rising edge of the internal clock, the internal high-side MOSFET turns on until the PWM comparator terminates the on cycle. During this on-time, current ramps up through the inductor, sourcing current to the output and storing energy in the inductor. The current mode feedback system regulates the peak inductor current as a function of the output voltage error signal. During the off cycle, the internal high-side P-channel MOSFET turns off, and the internal low-side N-channel MOSFET turns on. The inductor releases the stored energy as its current ramps down.

● Current Sense

An internal current-sense amplifier senses the current through the high-side MOSFET during on time and produces a proportional current signal which is used to sum the slope compensation signal. The summed signal then is compared with the error amplifier output by the PWM comparator to terminate the on cycle.

● Current Limit

There is a cycle-by-cycle current limit on the high-side MOSFET. When the current flowing out of SW exceeds this limit, the high-side MOSFET turns off and the synchronous rectifier turns on. The IC utilizes a frequency fold-back mode to prevent overheating during short-circuit output conditions. The device enters frequency fold-back mode when the FB voltage drops below 250mV, limiting the current to IPEAK and reducing power dissipation. Normal operation resumes upon removal of the short-circuit condition.

● Soft-Start

The IC has an internal soft-start circuit to reduce supply inrush current during startup conditions. When the device exits under-voltage lockout (UVLO), shutdown mode, or restarts following a thermal-overload event, the soft-start circuit slowly ramps up the output voltage.

● UVLO and Thermal Shutdown

If V_{IN} drops below 2.5V, the UVLO circuit inhibits switching. Once V_{IN} rises above 2.7V, the UVLO clears, and the soft-start sequence activates. Thermal-overload protection limits total power dissipation in the device. When the junction temperature exceeds $T_J = +160^{\circ}\text{C}$, a thermal sensor forces the device to shutdown, allowing the die to cool down. The thermal sensor turns the device on again after the junction temperature falls below 60°C . After a thermal-shutdown condition, the soft-start sequence begins.

■ APPLICATION INFORMATION

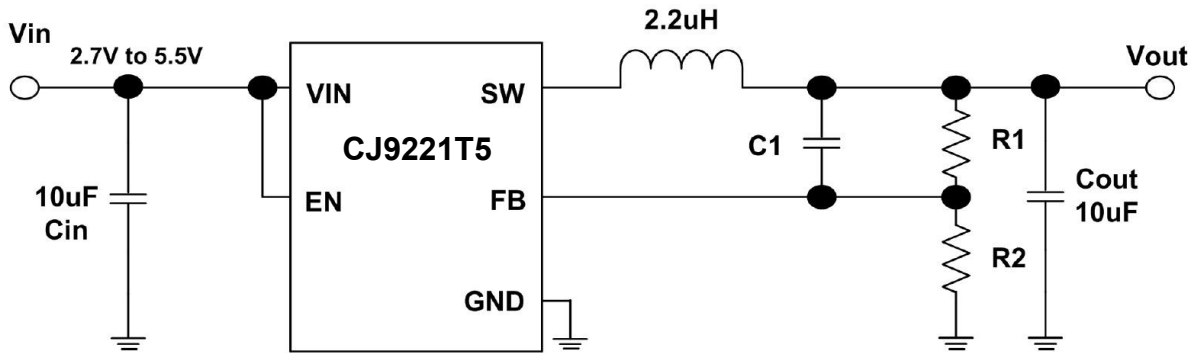
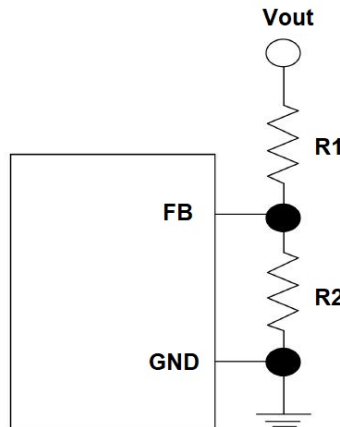


Figure1 Basic Application Circuit

Note: $V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right)$

• Setting Output Voltages

The resistive voltage divider allows the FB pin to sense a fraction of the output voltage shown as below.



For adjustable voltage mode, the output voltage is set by an external resistive voltage divider according to the following equation:

$$V_{OUT} = V_{FB} \left(1 + \frac{R1}{R2}\right)$$

where V_{FB} is the feedback reference voltage (0.6V typ.).

Typical Application

• Inductor Selection

The peak-to-peak ripple is set to 30% of the output current. This places the peak current far enough from the minimum over current trip level to ensure reliable operation while providing enough current ripples for the current mode converter to operate stably. The inductance is determined as the following equation:

$$L \geq \frac{(V_{IN} - V_{OUT}) \times D}{\Delta I_L \times f_{SW}}$$

Where ΔI_L is the inductor peak-to-peak ripple current D is the duty cycle determined by V_{OUT} / V_{IN} f_{SW} is the switching frequency.

• Output Capacitor Selection

For most applications a nominal 10 μ F or 22 μ F capacitor is suitable. The output capacitor keeps output ripple small and ensures control-loop stability.

The output capacitor must also have low impedance at the switching frequency. Ceramic, polymer, and Tantalum capacitors are suitable, with ceramic exhibiting the lowest ESR and high-frequency impedance. Output ripple with a ceramic output capacitor is approximately as follows:

$$V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8fC_{OUT}} \right]$$

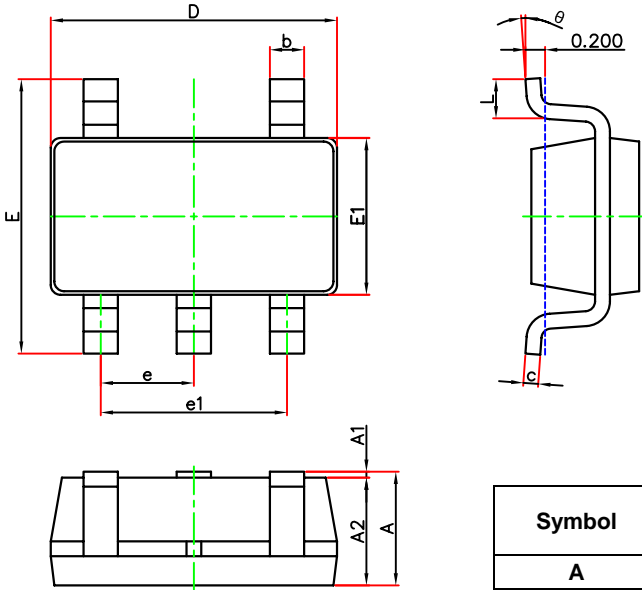
• Input Capacitor Selection

The input capacitance, C_{IN} , is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The RMS current is given by :

$$I_{RMS} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

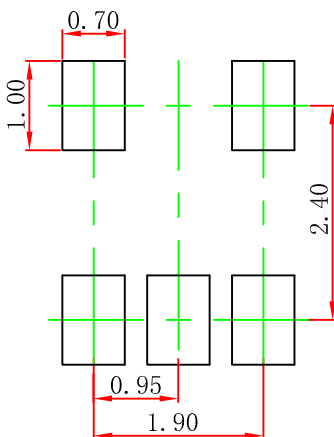
This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT} / 2$

SOT-23-5L Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	2.650	2.950	0.104	0.116
E1	1.500	1.700	0.059	0.067
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

SOT-23-5L Suggested Pad Layout



Note:

1. Controlling dimension "in" millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purpose only.

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

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