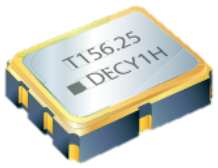
Product Features

1. Output Frequency :
   10 ~ 200 MHz (EA Series)
   50 ~ 156.25 MHz (EB Series)
2. Frequency Stability :
   ± 25 ppm @ (-40 ~ 85℃)
   ± 50 ppm @ (-40 ~ 105℃)
3. Supply Voltage : 1.8 , 2.5 , 3.3V (Typ.)
4. Output Type : LVPECL / LVDS / HCSL
5. Phase Jitter :
   50fs (Typ.) @156.25MHz LVPECL, 25℃
6. High Power Supply Noise Rejection Performance
7. Industry Standard Package :
   2.5 x 2.0 x 0.94 mm

Application :
- Optical Modules
- High Speed Network Interface Cards
- Data Center Switch



RoHS COMPLIANT
REACH COMPLIANT
Pb Free
Halogen Free HF

Test condition
Ambient temperature : 25 ± 5℃
Relative humidity : 40% ~ 70%

- Table 1 . Electrical Specifications

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions & Notes
LVPECL / LVDS / HCSL Common Electrical Characteristics						
Nominal Frequency	F		10 ~ 200		MHz	EA Series , Fundamental Mode
			50 ~ 156.25			EB Series , 3rd Overtone Mode
Frequency Stability	ST		± 25		ppm	@ -40~85℃ , Note 1
			± 50			@ -40~105℃ , Note 1
Operating Temperature	Topr	-40	-	85	℃	
		-40	-	105		
Supply Voltage	Vdd		1.8 , 2.5 , 3.3 (± 10%)		V	
Symmetry	TH/T	45	50	55	%	
Start-up Time	Tosc	-	-	10	ms	To 90% of Final Amplitude
LVPECL Electrical Characteristics						
Current Consumption	Icc	-	-	40	mA	RL=50Ω to VDD-2V
Standby Current	Icc(ST)	-	-	20	uA	OE = Low
Output Voltage High	VoH	VDD-1.025	-	VDD-0.74	V	
Output Voltage Low	VoL	VDD-1.81	-	VDD-1.405	V	
Output Voltage Range	Vdiff	600	1400	2000	mV	Differential Peak-to-Peak
Rise / Fall Time	Tr / Tf	-	-	0.5	ns	20% ~ 80% Output Swing
Enable Voltage High	-	0.7VDD	-	-	V	Note 2 , (Logic 1)
Enable Voltage Low	-	-	-	0.3VDD	V	Note 2 , (Logic 0)
Output Enable Delay Time	-	-	-	2	ms	
Output Disable Delay Time	-	-	-	200	ns	
RMS Phase Jitter	PJ	-	-	0.1	ps	Integrated from 12KHz ~ 20MHz @156.25MHz , 3.3V , Note3

Test condition
Ambient temperature：25 ± 5℃
Relative humidity： 40% ~ 70%

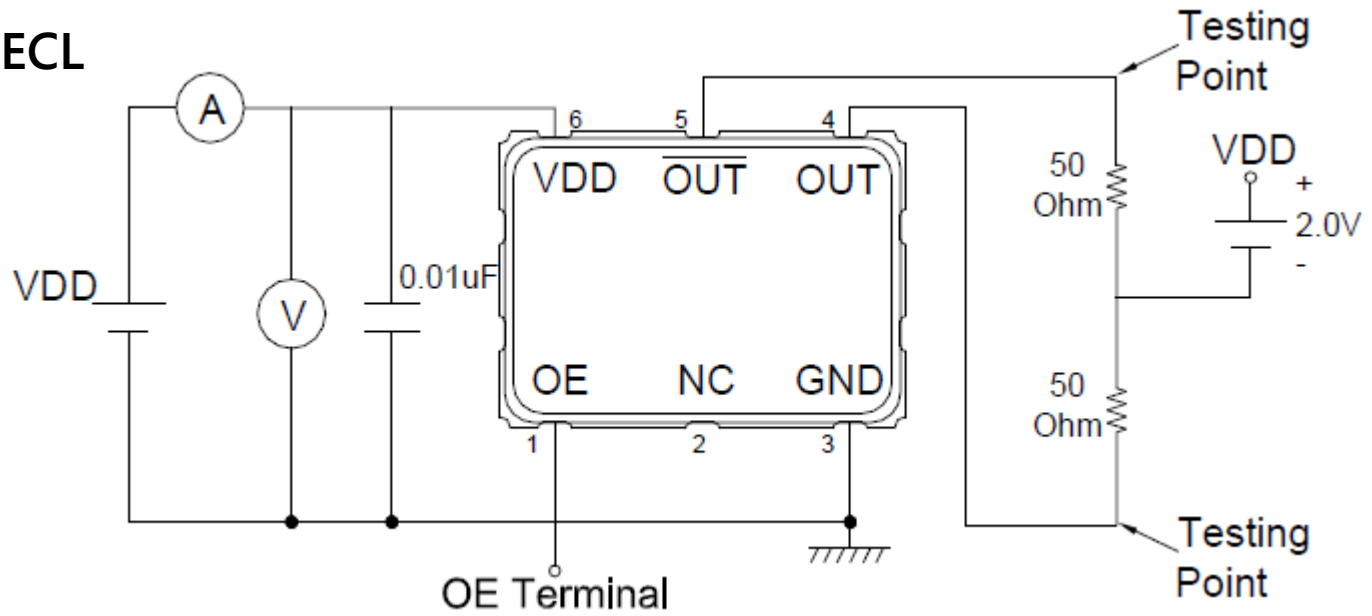
- Table 1 . Electrical Specifications (continued)

Parameters	Symbol	Min.	Typ.	Max.	Units	Notes
LVDS Electrical Characteristics						
Current Consumption	Icc	-	-	40	mA	RL=100Ω
Standby Current	Icc(ST)	-	-	15	uA	OE = Low
Output Voltage High	VoH	-	1.43	1.6	V	
Output Voltage Low	VoL	0.9	1.1	-	V	
Offset Voltage	-	1.125	1.250	1.375	V	
Output Swing (Single)	-	247	330	454	mV	Single Peak-to-Peak
Output Swing (Differential)	Vdiff	494	660	908	mV	Differential Peak-to-Peak
Rise / Fall Time	Tr / Tf	-	-	0.35	ns	20% ~ 80% Output Swing
Enable Voltage High	-	0.7VDD	-	-	V	Note 2
Enable Voltage Low	-	-	-	0.3VDD	V	Note 2
Output Enable Delay Time	-	-	-	2	ms	
Output Disable Delay Time	-	-	-	200	ns	
RMS Phase Jitter	PJ	-	-	0.2	ps	Integrated from 12KHz ~ 20MHz @156.25MHz , 3.3V , Note3
HCSL Electrical Characteristics						
Current Consumption	Icc	-	-	30	mA	RL=50Ω to VDD-2V
Standby Current	Icc(ST)	-	-	10	uA	OE = Low
Output Voltage High	VoH	660	740	850	mV	
Output Voltage Low	VoL	-150	0	150	mV	
Rise / Fall Time	Tr / Tf	-	-	0.5	ns	20% ~ 80% Output Swing
Enable Voltage High	-	0.7VDD	-	-	V	Note 2
Enable Voltage Low	-	-	-	0.3VDD	V	Note 2
Output Enable Delay Time	-	-	-	2	ms	
Output Disable Delay Time	-	-	-	200	ns	
RMS Phase Jitter	PJ	-	-	0.2	ps	Integrated from 12KHz ~ 20MHz @100MHz , 3.3V , Note3

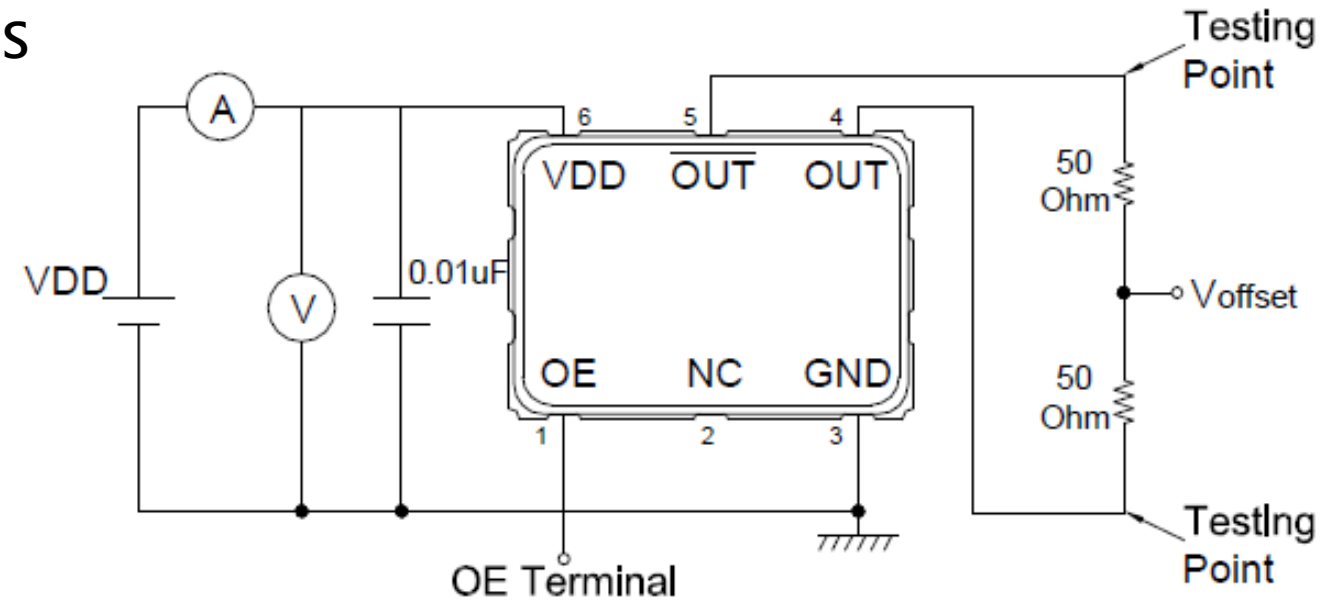
Note 1 : Inclusive of frequency tolerance at 25℃ , variation over temperature , supply voltage variation , 10 years aging and vibration.
Note 2 : Output will be enable if OE is Logic 1 or open ; Output will be disable if OE is Logic 0.
Note 3 : Phase Jitter will be slightly different according to output frequency and supply voltage.

- Test Diagram

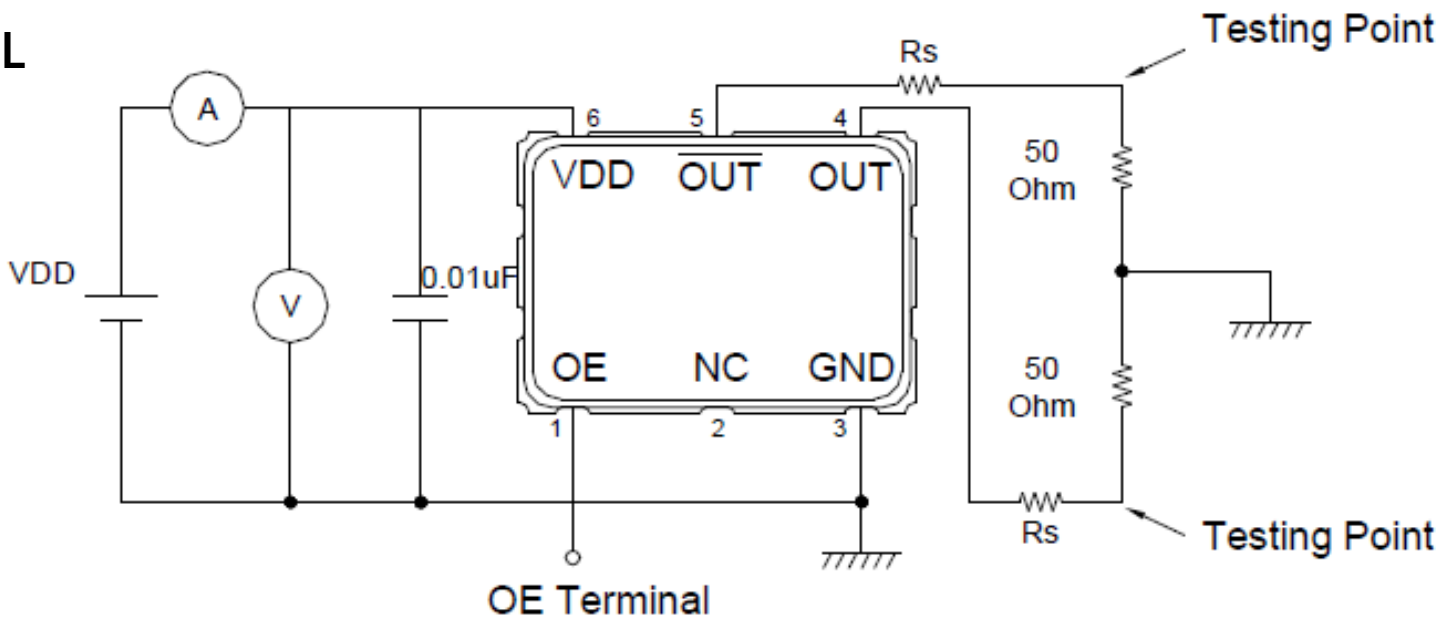
LVPECL



LVDS



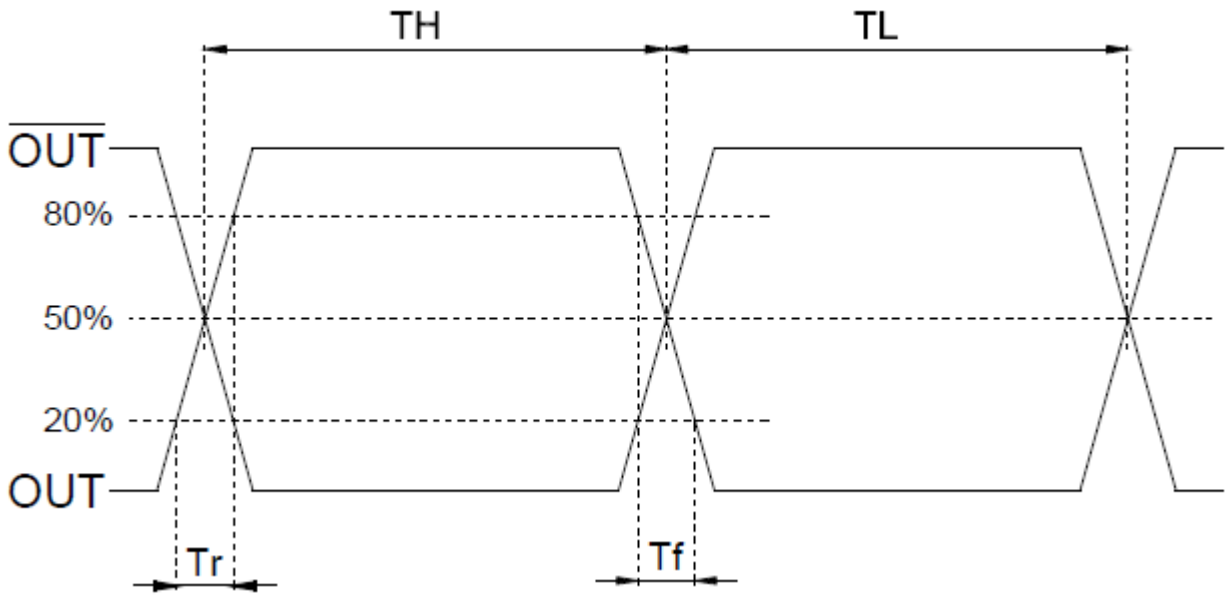
HCSL



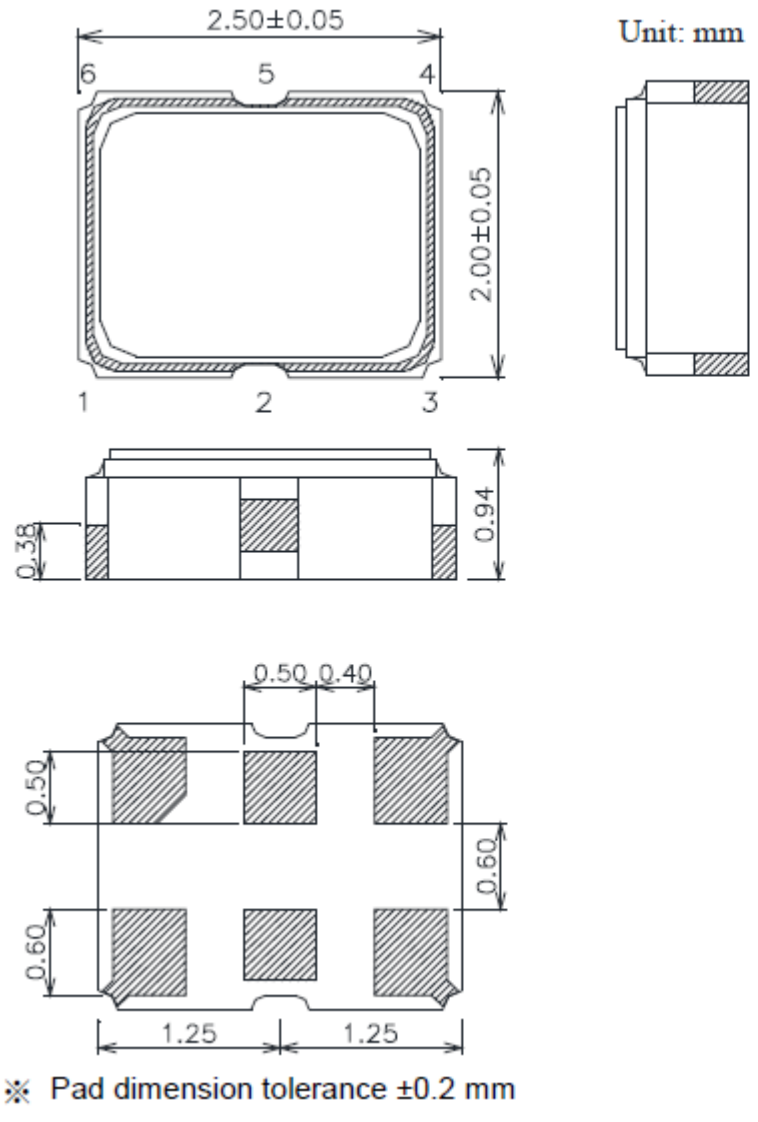
Testing Circuit Note:

1. Above testing circuits cover all the specifications except temperature test & Jitter measurement.
2. All the testing equipments are 50 Ohm terminal.
3. OE terminal is open connection except OE function test.
4. RS= 0 Ohm for test. 0 Ohm to 33 Ohm to minimize overshoot and ringback effect in application.

- Waveform Conditions



- Dimensions & Footprint(Recommended)



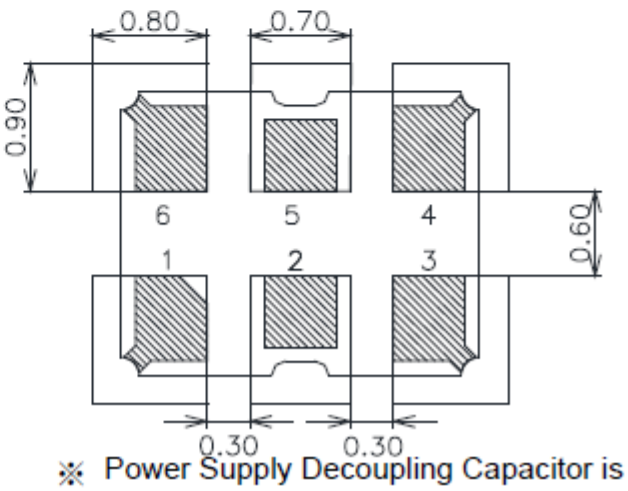
Unit: mm

※ Pad dimension tolerance ±0.2 mm

Pin Function:

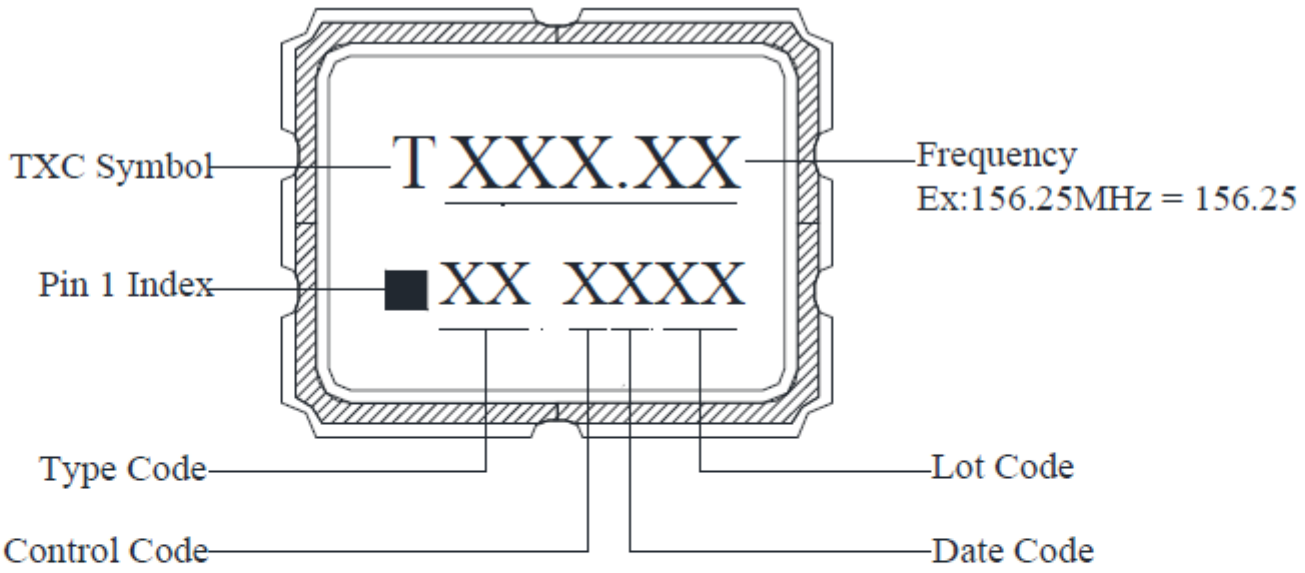
1. OE
2. NC
3. GND
4. OUT
5. $\overline{\text{OUT}}$
6. VDD

Land Pattern:



※ Power Supply Decoupling Capacitor is Required.

- Marking



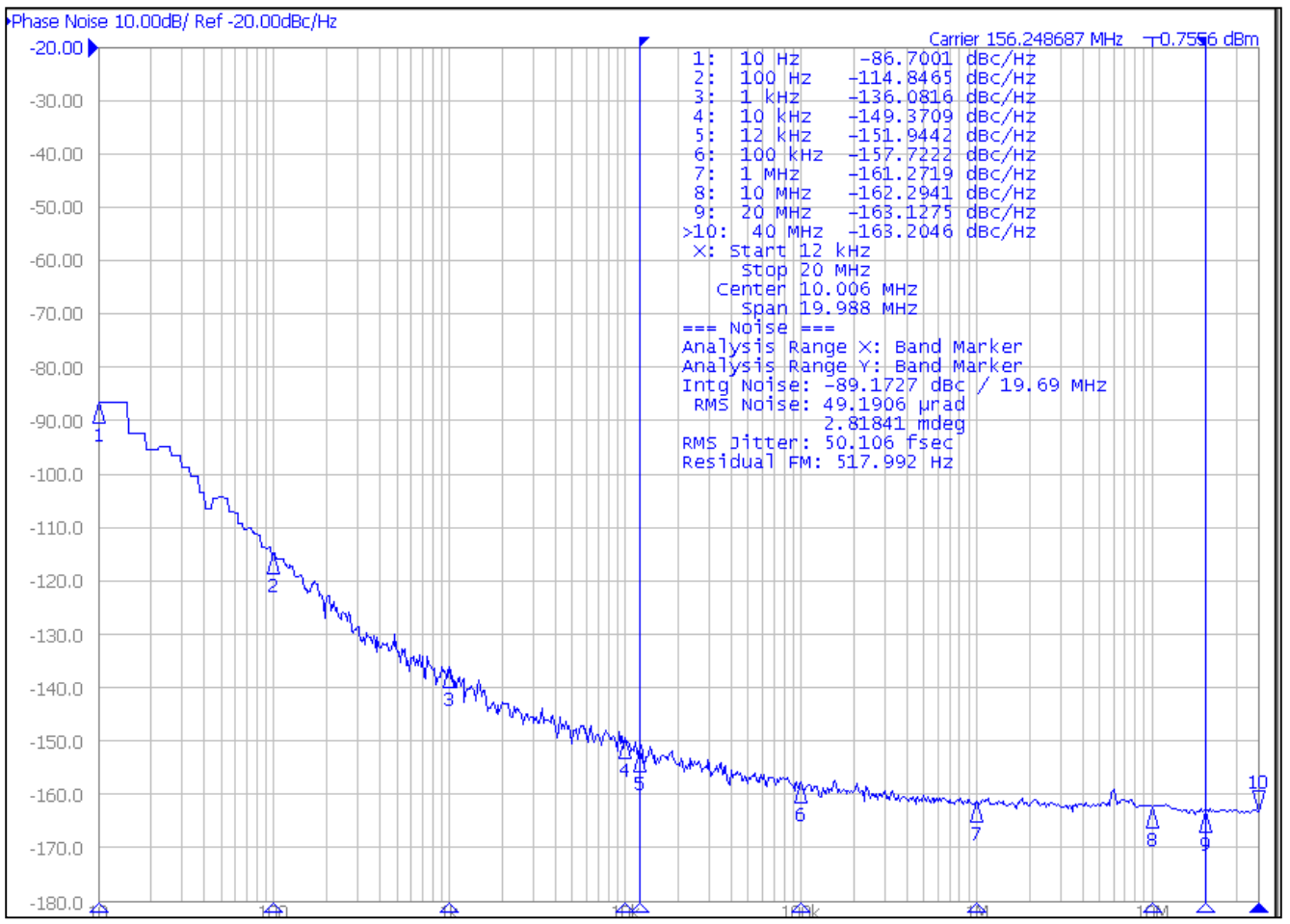
DATE CODE

MONTH / YEAR					JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT	NOV	DEC
2005	2009	2013	2017	2021	A	B	C	D	E	F	G	H	J	K	L	M
2006	2010	2014	2018	2022	N	P	Q	R	S	T	U	V	W	X	Y	Z
2007	2011	2015	2019	2023	a	b	c	d	e	f	g	h	j	k	l	m
2008	2012	2016	2020	2024	n	p	q	r	s	t	u	v	w	x	y	z

* This date code will be cycled every four years.

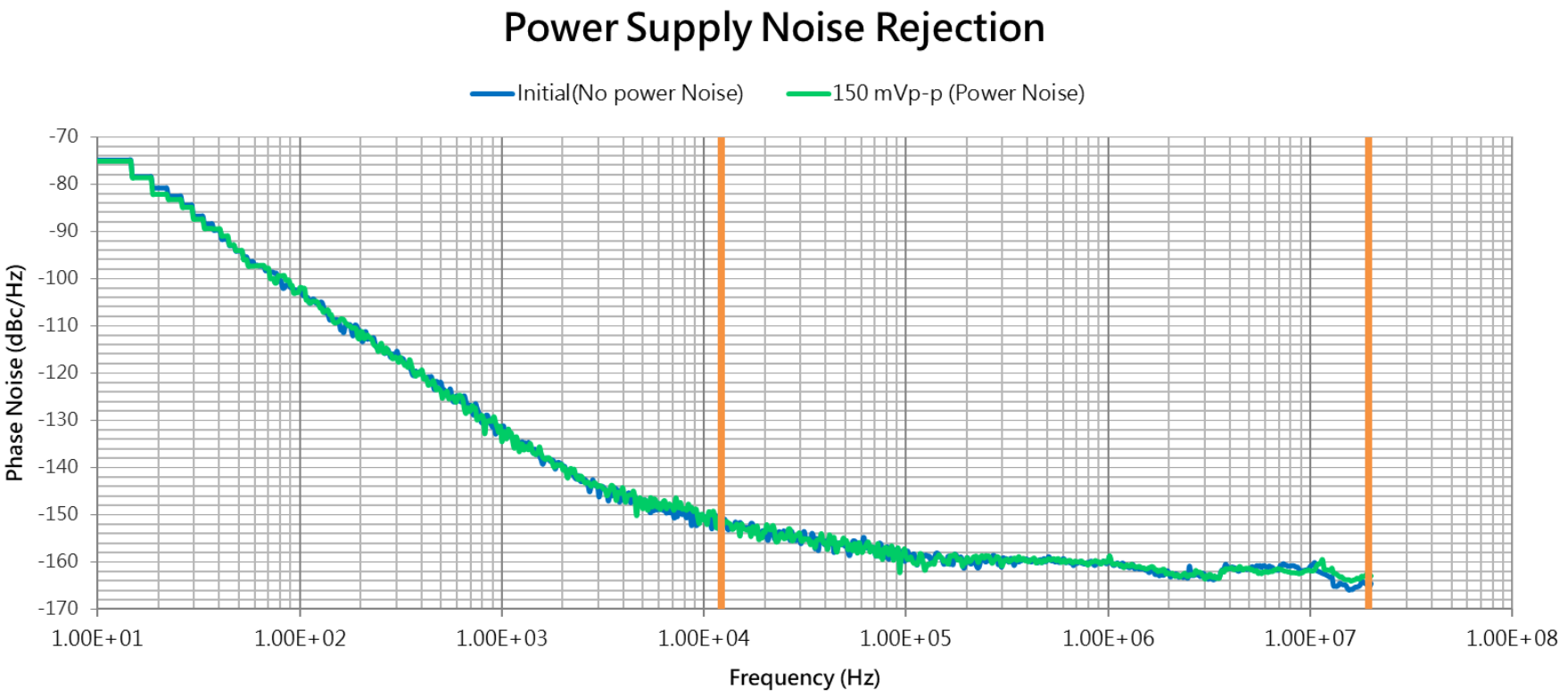
- Phase Noise & Jitter Performance

Test Condition ： 156.25MHz , 3.3V , LVPECL , @25℃ , Integrated from 12KHz ~ 20MHz



- Power Supply Noise Rejection Performance

Test Condition： 156.25MHz , 3.3V (Initial / Add 150m Vp-p White Noise) , @25℃
Integrated from 12KHz ~ 20MHz



- Table 2 . Revision History

Rev.	Revise Contents	Release Date
A	Initial released	2022.07.12