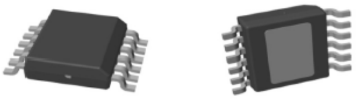
Datasheet

Dual high-side smart power solid state relay



PowerSSO-12™

Product status link
VNI2140J

Product label
SUSTAINABLE TECHNOLOGY

Features

- Nominal current: 0.75 A per channel
- Shorted-load protections
- Junction overtemperature protection
- Case overtemperature protection for thermal independence of the channels
- Thermal case shutdown restart not simultaneous for the various channels
- Protection against loss of ground
- Current limitation 1 A per channel
- Undervoltage shutdown
- Open-load in OFF-state and short to VCC detection
- Open-drain diagnostic outputs
- 3.3 V CMOS/TTL compatible inputs
- Fast demagnetization of inductive loads
- Conforms to IEC 61131-2

Applications

- Programmable logic control
- Industrial PC peripheral input/output
- Numerical control machines

Description

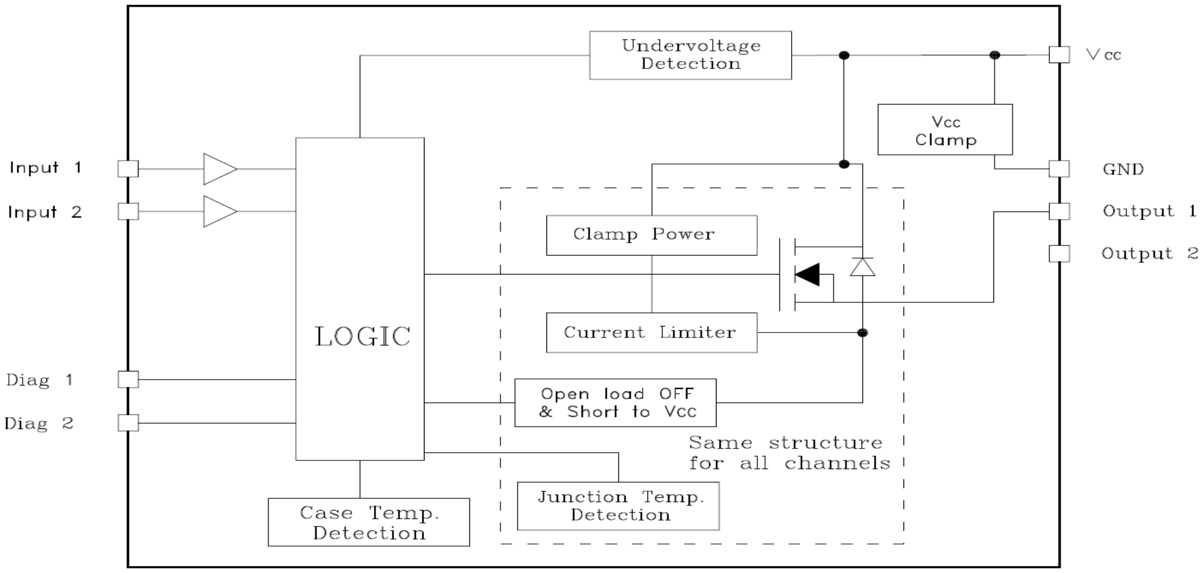
The VNI2140J is a monolithic device designed using STMicroelectronics' VIPower technology.

The device drives two independent resistive or inductive loads with one side connected to ground. Active current limitation prevents a drop in system power supply in cases of shorted-load, and built-in thermal shutdown protects the chip from damage due to overtemperature and short-circuit.

In overload conditions, channel turns OFF and ON automatically to maintain the junction temperature between T_{TSD} and T_R. If the case temperature reaches T_{CSD}, the overloaded channel is turned OFF and restarts only when case temperature decreases down to T_{CR}. In order to avoid high-peak current from the supply, when more than one channel is overloaded the T_{CSD} restart is not simultaneous. Non overloaded channels continue to operate normally. The open-drain diagnostics output indicates overtemperature conditions and open-load in OFF-state.

1 Block diagram

Figure 1. Block diagram



2 Pin connections

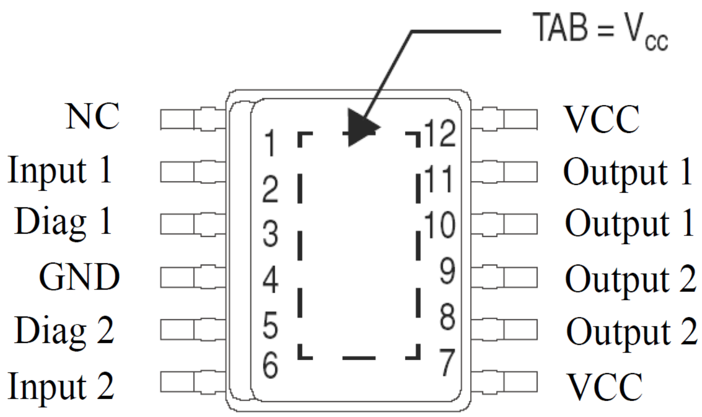


Figure 2. Pin connections (top view)

Table 1. Pin description

Pin	Name	Type	Description
1	NC	-	Not connected
2	Input 1	Logic input	Channel 1 input, 3.3 V CMOS/TTL compatible
3	Diag 1	Output/Open-drain	Channel 1 diagnostic in open-drain configuration
4	GND	Ground	Device ground connection
5	Diag 2	Output/Open-drain	Channel 2 diagnostic in open-drain configuration
6	Input 2	Logic input	Channel 2 input, 3.3 V CMOS/TTL compatible
7	VCC	Supply	Supply voltage
8	Output 2	Output	Channel 2 power stage output, internally protected
9	Output 2	Output	Channel 2 power stage output, internally protected
10	Output 1	Output	Channel 1 power stage output, internally protected
11	Output 1	Output	Channel 2 power stage output, internally protected
12	VCC	Supply	Supply voltage
TAB	TAB	Supply	Supply voltage

3 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Power supply voltage	45	V
$-V_{CC}$	Reverse supply voltage	-0.3	V
I_{GND}	DC ground reverse current	-250	mA
I_{OUT}	DC output current	Internally limited (1)	A
I_R	DC reverse output current (per channel)	-5	A
I_{IN}	Input pin current (per channel)	+/-10	mA
V_{IN}	Input pin voltage	$+V_{CC}$	V
V_{DIAG}	Diag pin voltage	$+V_{CC}$	V
I_{DIAG}	Diag pin current	+/-10	mA
V_{ESD}	Electrostatic discharge (R = 1.5k Ω; C = 100 pF)	2000	V
E_{AS}	Single pulse avalanche energy per channel, all channels driven simultaneously at T_{AMB} = 125 °C, I_{OUT} = 1 A	300	mJ
P_{TOT}	Power dissipation at T_C = 25 °C	Internally limited (1)	W
T_J	Junction operating temperature	Internally limited (1)	°C
T_{STG}	Storage temperature	-55 to 150	°C

1. *Protection functions are intended to avoid IC damage in fault conditions and are not intended for continuous operation. Continuous and repetitive operation of protection functions may reduce the IC lifetime.*

4 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th(JC)}$	Thermal resistance junction-case [1]	1	°C/W
$R_{th(JA)}$	Thermal resistance junction-ambient [2]	See Figure 11	°C/W

1. *Per channel*
2. *When mounted using minimum recommended pad size on FR-4 board.*

5 Electrical characteristics

9 V < V_{CC} < 36 V; -40 °C < T_J < 125 °C; unless otherwise specified

Table 4. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		9	-	45	V
$R_{DS(ON)}$	ON-state resistance	I_{OUT} = 0.5 A at T_J = 25 °C	-	0.080	-	Ω
		I_{OUT} = 0.5 A at T_J = 125 °C	-	-	0.150	Ω
I_S	V_{CC} supply current	All channels in OFF-state	-	300	-	µA
		ON-state with V_{IN} = 5 V, T_J = 125 °C	-	1.9	4	mA
V_{CLAMP}	V_{CC} clamp voltage	I_S = 20 mA	45	-	52	V
$V_{OUT(OFF)}$	OFF-state output voltage	V_{IN} = 0 V, I_{OUT} = 0 A	-	-	3	V
$I_{OUT(OFF)}$	OFF-state output current	V_{IN} = V_{OUT} = 0 V	0	-	5	µA
$I_{OUT(OFF1)}$		V_{IN} = 0 , V_{OUT} = 4 V	-35	-	0	µA
I_{LGND}	Output current at GND disconnection	V_{CC} = V_{IN1} or V_{IN2} = V_{DIAG} = V_{GND} = 24 V; V_{OUT} = 0 V	-	-	0.5	mA

Table 5. Switching

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(ON)}$	Output current turn-on delay time	V_{CC} = 24 V, R_L = 48 Ω, Input rise time < 0.1 µs, T_J = 25 °C, see Figure 6	-	8	-	µs
t_r	Output current rise time		-	15	-	µs
$t_{d(ON)} + t_r$	Turn-on response		-	-	35	µs
$t_{d(OFF)}$	Output current turn-off delay time		-	10	-	µs
t_f	Output current fall time		-	7	-	µs
$t_{d(OFF)} + t_f$	Turn-off response		-	-	40	µs
t_{DOL}	Delay time for open-load detection		-	500	-	µs
$dV/dt_{(ON)}$	Turn-on voltage slope		-	3	-	V/µs
$dV/dt_{m(OFF)}$	Turn-off voltage slope		-	4	-	V/µs

Table 6. Logic inputs

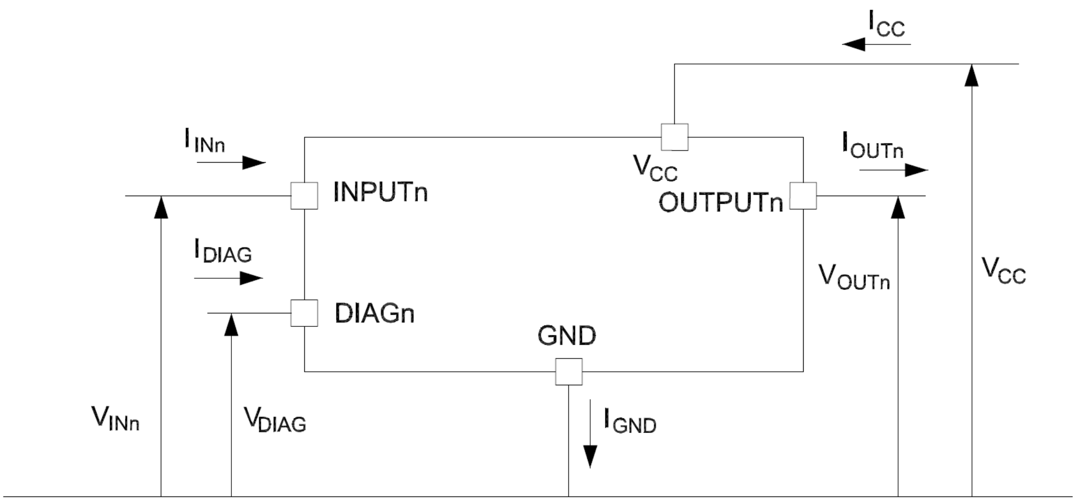
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage		-	-	0.8	V
V_{IH}	Input high level voltage		2.20	-	-	V
$V_{I(HYST)}$	Input hysteresis voltage		-	0.15	-	V
I_{IN}	Input current	V_{IN} = 15 V	-	-	10	µA
		V_{IN} = 36 V	-	-	210	

Table 7. Protection and diagnostic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{DIAG} [(1)]	Diag voltage output low	I_{DIAG} = 1.5 mA (fault condition)	-	-	0.6	V
V_{USD}	Undervoltage protection		7	-	9	V
V_{USDHYS}	Undervoltage hysteresis		0.4	0.5	-	V
I_{LIM}	DC short-circuit current	V_{CC} = 24 V, R_{LOAD} ≤ 10 mΩ	1	-	2	A
I_{LDIAG}	Diag leakage current	V_{CC} = 32 V	-	30	-	µA
V_{OL}	Open-load OFF-state voltage detection threshold	V_{IN} = 0 V	2	3	4	V
T_{TSD}	Junction shutdown temperature		150	170	-	°C
T_R	Junction reset temperature		135	155	200	°C
T_{HYST}	Junction thermal hysteresis		7	15	-	°C
T_{CSD}	Case shutdown temperature		125	139	146	°C
T_{CR}	Case reset temperature		110	-	-	°C
T_{CHYST}	Case thermal hysteresis		7	15	-	°C
V_{DEMAG}	Output voltage at turn-OFF	I_{OUT} = 0.5 A; L_{LOAD} ≥ 1 mH	V_{CC} - 45	V_{CC} - 50	V_{CC} - 52	V

1. *Diag determination > 100 ms after the switching edge.*

Figure 3. Current and voltage conventions



6 Truth table

Table 8. Truth table

Condition	$Input_n$	$Output_n$	$Diag_n$
Normal operation	L	L	H
	H	H	H
Overtemperature	L	L	H
	H	L	L
Undervoltage	L	L	X
	H	L	X
Shorted-load (current limitation)	L	L	H
	H	X	H
Output voltage > V_{OL}	L	Z[(1)]	L
	H	H	H
Short to V_{CC}	L	H	L
	H	H	H

1. Depending on the external circuit.

Note: X = don't care.

7 Switching waveforms

Figure 4. **Switching waveforms**

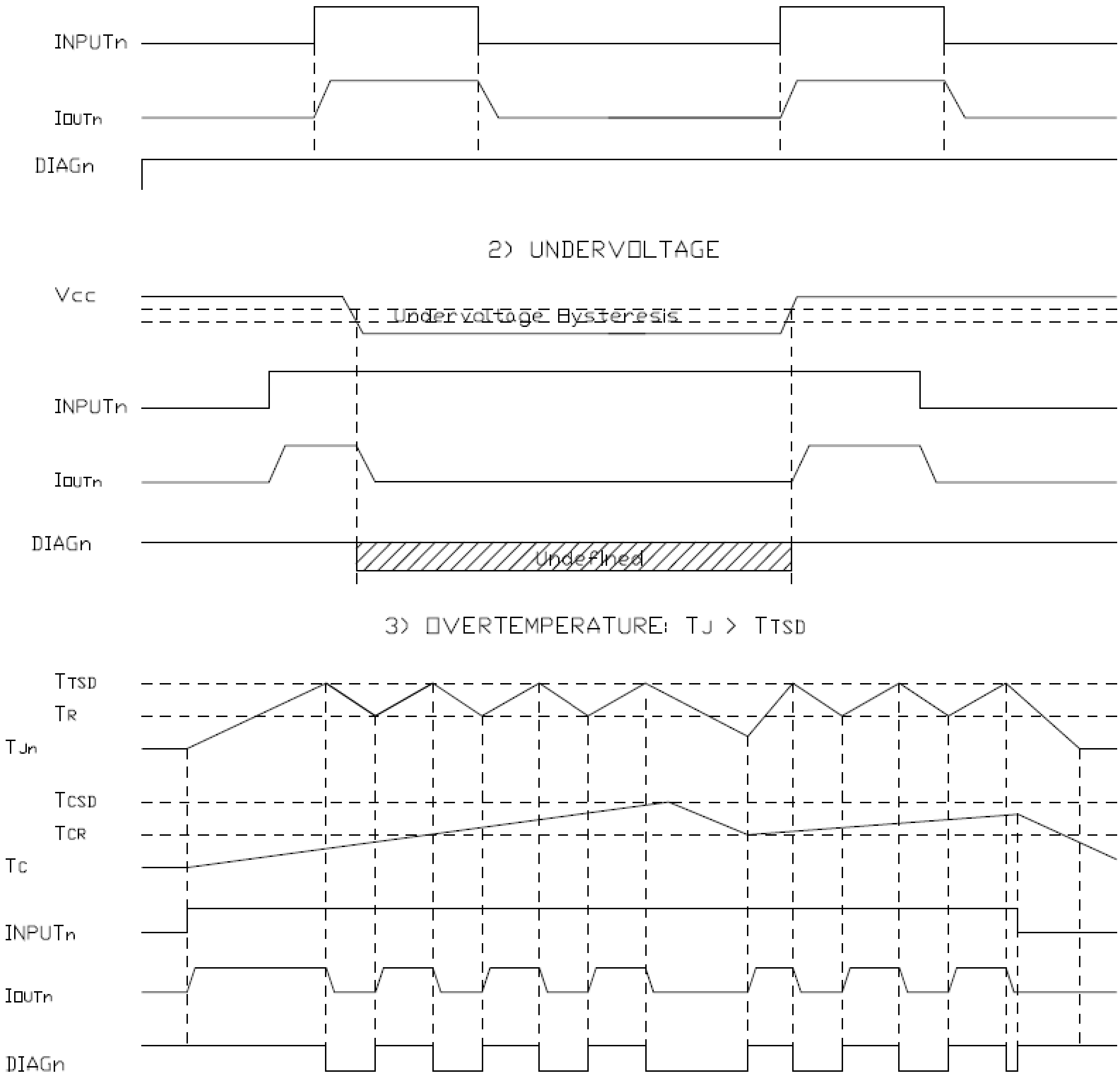


Figure 5. **Switching waveforms (continued)**

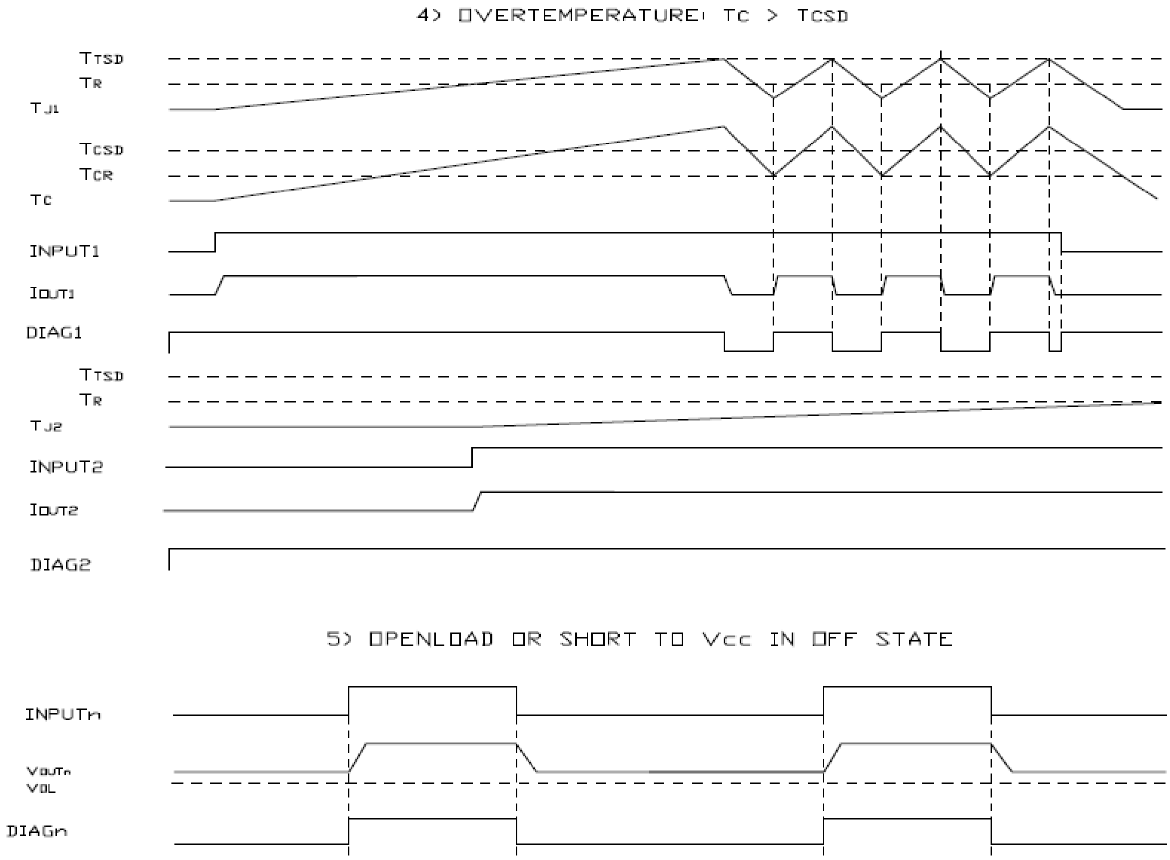


Figure 6. **Switching parameter test conditions**

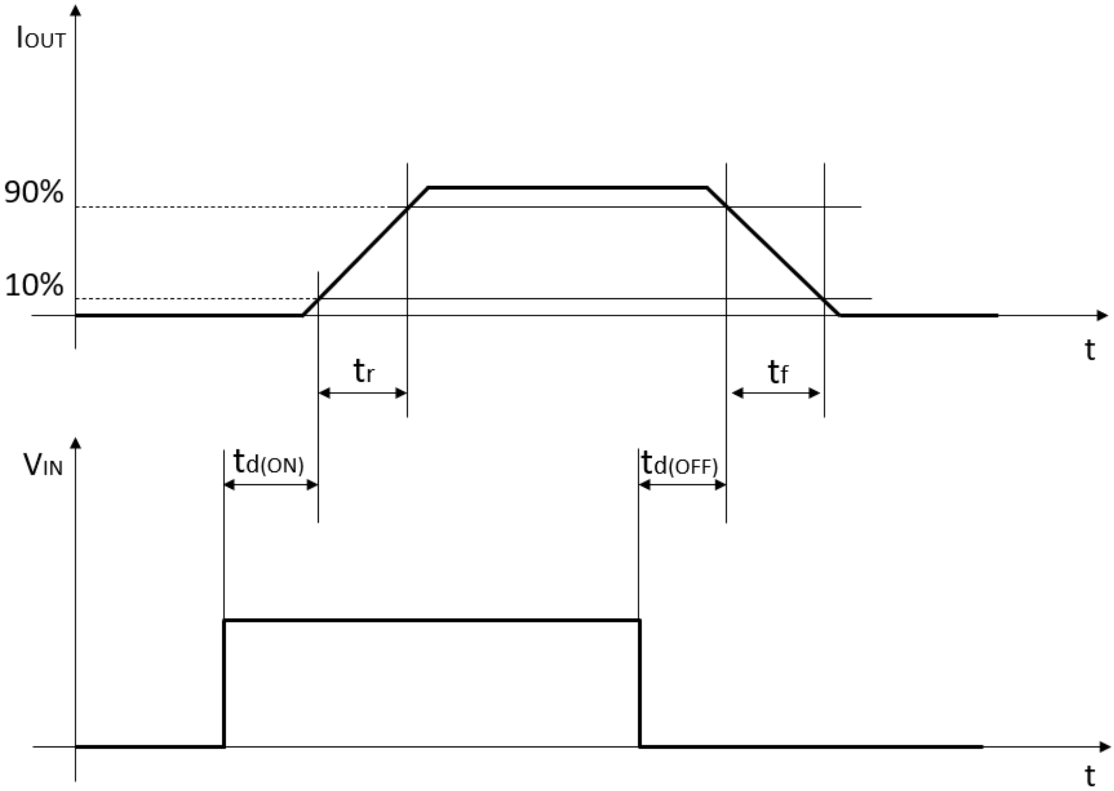
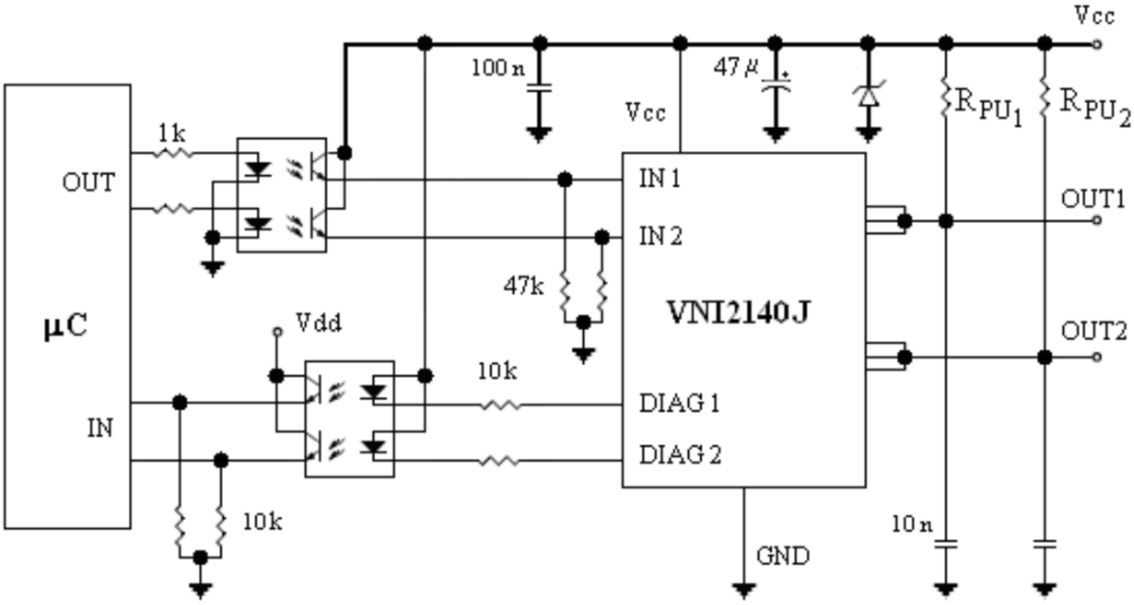


Figure 7. **Typical application circuit**



8 Open-load

In order to detect the open-load fault, a pull-up resistor must be connected between the V_{CC} line and the output pin.

In a normal condition, a current flows through the network made up of a pull-up resistor and a load. The voltage across the load is less than V_{OLMIN} and the DIAG pin is kept high.

This is the result in the condition:

Equation 1:

$V_{CC} [R_{LOAD} / (R_{LOAD} + R_{PU})] < V_{OLMIN}$

or

Equation 2:

$[(V_{CC} / V_{OLMIN}) - 1] R_{LOAD} < R_{PU}$

When an open-load event occurs the voltage on the output pin rises to a value higher than V_{OLMAX} (depending on the pull-up resistor) and the diag pin goes down.

This is the result in the condition:

Equation 3:

$R_{PU} < (V_{CC} - V_{OLMAX}) / |I_{OUT(OFF1)MIN}|$

Figure 8. **Open-load detection**

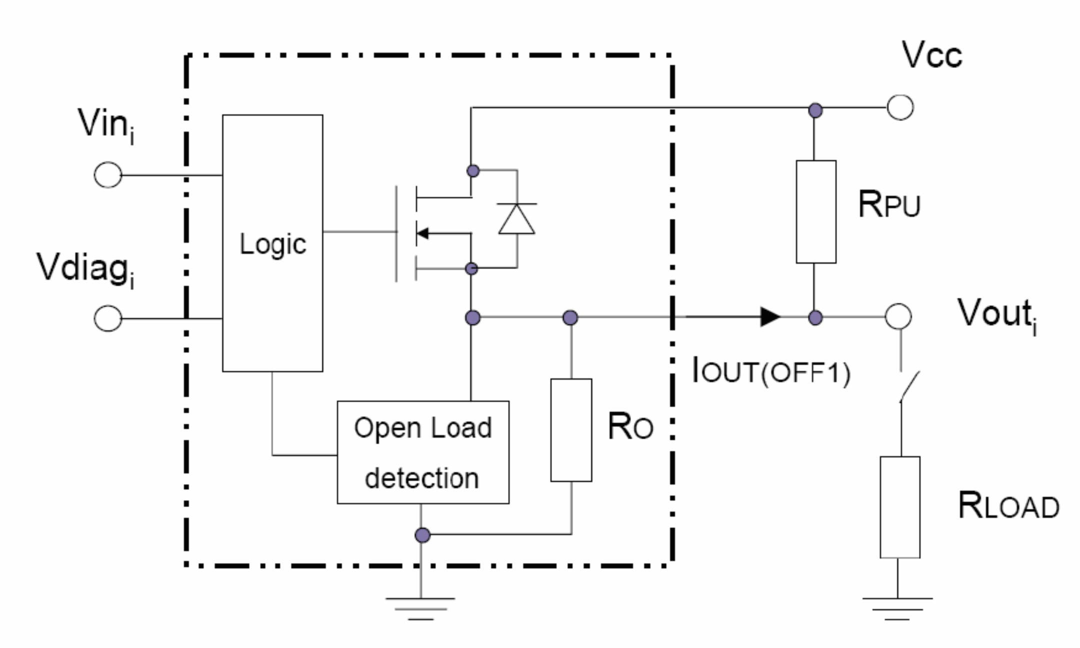
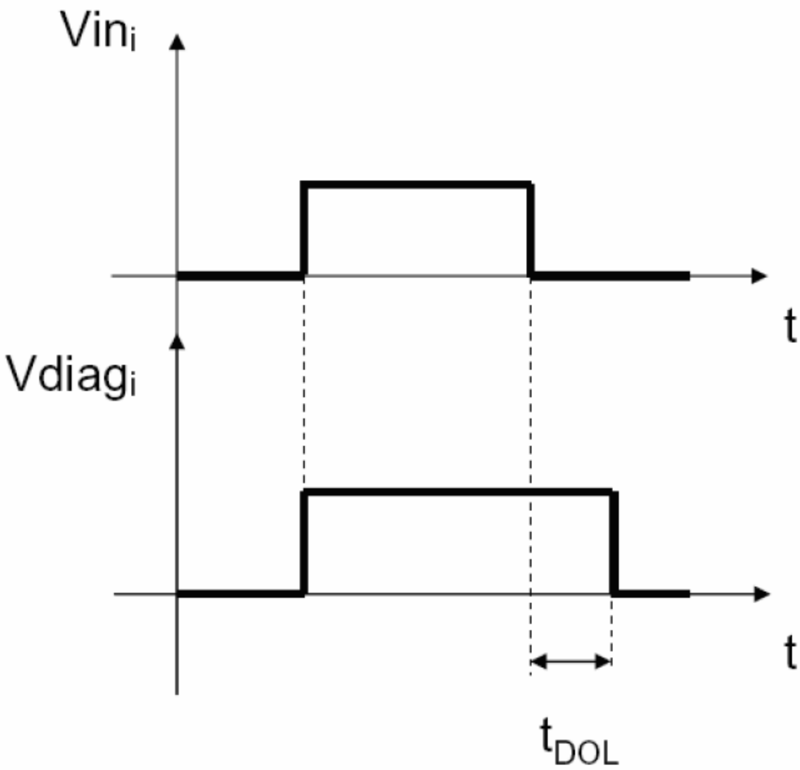
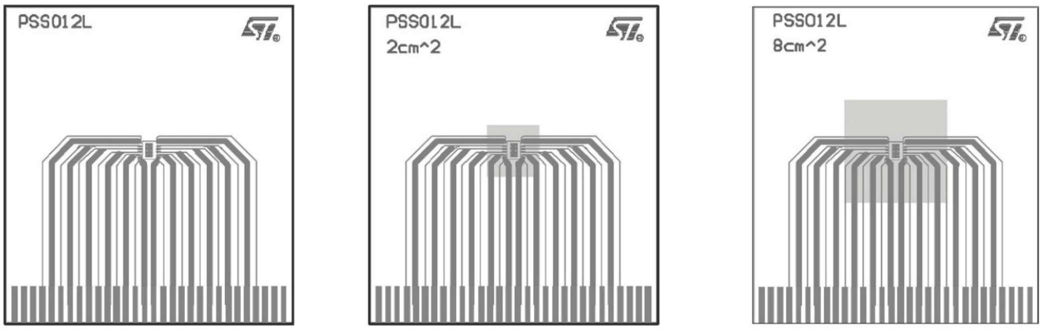


Figure 9. Turn-on/off to open-load



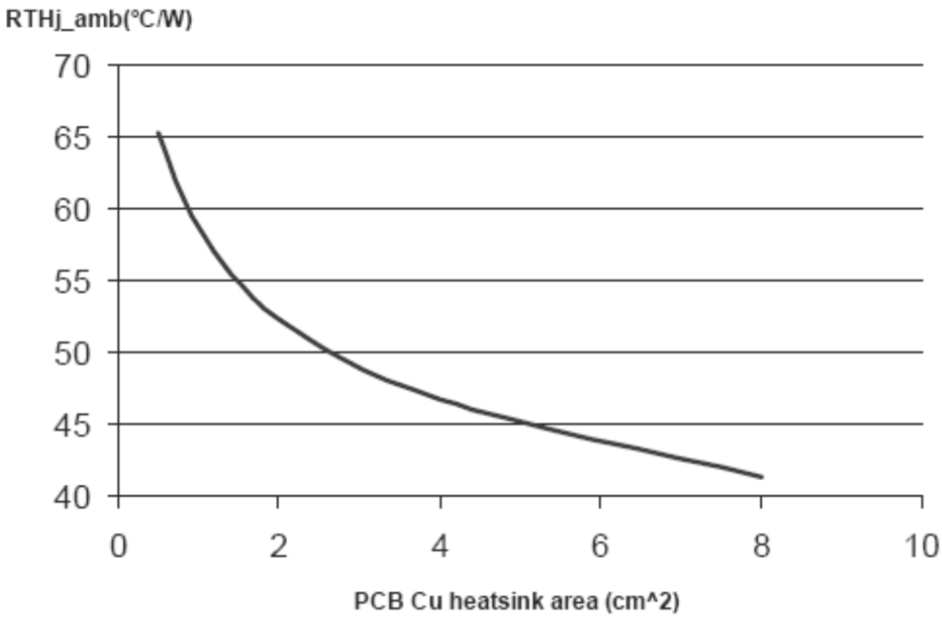
9 Package and PCB thermal data

Figure 10. PowerSSO-12 PC board



Layout condition of R_{th} and Z_{th} measurements (PCB: Double layer, Thermal Vias, FR4 area= 77mm x 86mm, PCB thickness=1.6mm, Cu thickness=70µm (front and back side), Copper areas: from minimum pad lay-out to 8cm^2).

Figure 11. R_{thJA} vs. PCB copper area in open box free-air condition



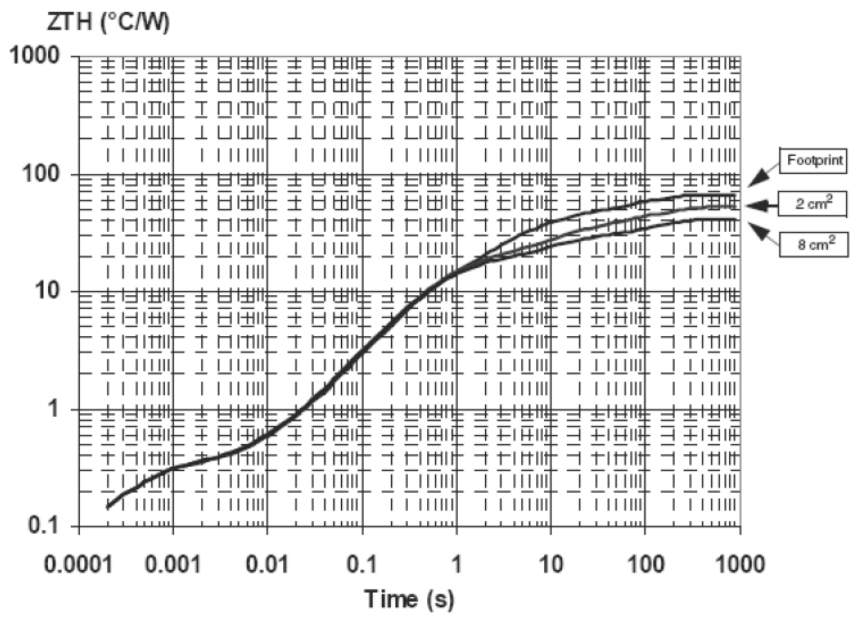


Figure 12. PowerSSO-12 thermal impedance junction ambient single pulse

Pulse calculation formula:

$Z_{TH\delta} = R_{TH} \times \delta + Z_{THtp} (1 - \delta)$

where $\delta = t_p / T$

Figure 13. Thermal fitting model of a double channel HSD in PowerSSO-12

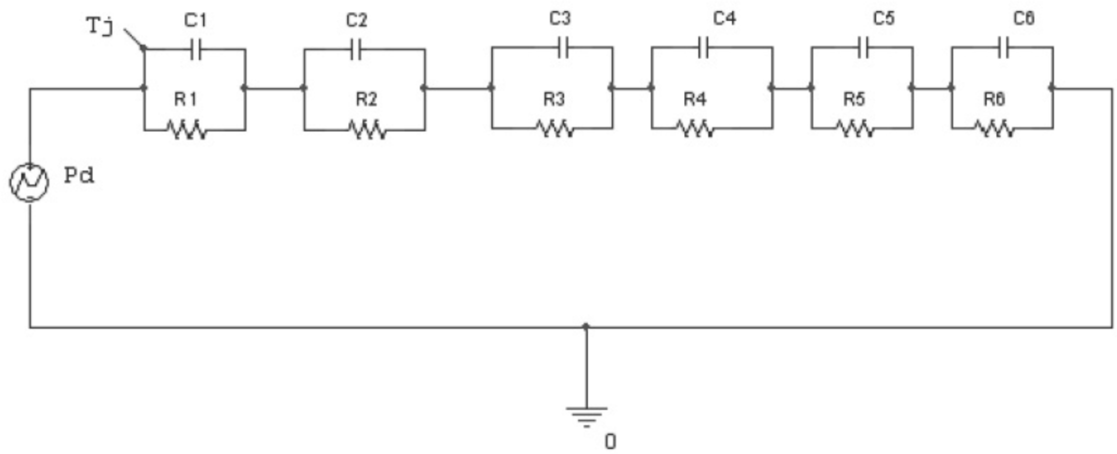


Table 9. Thermal parameter

Area/island (cm^2)	Footprint	2	8
R1 (°C/W)	0.1	-	-
R2 (°C/W)	0.2	-	-
R3 (°C/W)	7	-	-
R4 (°C/W)	10	10	9
R5 (°C/W)	22	15	10
R6 (°C/W)	26	20	15
C1 (W.s/°C)	0.0001	-	-
C2 (W.s/°C)	0.002	-	-
C3 (W.s/°C)	0.05	-	-
C4 (W.s/°C)	0.2	0.1	0.1
C5 (W.s/°C)	0.27	0.8	1
C6 (W.s/°C)	3	6	9

10 Reverse polarity protection

Reverse polarity protection can be implemented on-board using two different solutions:

1. Placing a resistor (R_{GND}) between IC GND pin and load GND
2. Placing a diode between IC GND pin and load GND

If option 1 is selected, the minimum resistance value has to be selected according to the following equation:

$R_{GND} \geq V_{CC} / I_{GND}$

where I_{GND} is the DC reverse ground pin current and can be found in Section 3 of this datasheet.

Power dissipated by R_{GND} (when $V_{CC} < 0$: during reverse polarity situations) is:

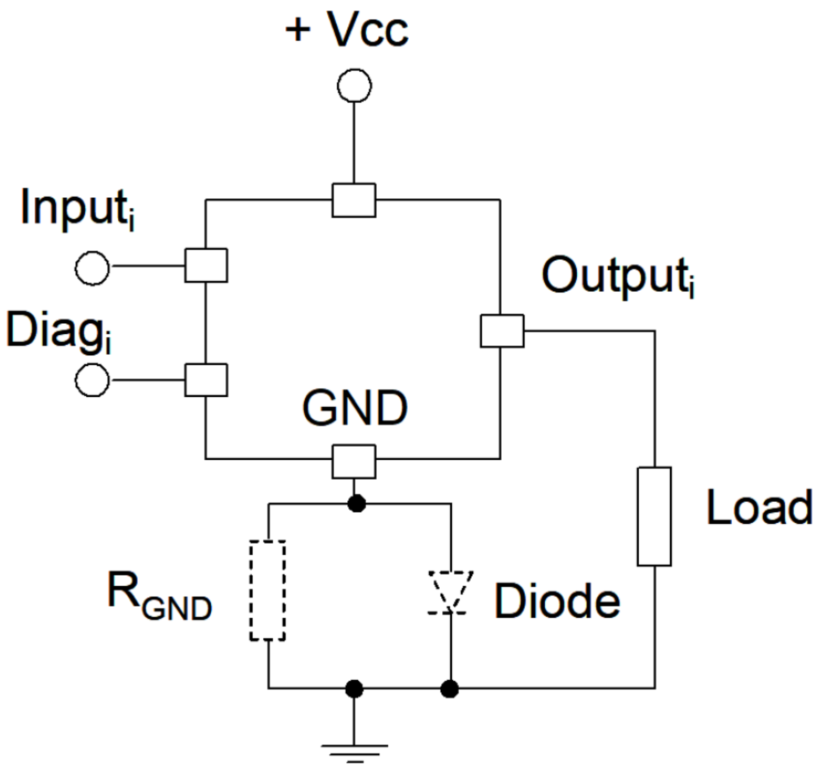
$P_D = (V_{CC})^2 / R_{GND}$

If option 2 is selected, the diode has to be chosen by taking into account VRRM >$|V_{CC}|$ and its power dissipation capability:

$P_D \geq I_S \times V_F$

Note: In normal conditions (no reverse polarity), due to the diode, there is a voltage drop between GND of the device and GND of the system.

Figure 14. Reverse polarity protection



This schematic can be used with any type of load.

11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

11.1 PowerSSO-12™ package information

Figure 15. PowerSSO-12™ package outline

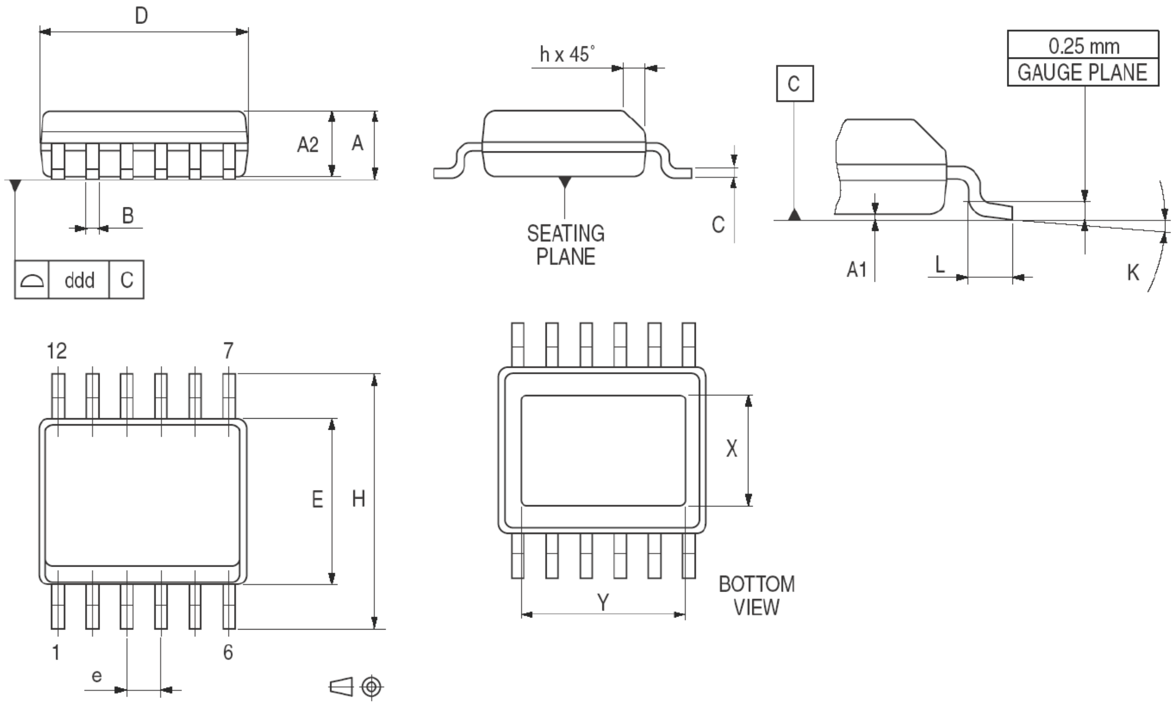
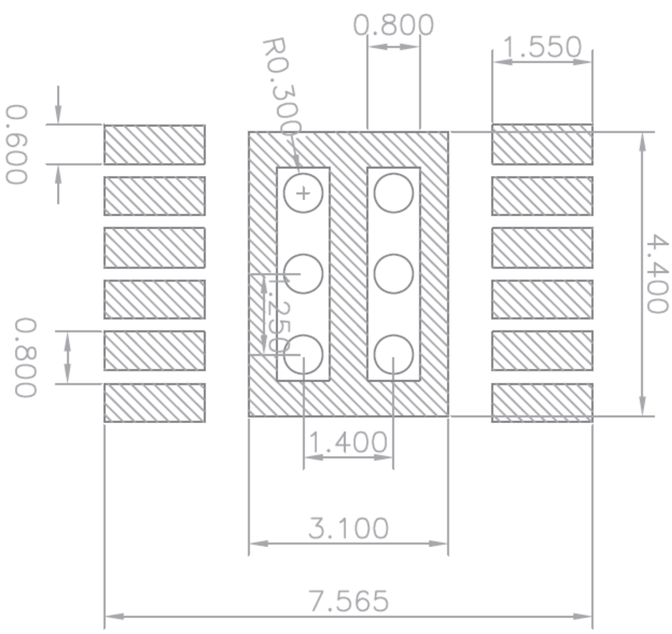


Table 10. PowerSSO 12, mechanical data

Symbol	Dimensions [mm]		
	Min.	Typ.	Max.
A	1.250	-	1.620
A1	0.000	-	0.100
A2	1.100	-	1.650
B	0.230	-	0.410
C	0.190	-	0.250
D	4.800	-	5.000
E	3.800	-	4.000
e	-	0.800	-
H	5.800	-	6.200
h	0.250	-	0.500
L	0.400	-	1.270
k	0°	-	8°
X	1.900	-	2.500
Y	3.600	-	4.200
ddd	-	-	0.100

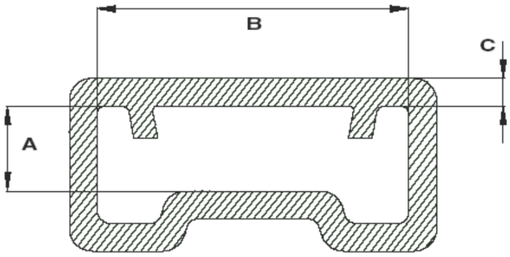
Figure 16. Suggested footprint



STMicroelectronics is not responsible for any PCB related issues. The footprint shown in the above figure is a suggestion, which might not be in line with the customer PCB supplier design rules.

12 PowerSSO-12™ packing information

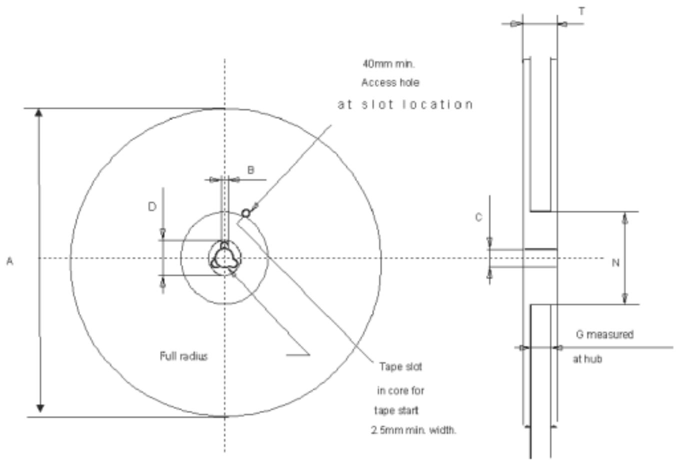
Figure 17. PowerSSO-12™ tube shipment (no suffix)



Base Q.ty	100
Bulk Q.ty	2000
Tube length (± 0.5)	532
A	1.85
B	6.75
C (± 0.1)	0.6

All dimensions are in mm.

Figure 18. PowerSSO-12™ tape and reel shipment (suffix "TR")



REEL DIMENSIONS

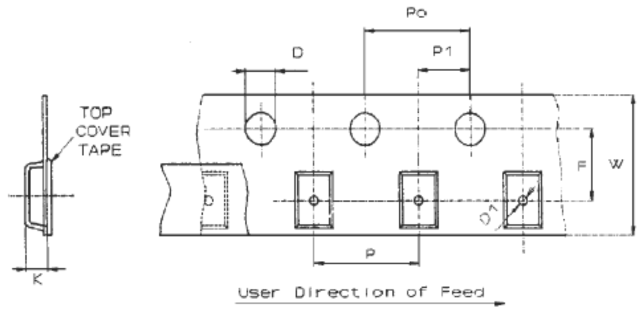
Base Q.ty	2500
Bulk Q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	12.4
N (min)	60
T (max)	18.4

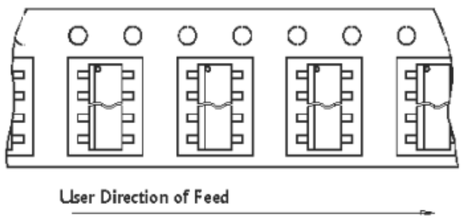
TAPE DIMENSIONS

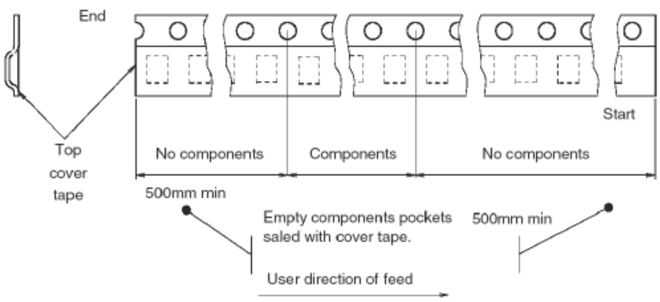
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	W	12
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	8
Hole Diameter	D (± 0.05)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.1)	5.5
Compartment Depth	K (max)	4.5
Hole Spacing	P1 (± 0.1)	2

All dimensions are in mm.







13 Ordering information

Table 11. Ordering information

Part number	Package	Packaging
VNI2140J	PowerSSO-12	Tube
VNI2140JTR		Tape and reel

Revision history

Table 12. **Document revision history**

Date	Version	Changes
16-Dec-2008	1	Initial release.
29-Apr-2009	2	Updated Table 5 on page 6
03-Jul-2009	3	Updated features in cover page and Table 5 on page 6
27-Aug-2009	4	Updated Section 9: Reverse polarity protection
25-Mar-2010	5	Updated Cover page and Table 4 on page 5
26-Apr-2010	6	Updated Table 5 on page 6
21-Jul-2010	7	Updated Table 8 on page 7
15-Nov-2011	8	Updated Figure 18 on page 21
09-Nov-2017	9	Updated Table 4 on page 5 and Table 7 on page 6. Minor modifications throughout document.
10-Dec-2019	10	Updated Section 9: Reverse polarity protection
13-Sep-2022	11	DS format changed; table 9: T_{CSD} values (Typ. and Max.) changed. Reduced the maximum value of I_{LGND}. Other minor text changes.

Contents

List of tables

List of figures