PD70211

PD Controller with Switching Regulator for AF/AT/UPOE/ HDBaseT/4-pair PoE Applications

Product Overview

Microchip's PD70211 is an advanced PD interface IC with integrated switching Pulse-Width Modulation (PWM) regulator control for powered devices in PoE applications. It supports IEEE® 802.3af, IEEE 802at, HDBaseT, and general 2/4-pair configurations.

The PD70211 front-end includes an advanced classification block that supports 2, 3, 4, and 6 event classification. Using the SUPP_Sx pins, it also identifies the four pairs of cable that actually receive power and generate appropriate flags.

The IC features an internal bleeder for discharging the input capacitor of the DC/DC converter rapidly to ensure fast re-detection and port power-up, in case of a sudden removal and re-insertion of the Ethernet cable into the RJ-45. The advanced PWM current-mode section supports synchronous Flyback and Active Clamp Forward topologies, as well as Buck, Boost, and so on.

Features

The PD70211 device has the following key features.

- Supports IEEE 802.3af/at, HDBaseT, and other 2-pair/4-pair configurations
- Wall adapter support (Rear Aux method)
- PD detection and programmable classification
- 2, 3, 4, and 6 event classification
- Integrated 0.3 Ω isolating (series-pass) FET
- Inrush current limiting
- Less than 10 µA offset current during detection
- Advanced PWM section
- Lead-free QFN-36 (6 mm × 6 mm) package

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The following table lists the Microchip PD products offerings.

Table 1. Microchip Powered Device Products Offerings

Part	Type	Package	IEEE 802.3af	IEEE 802.3at	HDBaseT (PoH)	UPoE
PD70100	Front end	3 mm × 4 mm 12L DFN	x	—	—	—
PD70101	Front end + PWM	5 mm × 5 mm 32L QFN	x	—	—	—
PD70200	Front end	3 mm × 4 mm 12L DFN	x	x	—	—
PD70201	Front end + PWM	5 mm × 5 mm 32L QFN	x	x	—	—
PD70210	Front end	4 mm × 5 mm 16L DFN	x	x	x	x
PD70210A	Front end	4 mm × 5 mm 16L DFN	x	x	x	x
PD70210AL	Front end	5 mm × 7 mm 38L QFN	x	x	x	x
PD70211	Front end + PWM	6 mm × 6 mm 36L QFN	x	x	x	x
PD70224	Ideal Diode Bridge	6 mm x 8 mm 40L QFN	x	x	x	x

Applications

The following are the applications of the PD70211 device.

- HDBaseT up to 95 W
- IEEE 802.3af and IEEE 802at
- Power forwarding
- Indoor and outdoor PoE

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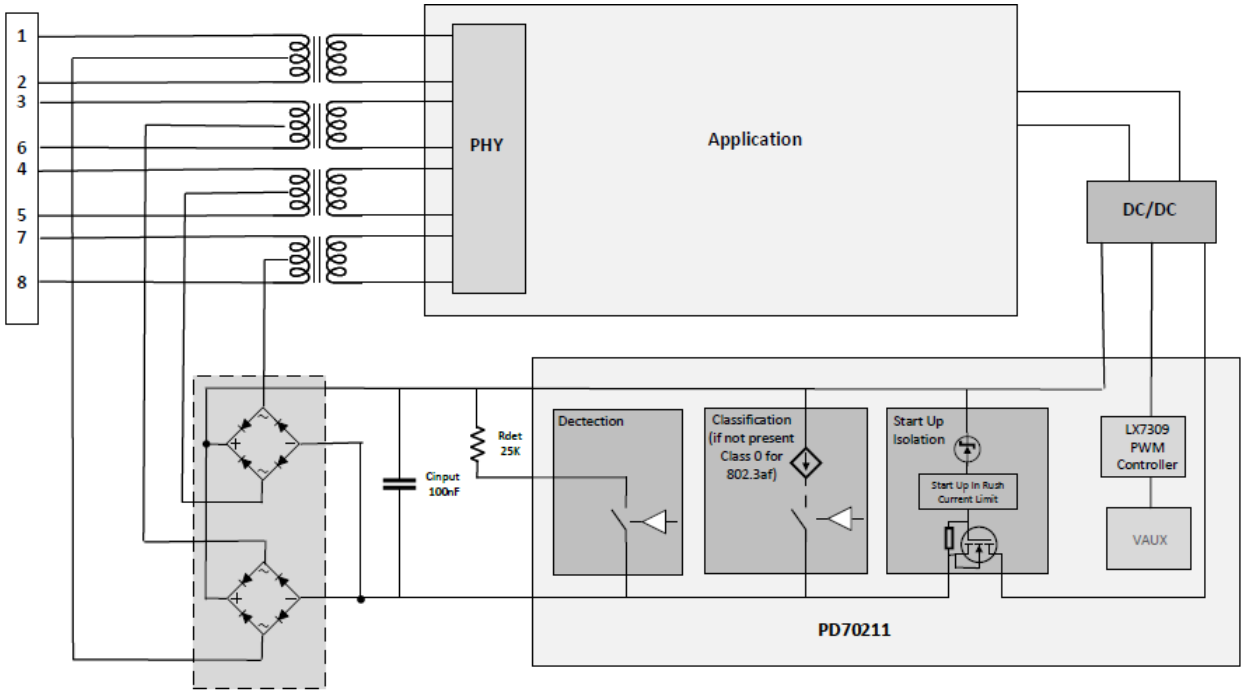
The following figure shows a basic PD block diagram using PD70211.

Figure 1. Basic PD Block Diagram



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1. Functional Descriptions

The following figures show the functional blocks of the PD70211 device.

Figure 1-1. PD70211 Block Diagram (Front-End Section)

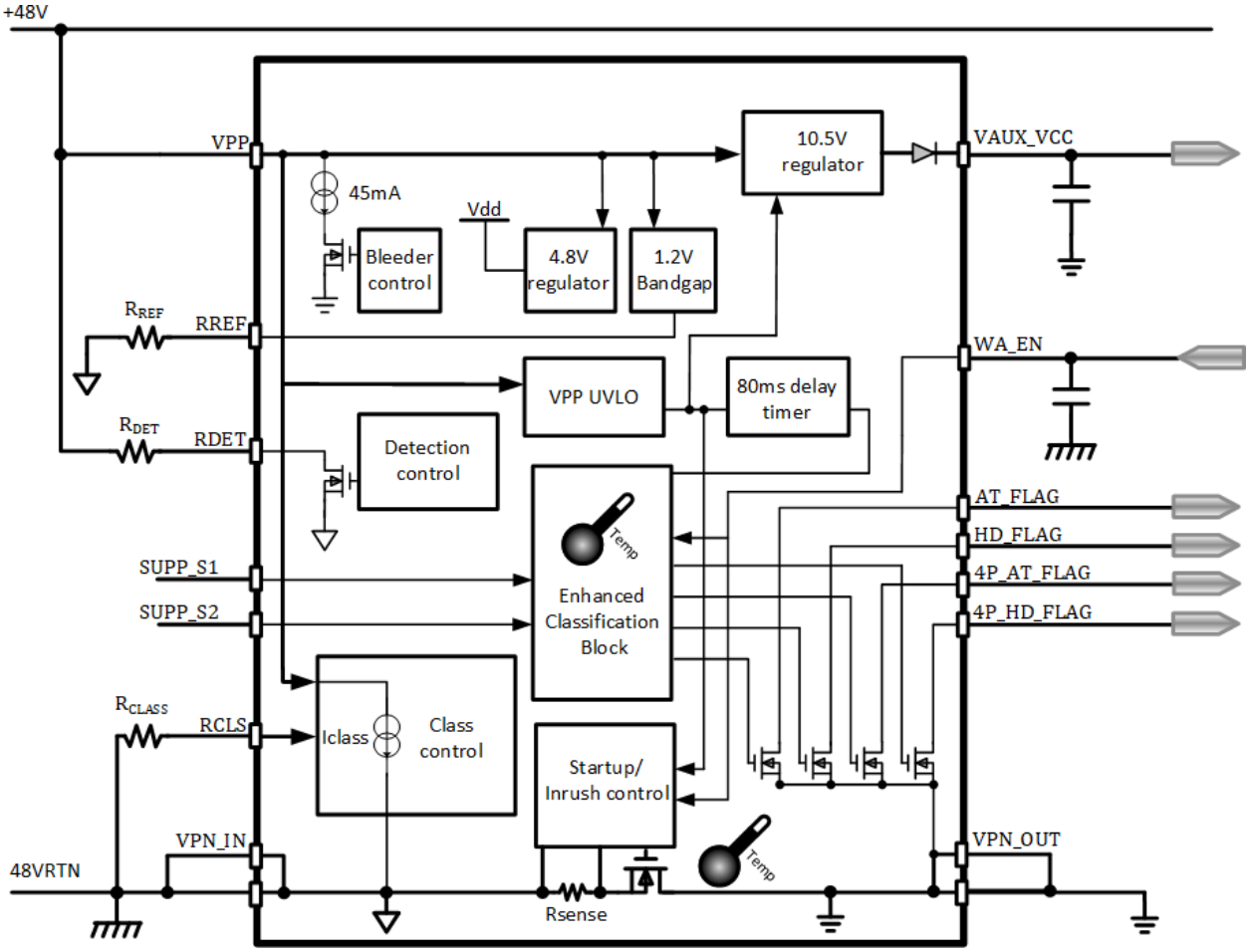
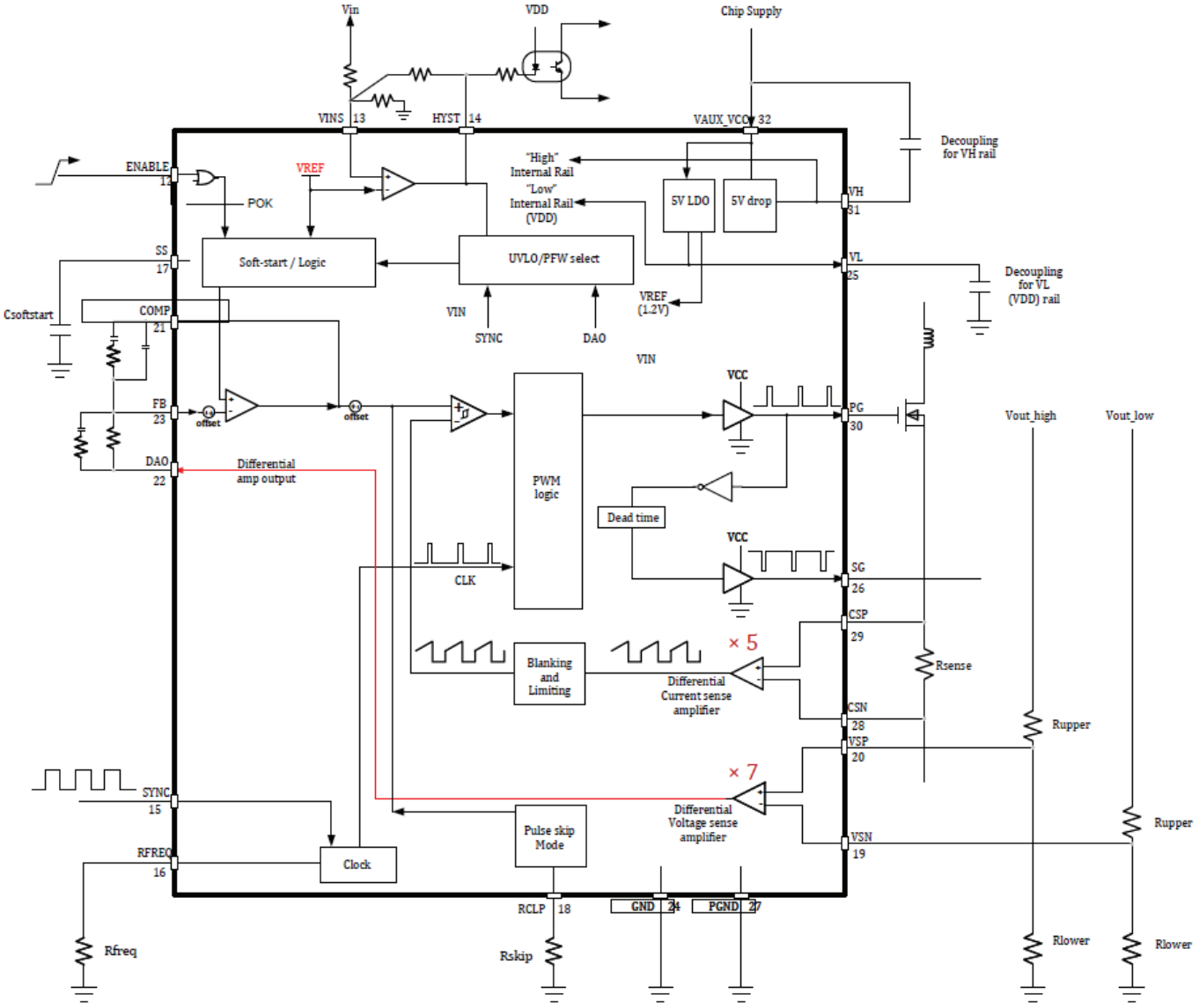


Figure 1-2. PD70211 Block Diagram (PWM Section)



2. Electrical Specifications

The following sections describe the electrical specifications of the PD70211 device.

2.1 Absolute Maximum Ratings

Performance is not necessarily guaranteed over this entire range. These are maximum stress ratings only. Exceeding these ratings, even momentarily, can cause immediate damage or negatively impact long-term operating reliability. Voltages are with respect to IC ground (VPN_IN).

Table 2-1. Absolute Maximum Ratings[1]

Parameter		Min	Max	Units
VPP, VPN_OUT, RDET		–0.3	74	V
AT_FLAG, HD_FLAG, 4P_AT_FLAG, 4P_HD_FLAG		–0.3	20	V
SUPP_S1, SUPP_S2		0	V_{VPP} + 1.5	V
RREF, RCLS, WA_EN		–0.3	5	V
VAUX_VCC		–0.3	20	V
PG, SG		–0.3	20	V
VL		–0.3	6	V
VH (with respect to VAUX_VCC)		0.3	–6	V
ENABLE				
All other pins		–0.3	VL + 0.3	V
Junction temperature		–40	150	°C
Lead soldering temperature (40 s, reflow)		—	260	°C
Storage temperature, MSL3		–65	150	°C
ESD rating	HBM	—	±1.5[1]	kV
	MM	—	±50	V
	CDM	—	±500	V

Note:

1. The VPP, VAUX/VCC, and RREF pins pass ±1 kV HBM only.

2.2 Operating Ratings

Performance is generally guaranteed over this range, as detailed in the 2.4.1 Electrical Characteristics of Front-End Section. Voltages are with respect to IC ground (VPN_IN).

Table 2-2. Operating Ratings of Front-End Section

Parameter	Min	Max	Units
VPP	0	57	V
Ambient temperature[1]	–40	85	°C
Detection range	1.1	10.1	V
Mark event range	4.9	10.1	V
Class event range	13.7	20.9	V

Note:

1. The corresponding maximum operating junction temperature is 125 °C.

Performance is generally guaranteed over the range, as detailed in the 2.4.2 Electrical Characteristics of PWM Section. Voltages are with respect to IC ground.

Table 2-3. Operating Ratings of PWM Section

Parameter	Min	Max	Units
VCC	7.8	20	V
F_{SW} (Adjustable Frequency Range)	100	500	kHz
Maximum duty cycle	—	44.5	%
f_{sw_synch} (Synchronization Frequency Range)	200	1000	kHz

2.3 Thermal Properties

The following table lists the thermal specifications of the PD70211 device.

Table 2-4. Thermal Properties

Thermal Resistance	Min	Typ	Max	Units
θ_{JA}	—	22.3	—	°C/W
θ_{JP}	—	3	—	°C/W
θ_{JC}	—	4	—	°C/W

Note: The θJx numbers assume no forced airflow. Junction temperature is calculated using $T_J = T_A + (P_D \times q_{jA})$. In particular, θ_{JA} is a function of the PCB construction. Published thermal resistance is for a four-layer board in accordance with the JESD-51 (JEDEC) standards.

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2.4 Electrical Characteristics

This section describes the electrical characteristics of the front-end and PWM sections, thermal protection mechanism against excessive internal temperature, and wall adapter mode functionality.

2.4.1 Electrical Characteristics of Front-End Section

Unless otherwise specified under conditions, the minimum and maximum ratings stated in the following table apply over the entire specified operating ratings of the PD70211 device. Typical values are determined either by design or by production testing at 25 °C ambient temperature. Voltages are with respect to IC ground (VPN_IN).

Table 2-5. Typical Electrical Performance

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Input Voltage						
I_{IN}	IC input current with I_{CLASS} off	VPP = 55 V	—	1	3	mA
Detection Phase						
V_{DET}	Detection range	—	1.1	—	10.1	V
R_{DET_TH}	R_{DET} disconnect threshold	—	10.1	—	12.8	V
$R_{DS\_DET\_ON}$	ON-Resistance of internal FET during detection	—	—	—	50	Ω
$R_{DS\_DET\_OFF}$	OFF-Resistance of internal FET after detection	—	2	—	—	MΩ
I_{OFFSET_DET}	Input offset current	1.1 V ≤ VPP ≤ 10.1 V, T_J ≤ 85 °C	—	—	5	µA
$V_{R\_DET\_ON}$	Threshold when VPP goes low	—	2.8	3.0	4.85	V
Classification Phase						
V_{CLS_ON}	Classification sink turn-ON threshold	—	11.4	—	13.7	V
V_{CLS_OFF}	Classification sink turn-OFF threshold	—	20.9	—	23.9	V
$V_{HYS\_CLS\_ON}$	Hysteresis of VCLS_ON threshold	—	—	1	—	V
V_{MARK_TH}	Mark detection threshold (VPP falling)	—	10.1	—	11.4	V
I_{MARK}	Current sink in the mark event region	—	0.25	—	4	mA
I_{CLASS_CLIM}	Current limit of class current	—	50	68	80	mA

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Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CLASS}	Classification current sink	R_{CLASS} = not present (class 0)	—	—	3	mA
		R_{CLASS} = 133 Ω (class 1)	9.5	10.5	11.5	mA
		R_{CLASS} = 69.8 Ω (class 2)	17.5	18.5	19.5	mA
		R_{CLASS} = 45.3 Ω (class 3)	26.5	28.0	29.5	mA
		R_{CLASS} = 30.9 Ω (class 4)	38.0	40.0	42.0	mA
Isolation FET						
R_{DSON}	ON resistence	Total resistance between VPN_IN to VPN_OUT; I_{LOAD} < 600 mA, –40 ºC < T_A < 85 ºC	—	—	0.3	Ω
I_{CLIM_INRUSH}	Inrush current limit	—	105	240	325	mA
OCP	Overcurrent protection	—	2.2	—	—	A
ILOAD	Continuous operation load	—	—	—	2	A
Undervoltage Lockout						
$UVLO_{ON}$	Threshold that marks start of inrush phase	—	36	—	42	V
$UVLO_{OFF}$	Threshold where pass- FET turns OFF as VPP collapses	—	30.5	—	34.5	V
DC-DC Input Cap Discharger						
I_{CAP_DIS}	Discharge current	7 V ≤ VPP ≤ 30 V	22.8	—	60	mA
t_{dis}	Discharge time	C_{DC_DC} ≤ 264 µF (by design, not tested)	—	—	500	ms
$timer_{dis}$	Discharge timer	Time for which discharge circuit is activated	430	—	—	ms
References, Rails, and Logic						
V_{AUX}	Auxiliary voltage	0 mA < I_{AUX} < 4 mA	9.8	10.5	12.0	V
I_{AUX}	Maximum continuous current from V_{AUX}	—	4	—	—	mA
I_{AUX}	Auxiliary current limit	—	10	—	32	mA
V_{REF}	Bandgap reference voltage	—	1.17	1.2	1.23	V
t_{FLAG_LO}	Low level flag	For AT_FLAG, HD_FLAG, 4P_AT_FLAG, 4P_HD_FLAG, I_{FLAG} = 3 mA	—	—	0.4	V
I_{FLAG}	Flag current driving capability	For AT_FLAG, HD_FLAG, 4P_AT_FLAG, 4P_HD_FLAG	5	—	—	mA

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Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
t_{FLAG}	Delay timer between start of inrush and flags declared	For AT_FLAG, HD_FLAG, 4P_AT_FLAG, 4P_HD_FLAG	80	—	—	ms
V_{SUPP_HI}	SUPP_Sx high voltage threshold	For SUPP_S1 and SUPP_S2	25	—	35	V
Wall Adapter						
V_{IH}	Input high logic	—	2.4	—	—	V
V_{IL}	Input low logic	—	—	—	0.8	V

Table 2-6. Truth Table for Status of Flags

Number of Fingers "N" (N-Event classification)	SUPP_S1	SUPP_S2	AT_FLAG	HD_FLAG	4P_AT_FLAG	4P_HD_FLAG
1	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z
2	H	L	0V	Hi-Z	Hi-Z	Hi-Z
2	L	H	0V	Hi-Z	Hi-Z	Hi-Z
2	H	H	0V	Hi-Z	0V	Hi-Z
3	L	H	0V	0V	Hi-Z	Hi-Z
3	H	L	0V	0V	Hi-Z	Hi-Z
3	H	H	0V	0V	0V	Hi-Z
4	X	X	0V	0V	0V	Hi-Z
5	Reserved for future					
6	X	X	0V	0V	0V	0V

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2.4.2 Electrical Characteristics of PWM Section

Unless otherwise specified under conditions, the minimum and maximum ratings listed in the following table apply over the entire specified operating ratings of the PD70211 device. Typical values stated, are determined either by design or by production testing at 25 °C ambient. Voltages are with respect to IC ground (VPN_IN).

Table 2-7. Typical Electrical Performance

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Input Voltage Current						
$V_{CC\_UVLO\_UP}$	UVLO threshold with input rising	V_{CC} rise time ≥ 0.5 ms	8.85	9.15	9.5	V
$V_{CC\_UVLO\_DN}$	UVLO threshold with input falling	V_{CC} rise time ≥ 0.5 ms	7	7.3	7.6	V
I_{VCC_SD}	IC input current (no switching)	V_{ENABLE} = Low, or $V_{VCC} < V_{CC\_UVLO\_UP}$	—	1	2000	µA
I_{VCC_Q}	IC input current (switching, no load on SG, PG, VDD)	V_{ENABLE} = High, and $V_{VCC} > V_{CC\_UVLO\_UP}$, f_{SW} = 500 kHz	—	—	3	mA
Input UVLO/PFW						
V_{INS_TH}	Threshold on VINS pin	Rising or falling	1.171	1.200	1.229	V
V_{HYST_HIGH}	Hysteresis pin high voltage	$I_{HYST\_SOURCING}$ = 1 mA	2.8	—	—	V
V_{HYST_LOW}	Hysteresis pin low voltage	$I_{HYST\_SINKING}$ = 3 mA	—	—	0.4	V
LDOs						
VL	—	I_{VDD_EXT} < 5 mA (current out of pin)	4.75	5	5.25	V
VH	VH rail (with respect to V_{CC})	—	—	–5	—	V
Soft Start						
I_{SS_CH}	Current out of SS pin during charging phase	RFREQ = 33.3 kΩ, V_{SS} = 0.5 V	32	36	40	µA
I_{SS_DISCH}	Current into SS pin during discharging phase	RFREQ = 33.3 kΩ, V_{SS} = 0.5 V	—	10	—	% of I_{SS_CH}
V_{SS_CH}	Soft start charge completed threshold	By design only	90	—	95	% of VREF
V_{SS_DISCH}	Soft start discharge completed threshold	—	—	50	—	mV
R_{SS_DISCH}	Soft-start pin discharge FET resistance	—	—	50	—	Ω

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Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{DISCH}	Soft-start discharge FET on-time	—	—	32	—	Switch cycles
Switching Frequency and Synchronization						
f_{sw_range}	Switching frequency accuracy	RFREQ = 33.2 kΩ	285	315	345	kHz
f_{sync_max}	Maximum synchronization frequency	—	1	—	—	MHz
V_{SYNC_HI}	SYNC pin high threshold	—	2.4	—	—	V
V_{SYNC_LO}	SYNC pin low threshold	—	—	—	0.8	V
t_{sync}	Minimum pulse width of SYNC pulse	—	100	—	—	ns
D_{sync_max}	Maximum SYNC pulse duty cycle	—	—	—	90	%
Error Amplifier						
VREF	Reference voltage	—	1.171	1.200	1.229	V
$Gain_{DC\_OPL}$	DC open-loop gain	Rload = 100 kΩ	70	100	—	dB
AV_{UGBW}	Unity gain bandwidth	Cload = 10 pF (By design only)	2	5	—	MHz
I_{COMP_OUT}	Output sourcing current	0.2 V ≤ V_{COMP} ≤ 1.3 V	110	—	620	µA
I_{COMP_IN}	Output sinking current	0.2 V ≤ V_{COMP} ≤ 1.3 V	145	—	495	µA
$V_{EA\_CMR\_MAX}$	Maximum of input common-mode range	—	2	—	—	V
V_{CLAMP}	COMP pin high clamp	—	1.8	2.1	2.6	V
PWM Comparator						
V_{OFFSET}	Inserted offset in inverted input	—	200	—	300	mV
V_{RCLP}	Voltage set on RCLP pin by external resistor to GND	—	0	—	1	V
Current Sense Amplifier						
$Gain_{CSA}$	DC Gain	0 mA < I_{AUX} < 4 mA	4.75	5	5.25	V
I_{AUX}	Maximum continuous current from V_{AUX}	—	4	—	—	mA
$V_{CSA\_CMR\_MAX}$	Maximum input common-mode range	—	2	—	—	V

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Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{BLANK}	Blanking time	—	50	—	100	ns
V_{ILIM}	Current limit threshold on output of current sense amplifier	Where PWM pulses start to get truncated	1.1	1.2	1.3	V
$V_{ILIMHICCUP}$	Current limit threshold on output of current sense amplifier capability	Where PWM pulses start to get omitted in hiccup mode	1.7	1.8	1.9	V
Differential Voltage Amplifier						
$Gain_{DA}$	DC gain of differential voltage amplifier	—	6.68	7.0	7.14	V
A_{VUGBW_DA}	Unity gain bandwidth of differential voltage amplifier	—	—	5	—	MHz
$V_{DA\_CMR\_MAX}$	Maximum of input common-mode range	—	3.5	—	—	V
Drivers						
R_{PG_HI}	Drive resistance when PG is high	—	—	10	—	Ω
R_{PG_LO}	Drive resistance when PG is low	—	—	5	—	Ω
t_{PG_MIN}	Minimum on-time of PG	—	—	—	120	ns
D_{MAX}	PG maximum duty cycle	—	44.5	—	50	%
R_{SG_HI}	Drive resistance when SG is high	—	—	10	—	Ω
R_{SG_LO}	Drive resistance when SG is low	—	—	10	—	Ω
t_{DEAD}	Deadtime	—	60	110	190	ns
Logic Levels on VINS and ENABLE						
V_{HI}	Input high threshold	—	2	—	—	V
V_{LO}	Input low threshold	—	—	—	0.8	V
Thermal Protection						
T_{SD}	Thermal shutdown (rising)	—	—	157	—	°C
T_{HYST}	Thermal shutdown hysteresis	—	—	15	30	°C

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2.4.3 Thermal Protection

The PD70211 device is protected from the excessive internal temperatures that might occur during various operating procedures. The following two temperature sensors are located on the chip monitor temperatures.

- Isolating switch (pass-FET)
- Classification current sink

Each of the given temperature sensors activates a protection mechanism that disconnects the Isolation (pass) FET or the classification circuit, respectively. This action protects the device from being permanently damaged or even from long-term degradation.

2.4.4 Wall Adapter Mode

The PD70211 device supports wall adapter functionality. That is, by setting WA_EN pin high, it gives priority to the wall adapter jack to supply the load.

The WA_EN pin is used while connecting a wall adapter voltage between VPP and VPN_OUT by means of an OR-ing diode.

While WA_EN, the wall adapter enable pin, is held low (referenced to VPN_IN), the front-end works as a normal PD.

When WA_EN pin is raised high (referenced to VPN_IN), the following three internal operations are forced:

- The Isolation FET is turned OFF.
- All output flags, like AT_FLAG, HD_FLAG, 4P_AT_FLAG, and 4P_HD_FLAG are activated (low state).
- V_{AUX} output voltage is turned ON.

While activating the WA_EN pin, the wall adapter supplies the input voltage for the DC-DC converter. Having WA_EN pin at high state does not disable detection and classification modes.

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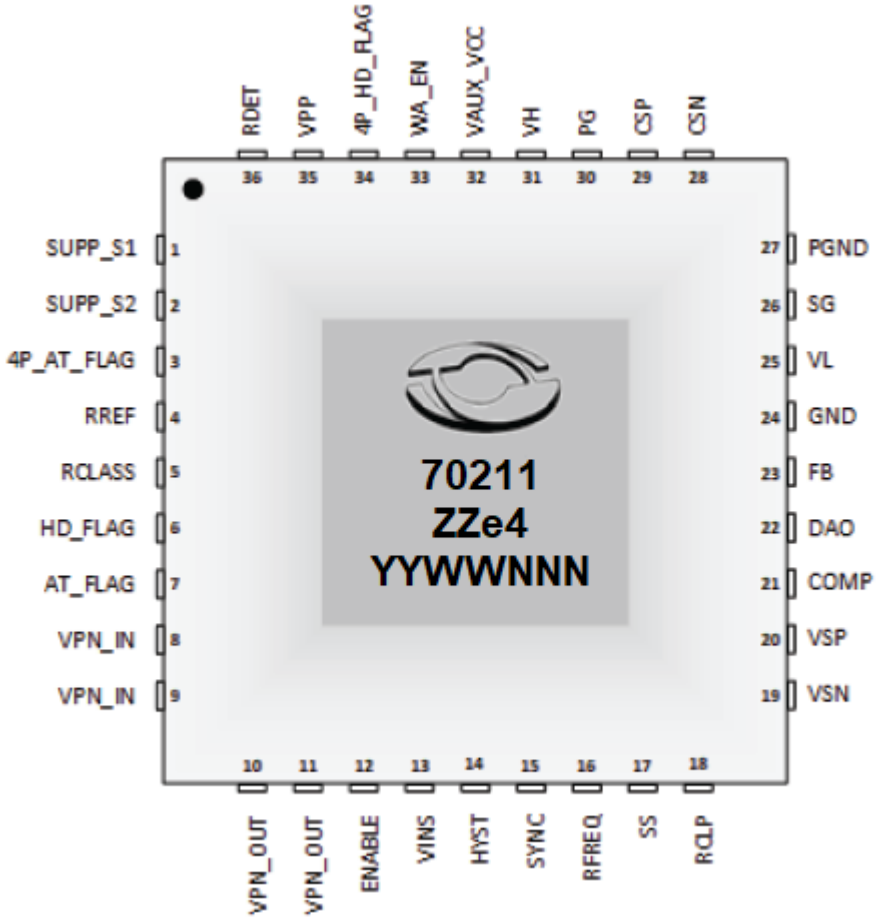
3. Pin Configuration

The following figure shows the device pin diagram from the top-view.

Figure 3-1. PD70211 Pinout



The following table lists the pin descriptions of the PD70211 device.

Table 3-1. Pin Descriptions

Pin Number	Designator	Description
1	SUPP_S1	Input pin for sensing the voltage on the diode bridge connected to the data pairs. This pin along with the SUPP_S2 pin can be used to distinguish between 2-pair and 4-pair operation. (For PSEs that operate in 4 pairs but generates the classification procedure on only one pair and not on both pairs). Signal is referenced to VPN_IN. Place a 10 kΩ resistor in the input of this pin.
2	SUPP_S2	Input pin for sensing the voltage on the diode bridge connected to the data pairs. This pin along with the SUPP_S1 pin can be used to distinguish between 2-pair and 4-pair operation. (For PSEs that operate in 4 pairs but generates the classification procedure on only one pair and not on both pairs). Signal is referenced to VPN_IN. Place a 10 kΩ resistor in the input of this pin.

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Pin Number	Designator	Description
3	4P_AT_FLAG	Open drain output. The pin gets actively pulled low when a 4-pair version of a (non-standard) Type 2 PD-PSE mutually identify each other via classification. There is a minimum 80 ms delay from the moment when the input capacitor is fully charged to this signal activity. Signal is referenced to VPN_OUT.
4	RREF	Bias current resistor. A 60.4 kΩ, 1% resistor is connected between RREF and IC ground (VPN_IN).
5	RCLASS	Sets the Class of the PD. Connect RCLASS (programming resistor) between this pin and IC ground (VPN_IN). Allowed values are 133 Ω, 69.8 Ω, 45.3 Ω, and 30.9 Ω for Class 1, 2, 3, and 4 respectively. If RCLASS is not present, the PD draws up to 3 mA during classification, therefore, indicating Class 0 (default Type 1) to the PSE. Signal is referenced to VPN_IN.
6	HD_FLAG	Open drain output. The pin gets actively pulled low when a 2-pair HDBaseT PD-PSE mutually identify each other through classification. There is a minimum of 80 ms delay from the moment when the input capacitor is fully charged to this signal activity. Signal is referenced to VPN_OUT.
7	AT_FLAG	Open drain output. This pin gets actively pulled low when a Type 2 PD-PSE mutually identifies each other through classification. There is a minimum of 80 ms delay from the moment when the input capacitor is fully charged to this signal activity. Signal is referenced to VPN_OUT.
8, 9	VPN_IN	Lower rail of the incoming PSE voltage rail—from the negative terminal of the two OR-ed bridge rectifiers (the corresponding upper PoE rail is VPP).
10, 11	VPN_OUT	This is in effect, the switched ground for establishing continuity to the PWM section after successful detection, classification, and power-up. It is connected to the power ground and PWM controller IC's ground plane of the DC-DC converter section.
12	ENABLE	A logic-level input to enable the converter. It can be pulled up constantly, for example, with a 100 kΩ resistor to VDD, to forcibly enable the converter, provided the input supply has exceeded any applicable UVLO thresholds as set on the VINS pin or on the VCC pin. Internally, the ENABLE pin goes to the input of an OR-gate, the other input terminal of which is tied to "POK"—a signal provided by the front-end. If the ENABLE pin is forced high, the output of the OR-gate goes high and the converter is allowed to start (provided all UVLO's are past). If the ENABLE pin is held low, the internal node "POK" goes active/high when the PD's front-end conducts (power OK), so the OR-gate goes high once again. In this case, the switching converter turns ON as required by the PoE standard. However, for supporting wall adapters, injecting power after the front-end (at the input of the converter), the converter can be turned ON forcefully, without the front-end signaling "PGOOD", by not tying the ENABLE pin low, but by tying it high (to VDD). That turns ON the converter irrespective of the state of the front-end (conducting or not), and whether there is any incoming PoE power or not.

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Pin Number	Designator	Description
13	VINS	The VINS pin is a programmable UVLO pin. The converter turns ON provided the voltage on the VINS pin is above 1.2 V (and VCC is not in UVLO, and ENABLE pin is also high—connected to VDD, for example). The converter stops switching (turns OFF) when the voltage on the VINS pin falls below 1.2 V (or if ENABLE is taken low, or if VCC falls outside its operating range). Thus, by connecting a voltage divider between input rail and IC ground, the UVLO threshold to enable switching can be set. However, to have a smooth startup, it is advisable to have some hysteresis too, by means of a resistor between VINS and HYST as explained in pin 14.
14	HYST	This is the output of the UVLO comparator as shown in the Figure 1-2. PD70211 Block Diagram (PWM Section) "hysteresis resistor" from HYST pin must be connected to VINS pin to create positive feedback (and hysteresis). Initially, as the input voltage is rising, the VINS pin voltage is below 1.2 V and so the output of the UVLO comparator is low, leading the hysteresis resistor to fall in parallel to the lower resistor of the UVLO divider placed at the VINS pin, assisting it to pull down the VINS pin voltage further. As soon as the rising UVLO threshold is exceeded (VINS > 1.2 V), the output of the UVLO comparator suddenly goes high (up to VDD) and the hysteresis resistor, effectively comes partially across the upper resistor of the UVLO divider, assisting it in to pull up the voltage on the VINS pin. This feedback, therefore, increases the voltage on the VINS pin. Now, the input rail has to fall to a much lower level to allow the VINS pin voltage to fall below 1.2 V. That is how hysteresis is created by positive feedback action through the hysteresis resistor. The exact math is shown in the 5. Applications Information section. Note that the HYST pin always toggles between high or low depending on whether the voltage on the VINS pin is above or below 1.2 V, respectively. This can always be used to indicate when the input rail is above the programmed rising threshold and when it falls below the programmed falling threshold.
15	SYNC	Synchronizes the LX7309 to a frequency higher than its default value as set on R_{FREQ} pin. The synchronizing clock must be 2x the desired sync frequency, with a maximum synchronizing clock frequency of 1 MHz (for 500 kHz PWM frequency). The PG pin's rising edge occurs at the same instant as the rising edge of the clock being applied on the SYNC pin.
16	RFREQ	Connect a programming resistor from this pin to IC ground (pin GND) to set the switching frequency. A typical value of the programming resistor is 49.9 kΩ, and this value provides a frequency of 215 kHz. Halving it roughly doubles the frequency, whereas doubling it halves the frequency. Note that the converter is designed to operate from 100 kHz to 500 kHz based on this pin. Switching frequency equation: $Freq = \frac{1}{(90pF \times R_{FREQ}) + 150ns}$ where Freq is [Hz] and R_{FREQ} is in [Ω] For more information, see the 5.2 Setting Switching Frequency section.

.....continued

Pin Number	Designator	Description
17	SS	This is the soft-start pin. Typically, a 0.1 µF capacitor, the “soft-start capacitor”, is connected between this pin and IC ground (pin GND). The capacitor gets charged up to 1.2 V by an internal resistor, and the voltage on the capacitor, in effect, forms the input voltage reference V_{REF} of the error amplifier. But, note that this capacitor serves other functions too; for example, it controls the rate of hiccupping under overcurrent fault conditions. Therefore, even if the internal reference is not being used (as in isolated topologies with a TL431 on the secondary side), the soft-start capacitor is recommended to be in place always. The actual capacitor used is determined by the application. For more information, see the 5.3 Setting Soft-Start section.
18	RCLP	Low power clamp resistor. A resistor can be connected from this pin to IC ground (pin GND) to set the exact level at which pulse-skipping mode is entered at light loads. However, the usual default is to connect this pin directly to IC ground, in which case pulse-skipping mode is disabled. The method to select the threshold (and RCLP resistor value) is described in the 5. Applications Information section.
19	VSN	The negative input of the internal differential-sense voltage amplifier. Note that the common-mode range of the differential voltage amplifier is 3.5 V and its gain is 7. This differential amplifier can be used for implementing topologies where the “system (output) ground” is different from the IC ground. Both output rails (output rail and its return) can then be step-downed, by equal amounts, using identical voltage dividers, to bring the voltage below 3.5 V. Then, differential sensing can be used, and finally the output of the differential voltage amplifier (pin DAO) can be connected to the FB pin.
20	VSP	The positive input of the internal differential-sense voltage amplifier. Note that it must always be connected in such a way that VSP is at a higher voltage than VSN. Also, keep in mind that since the differential voltage amplifier has a gain of 7 and the output of that amplifier is connected to the feedback pin, which compares that against a 1.2 V reference, in effect, the difference between VSP and VSN stabilizes to 1.2 V/7 = 0.171 V in steady state. That is how the (identical) voltage dividers present on VSP and VSN are designed.
21	COMP	This is the output of the internal error amplifier, and the input of the PWM comparator. It is brought out to support isolated topologies because in such cases, there is an error amplifier already present on the secondary side (for example, a TL431 or equivalent). Therefore, the error amplifier of the converter section can be passed. On the other hand, in non-isolated topologies, the error amplifier of the converter can be used directly or through the differential voltage amplifier stage.
22	DAO	This is the output of the internal differential voltage amplifier (gain = 7). When this amplifier is used, DAO is connected to the feedback pin (FB). Part of the compensation network is between the two pins, and this network is typical of any Type 3 error amplifier input, with or without a differential amplifier.
23	FB	This is the feedback pin of the IC. It is internally compared to a 1.2 V reference. If the internal error amplifier is not used and the COMP pin is being used to inject the error signal (as in isolated topologies), the FB pin can be either tied high (to VDD), or connected to COMP.

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.....continued

Pin Number	Designator	Description
24	GND	This is the IC ground or the analog (quiet) ground of the IC. Pin 20 is the Power Ground (PGND). Typically, the analog ground and PGND can be connected on a copper island on the component side, and then connect that through several vias very close to the chip on to a large ground plane which extends up to the lower side of the current sense resistor. All chip decoupling can then be very simple with respect to the copper island on the component side.
25	VL	This is created by an internal LDO and basically provides a housekeeping rail for the IC itself, which is 5 V with respect to the IC ground. A 1 µF ceramic cap placed close to this pin, connected to IC ground is recommended for proper decoupling. This pin can also provide up to 5 mA for external circuitry if required, thermal aspects (IC dissipation) being considered.
26	SG	Secondary gate driver. It drives a synchronous FET or an active clamp FET. It is derived from VCC (~12 V), and has a 10 Ω limiting resistor. Therefore, it can be used to drive a gate-drive transformer directly. It is usually complementary to the primary gate driver pin (PG). But, there is a typical 110 ns blanking time between the two to prevent cross-conduction. SG is held firmly low in pulse-skip mode (if allowed). It is also low during soft-start. It allows forced PWM (continuous conduction) mode by allowing negative inductor currents. It does not support diode-emulation mode (discontinuous conduction mode). However, in pulse-skip mode, as the SG stays OFF, the converter automatically lapses into discontinuous conduction mode through the body-diode of the synchronous FET. This pin can be left floating, if unused.
27	PGND	Power ground (for internal SG and PG drivers). This is ideal for VCC decoupling and the Primary-side current sense resistor's lower terminal. GND and PGND can be combined into a single large ground plane. Note that the power ground plane is firmly connected to VPN_OUT, which is the drain side of the PD's low-side pass-FET (it stands for Negative Port Voltage Out).
28	CSN	The negative input of the internal current-sense voltage amplifier. Note that the common-mode range of the differential current-sense amplifier is 2 V and its gain is 5. This is used for high-side current sensing up to 2 V. It is then placed on the (steady) output side of a Buck inductor, and the maximum output voltage is 1.8 V for using this type of sensing. Ensure that CSN is at a lower voltage compared to the positive input of the current-sense amplifier (CSP). Current sensing can also be implemented in a more basic fashion for "low-side" sensing, with a resistor in the return (ground) of the Buck. In that case, CSN is shown connected to IC ground. However, to avoid noise from ground bounce, it is best to route this on the PCB in Kelvin manner to the lower end of the sense resistor. This is important because the peak operating voltage on the sense resistor is only 200 mV and PCB-related noise can cause jitter in the switching waveform in current-mode control.
29	CSP	The positive input of the internal current-sense voltage amplifier. See description of pin 28 (CSN). Note that the output of the current-sense amplifier is amplified five times. Therefore, a 0.2 V current-sense voltage translates to a 1 V swing at the input of the PWM comparator. Higher voltages lead to hiccup mode protection.
30	PG	This stands for primary gate driver. It drives the main FET, and has a 5 Ω or 10 Ω limiting drive resistor switched between a voltage close to VCC rail and the IC ground. For guaranteeing proper shutdown during OFF time, it is necessary to add a 470 kΩ resistor from PG to VINS, as shown in Figure 1.

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.....continued

Pin Number	Designator	Description
31	VH	Internal rail of –5 V with respect to VCC, brought out only for decoupling purposes. Connect a 0.1 µF ceramic cap very close, from this pin to VAUX_VCC pin.
32	VAUX_VCC	Auxiliary voltage rail from front-end to the VCC (supply) input of the PWM section. The front-end provides a few mA of startup current for the PWM controller (at typically 10.5 V). Signal is referenced to VPN_OUT and is activated once front-end power up sequence ends. After initial startup of PWM section, a bias winding can be connected to this pin through a diode, to sustain the PWM section.
33	WA_EN	While this input is low (referenced to VPN_IN) the chip work according to internal flow diagram. When this input is high, it enable wall adapter feature. Place 100 nF to 1 uF/10 V capacitor from WA_EN to VPN_IN pins, locate it close to device. When WA_EN is not used, connect it to VPN_IN. For further information, see the Operation with an External DC Source section.
34	4P_HD_FLAG	Open drain output. The pin gets actively pulled low when a 4-pair HDBaseT PD-PSE mutually identify each other via classification. There is a minimum 80 ms delay from the moment that the input capacitor is fully charged to this signal activity. Signal is referenced to VPN_OUT.
35	VPP	Upper rail of the incoming PSE voltage rail—from the positive terminal of the two OR-ed bridge rectifiers (the corresponding lower PoE rail is VPN_IN).
36	RDET	Internally connects to VPN_IN during detection phase and disengages after it is over. A 25 kΩ (or 24.9 kΩ), 1% resistor is connected between this pin and VPP.
37	EPAD	Connected on PCB plane to VPN_IN.

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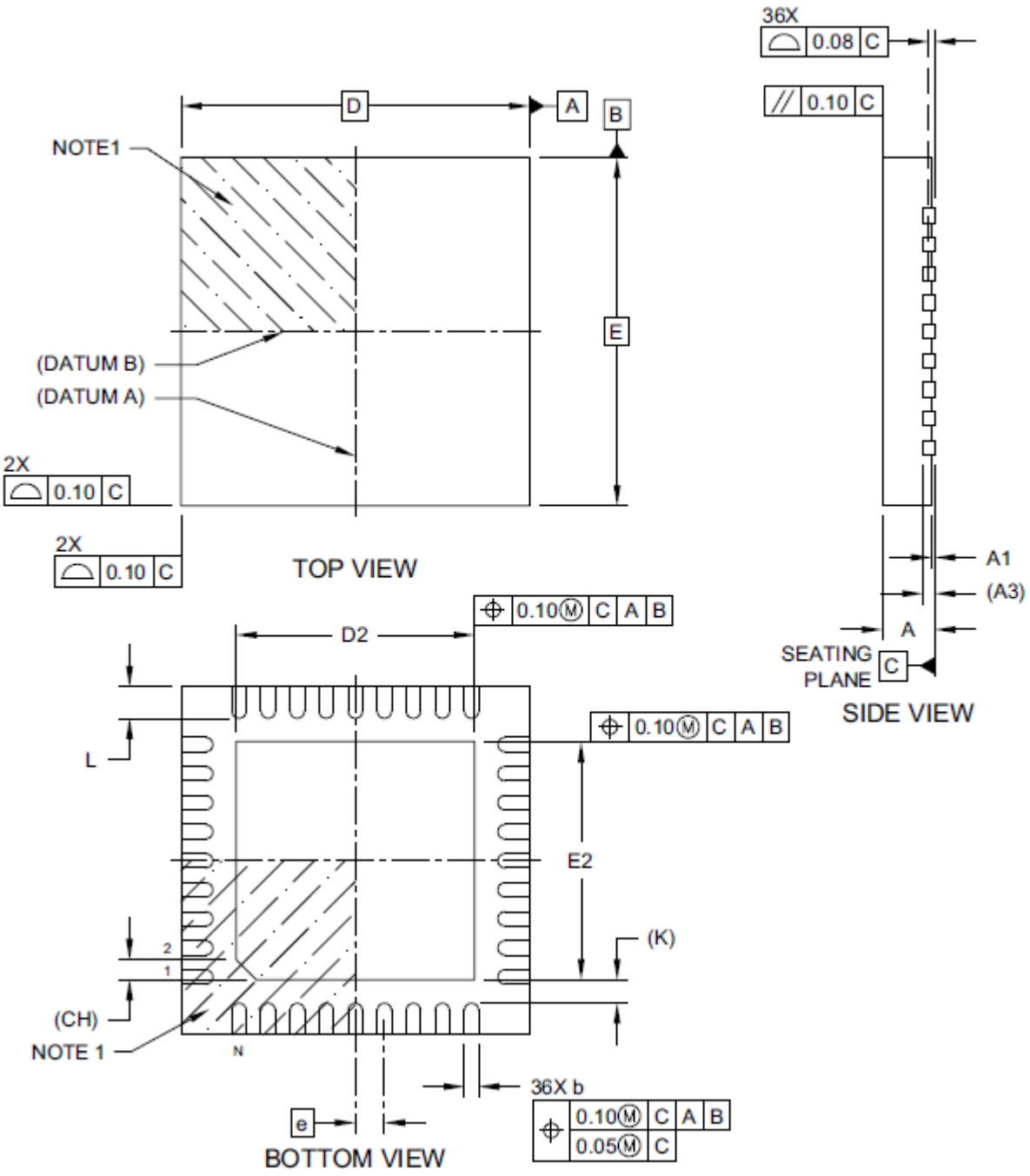
4. Package Specifications

The following figure shows a 6 mm × 6 mm, 36-pin QFN PD70211 package.

Figure 4-1. QFN Package



Note: Dimensions do not include protrusions; they must not exceed 0.155 mm (0.006″) on any side. Lead dimension does not include solder coverage.

Table 4-1. Package Dimensions[1, 2, 3, 4]

Units		Millimeters		
Dimension Limits		**Min.**	**Nom.**	**Max.**
Number of Terminals	N	36		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.20 REF		
Overall Length	D	6.00 BSC		
Exposed Pad Length	D2	4.00	4.10	4.20
Overall Width	E	6.00 BSC		
Exposed Pad Width	E2	4.00	4.10	4.20
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.45	0.55	0.65
Terminal-to-Exposed-Pad	K	0.40 REF		
Exposed Pad Index Chamfer	CH	0.35 REF		

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
   a. BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   b. REF: Reference Dimension, usually without tolerance, for information purposes only.
4. For the most current package drawings, please see the Microchip Packaging Specification located at www.microchip.com/packaging.

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4.1 Recommended PCB Layout

The following figures show the PD70211 PCB layout based on the IPC7093A October 2020 standard. All previously published footprints are still supported.

Figure 4-2. Solder Mask (Top View)

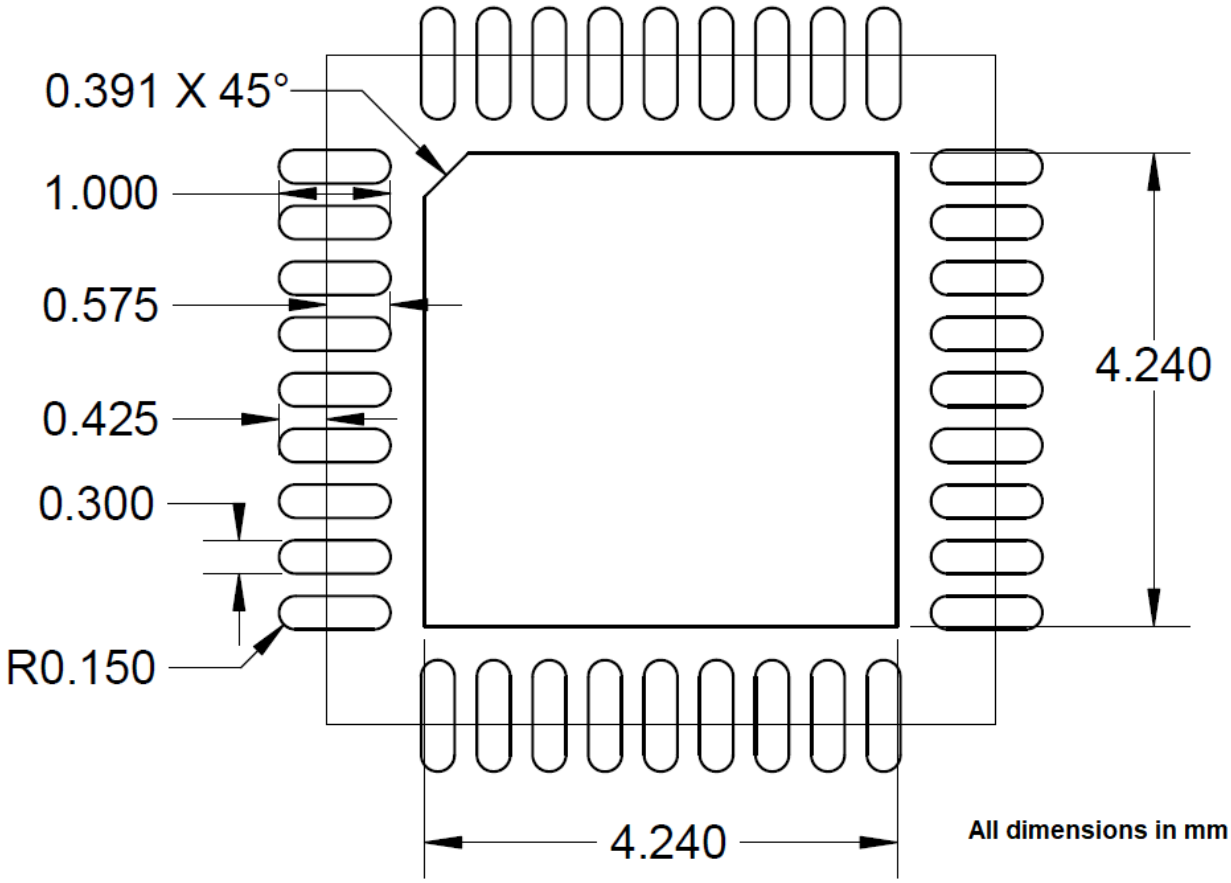


Figure 4-3. Copper Layer (Top View)

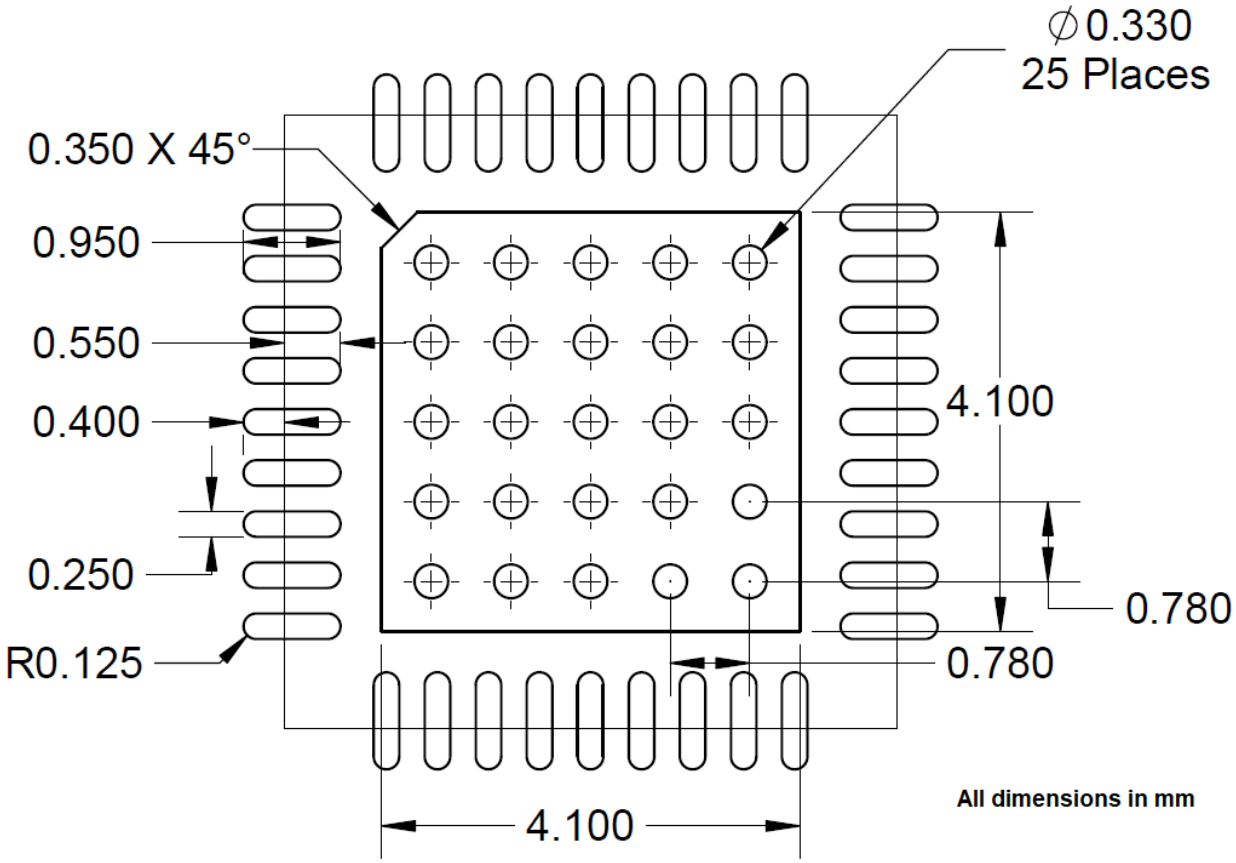
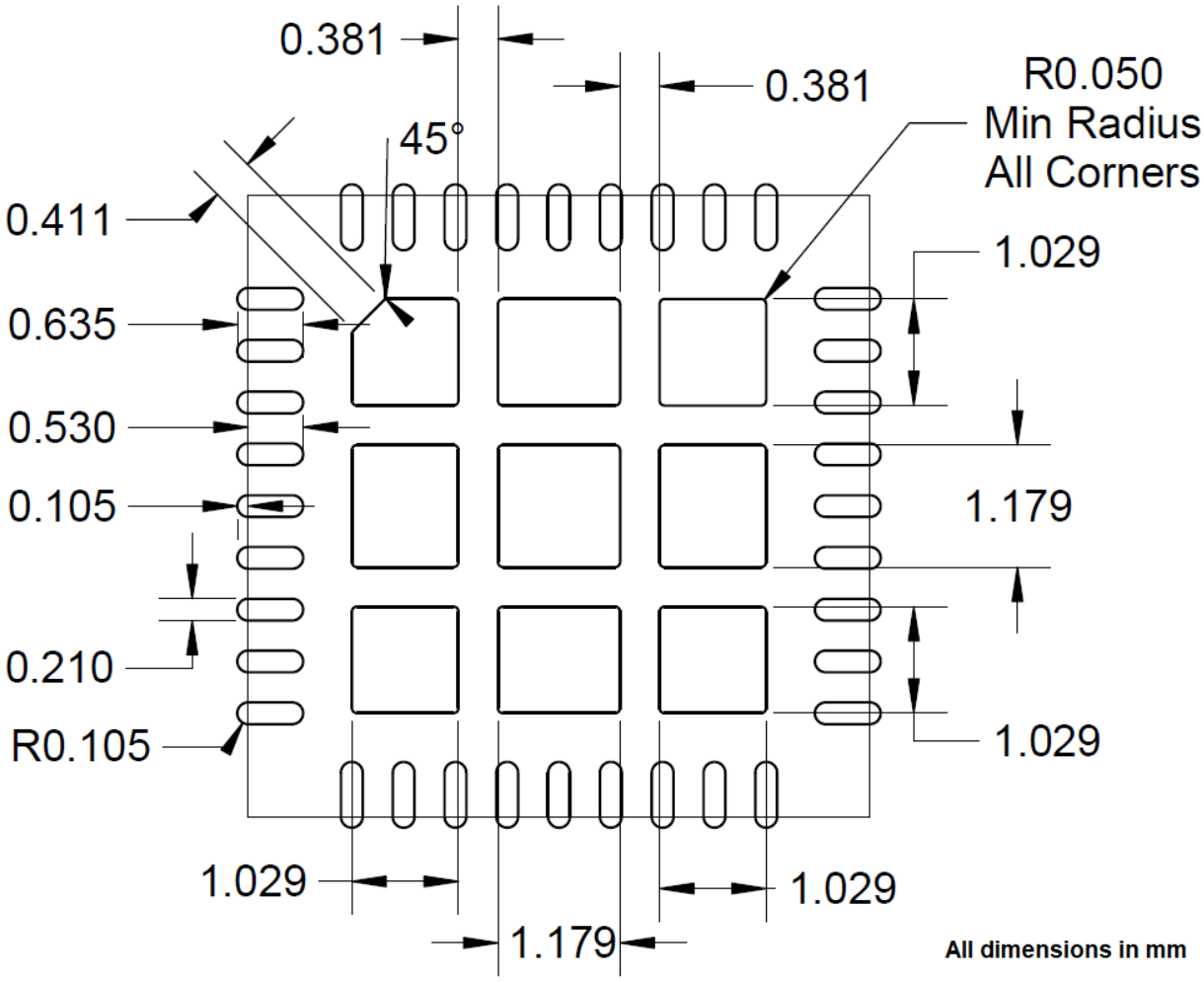
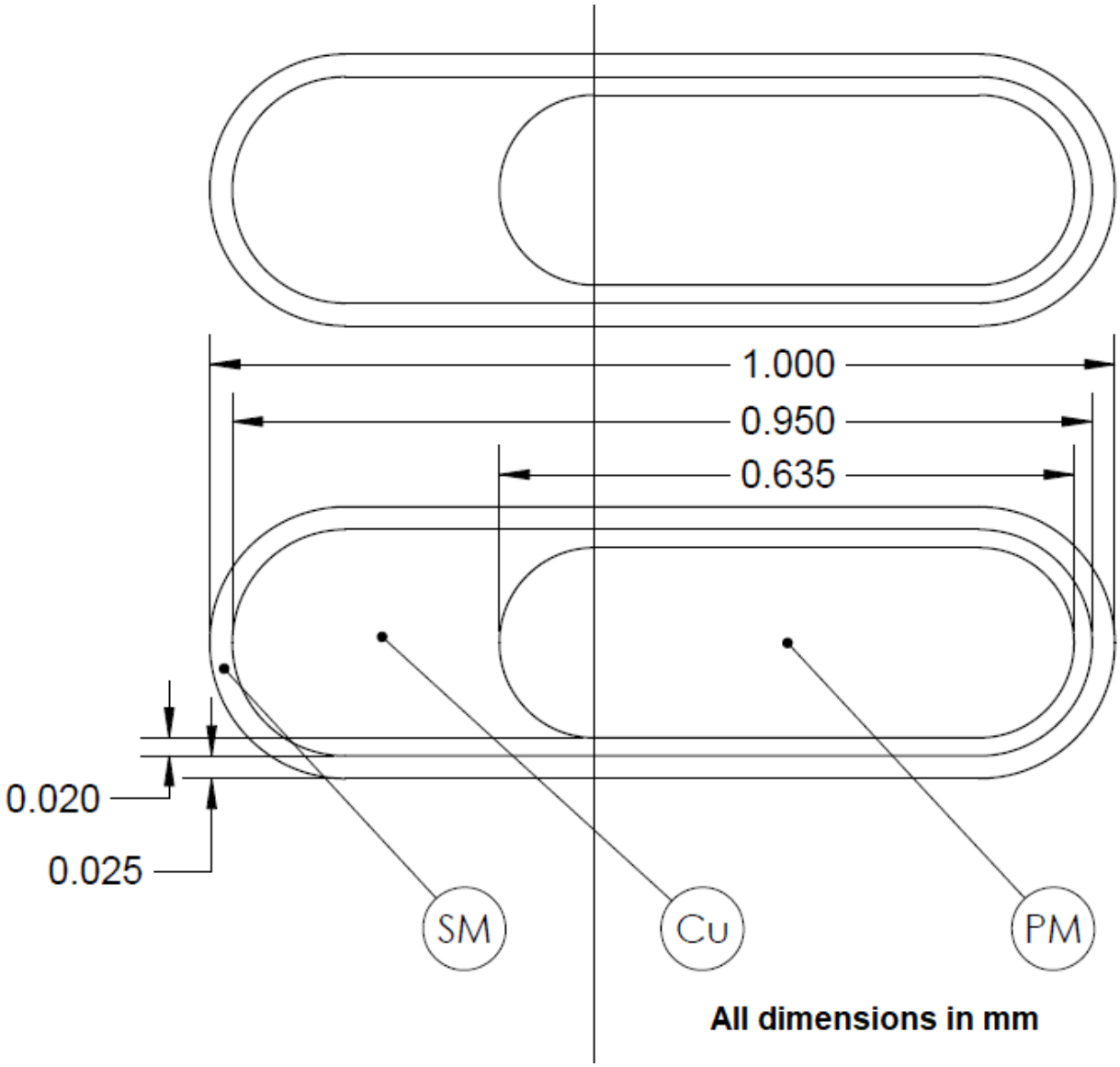


Figure 4-4. Paste Mask (Top View)



Note: Paste mask stencil is 5mil thick. All paste mask openings have a radius of 0.05 mm.

Figure 4-5. Pin Geometry



5. Applications Information

The following sections describe the PD70211 application.

5.1 Peripheral Devices

An 82 nF to 100 nF/100 V capacitor must be placed between device VPP and VPN_IN pins, and located as close as possible to the device.

A 58 V TVS must be placed between device VPP and VPN_IN pins for protection against voltage transients. For complete surge protection, see www.microchip.com/DS00003410B.

A 10 KΩ resistor must be placed on SUPP_S1 and SUPP_S2 lines between diode bridge and PD70211 device.

When WA_EN is used, a 100 nF to 1 uF/10V capacitor must be placed between WA_EN and VPN_IN pins close to PD70211 device. Consult Microchip Technology for optimized recommendation.

When not used, WA_EN must be connected to VPN_IN pin.

5.2 Setting Switching Frequency

The R_{FREQ} resistor is connected from R_{FREQ} pin to IC ground. Based on that, the following frequency is obtained:

$$Freq = \frac{1}{(90pF \times R_{FREQ}) + 150ns}$$

where, Freq is [Hz] and R_{FREQ} is Ω.

For example, by setting R_{FREQ} = 49900Ω:

$$Freq = \frac{1}{(90pF \times 49900\Omega) + 150ns} = \sim 215000Hz$$

Any frequency between 100 kHz to 500 kHz can be set.
Note: When synchronizing, the default frequency (as set by R_{FREQ}) must be lower than the synchronization clock. If the synchronization breaks, the converter lapses back to the default value. When synchronizing, the frequency can be increased to 1 MHz.

5.3 Setting Soft-Start

A capacitor is connected between SS pin and IC ground. The current charging of the capacitor is:

$$I_{SS\_CHG} = \frac{1.2V}{RFREQ} \text{ (in seconds)}$$

For example, if R_{FREQ} = 49.9k, then:

$$I_{SS\_CHG} = \frac{1.2V}{49.9 \times 10^3} \text{ (in Amperes)} = 2.4 \times 10^{-5} \Rightarrow 24\mu A$$

Therefore, charging a 0.1 µF ceramic cap on the SS pin from 0 V to 1.2 V takes:

$$t_{SS} = \frac{C \times \Delta V}{I_{SS\_CHG}} \text{ (in seconds)} = \frac{0.1\mu \times 1.2}{24\mu} \text{ (in seconds)} = \frac{0.12}{24} \text{ (in seconds)} = 5 \times 10^{-3} \text{(in seconds)} \Rightarrow 5ms$$

This is the soft-start time in this case.

5.4 Setting Pulse-Skip Mode Threshold

If an RCLP programming resistor is placed between RCLP pin and IC ground, the clamping voltage level is given by:

$$V_{CLP} = \frac{0.3 \times RCLP}{RFREQ} \text{ (in Volts)}$$

For example, if RCLP = R_{FREQ}, assuming that both are 49.9k, then the converter enters pulse skipping when the output of the current sense amplifier drops to 0.3 V.
Note: The gain with this current amplifier is 5.

Therefore, in terms of the voltage on the sense resistor (input of the current amplifier), 0.3 V/5 = 0.06 V. As the converter is usually designed in such a way that its peak is around 0.2 V (the peak of Rsense voltage before it starts to current limit), ratio of 0.06 V/0.2 V = 0.3 is obtained. In other words, the converter enters pulse-skipping when the output current is 30% of the maximum designed output current.

5.5 Setting UVLO/Hysteresis Thresholds

Note: A 470k resistor from PG pin to VINS pin is required for guaranteeing proper termination of gate drive pulse during UVLO.

For example, a divider is connected to input at the VINS pin, and resistors are called R_{UPPER} and R_{LOWER}. RHYST, a hysteresis resistor from the output of the UVLO comparator, which provides positive feedback on to the VINS pin, is also present, as explained in the 3. Pin Configuration section. When the input voltage is rising, in effect, the hysteresis resistor is in parallel to the lower resistor R_{LOWER}. When the voltage on the VINS pin rises above 1.2 V, the UVLO comparator flips and the hysteresis resistor appears connected to 5 V (output of the UVLO comparator). The equivalent configurations are shown in Figure 5-1. After solving the equations, the following example indicates the set thresholds. The values are as used in Figure 1-2.

$$R_{UPPER} = 270k; R_{LOWER} = 8.66k;\ R_{HYST} = 270k$$

Part 1: (VINS less than 1.2V)

Equivalent lower resistor is a parallel combination of R_{LOWER} and R_{HYST}

$$R_{LOWER\_EQUIV} = \frac{R_{LOWER} \times R_{HYST}}{R_{LOWER} + R_{HYST}} = \frac{8.66k \times 270k}{8.66k + 270k} = 8.391k$$

The rising voltage threshold is

$$V_{UVLO\_UP} = VREF \times \frac{R_{UPPER} + R_{LOWER\_EQUIV}}{R_{LOWER\_EQUIV}} = 1.2V \times \frac{270k + 8.391k}{8.391k} = 39.8V$$

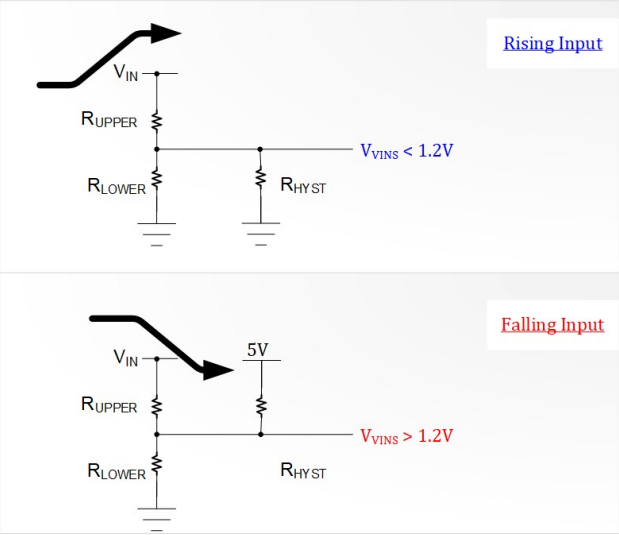
Part 2: (VINS greater than 1.2V)

$$V_{UVLO\_DN} = VREF \times \frac{R_{UPPER}}{R_{LOWER}} - (VDD - VREF) \times \frac{R_{UPPER}}{R_{HYST}} + VREF$$

$$1.2V \times \frac{270k}{8.66k} - (3.8V) \times \frac{270k}{270k} + 1.2 = 34.8V$$

Therefore, with the selected resistors, a rising threshold of 39.8 V and a falling threshold of 34.8 V is achieved.

Figure 5-1. Equivalent Diagrams for UVLO and Hysteresis



5.6 Setting the Voltage Divider for Output Rails

Generically, the equation is stated as:

$$V_{OUT} = V_X \times \frac{R_{UP} + R_{LOW}}{R_{LOW}}$$

Where, R_{UP} is the name given to the upper resistor (connected to output rail) and R_{LOW} is the name given to the resistor connected to lower rail (usually IC ground). However, with so many topologies, in effect the following three cases in all the typical schematics presented so far are present.

- Non-isolated topologies with simple divider connected directly to FB pin. For this, V_X = 1.2 V is used.
- Isolated topologies with divider to another reference (such as TL431 with an internal reference of 2.5 V). For this, V_X = 2.5 V is used.
- Non-isolated topologies with a differential divider connected to differential voltage amplifier of the LX7309. The same preceeding divider equation is used, but with V_X = 0.171 V (that is, 1.2 V divided by the gain of the differential amplifier 7). Two identical dividers are required.

5.7 Selecting the Sense Resistor

In a Buck topology, the center of the switch current ramp equals the output current. To that, about 30% for the "I_{PEAK+}" peak current must be added because of the rising ramp caused by the inductor. That is a factor of 1.3. Some headroom for proper transient response at maximum load must also be included. As the peak voltage on the sense resistor is 0.2 V, to leave headroom, it must be planned in such a way that the switch current peak stays at around 0.18 V at the most, at maximum load. This means the following:

$$R_{SENSE} = \frac{0.138}{5A} = 0.028\ \Omega$$

An adjust resistor must be placed in parallel (for example, the 22 Ω placeholder).

For a Forward converter (Buck with a transformer), instead of the I_{OR} load current as shown in the preceeding equation, the reflected load current of $I_{O/n}$ can be used, where n is the turns ratio (number of primary-side turns divided by number of secondary-side turns). The sense resistance must also be lowered further (by means of the adjust resistor), to account for the magnetization current component on the switch side.

Therefore, roughly:

$$R_{SENSE} \approx \frac{0.138}{I_O} \times \frac{N_P}{N_S} \text{ (Forward)}$$

For a Boost or Buck-Boost, account for the fact must be made that the peak current is not just 1.3 times of maximum load current, but it is actually:

$$I_{PEAK} = 1.3 \times \frac{I_O}{1-D} \text{ (where D can be as high as 44\%)}$$

Therefore, the following equation for sense resistor must be used.

$$R_{SENSE} = \frac{0.18 \times (1-D)}{1.3 \times I_O} = \frac{0.101}{1.3 \times I_O} = \frac{1}{13 \times I_O}$$

$$R_{SENSE} = \frac{0.077}{I_O} \text{ (Boost, Buck-Boost)}$$

For example, if the maximum load current is 5 A, the sense resistor value to use is:

$$R_{SENSE} = \frac{0.077}{5A} = 0.015\ \Omega$$

This is roughly half of the Buck (same load current).

For a Flyback topology (Buck-Boost with a transformer), the reflected output current is used:

$$R_{SENSE} \approx \frac{0.077}{I_O} \times \frac{N_P}{N_S} \text{ (Flyback)}$$

5.8 Operation with an External DC Source

PD applications utilizing PD70211 IC might be operated with an external power source (DC wall adaptor). Figure 5-2 and Figure 5-3 show the two cases of providing power with an external source.

- External source connected to application's low voltage supply rails. External source voltage level is dependent on DC-DC output characteristics. See Figure 5-2 for more details.
- External source connected to PD device output connection towards the application (VPP to VPNOUT). External source voltage level is dependent on DC-DC input requirements. See Figure 5-3 for more details.

Figure 5-2. External Power Input Connected to Application Supply Rails

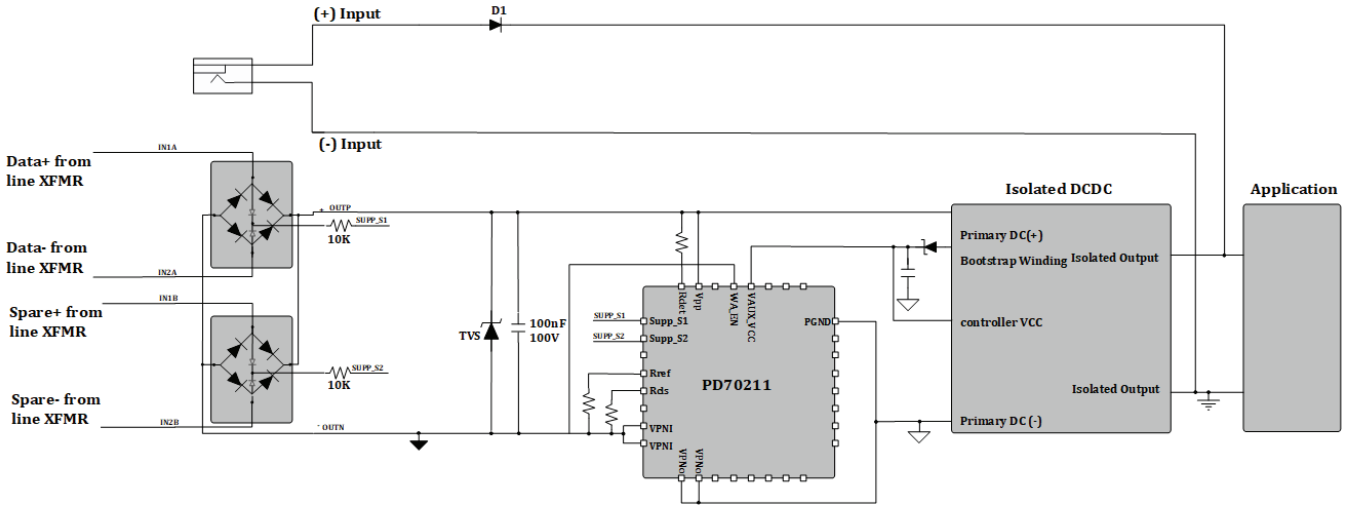
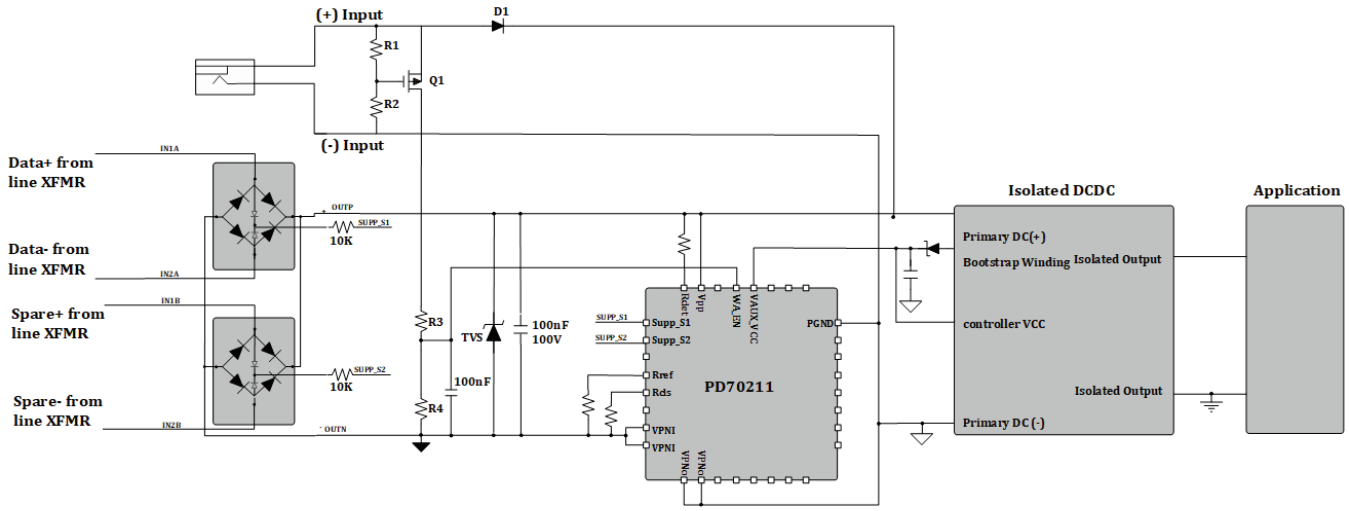


Figure 5-3. External Power Input Connected to PD70211 Output

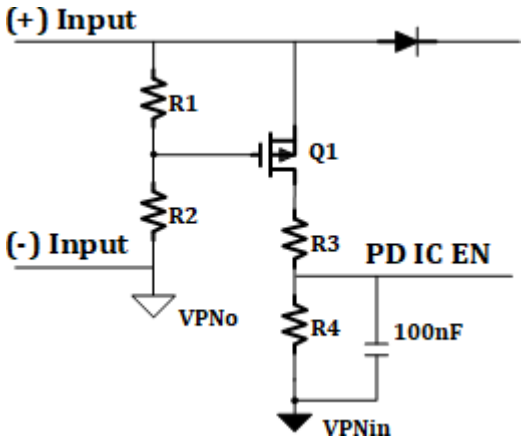


The PD70211 WA_EN pin disables the Isolation switch and the PSE input power, when an external adapter is connected.

The WA_EN resistors divider depends on the V_{INH} threshold of the PD70211.

Figure 5-4 shows the resistors that must be selected in external adapter connection.

Figure 5-4. External Power Input Resistors Dividers



R1 and R2 set a rough threshold for PFET Q1 enable, to detect whether the external adapter exists or not. It must be set at a lower threshold than the PD70211 disable levels.

R3 and R4 set the PD70211 disable threshold.

Therefore, in case of 36 V – 57 V external adapter, the disable setting can be selected as follows:

PFET enable threshold = 30 V.

R1 and R2 setting must be such that the value of Q1 VGS is less than 20 V at maximum voltage condition of the external adapter.

While external adapter voltage is more than 30 V, Q1 is above its VGS_{th} value.

$$VGS = Vext\_adapter \times \frac{R1}{R1 + R2}$$

R1 is selected as 2 kΩ.

$$R2 = R1 \times \frac{Vext\_adapter - VGS}{VGS}$$

Using R1 = 2 kΩ, Vext_adapter = 30 V, and VGS = maximum VGS_{th} = 3.5 V, the R2 value is obtained:

$$R2 = 15k\Omega$$

R3 and R4 are set to the range of few kΩ (10's of kΩ) using the following equation:

$$(I) \qquad PD70211\_Wa\_en = Vext\_adapter\_PD70211 \text{ x } \frac{R4}{(R3+R4)}$$

Using R3 = 15 kΩ, Vext_adapter = 33.7 V, and from this data sheet PD70211_WA_EN = 2.4 V as the turn OFF minimum threshold.

Solving the equation, the valid resistor's values for an adapter of 36 V and above are achieved.

$$R3 = 15k\Omega$$

$$R4 = 1.15k\Omega$$

For complete information and details of various connection methods, see www.microchip.com/DS00003472A.

6. Ordering Information

The following table lists the ordering information of the PD70211 device.

Table 6-1. Ordering Information

Ambient Temperature	Type	Part Marking	Ordering P/N	Package
–40 °C to 85 °C	RoHS compliant, Pb-free	MSCC Logo 70211 Z Z e4[1] YYWWNNN[2]	PD70211ILQ-TR	QFN-36 (6 mm × 6 mm, 0.5 mm pitch)

Notes:

1. ZZ e4: ZZ = Random character with no meaning, e4 = Second level interconnect.
2. YY = Year, WW = Week, NNN = Trace code.

7. Reference Documents

1. AN3533 PD70210(A) PD70211 System Layout Guidelines.
2. AN3471 Designing a Type 1/2 802.3 or HDBaseT Type 3 Powered Device Using PD702x1 and PD701x1 ICs.
3. AN3472 Implementing Auxiliary Power in PoE.

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8. Revision History

Revision	Date	Description
B	09/2021	• Updated Figure 4-1. QFN Package and Table 4-1. Package Dimensions. • Updated section Recommended PCB Layout.
A	10/2020	Following is the summary of changes: • The document was updated as per the Microchip standards. • Document ID PD-000390461 was changed to DS00003672A. • Added Table 1 to the Features section. • Added new Figure 1 and note in the 2 Applications section. • Updated units column of Table 2-5. • Updated units column of Table 2-7. • Edited the note in the 2.3 Thermal Properties section. • Updated Figure 3-1 and Table 3-1 in the Pin Configuration section. • Added K dimension values in Table 4-1 in the Package Specifications section. • Changed Figure 4-4 in the Recommended PCB Layout section. • Updated the 5.1 Peripheral Devices section. • Edited the 5.7 Selecting the Sense Resistor section. • Added the 7. Reference Documents section. • Updated package specifications in Table 6-1 and notes in the 6. Ordering Information section.
2.0	09/2019	Following is the summary of changes: • Re-drew the QFN package diagram. • Corrected a typo in pin name in the Applications Information section. • Removed the column 'note' was from the Ordering Information table. • Converted the document to Microsemi formatting standards.
1.4	07/2017	Updated the marking and MSL3 information
1.31	07/2016	Following is the summary of changes: • Removed 'PD' in IC marking description • Removed name of the front-end die (PD70210A) in functional block diagram • Updated revision number and date in the footer
1.3	10/2015	Following is the summary of changes: • Fixed Vaux pin description • Added UVLO_ON missing information • PD70224 was changed to PD70211 in figures 9, 10, and 11.
1.2		Updated a typo in part marking definition.
1.1	01/2015	Added a PCB footprint recommendation.
1.0	08/2014	Added frequency setting information.
0.6	07/2014	Flags maximum voltage was reduced and WA_EN information was added.
0.3	03/2013	General updates were made.
0.2	03/2012	Minor edits were made to the class values.
0.1	02/2012	It was the first publication of this document.

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