METORAGE SEMICONDUCTOR TECHNOLOGY Co.,Ltd.

Tentative Product Specification

- RITFXXXHM1AQ –

- RWTFXXXHM1AQ -

16GB microSDHC Memory Card
24GB microSDHC Memory Card
48GB microSDXC Memory Card
96GB microSDXC Memory Card

Document Number: M22022 (Version 1.0)

【Overview】

- **Flash Type**
  - YMTC
- **Bus Speed Mode**
  - UHS-I, SDR104
- **Speed Class**
  - Class 10
  - A2
  - U1 (16/24GB) / U3 (48/96GB)
  - V10 (16/24GB) / U3 (48/96GB)
- **Power Consumption**
  - Power Up Current < 250uA
  - Standby Current < 1000uA
  - Read Current < 150mA
  - Write Current < 150mA
- **Advanced Flash Management**
  - ECC Correction
  - Wear Leveling
  - Bad Block Management
- **Supply Voltage 2.7 ~ 3.6V**
- **Temperature Range(Ta)**
  - Operation:
    -25℃ ~ 85℃(RI)
    -40℃ ~ 85℃(RW)
  - Storage: -40℃ ~ 85℃
- **RoHS compliant**

Metorage Semiconductor Technology Co.,Ltd.

History of Specification Change

Revision	History	Date	Author
1.0	First release. （Tentative Specification）	2022/08/10	Fang

Requirement and Notice

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1. INTRODUCTION

1.1. General Description

The microSD card is fully compliant with the standards released by the SD Card Association. The Command List supports [Part 1 Physical Layer Specification Ver6.10 Final] definitions.
The microSD card comes with an 8-pin interface, designed to operate at a maximum frequency of 208MHz. It can alternate communication protocol between the SD mode and SPI mode. It performs data error detection and correction with very low power consumption. SD card are one of the most popular removable storage cards today due to its high performance and good reliability.

1.2. Flash Management

1.2.1. Error Correction Code

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, microSD card applies ECC Algorithm, which can detect and correct errors during Read processes, ensuring data is read correctly, as well as protecting data from corruption.

1.2.2. Wear Leveling

NAND Flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some area gets updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Wear Leveling technique is applied to extend the lifespan of NAND Flash by evenly distributing write and erase cycles across the media.
Metorage provides advanced Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static Wear Leveling algorithms, the life expectancy of the NAND Flash is greatly improved.

1.2.3. Bad Block Management

Bad blocks are blocks that include one or more invalid bits, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Initial Bad Blocks”. Bad blocks that are developed during the lifespan of the flash are named “Later Bad Blocks”. Metorage implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages any bad blocks that appear with use. This practice further prevents data being stored into bad blocks and improves the data reliability.

1.2.4. Pseudo SLC (for pSLC product only)

Pseudo SLC can be considered as an extended version of TLC. While TLC does Full Sequence Programming into 8 Vth distribution, pSLC only does Lower page programming into 2 Vth distribution. Accordingly, because only Lower pages are programmed, pSLC provides better performance and endurance than TLC. Moreover, pSLC performs similarly with SLC, yet pSLC is more cost-effective.

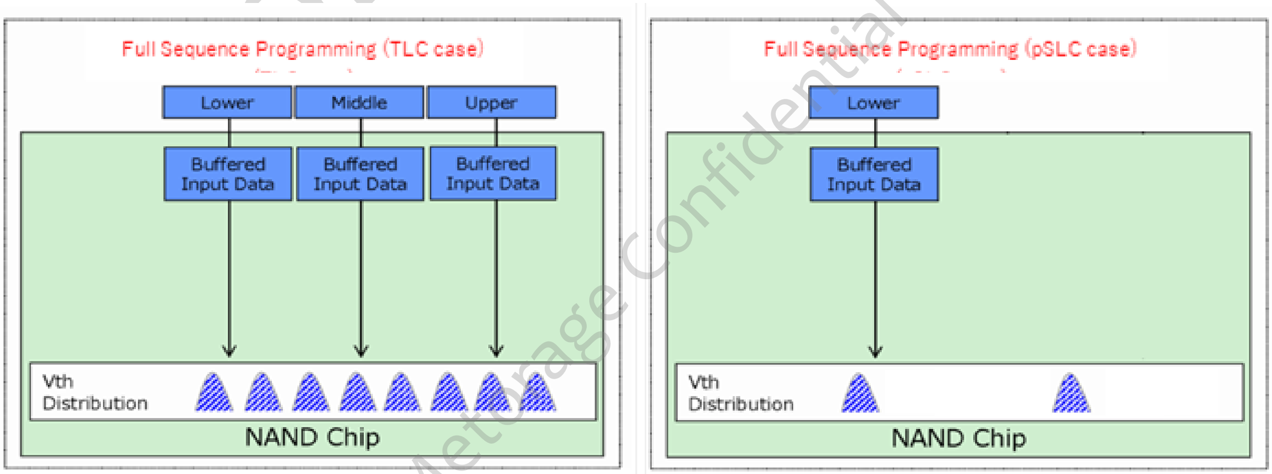


Figure 1-1 Cell Content of TLC (Left) and Pseudo SLC (Right)

2. PRODUCT SPECIFICATIONS

- **Compliant Specifications - SD Memory Card Specifications:**
  - Compliant with Part 1 Physical Layer Specification Ver. 6.10
  - Compliant with Part 2 File System Specification Ver. 3.00
- **Support SD SPI mode**
- **Bus Speed Mode (use 4 parallel data lines)**
  - **Non-UHS Mode**
    - Default speed mode: 3.3V signaling, frequency up to 25MHz, up to 12.5 MB/sec
    - High speed mode: 3.3V signaling, frequency up to 50MHz, up to 25 MB/sec
  - **UHS Mode**
    - SDR12: 1.8V signaling, frequency up to 25MHz, up to 12.5 MB/sec
    - SDR25: 1.8V signaling, frequency up to 50MHz, up to 25 MB/sec
    - SDR50: 1.8V signaling, frequency up to 100MHz, up to 50 MB/sec
    - SDR104: 1.8V signaling, frequency up to 208MHz, up to 104MB/sec
    - DDR50: 1.8V signaling, frequency up to 50MHz, sampled on both clock edges, up to 50 MB/sec

NOTES: 1. Timing in 1.8V signaling is different from that of 3.3V signaling.
2. To properly run the UHS mode, please ensure the device supports UHS-I mode.

- **The command list supports [Part 1 Physical Layer Specification Ver. 6.10] definitions**
  - Command list are described in "Table 3-2 SD mode Command Set " and "Table 3-3 SPI mode Command Set" in this document.
- **Support Hot Plug**
  - Card removal during read operation will never harm the content.
- **Password Protection of cards (Support)**

3. ELECTRICAL INTERFACE OUTLINES

3.1. microSD Card Pins

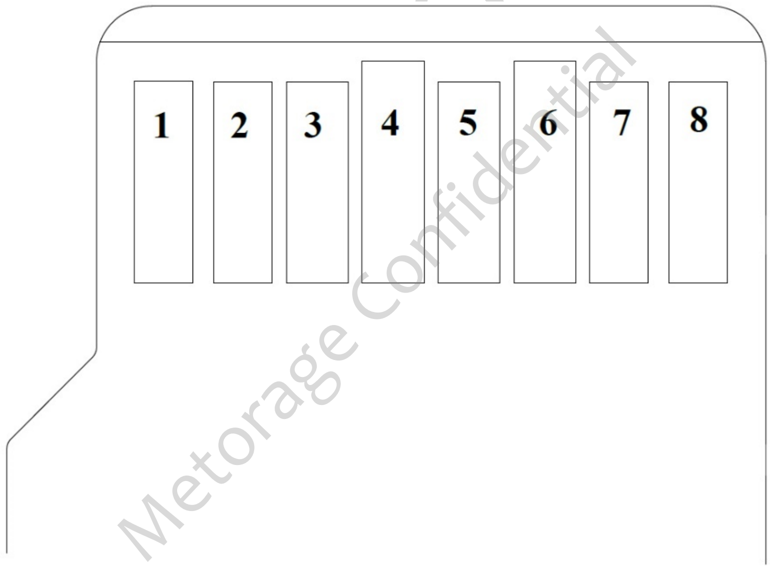


Figure 3-1 microSD Card Pin assignment (Back View of the card)

Table 3-1 microSD Memory Card Pad Assignment

Pin	SD Mode			SPI Mode		
	Name	Type[1]	Description	Name	Type	Description
1	DAT2	I/O/PP	Data Line [bit2]	RSV		-
2	CD/DAT3 [2]	I/O/PP [3]	Card Detect/ Data Line [bit3]	CS	I [3]	Chip Select (neg. true)
3	CMD	PP	Command/Response	DI	I	Data In
4	V_{DD}	S	Supply voltage	V_{DD}	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	V_{SS}	S	Supply voltage ground	V_{SS}	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [bit0]	DO	O/PP	Data Out
8	DAT1	I/O/PP	Data Line [bit1]	RSV		-

(1) S: power supply, I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers.
(2) The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode as well while they are not used. It is defined so in order to keep compatibility to MultiMedia Cards.
(3) At power up, this line has a 50KOhm pull up enabled in the card. This resistor serves two functions: Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode, it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user during regular data transfer with SET_CLR_CARD_DETECT (ACMD42) command.

3.2. microSD Card Bus Topology

The microSD Card supports 2 alternative communication protocols, SD and SPI BUS mode.
Host can choose either one of both bus mode, same data can be read or written by both modes.
SD mode allows 4-bits data transfer way, it provides high performance. SPI mode supports 1-bit data transfer and of course the performance is lower compared to SD mode.

3.3. microSD Bus Mode Protocol

In default speed, the microSD Memory Card bus has a single master (application); multiple slaves (Cards), synchronous star topology (refer to Figure 3-2). In high speed and UHS-I, the microSD Memory Card bus has a single master (application) and single slave (card), synchronous point to point topology. Clock, power and ground signals are common to all cards. Command (CMD) and data (DAT0-DAT3) signals are dedicated to each card providing continues point to point connection to all the cards. During initialization process commands are sent to each card individually, allowing the application to detect the cards and assign logical addresses to the physical slots. Data is always sent (received) to (from) each card individually. However, in order to simply the handling of the card stack, after the initialization process, all commands may be sent concurrently to all cards. Addressing information is provided in the command packet.
SD bus allows dynamic configuration of the number of data lines. After power up, by default, the microSD Memory Card will use only DAT0 for data transfer. After initialization the host can change the bus width (number of data active lines). This feature allows easy tradeoff between HW cost and system performance. Note that while DAT1 to DAT3 are not in use, the related Host's DAT lines should be in tri-state (input mode). For SDIO cards DAT1 and DAT2 are used for signaling.

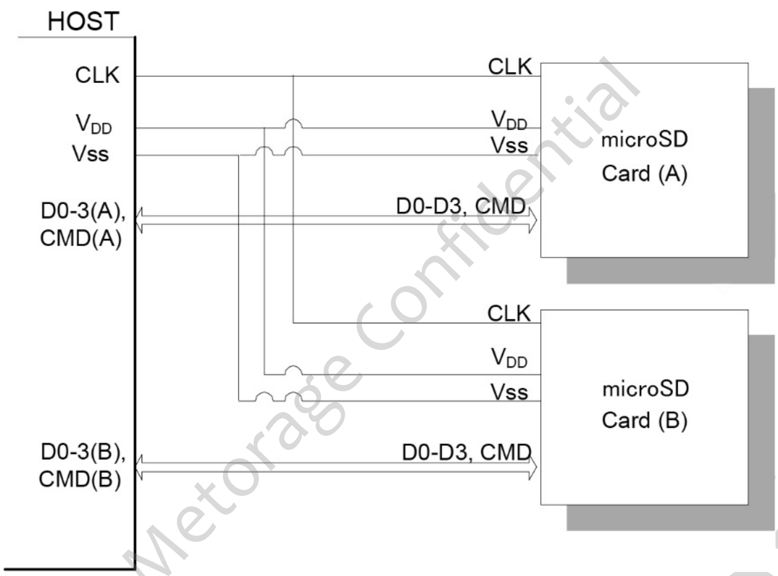


Figure 3-2 SD Memory Card System Bus Topology

The microSD bus includes the following signals:

CLK: Host to card clock signal

CMD: Bidirectional Command/Response signal

DAT0-DAT3: 4 Bidirectional data signals

V_{DD}, V_{SS1}, V_{SS2}: Power and ground signals

Table 3-2 SD Mode Command Set

Card Command Class (CCC)	0 Basic	1 Command Queue	2 Block read	3 Reserved	4 Block write	5 Erase	6 Write protection	7 Lock card	8 Application specific	9 I/O mode	10 Switch	11 Extension
CMD0	+											
CMD2	+											
CMD3	+											
CMD4	+											
CMD5										+		
CMD6											+	
CMD7	+											
CMD8	+											
CMD9	+											
CMD10	+											
CMD11	+											
CMD12	+											
CMD13	+											
CMD15	+											
CMD16			+		+			+				
CMD17			+									
CMD18			+									
CMD19			+									
CMD20			+		+							
CMD21												+
CMD23			+		+							
CMD24					+							
CMD25					+							
CMD27					+							
CMD28							+					
CMD29							+					
CMD30							+					
CMD32						+						
CMD33						+						
CMD34-37											+	
CMD38						+						
CMD40								+				
CMD42								+				
CMD43-47		+										
CMD48												+
CMD49												+
CMD50											+	
CMD52										+		
CMD53										+		

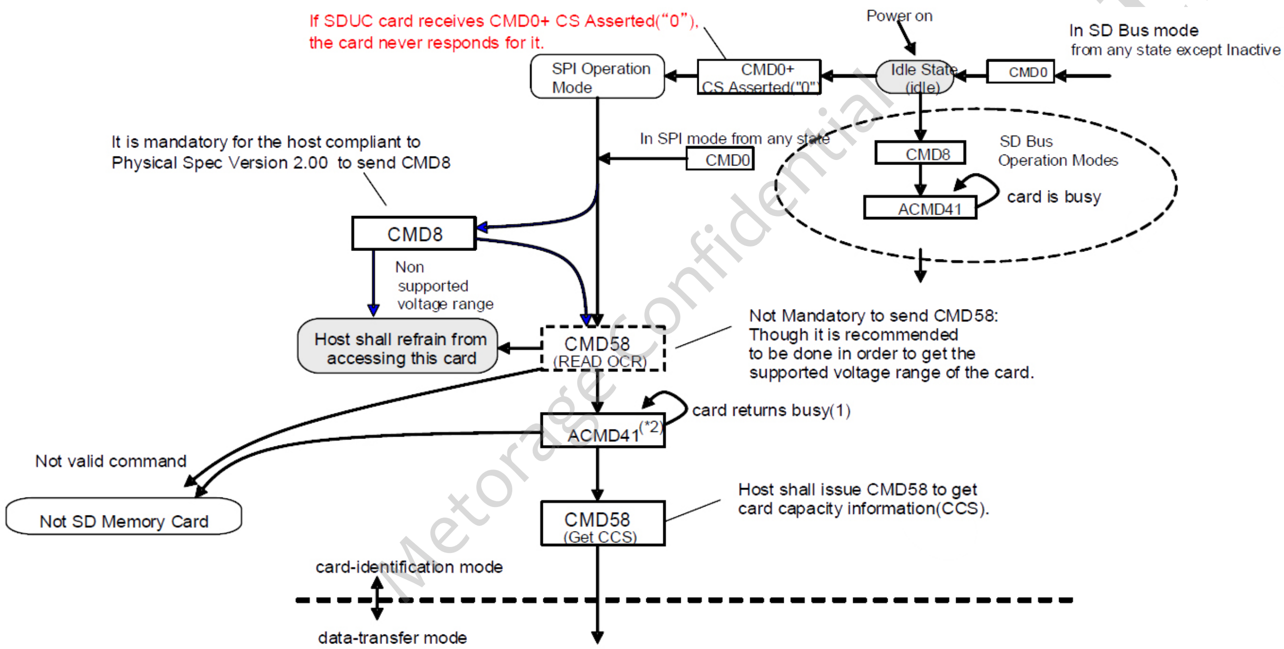
Card Command Class (CCC)	0	1	2	3	4	5	6	7	8	9	10	11
	Basic	Command Queue	Block read	Reserved	Block write	Erase	Write protection	Lock card	Application specific	I/O mode	Switch	Extension
CMD55									+			
CMD56									+			
CMD57											+	
CMD58												+
CMD59												+
ACMD6									+			
ACMD13									+			
ACMD14									+			
ACMD15									+			
ACMD16									+			
ACMD22									+			
ACMD23									+			
ACMD28									+			
ACMD41									+			
ACMD42									+			
ACMD51									+			

Commands	Support requirements
CMD0	Mandatory
CMD2	Mandatory
CMD3	Mandatory
CMD4	Mandatory
CMD5	Optional
CMD6	Mandatory for cards version 1.10 and after.
CMD7	Mandatory
CMD8	Mandatory for cards version 2.00 and after.
CMD9	Mandatory
CMD10	Mandatory
CMD11	Mandatory for cards supporting UHS-I. Optional for cards that do not support UHS-I.
CMD12	Mandatory
CMD13	Mandatory
CMD15	Mandatory
CMD16	Mandatory
CMD17	Mandatory
CMD18	Mandatory
CMD19	Mandatory for cards supporting UHS-I. Optional for cards that do not support UHS-I.

Commands	Support requirements
CMD20	Not support for SDSC cards. Mandatory for SDHC and SDXC cards that support Video Speed Class. Optional for SDHC cards that support: a) Speed Class; or b) UHS Speed Grade, and do not support Video Speed Class. Mandatory for SDXC cards that support Speed Class or UHS Speed Grade.
CMD21	Optional
CMD23	Not support for SDSC cards. Mandatory for SDHC and SDXC cards that support UHS104. Optional for SDHC cards and SDXC cards that do not support UHS104.
CMD24	Mandatory for writable type of cards.
CMD25	Mandatory for writable type of cards.
CMD27	Mandatory for writable type of cards.
CMD28	Optional
CMD29	Optional
CMD30	Optional
CMD32	Mandatory for writable type of cards.
CMD33	Mandatory for writable type of cards.
CMD34-37	Optional for cards version 1.10 and after.
CMD38	Mandatory for writable type of cards. Discard and FULE support is optional.
CMD40	Optional
CMD42	Optional for cards version 1.01 and 1.10. Mandatory for cards version 2.00 and after. COP support is optional for CMD42.
CMD43-47	Mandatory for cards supporting Command Queue.
CMD48	Optional Mandatory for cards supporting Performance Enhancement functions.
CMD49	Optional Mandatory for cards supporting Performance Enhancement functions.
CMD50	Optional for cards version 1.10 and after.
CMD52	Optional
CMD53	Optional
CMD55	Mandatory
CMD56	Mandatory
CMD57	Optional for cards version 1.10 and after.
CMD58	Optional
CMD59	Optional
ACMD6	Mandatory
ACMD13	Mandatory
ACMD14	Optional
ACMD15	Optional
ACMD16	Optional
ACMD22	Mandatory for writable types of cards.
ACMD23	Mandatory for writable types of cards.
ACMD28	Optional
ACMD41	Mandatory
ACMD42	Mandatory
ACMD51	Mandatory

3.4. SPI Bus Mode Protocol

While the SD Memory Card channel is based on command and data bit streams that are initiated by a start bit and terminated by a stop bit, the SPI channel by byte oriented. Every command or data block is built for 8-bit bytes and is byte aligned with the CS signal (i.e. the length is a multiple of 8 clock cycles). The card starts to count SPI bus clock cycle at the assertion of the CS signal. Every command or data token shall be aligned with 8-clock cycle boundary.
Similar to the SD Memory Card Protocol, the SPI messages consist of command, response and data-block tokens.
The advantage of SPI mode is reducing the host design effort, especially for MMC host side, it just be modified by little change. Note: please use SD card specification to implement SPI mode function, not use MMC specification. For example, SPI mode is initialized by ACMD41, and the registers are different from MMC card, especially CSD register.



(*1) Note: Card returns busy when
- Card executes internal initialization process.
- If the card is High capacity SD Memory Card, there are 2 cases
    1. CMD8 was not issued before ACMD41
    2. ACMD41 is issued with HCS=0

(*2) Note: 2.1mm SD Memory Card can be initialized using CMD1 and Thin (1.4mm) SD Memory Card can be initialized using CMD1 only after firstly initialized by using CMD0 and ACMD41. In any of the cases CMD1 is not recommended because it may be difficult for the host to distinguish between MultiMediaCard and SD Memory Card.
If the SD card is initialized by CMD1 and the host treat it as MMC card, not SD card, the Data of the card may be damaged because of wrong interpretation of CSD and CID registers.

Figure 3-3 SD Memory Card State Diagram (SPI mode)

Table 3-3 SPI Mode Command Set

Card Command Class (CCC)		0	1	2	3	4	5	6	7	8	9	10	11
Supported commands	Class description	Basic	Reserved	Block read	Reserved	Block write	Erase	Write protection	Lock card	Application specific	I/O mode	Switch	Reserved
CMD0	Mandatory	+											
CMD1	Mandatory	+											

CMD5	Optional										+		
CMD6[2]	Mandatory											+	
CMD8[3]	Mandatory	+											
CMD9	Mandatory	+											
CMD10	Mandatory	+											
CMD12	Mandatory	+											
CMD13	Mandatory	+											
CMD16	Mandatory			+		+			+				
CMD17	Mandatory			+									
CMD18	Mandatory			+									
CMD24	Mandatory1					+							
CMD25	Mandatory1					+							
CMD27	Mandatory1					+							
CMD28	Optional							+					
CMD29	Optional							+					
CMD30	Optional							+					
CMD32	Mandatory1						+						
CMD33	Mandatory1						+						
CMD34-37[2]	Optional											+	
CMD38	Mandatory1						+						
CMD424	(Note4)								+				
CMD50[2]	Optional											+	
CMD52	Optional										+		
CMD53	Optional										+		
CMD55	Mandatory1									+			
CMD56	Mandatory1									+			
CMD57[2]	Optional											+	
CMD58	Mandatory	+											
CMD59	Mandatory	+											
ACMD13	Mandatory									+			
ACMD22	Mandatory1									+			
ACMD23	Mandatory1									+			
ACMD41	Mandatory									+			
ACMD42	Mandatory1									+			
ACMD51	Mandatory1									+			

Note(1):The commands related write and erase are mandatory for the Writable types of Cards.

Note(2):This command was defined in spec version 1.10.

Note(3):This command is newly defined in version 2.00.

Note(4):This command is optional in Version 1.01 and 1.10 and mandatory from Version 2.00. COP support is optional for CMD42.

3.5. microSD card initialization

Figure 3-4 presents the initialization flow chart for UHS-I hosts and Figure 3-5 shows sequence of commands to perform voltage switch.

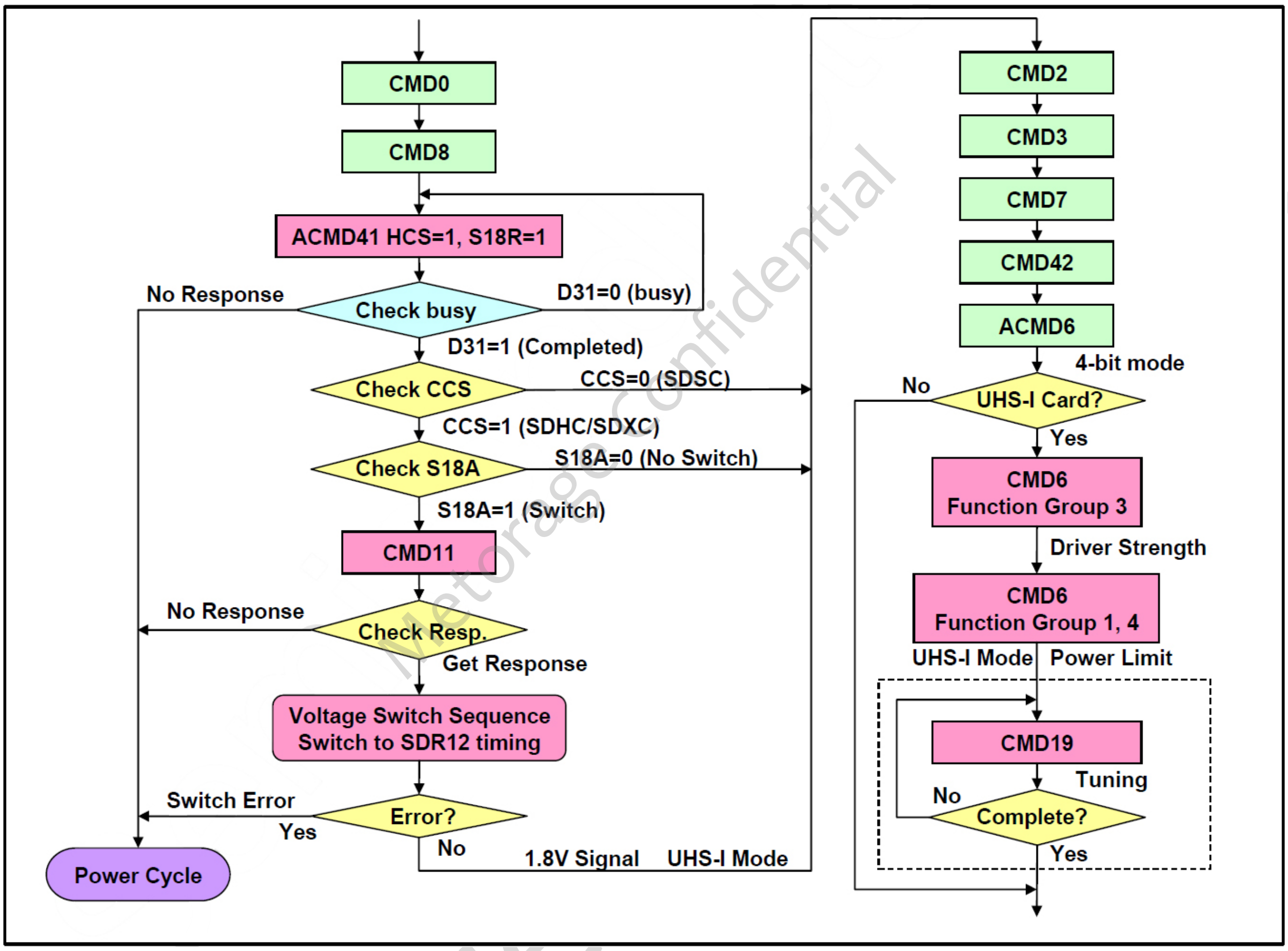


Figure 3-4 UHS-I Host Initialization Flow Chart

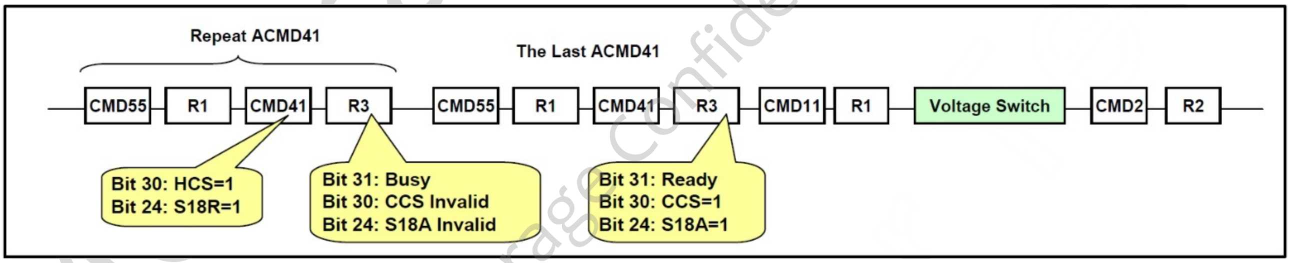


Figure 3-5 ACMD41 Timing Followed by Voltage Switch Sequence

When signaling level is 3.3V, host repeats to issue ACMD41 with HCS=1 and S18R=1 until the response indicates ready. The argument (HCS and S18R) of the first ACMD41 is effective but the all following ACMD41 should be issued with the same argument.
If Bit31 indicates ready, host needs to check CCS and S18A.
The card indicates S18A=0, which means that voltage switch is not allowed and the host needs to use current signaling level.

Table 3-4 S18R and S18A Combinations

Current Signaling Level	S18R	S18A	Comment
3.3V	0	0	1.8V signaling is not requested
	1	0	The card does not support 1.8V signaling
	1	1	Start signal voltage switch sequence
1.8V	X	0	Already switched to 1.8V

To change signaling level at the same time between host and card, signal voltage switch sequence is invoked by CMD11 as shown in Figure 3-6. CMD11 is issued only when S18A=1 in the response of ACMD41.

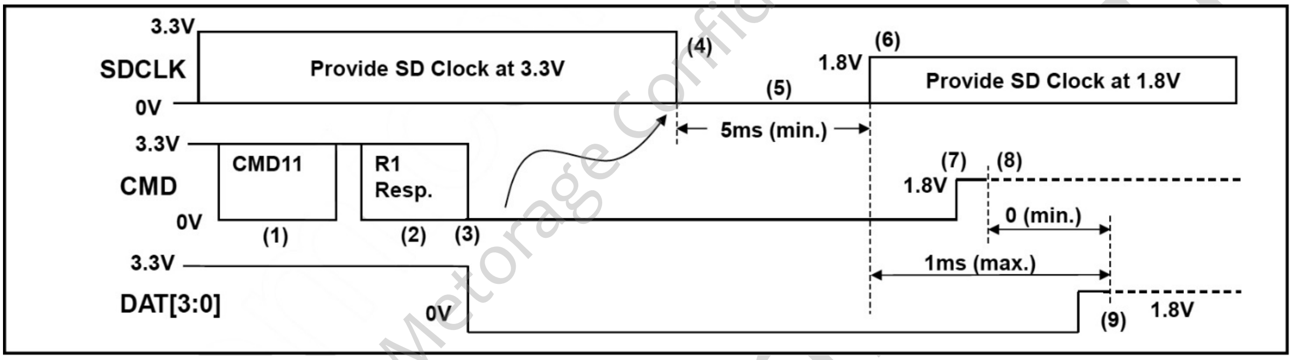


Figure 3-6 Signal Voltage Switch Sequence

4. SD CARD COMPARISON

Table 4-1 Comparing microSDHC, and microSDXC

	microSDHC	microSDXC
File System	FAT32	exFAT
Addressing Mode	Block (512 byte unit)	Block (512 byte unit)
HCS/CCS bits of ACMD41	Support	Support
CMD8 (SEND_IF_COND)	Support	Support
CMD16 (SET_BLOCKLEN)	Support (Only CMD42)	Support (Only CMD42)
Partial Read	Not Support	Not Support
Lock/Unlock Function	Mandatory	Mandatory
Write Protect Groups	Not Support	Not Support
Supply Voltage 2.7v – 3.6v (for operation)	Support	2.7v-3.6v
Total Bus Capacitance for each signal line	40pF	40pF
CSD Version (CSD_STRUCTURE Value)	2.0 (0x1)	2.0 (0x1)
Speed Class	Mandatory (Class 2 / 4 / 6 / 10)	Mandatory (Class 2 / 4 / 6 / 10)

Table 4-2 Comparing UHS Speed Grade Symbols

	U1 (UHS Speed Grade 1)	U3 (UHS Speed Grade 3)
Operable Under	*UHS-I Bus I/F, UHS-II Bus I/F	
SD Memory Card	microSDHC UHS-I and UHS-II, microSDXC UHS-I and UHS-II	
Mark	U1	U3
Performance	10 MB/s minimum write speed Under the UHS Class speed condition	30 MB/s minimum write speed Under the UHS Class speed condition
Applications	Full higher potential of recording realtime broadcasts and capturing large-size HD videos.	Capable of recording 4K 2K video.

*UHS (Ultra High Speed), the fastest performance category available today, defines bus-interface speeds up to 312 Megabytes per second for greater device performance. It is available on microSDXC and microSDHC memory cards and devices.

5. ELECTRICAL SPECIFICATIONS

5.1. Power Consumption

The table below is the power consumption of microSD card with different flash memory types.

Table 5-1 Power Consumption of microSD card

Flash Mode		Max. Read Current (mA)	Max. Write Current (mA)
Default Speed Mode		150	150
High Speed Mode		150	150
UHS-I Mode	UHS50/DDR50	150	150
	UHS104/ DDR50	150	150

Note： The test data is tentative, current numbers might be subject to changes without notice.

5.2. Working Rating

Table 5-2 Working Rating of microSD card

Item	Symbol	Parameter	Min	Max	Unit
1	T_a	Operating Temperature	-25(RI)/ -40(RW)	+85	℃
2	T_{st}	Storage Temperature	-40	+85	℃
3	V_{DD}	Voltage	2.7	3.6	V

Note： The samples are engineering samples and the data is tentative.

5.3. DC Characteristic

5.3.1. Bus Operation Conditions for 3.3V Signaling

Table 5-3 Threshold Level for High Voltage Range

Parameter	Symbol	Min	Max	Unit	Condition
Supply Voltage	V_{DD}	2.7	3.6	V	-
Output High Voltage	V_{OH}	0.75*V_{DD}	-	V	I_{OH}=-2mA V_{DD} Min
Output Low Voltage	V_{OL}	-	0.125*V_{DD}	V	IOL=2mA V_{DD} Min
Input High Voltage	V_{IH}	0.625*V_{DD}	V_{DD}+0.3	V	-
Input Low Voltage	V_{IL}	V_{SS}-0.3	0.25*V_{DD}	V	-
Power Up Time	-	-	250	ms	From 0V to V_{DD} min

Table 5-4 Peak Voltage and Leakage Current

Parameter	Symbol	Min	Max	Unit	Remarks
Peak voltage on all lines	-	-0.3	V_{DD}+0.3	V	-
All Inputs					
Input Leakage Current	-	-10	10	uA	-
All Outputs					
Output Leakage Current	-	-10	10	uA	-

Table 5-5 Threshold Level for 1.8V Signaling

Parameter	Symbol	Min	Max	Unit	Condition
Supply Voltage	V_{DD}	2.7	3.6	V	-
Regulator Voltage	V_{DDIO}	1.7	1.95	V	Generated by V_{DD}
Output High Voltage	V_{OH}	1.4	-	V	I_{OH}=-2mA
Output Low Voltage	V_{OL}	-	0.45	V	I_{OL}=2mA
Input High Voltage	V_{IH}	1.27	2.00	V	-
Input Low Voltage	V_{IL}	V_{ss}-0.3	0.58	V	-

Table 5-6 Input Leakage Current for 1.8V Signaling

Parameter	Symbol	Min	Max	Unit	Remarks
Input Leakage Current	-	-2	2	uA	DAT3 pull-up is disconnected.

5.3.2. Bus Signal Line Load

Bus Operation Conditions – Signal Line's Load

Total Bus Capacitance = C_{HOST} + C_{BUS} + N C_{CARD}

Table 5-7 Bus Signal Line Load of microSD Card

Parameter	Symbol	Min	Max	Unit	Remark
Pull-up resistance	R_{CMD} R_{DAT}	10	100	kΩ	to prevent bus floating
Total bus capacitance for each signal line	C_L	-	40	pF	1 card C_{HOST}+C_{BUS} shall not exceed 30 pF
Card Capacitance for each signal pin	C_{CARD}	-	10^1	pF	-
Maximum signal line inductance	-	-	16	nH	-
Pull-up resistance inside card (pin1)	R_{DAT3}	10	90	kΩ	May be used for card detection
Capacity Connected to Power Line	C_C	-	5	uF	To prevent inrush current

5.3.3. Power Up Time of Host

The host needs to keep power line level less than 0.5V and more than 1ms before power ramp up.

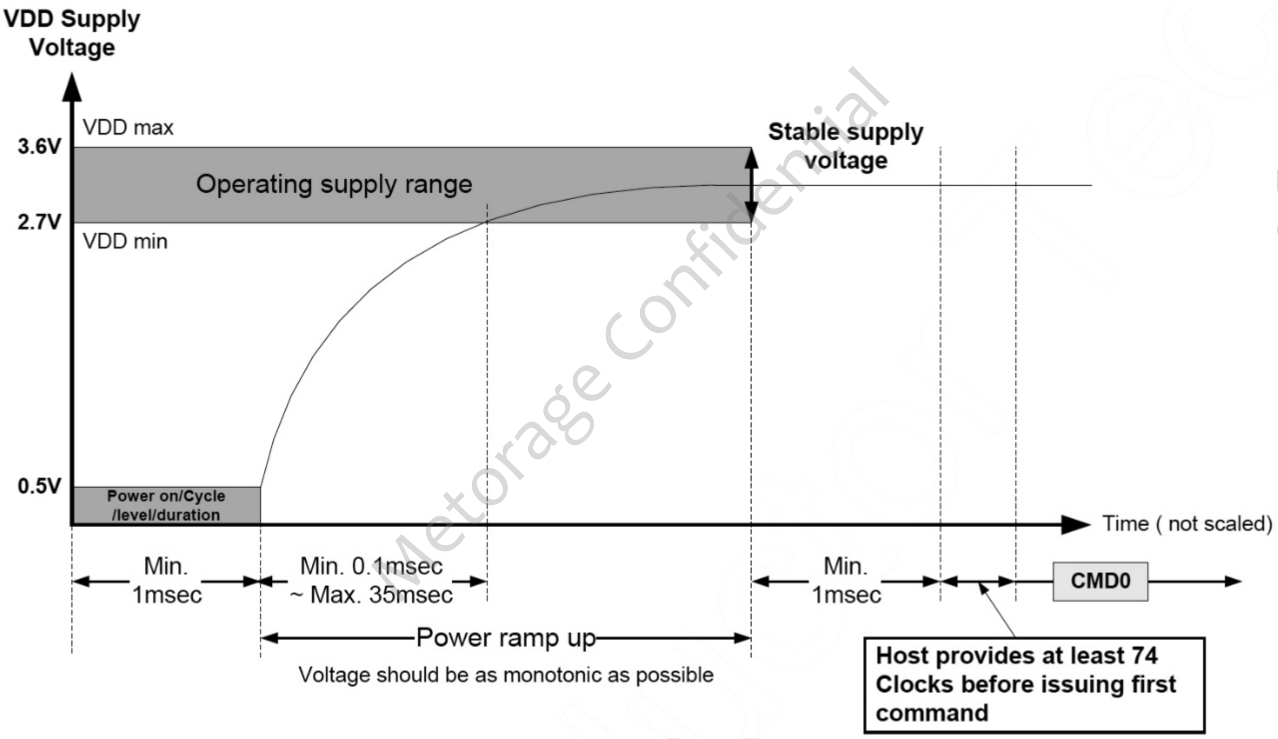


Figure 5-1 Power Up Diagram of Host

Power On or Power Cycle
Followings are requirements for Power on and Power cycle to assure a reliable microSD Card hard reset.
(1) Voltage level shall be below 0.5V.
(2) Duration shall be at least 1ms.

Power Supply Ramp Up
The power ramp up time is defined from 0.5V threshold level up to the operating supply voltage which is stable between VDD (min.) and VDD (max.) and host can supply SDCLK.
Followings are recommendations of Power ramp up:
(1) The voltage of power ramp up should be monotonic as much as possible.
(2) The minimum ramp up time should be 0.1ms.
(3) The maximum ramp up time should be 35ms for 2.7-3.6V power supply.
(4) Host shall wait until VDD is stable.
(5) After 1ms VDD stable time, the host provides at least 74 clocks before issuing the first command.

Power Down and Power Cycle
(1) When the host shuts down the power, the card V_{DD} shall be lowered to less than 0.5Volt for a minimum period of 1ms. During power down, DAT, CMD, and CLK should be disconnected or driven to logical 0 by the host to avoid a situation that the operating current is drawn through the signal lines.
(2) If the host needs to change the operating voltage, a power cycle is required. Power cycle means the power is turned off and supplied again. A power cycle is also needed for accessing cards that are already in *Inactive State*. To create a power cycle the host shall follow the power down description before power up the card (i.e. the card V_{DD} shall be once lowered to less than 0.5Volt for a minimum period of 1ms).

5.3.4. Power Up Time of Card

A device shall be ready to accept the first command within 1ms from detecting VDD min.

The device may use up to 74 clocks for preparation before receiving the first command.

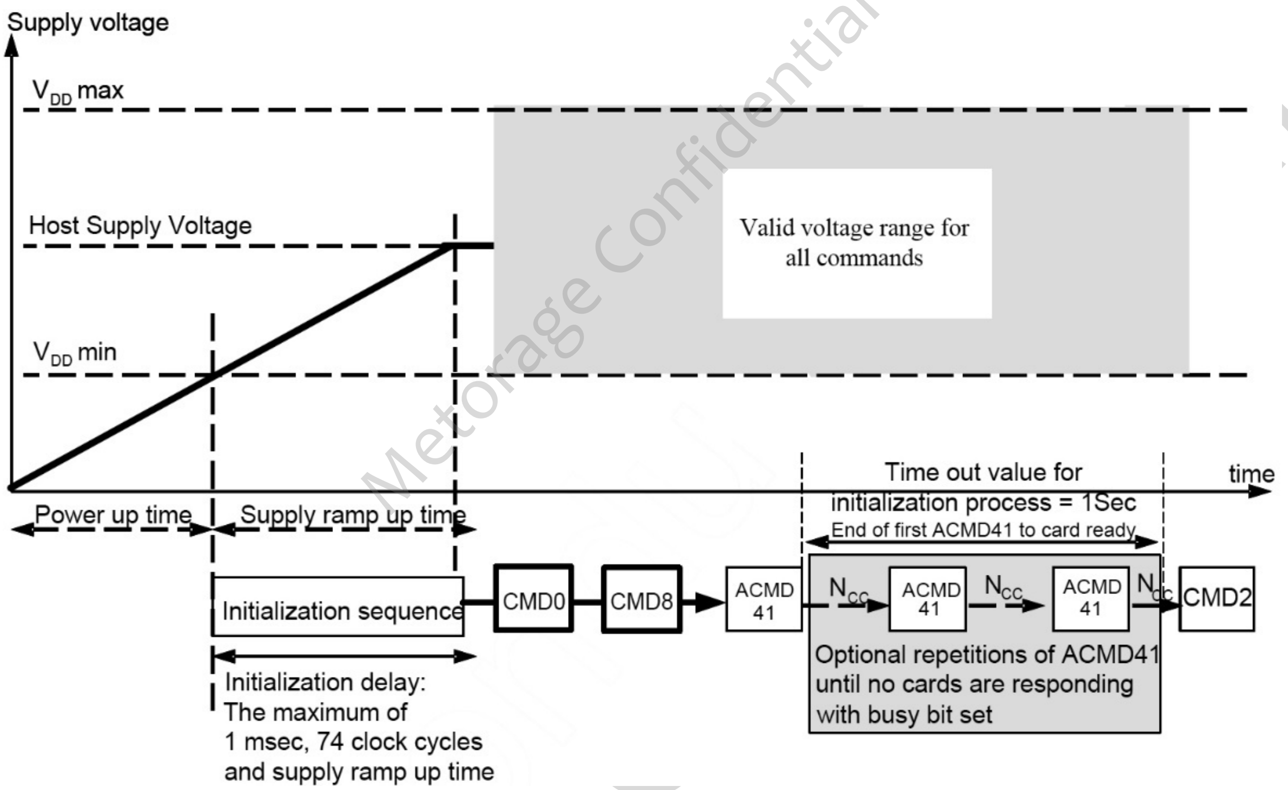


Figure 5-2 Power Up Diagram of Card

5.4. AC Characteristic

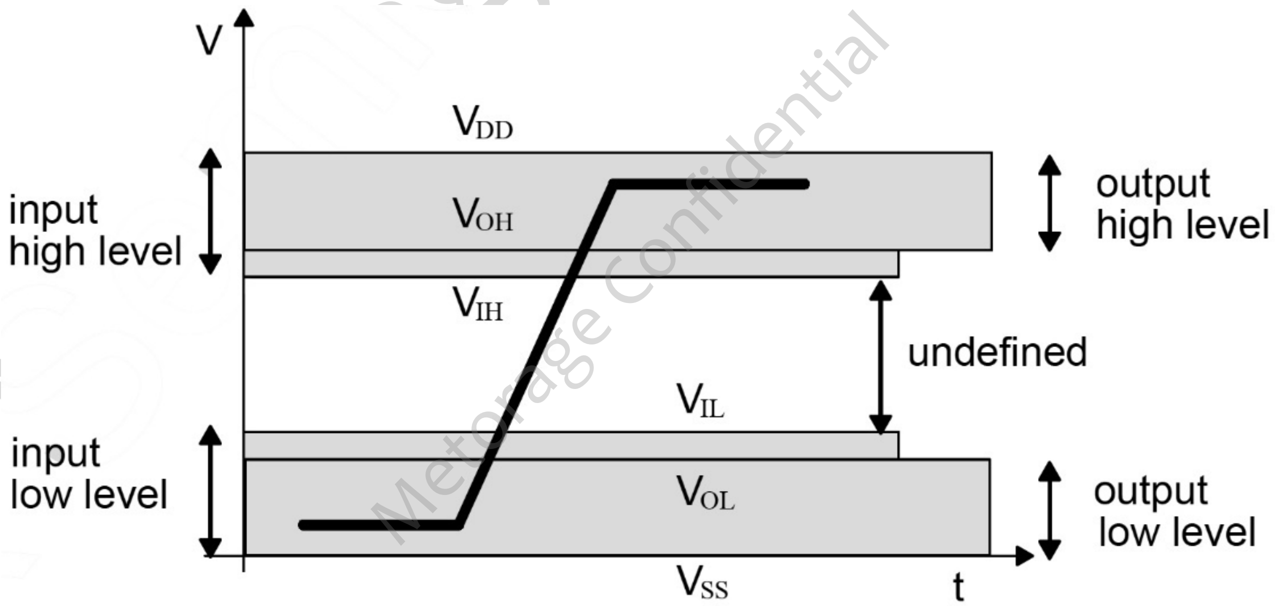


Figure 5-3 Bus Signal Level

5.4.1. microSD Interface Timing (Default)

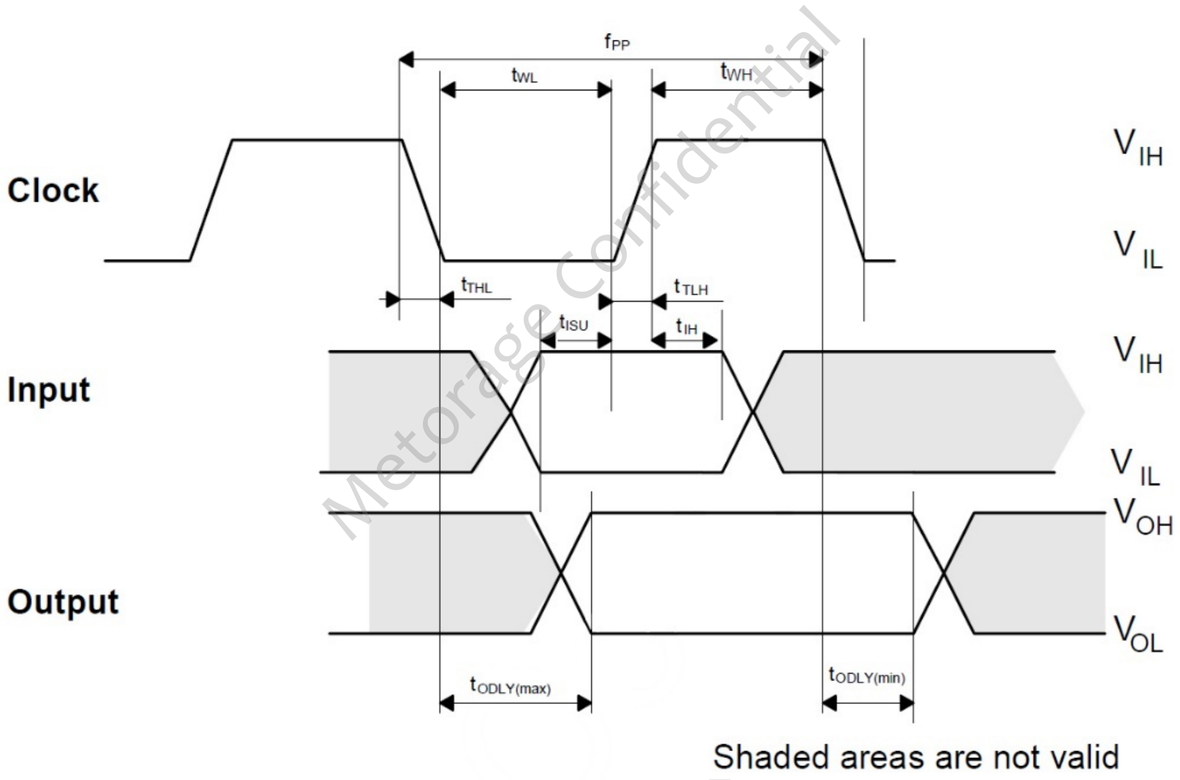


Figure 5-4 Card Input/Output Timing (Default Speed Card)

Table 5-8 Bus Timing – Parameters Values (Default Speed)

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	25	MHz	C_{card}≤ 10 pF (1 card)
Clock frequency Identification Mode	f_{OD}	0(1)/100	400	kHz	C_{card}≤ 10 pF (1 card)
Clock low time	t_{WL}	10	-	ns	C_{card}≤ 10 pF (1 card)
Clock high time	t_{WH}	10	-	ns	C_{card}≤ 10 pF (1 card)
Clock rise time	t_{TLH}	-	10	ns	C_{card}≤ 10 pF (1 card)
Clock fall time	t_{THL}	-	10	ns	C_{card}≤ 10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	5	-	ns	C_{card}≤ 10 pF (1 card)
Input hold time	t_{IH}	5	-	ns	C_{card}≤ 10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	0	14	ns	C_L≤ 40 pF (1 card)
Output Delay time during Identification Mode	t_{ODLY}	0	50	ns	C_L≤ 40 pF (1 card)

(1) 0Hz means to stop the clock. The given minimum frequency range is for cases where continuous clock is required.

5.4.2. microSD Interface Timing (High-Speed Mode)

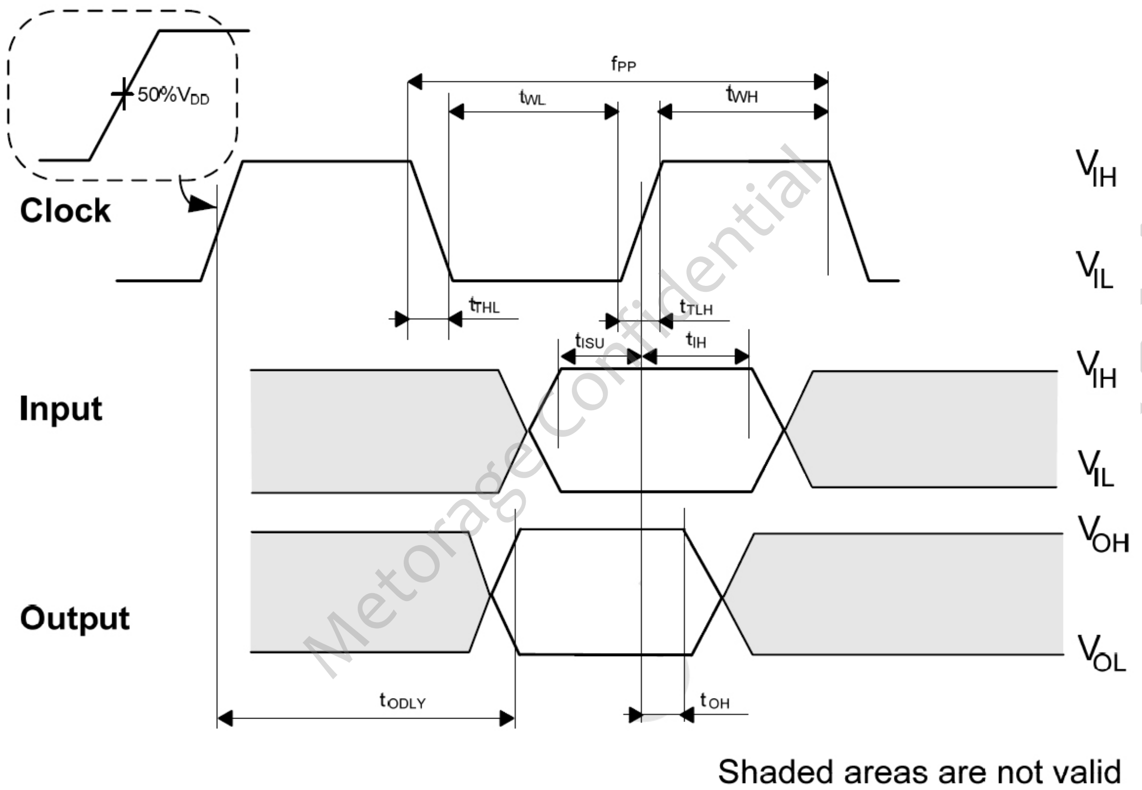


Figure 5-5 Card Input/Output Timing (High Speed Card)

Table 5-9 Bus Timing – Parameters Values (High Speed)

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	50	MHz	$C_{card} \leq 10$ pF (1 card)
Clock low time	t_{WL}	7	-	ns	$C_{card} \leq 10$ pF (1 card)
Clock high time	t_{WH}	7	-	ns	$C_{card} \leq 10$ pF (1 card)
Clock rise time	t_{TLH}	-	3	ns	$C_{card} \leq 10$ pF (1 card)
Clock fall time	t_{THL}	-	3	ns	$C_{card} \leq 10$ pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	6	-	ns	$C_{card} \leq 10$ pF (1 card)
Input hold time	t_{IH}	2	-	ns	$C_{card} \leq 10$ pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	-	14	ns	$C_L \leq 40$ pF (1 card)
Output Hold time	T_{OH}	2.5	-	ns	$C_L \leq 15$ pF (1 card)
Total System capacitance of each line[1]	C_L	-	40	pF	CL ≤ 15 pF (1 card)

(1) In order to satisfy severe timing, the host shall drive only one card.

5.4.3. microSD Interface Timing (SDR12, SDR25, SDR50 and SDR104 Modes)

Input

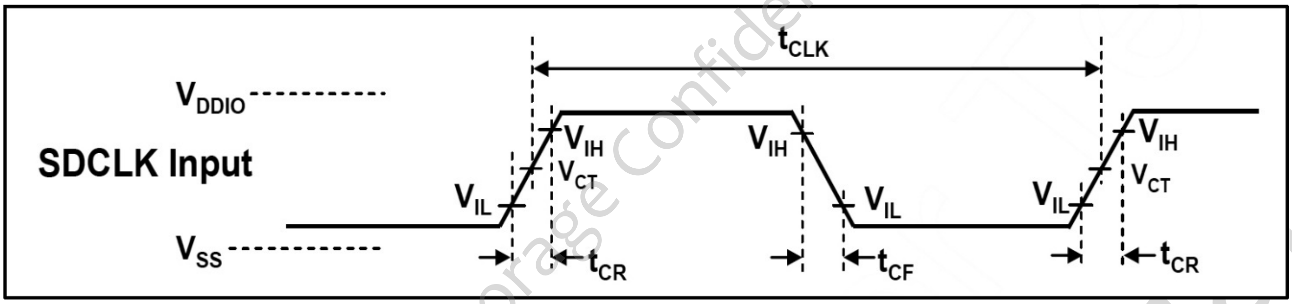


Figure 5-6 Clock Signal Timing

Table 5-10 Clock Signal Timing

Symbol	Min	Max	Unit	Remark
t_{CLK}	4.80	-	ns	208MHz (Max.), Between rising edge, V_{CT}= 0.975V
t_{CR}, t_{CF}	-	0.2* t_{CLK}	ns	t_{CR}, t_{CF} < 0.96ns (max.) at 208MHz, C_{CARD}=10pF t_{CR}, t_{CF} < 2.00ns (max.) at 100MHz, C_{CARD}=10pF The maximum value of t_{CR}, t_{CF} is 10ns regardless of clock frequency
Clock Duty	30	70	%	-

SDR50 and SDR104 Input Timing

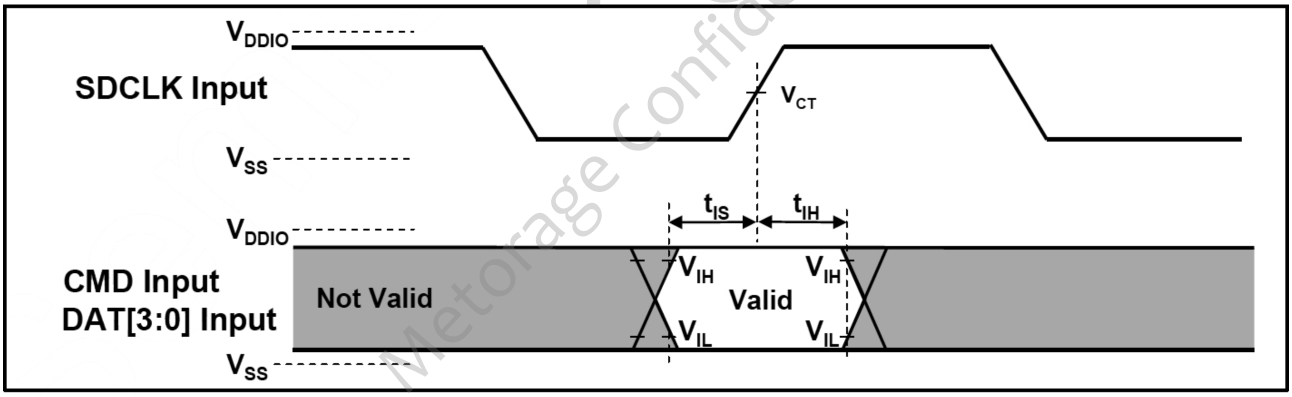


Figure 5-7 Card Input Timing

Table 5-11 SDR50 and SDR104 Input Timing

Symbol	Min	Max	Unit	SDR104 Mode
t_{IS}	1.40	-	ns	C_{CARD} =10pF, V_{CT}= 0.975V
t_{IH}	0.80[1]	-	ns	C_{CARD} = 5pF, V_{CT}= 0.975V
Symbol	**Min**	**Max**	**Unit**	**SDR50 Mode**
t_{IS}	3.00	-	ns	C_{CARD} =10pF, V_{CT}= 0.975V
t_{IH}	0.80[1]	-	ns	C_{CARD} = 5pF, V_{CT}= 0.975V

Output(SDR12, SDR25, SDR50)

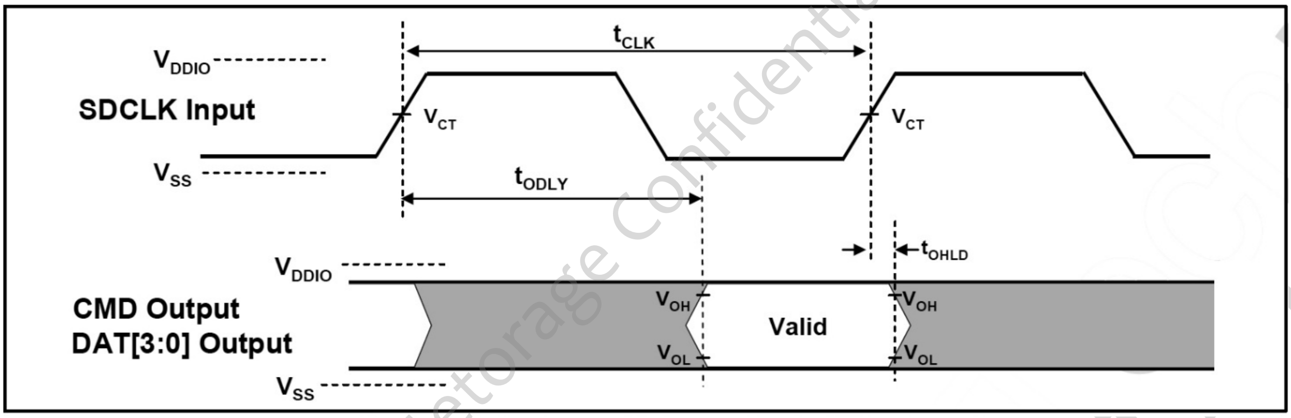


Figure 5-8 Output Timing of Fixed Data Window

Table 5-12 Output Timing of Fixed Data Window (SDR12, SDR25, SDR50)

Symbol	Min	Max	Unit	Remark
t_{ODLY}	-	7.5	ns	t_{CLK}>=10.0ns, C_L=30pF, using driver Type B, for SDR50
t_{ODLY}	-	14	ns	t_{CLK}>=20.0ns, C_L=40pF, using driver Type B, for SDR25 and SDR12
T_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min.), C_L=15pF

Output(SDR104 Modes)

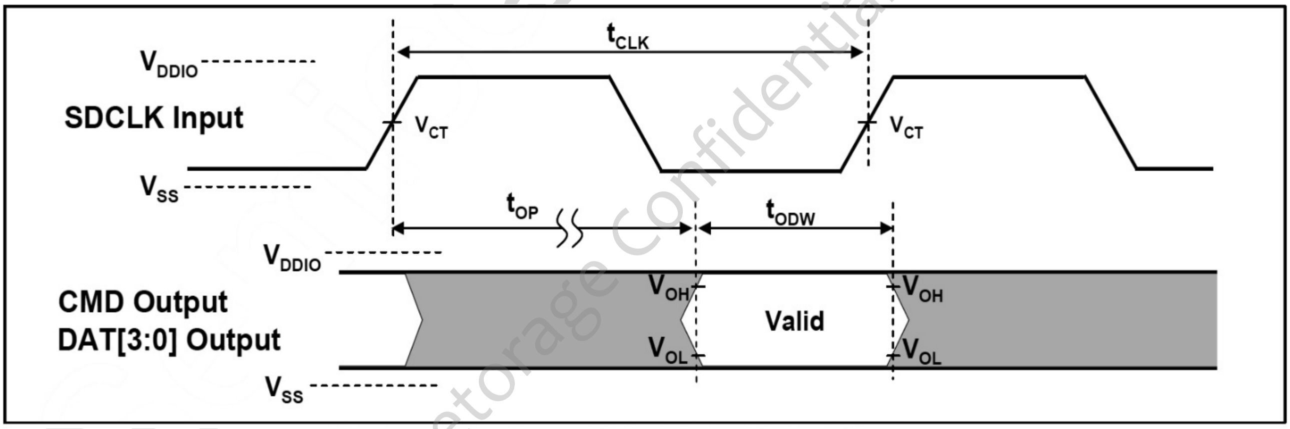


Figure 5-9 Output Timing of Variable Data Window

Table 5-13 Output Timing of Variable Window (SDR104)

Symbol	Min	Max	Unit	Remark
t_{OP}	0	2	UI	Card Output Phase
Δt_{OP}	-350	+1550	ps	Delay variable due to temperature change after tuning
t_{ODW}	0.60	-	UI	t_{ODW} = 2.88ns at 208MHz

5.4.4. microSD Interface Timing (DDR50 Mode)

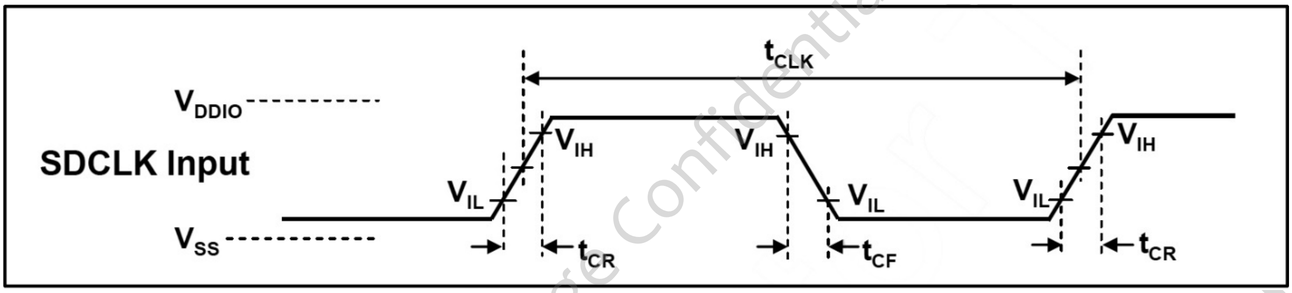


Figure 5-10 Clock Signal Timing

Table 5-14 Clock Signal Timing

Symbol	Min	Max	Unit	Remark
t_{CLK}	20	-	ns	50MHz (Max.), Between rising edge
t_{CR}, t_{CF}	-	0.2* t_{CLK}	ns	t_{CR}, t_{CF} < 4.00ns (max.) at 50MHz, C_{CARD}=10pF
Clock Duty	45	55	%	-

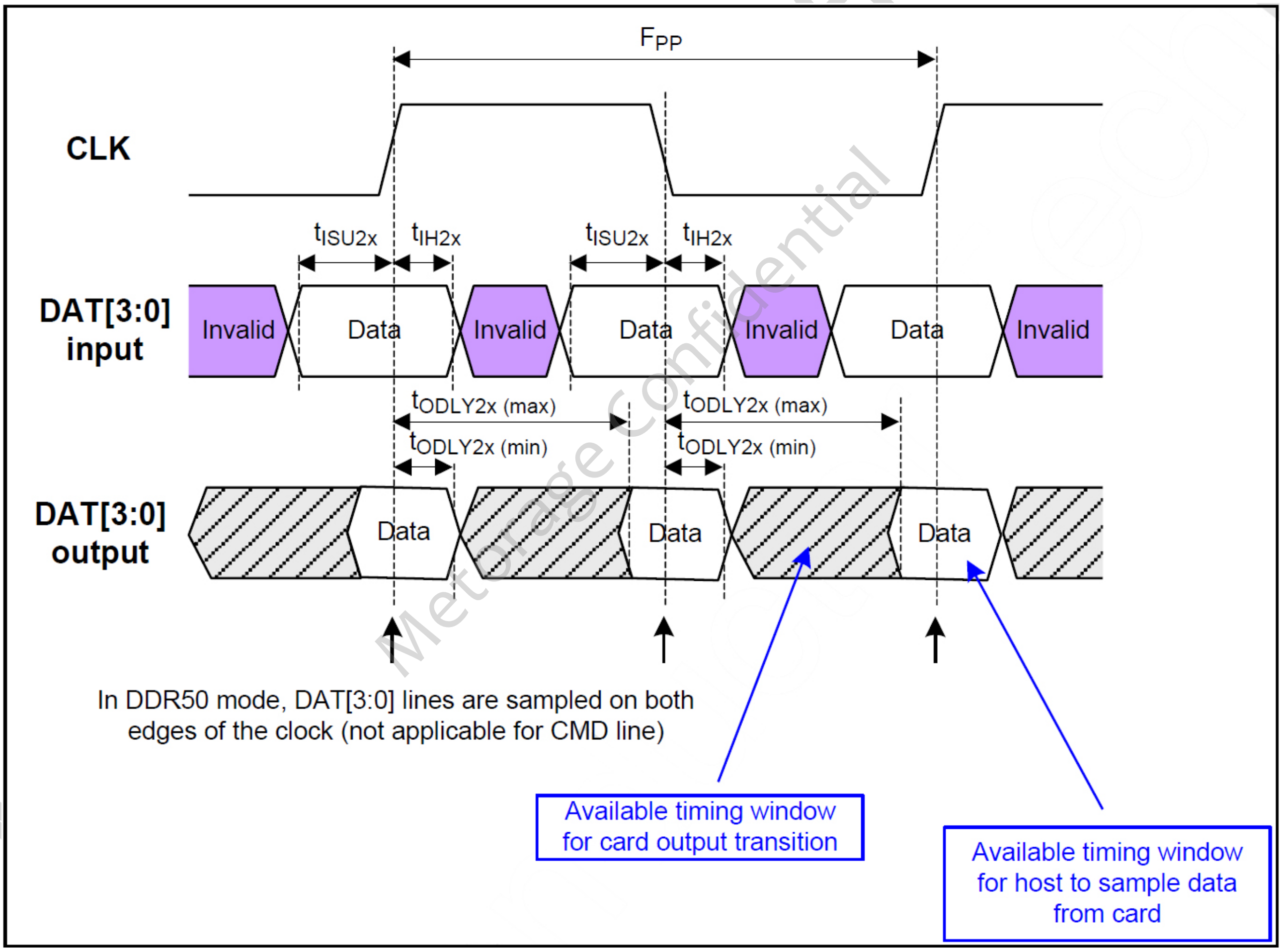


Figure 6-11 Timing Diagram DAT Inputs/Outputs Referenced to CLK in DDR50 Mode

Table 5-15 Bus Timings – Parameters Values (DDR50 Mode)

Parameter	Symbol	Min	Max	Unit	Remark
Input CMD (referenced to CLK rising edge)					
Input set-up time	t_{ISU}	3	-	ns	$C_{card} \leq$ 10 pF (1 card)
Input hold time	t_{IH}	0.8	-	ns	$C_{card} \leq$ 10 pF (1 card)
Output CMD (referenced to CLK rising edge)					
Output Delay time during Data Transfer Mode	t_{ODLY}	-	13.7	ns	$C_L \leq$ 30 pF (1 card)
Output Hold time	T_{OH}	1.5	-	ns	$C_L \geq$ 15 pF (1 card)
Inputs DAT (referenced to CLK rising and falling edges)					
Input set-up time	t_{ISU2x}	3	-	ns	$C_{card} \leq$ 10 pF (1 card)
Input hold time	t_{IH2x}	0.8	-	ns	$C_{card} \leq$ 10 pF (1 card)
Outputs DAT (referenced to CLK rising and falling edges)					
Output Delay time during Data Transfer Mode	t_{ODLY2x}	-	7.0	ns	$C_L \leq$ 25 pF (1 card)
Output Hold time	T_{OH2x}	1.5	-	ns	$C_L \geq$ 15 pF (1 card)

6. HOST SYSTEM DESIGN GUILDELINES

6.1. Efficient Data Writing to microSD Memory Card

In order to optimize sequential writing performance and WAF (Write Amplification Factor), it is recommended to use allocation unit (AU) writing.
It is recommended that Multiple_Block_Write shall be used as a command for writing data, and the size of data written by each command should be the FAT cluster x n (n: integer)

6.1.1. Write_Single_Block and Write_Multiple_Block

Write single block (CMD24) was written by one sector (512Bytes), which is suitable to write small area such like updating file system area (FAT). Besides, write multiple blocks (CMD25) is a command for writing data to blocks that have sequential address per command, which is suitable to write large area such as user data. Write multiple blocks with a cluster unit (512Byte x 128 Sectors = 64KByte) in the file system is an efficient access to the flash memory, it is obviously to provide higher speed to compared to single write block.
And it could be estimated that microSD card internal process would be reduced to save power consumption and flash write amplification factor, that is why the efficient data writing was recommended. To avoid the command issued by 512Bytes with single write block, software processes in the host device become faster. For this operation, check the sectors in the microSD card and file system as Figure 7-1

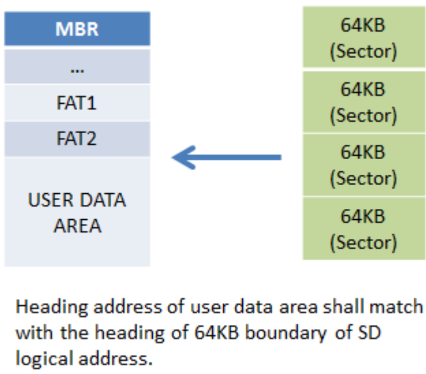


Figure 6-1 Matching between logical address and file system

Note: Large Cluster unit is better for performance and WAF, for example, 128KB, 256KB or 512KB. Large cluster unit also can save write command numbers and few transfer time.

6.2. Basic Process of Error Handling

6.2.1. Retry Process

Execute the process by sending commands again, especially for signal issue between card and host.

6.2.2. Recovery Process

Confirm card status is in Transfer State, if card status is not in Transfer State, please issue Stop command to recover it and execute or continue flow. If there was UECC during read/write status, we could use recovery process to recover it.

6.2.3. Tuning Write Command Process

In order to adjust Host CMD and CLK timing, the way is issue tuning command to confirm what the device response and data was received by host. Based on the response, host was adjusting the timing step by step and recording the pass range. Through this flow host could adjust the appropriate timing settings to avoid unexpected handshaking issue.

6.2.4. Tuning Read Command Process

In order to adjust Host CLK and DAT timing, the way is issue tuning command to confirm what the device response and data was received by host. Based on the response, host was adjusting the timing step by step and recording the pass range. Through this flow host could adjust the appropriate timing settings to avoid unexpected handshaking issue.

6.2.5. Exception Handling Process

No doubt that sometimes we would face all error handling above could not recover it successfully, and we could react based on the situation.

- If there was error in response, we could re-initialize the card.
- If it was signal issue, we could set up signal status by reading data and tuning command.

6.3. Common Error Handling in SPI and SD mode

6.3.1. Time-out

Run the Retry Process. No response from CMD, it might be signal or status got problem. To avoid the infinite loop, implement a retry counter in the host so that, if the retry counter expires, the exception handling starts in the host.

6.3.2. Error Detect (CMD CRC Error)

Run the Recovery Process. If it got second time failure with CRC, the setting might be too margin to receive response stably. Suggestion is use tuning write command to fix timing and then retry it.

6.3.3. Error Detect (Other Error) in SPI and SD mode

Run the Recovery Process.

6.3.4. Others

Most errors could be recovered by running the Recovery Process, let card come into Transfer State and then executing the flow we planned. If it does not work, please use exception method to come back initial state.

6.4. Data Error Handling in SPI and SD mode

6.4.1. Time-out

Run the Recovery Process. While the state was recovered, run the flow again.

6.4.2. Read CRC16 Error

Run the Recovery Process. If it got second time failure with CRC, the setting might be too margin to receive data stably. Suggestion is use tuning read date to fix timing and then retry it.

6.4.3. Write CRC Status Error

Run the Recovery Process. If it got second time failure with CRC, the setting might be too margin to receive CRC status stably. Suggestion is use tuning read date to fix timing and then retry it.

6.4.4. Others

Most errors could be recovered by running the Recovery Process, let card come into Transfer State and then executing the flow we planned.

6.5. Multiple Block Write (CMD25) Process

- If Response is ADDRESS_OUT_OF_RANGE, please confirm writing address.
- If Response is DEVICE_IS_LOCKED, please stop writing data.
- If Response is COM_CRC_ERROR, run retry or tuning.

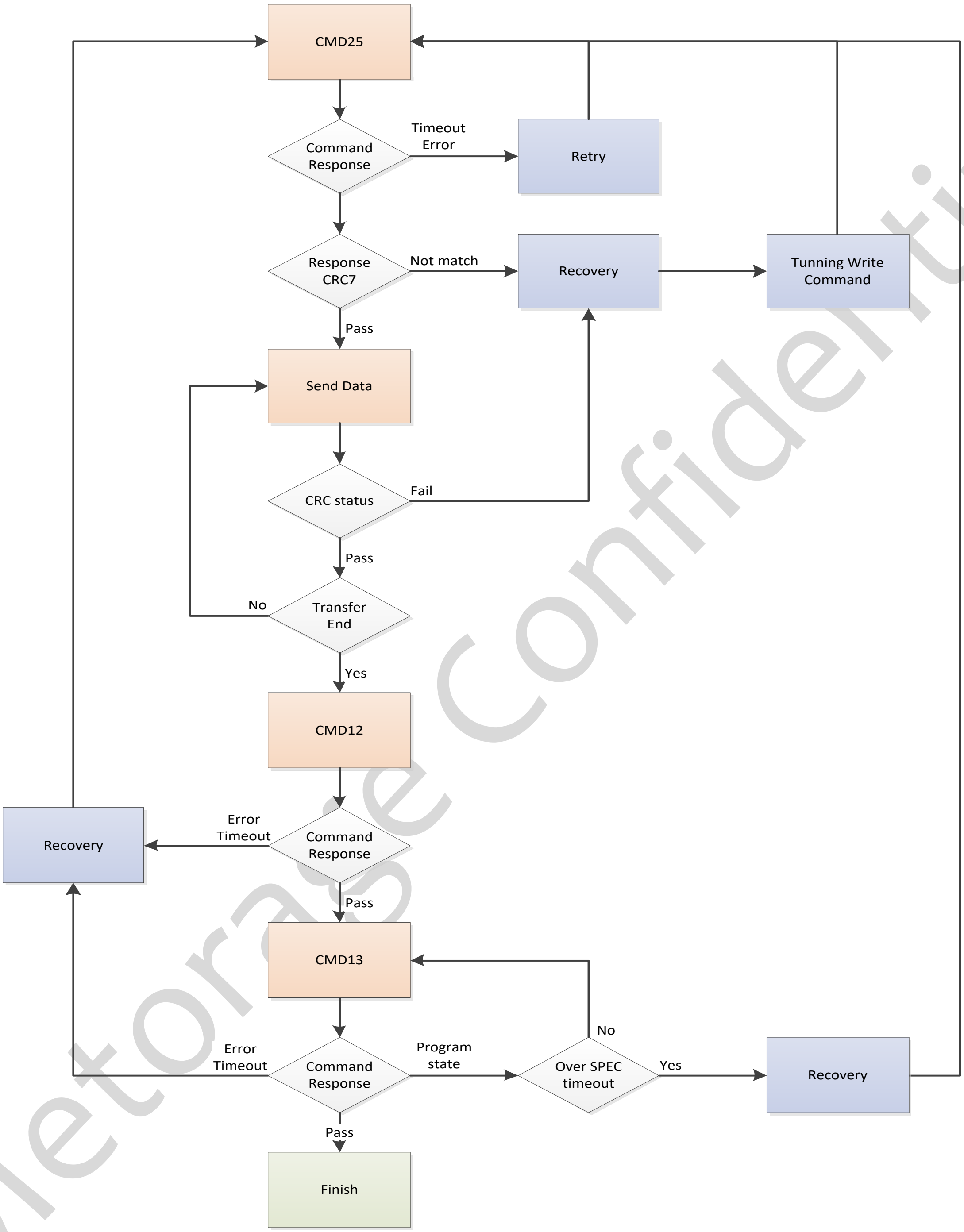


Figure 6-2 Multiple Write (CMD25) Error Handling

6.6. Retry Error handling

In order to avoid signal issue caused unexpected response from device, we could use Retry Process to fix it.

- Please make sure card state is in transfer state before issuing following commands.
- To avoid the infinite loop, implement a retry counter in the host.
- If the device could not respond to CMD13 normally, please run exception handling to recover card status.

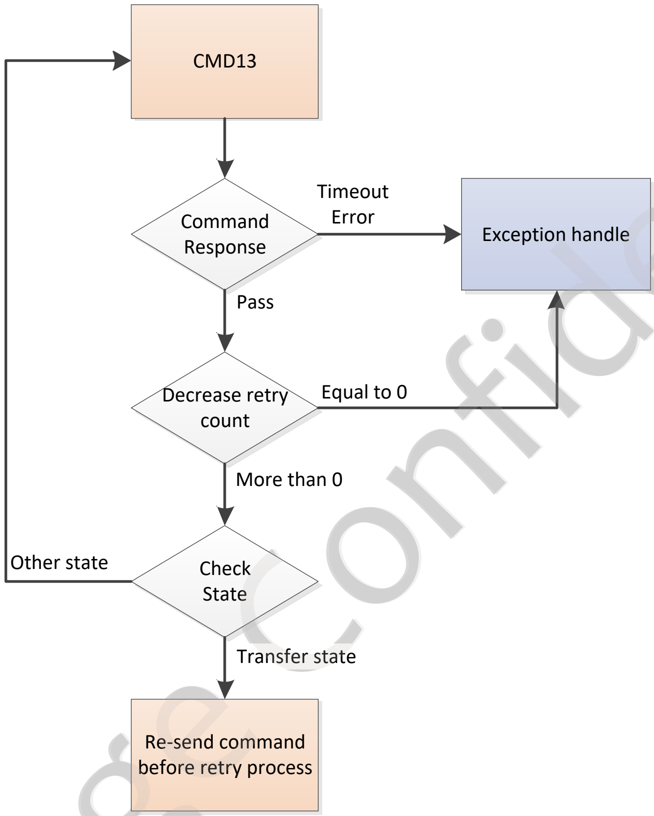


Figure 6-3 Retry Error Handling Process

6.7. Recovery Error Handling

Sometimes the device failure could not be recovered by Retry Process, it suggests to execute STOP Command (CMD12) to stop whole commands and response and then run following flow.

- Please confirm card status is in Transfer state
- In order to avoid infinite loops, host has to set up a retry counter number.

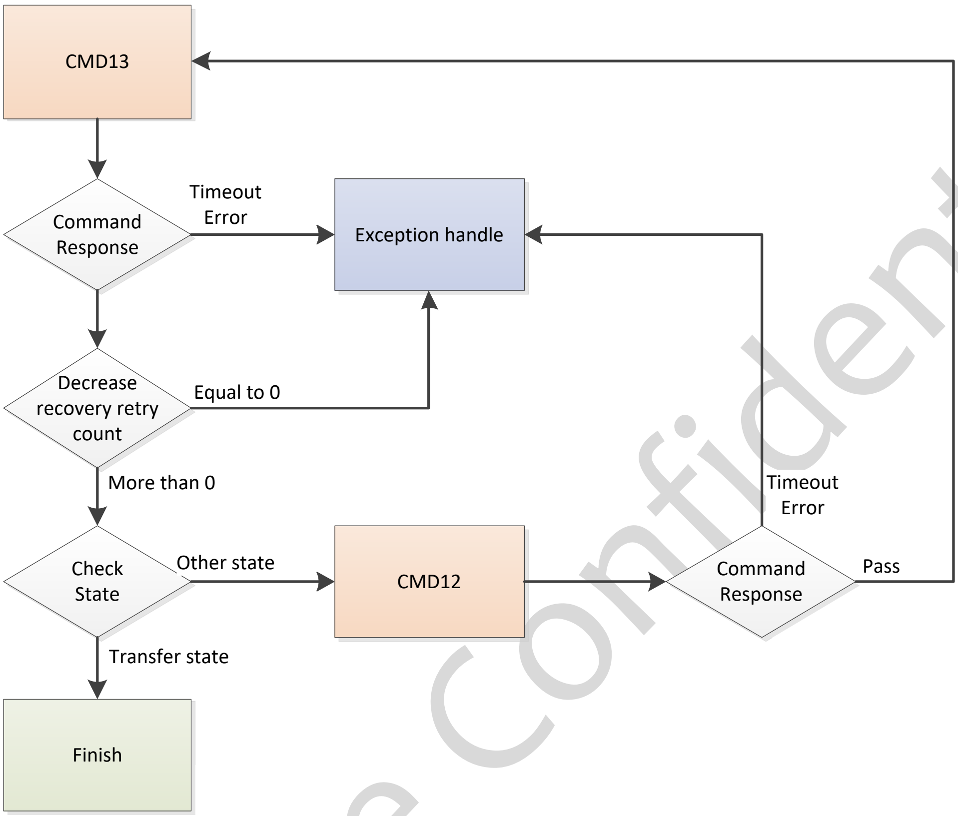


Figure 6-4 Recovery Error Handling Process

6.8. Tuning Write Command Error Handling

Reconfirm the card's pass range, to make sure card could receive host commands.

- If there was no any pass window, it might be connect issue or signal issue
- Pass Range depends on frequency level, higher frequency makes fewer pass range

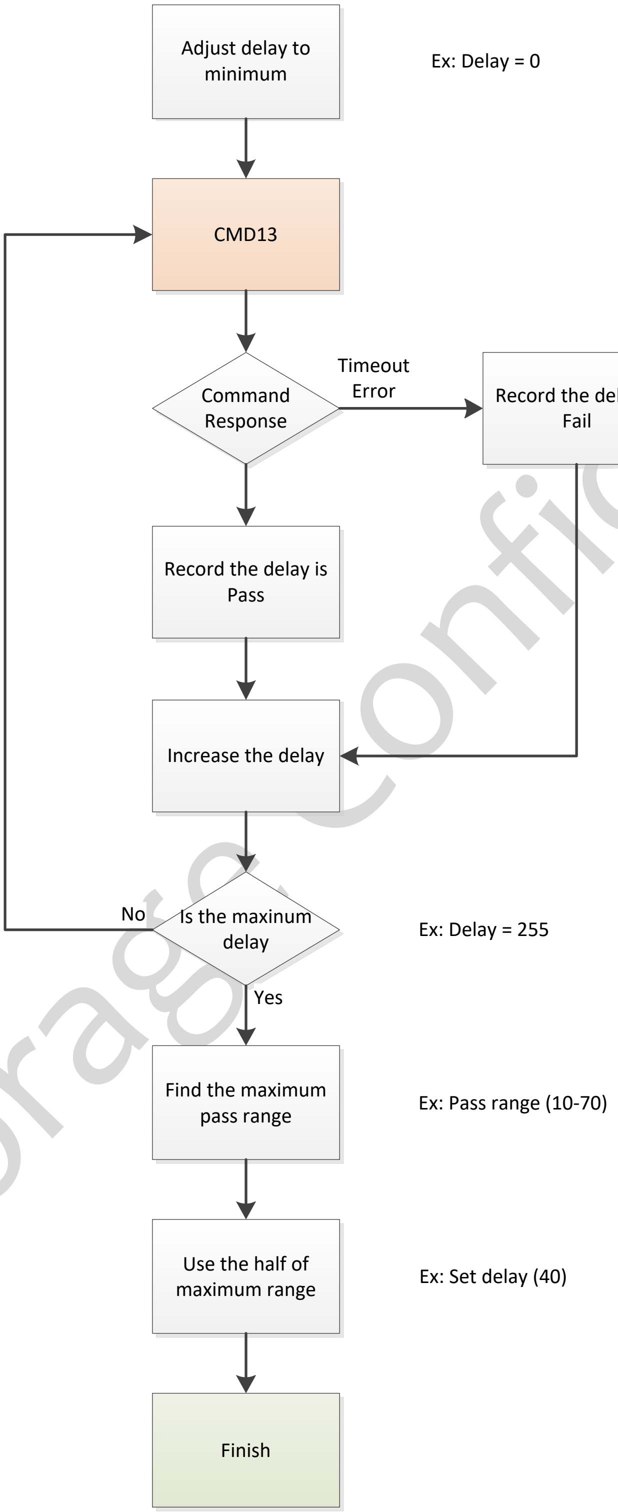


Figure 6-5 Tuning Write Command Error Handling Process

6.9. Exception Error Handling

- Error in Card's response or data output time-out, it could re-initialize the card.
- If there was CMD CRC7 issue, it could use tuning write command process to find out appropriate timing.
- If there was DAT CRC16 issue, it could use tuning read command process to find out appropriate timing.

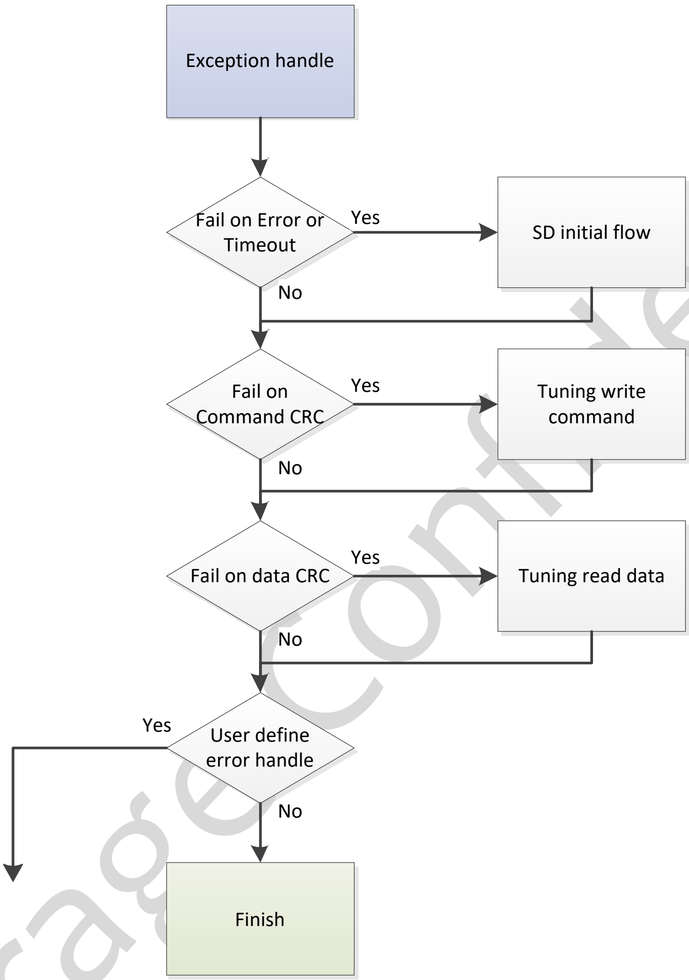


Figure 6-6 Exception Error Handling Process

Metorage
Metorage Semiconductor technology Co., Ltd #1201-1206 12F Block11, Cloud Park Phase2 Bantian Street, Longgang District, Shenzhen CHINA
深圳星火半导体科技有限公司 深圳市龙岗区坂田街道岗头社区天安云谷产业园二期（02-08地块）11栋 1201-1206

6.10. Multiple Blocks Read (CMD18) Error Handling Process

- If card responded ADDRESS_OUT_OF_Range, please check writing address
- If card responded DEVICE_IS_LOCKED, please stop writing data
- If card responded COM_CRC_ERROR, run Retry or Tuning Process

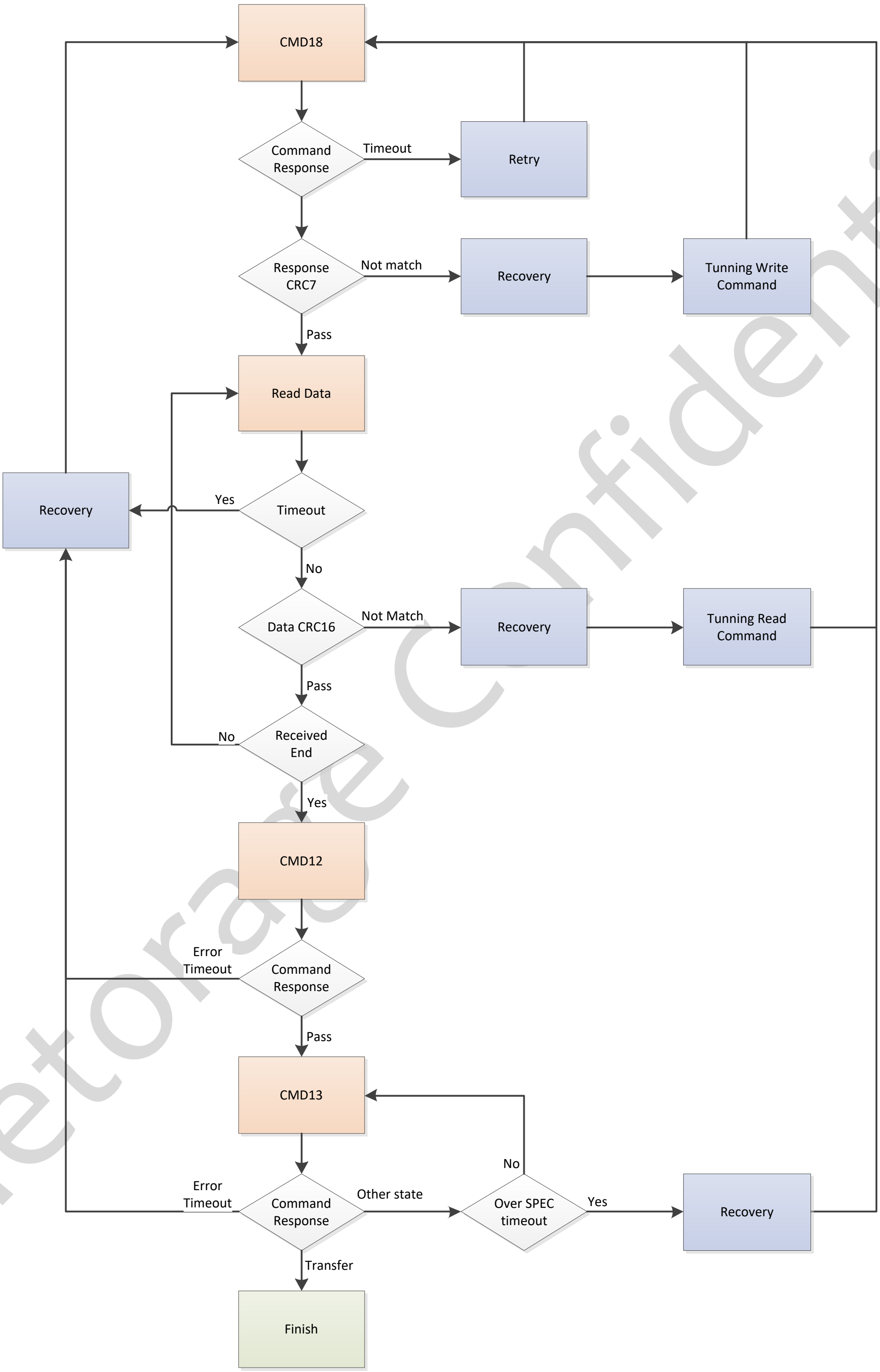


Figure 6-7 Multiple Blocks Read (CMD18) Error Handling Process

6.11. Tuning Read Data Error Handling

Reconfirm the card's pass range, to make sure host could receive card's Response and Data.

- If there was no any pass window, it might be connect issue or signal issue
- Pass Range depends on frequency level, higher frequency makes fewer pass range

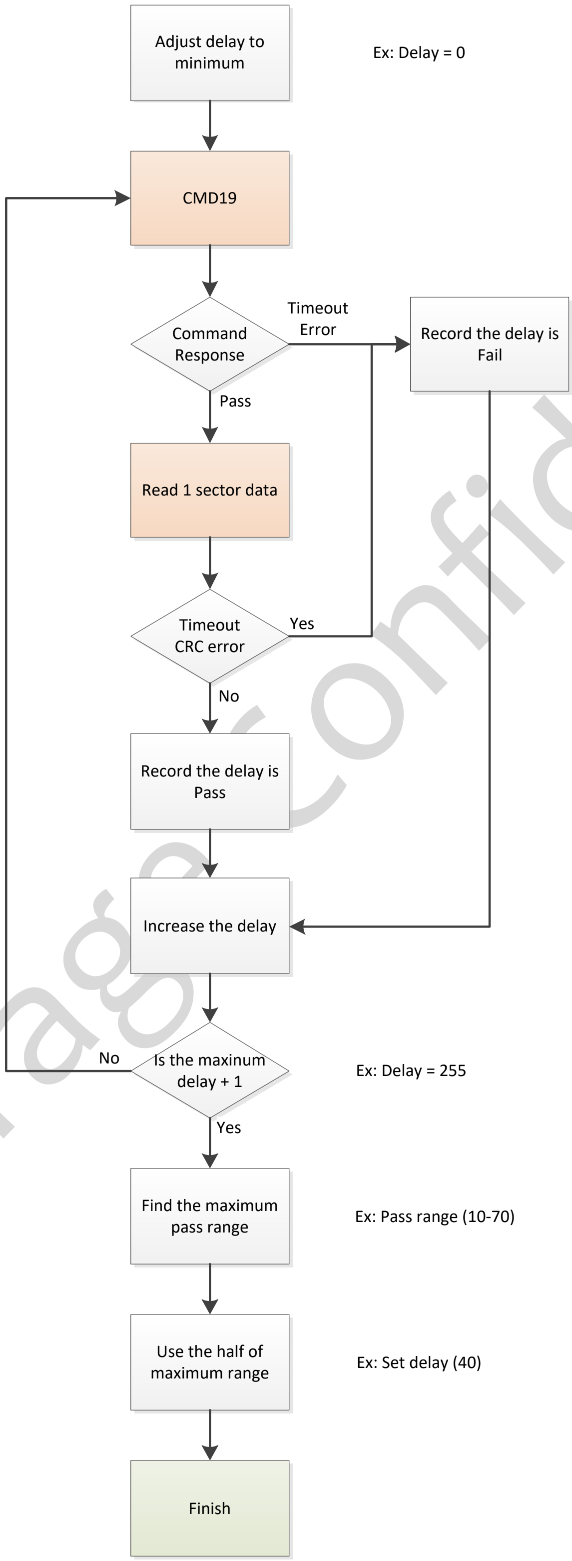


Figure 6-8 Tuning Read Data Error Handling Process

7. CARD REGISTERS

7.1. Card Identification Register (CID)

The Card Identification (CID) register is 128 bit wide. It contains the card identification information used during the card identification phase. Every individual flash card shall have a unique identification number.

The structure of the CID register is defined in the following table.

Table 7-1 Card Identification Register (CID) fields

CID Bit	Width	Name	Field	Code
[127:120]	8	Manufacture ID	MID	B5h
[119:104]	16	OEM/Application ID	OID	4D56h
[103:64]	40	Product Name	PNM	4D45544F52h
[63:56]	8	Product Revision	PRV	---
[55:24]	32	Product Serial Number	PSN	---
[23:20]	4	Reserved	---	---
[19:8]	12	Manufacturing Date	MDT	---
[7:1]	7	CRC7 check sum	CRC	---
[0]	1	Not used, always"1	---	---

All contents in the CID table are programmable; Manufacturers can update the CID data through utility. Manufacturers should license MID and OID field form the SD Card Association(SDA).

7.2. Card Specific Data Register (CSD)

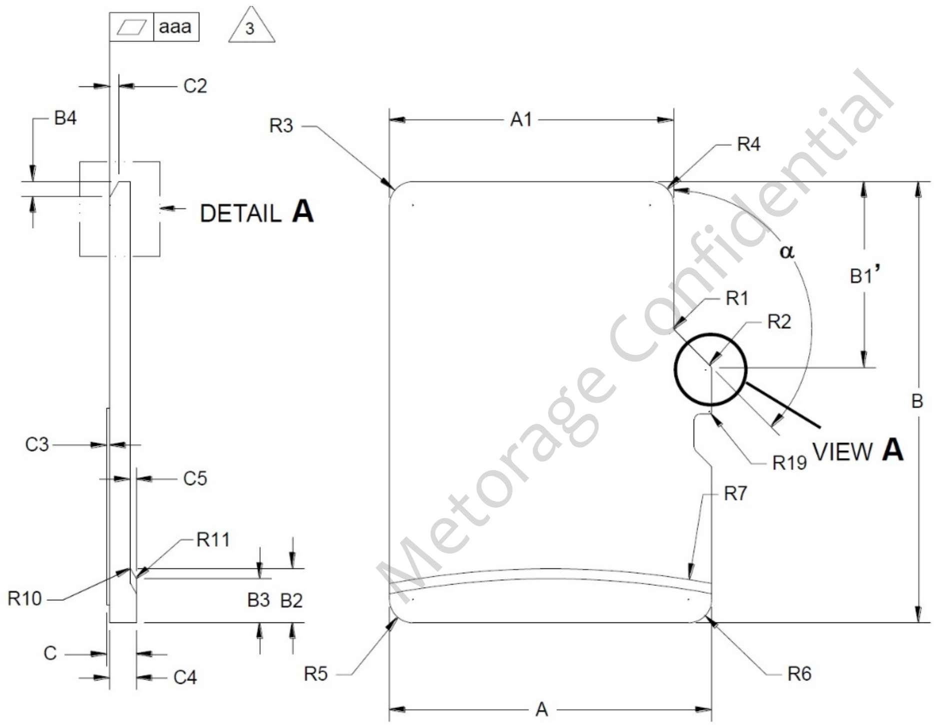
The Card-Specific Data register provides information regarding access to the card contents. The CSD defines the data format, error correction type, maximum data access time, whether the DSR register can be used, etc. The programmable part of the register (entries marked by W or E, see below) can be changed by CMD27. The CSD Table Version 2.0(as shown below) is applied to SDHC and SDXC Cards. Note that bits [15:0] are programmable by the host side. Refer to the SD specification for detailed information.

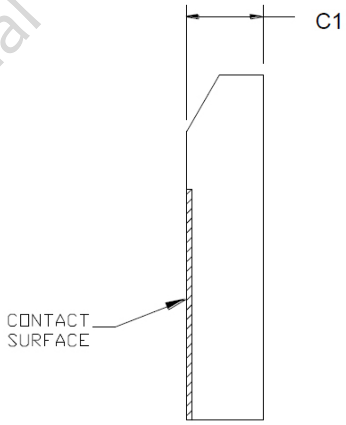
Table 7-2 Card Specific Data Register (CSD) fields

CSD Bit	Width	Name	Field	Code	Note
[127:126]	2	CSD structure	CSD_STRUCTURE	01 b	Ver2.0
[125:120]	6	Reserved	---	---	---
[119:112]	8	Data read access-time 1	TAAC	0E h	1ms
[111:104]	8	Data read access-time2 in CLK cycles(NSA*100)	NSAC	00 h	---
[103:96]	8	Max data transfer rate	TRAN_SPEED	32 h 5A h 0B h 2B h	Default High speed SDR50/DDR50 SDR104
[95:84]	12	Card command classes	CCC	5B5 h	0,2,4,5,7,8,10
[83:80]	4	Max. read data block length	READ_BL_LEN	9 h	512 Byte
[79]	1	Partial block read allowed	READ_BL_PARTIAL	0 b	No
[78]	1	Write block misalignment	WRITE_BLK_MISALIGN	0 b	No
[77]	1	Read block misalignment	READ_BLK_MISALIGN	0 b	No
[76]	1	DSR implemented	DSR_IMP	0 b	No
[75:70]	6	Reserve	---	---	---
[69:48]	22	Device size	C_SIZE	See Note	803Fh-16GB C05Fh-24GB 180BFh-48GB 3017Fh-96GB
[47]	1	Reserved	---	---	---
[46]	1	Erase single block enable	ERASE_BLK_EN	1 b	Yes
[45:39]	7	Erase sector size	SECTOR_SIZE	7F h	128
[38:32]	7	Write protect group size	WP_GRP_SIZE	00 h	Not supported
[31]	1	Write protect group enable	WP_GRP_ENABLE	0 b	No
[30:29]	2	Reserved	---	0 b	---
[28:26]	3	Write speed factor	R2W_FACTOR	010 b	x4
[25:22]	4	Max. write data block length	WRITE_BL_LEN	9 h	512 Byte
[21]	1	Partial block write allowed	WRITE_BL_PARTIAL	0 b	No
[20:16]	5	Reserved	---	---	---
[15]	1	File format group	FILE_FORMAT_GRP	0 b	Not use
[14]	1	Copy flag	COPY	0 b	Original
[13]	1	Permanent write protection	PERM_WRITE_PROTECT	0 b	Not Protected
[12]	1	Temporary write protection	TMP_WRITE_PROTECT	0 b	Not Protected
[11:10]	2	File format	FILE_FORMAT	00 b	Not use
[9:8]	2	Reserved	---	---	---

[7:1]	7	CRC	CRC	CRC7	---
[0]	1	Not used,always'1'	---	1 b	---

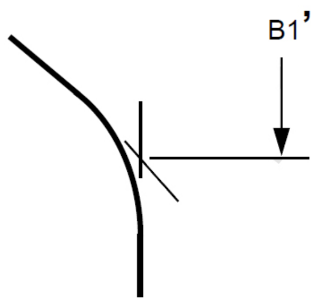
8. PHYSICAL DIMENSION



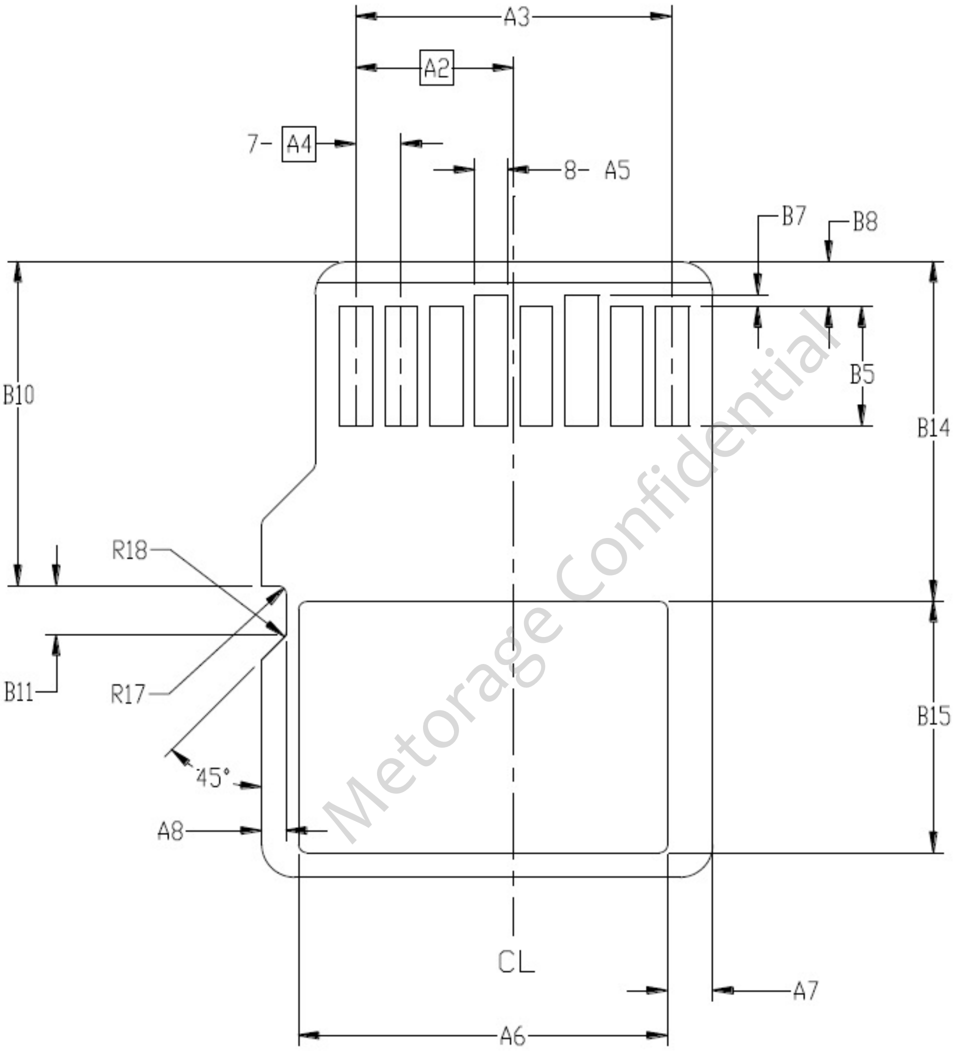


DETAIL A

VIEW A



As measurement point is changed like as VIEW A, symbol B1 is changed to symbol B1'. There is no modification in mechanical dimension.



Type A

	COMMON DIMENSION			
SYMOL	MIN	NOM	MAX	NOTE
A	10.90	11.00	11.10	
A1	9.60	9.70	9.80	
A2	-	3.85	-	BASIC
A3	7.60	7.70	7.80	
A4	-	1.10	-	BASIC
A5	0.75	0.80	0.85	
A6	-	-	8.50	
A7	0.90	-	-	
A8	0.60	0.70	0.80	
B	14.90	15.00	15.10	
B1’	6.13	6.23	6.33	
B2	1.64	1.84	2.04	
B3	1.30	1.50	1.70	
B4	0.42	0.52	0.62	
B5	2.80	2.90	3.00	
B7	0.20	0.30	0.40	

Notes:
1. DIMENSIONING and TOLERANCING per ASME Y14.5M-1994.
2. Dimensions are in millimeters.
3. (△) COPLANARITY is additive to C_1 MAX thickness.
4. (△) All edges shall not be sharp as tested per UL1439 "Test for Sharpness of Edges on Equipment."
5. Refer to Appendix E about test method of warpage.
6. As measurement point is changed, symbol B_1 is changed to symbol B_1’.
7. C_4 and C_5 are added from Version 4.00.

B8	1.00	1.10	1.20	
B10	7.80	7.90	8.00	
B11	1.10	1.20	1.30	
B14	8.20	-	-	
B15	-	-	6.20	
C	0.90	1.00	1.10	
C1	0.60	0.70	0.80	
C2	0.20	0.30	0.40	
C3	0.00	-	0.15	
C4	0.80	-	1.10	
C5	0.15	-	-	
R1	0.20	0.40	0.60	
R2	0.20	0.40	0.60	
R3	0.70	0.80	0.90	
R4	0.70	0.80	0.90	
R5	0.60	0.80	0.90	
R6	0.60	0.80	0.90	
R7	29.50	30.00	30.50	
R10	-	0.20	-	
R11	-	0.20	-	
R17	0.10	0.20	0.30	
R18	0.20	0.40	0.60	
R19	0.05	-	0.20	
α	133°	135°	137°	
aaa	-	-	0.10	

9. APPENDIX

9.1. Endurance characteristic

3,000cycles/block (nominal value： under specified conditions)

*This value is not guaranteed