

General Description

The WSP11N10T is the highest performance trench Dual N-Ch MOSFET with extreme high cell density, which provide excellent R_{DS(on)} and gate charge for most of the synchronous buck converter applications.

The WSP11N10T meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent C_{dv/dt} effect decline
- Green Device Available

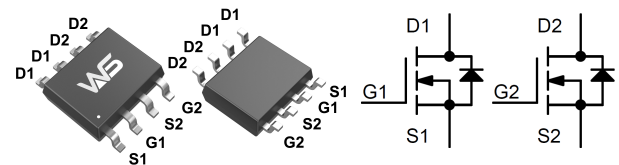
Product Summary

BVDSS	R _{DS(on)}	I _D
100V	70mΩ	12A

Applications

- High Frequency Point-of-Load Synchronous Buck Converter for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- Load Switch

SOP-8 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	100	V
V _{GS}	Gate-Source Voltage	±20	V
I _D @T _C =25°C	Continuous Drain Current, V _{GS} @ 10V ¹	12	A
I _D @T _C =100°C	Continuous Drain Current, V _{GS} @ 10V ¹	6.0	A
I _{DM}	Pulsed Drain Current ²	35	A
EAS	Single Pulse Avalanche Energy ³	6.25	mJ
I _{AS}	Avalanche Current	5	A
P _D @T _A =25°C	Total Power Dissipation ⁴	1.5	W
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction-ambient ¹	---	85	°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹	---	62	°C/W

Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	100	---	---	V
ΔBV _{DSS} /ΔT _J	BVDSS Temperature Coefficient	Reference to 25°C, I _D =1mA	---	0.098	---	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =5A	---	70	95	mΩ
		V _{GS} =4.5V, I _D =3A	---	80	115	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =250uA	1.2	1.8	2.5	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	-5.52	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =100V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =100V, V _{GS} =0V, T _J =55°C	---	---	100	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	3.0	---	Ω
Q _g	Total Gate Charge (10V)	V _{DS} =50V, V _{GS} =10V, I _D =10A	---	12	---	nC
Q _{gs}	Gate-Source Charge		---	2.9	---	
Q _{gd}	Gate-Drain Charge		---	1.5	---	
T _{d(on)}	Turn-On Delay Time	V _{DD} =50V, V _{GEN} =10V, R _G =6Ω, I _D =1A, R _L =30Ω	---	11.8	---	ns
T _r	Rise Time		---	3.1	---	
T _{d(off)}	Turn-Off Delay Time		---	15	---	
T _f	Fall Time		---	4.5	---	
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz	---	1055	---	pF
C _{oss}	Output Capacitance		---	58	---	
C _{riss}	Reverse Transfer Capacitance		---	42	---	

Guaranteed Avalanche Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
EAS	Single Pulse Avalanche Energy ⁵	V _{DD} =50V, L=0.5mH, I _{AS} =5A	3	---	---	mJ

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _S	Continuous Source Current ^{1,6}	V _G =V _D =0V, Force Current	---	---	11	A
I _{SM}	Pulsed Source Current ^{2,6}		---	---	30	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =5A, T _J =25°C	---	---	1.1	V
t _{rr}	Reverse Recovery Time	IF=5A, dI/dt=100A/μs, T _J =25°C	---	21	---	nS
Q _{rr}	Reverse Recovery Charge		---	25	---	nC

Note :

- The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper, t<10sec.
- The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%
- The EAS data shows Max. rating. The test condition is V_{DD}=50V, V_{GS}=10V, L=0.5mH, I_{AS}=5A
- The power dissipation is limited by 150°C junction temperature
- The Min. value is 100% EAS tested guarantee.
- The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

Typical Characteristics

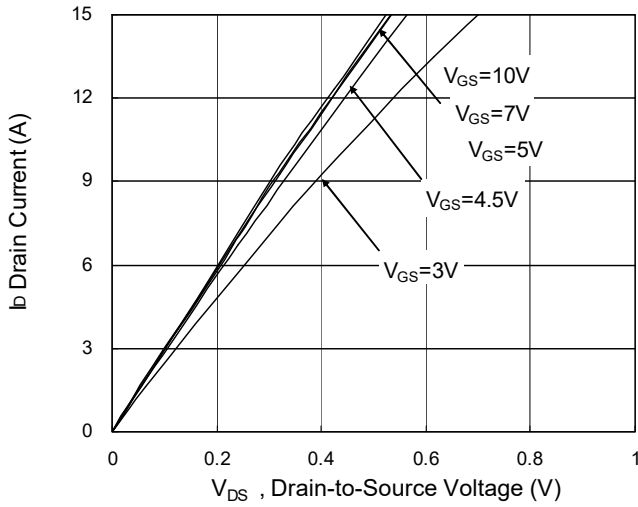


Fig.1 Typical Output Characteristics

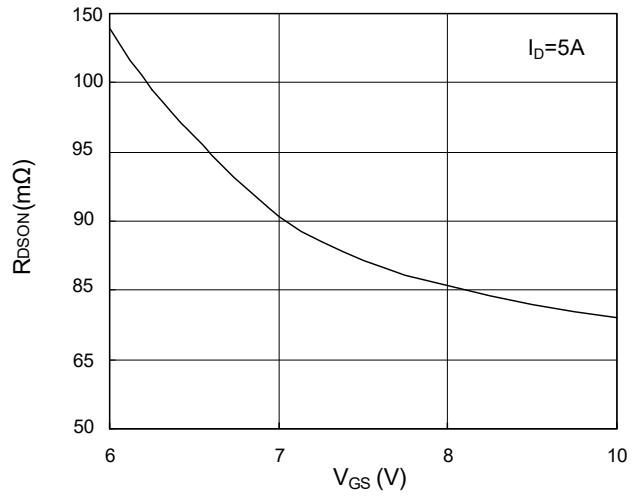


Fig.2 On-Resistance vs. Gate-Source

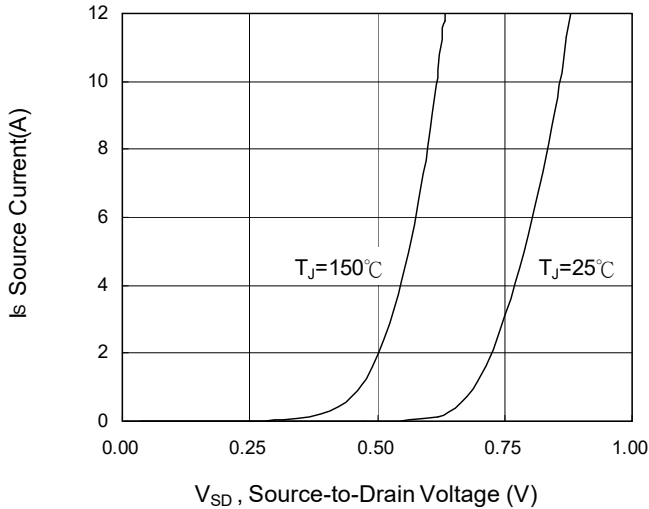


Fig.3 Forward Characteristics Of Reverse

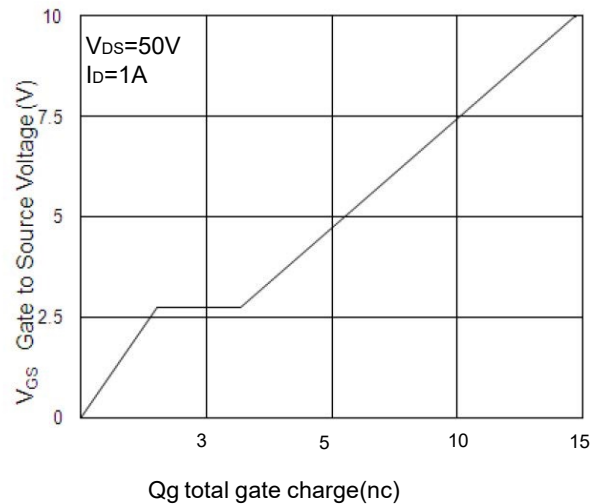


Fig.4 Gate-Charge Characteristics

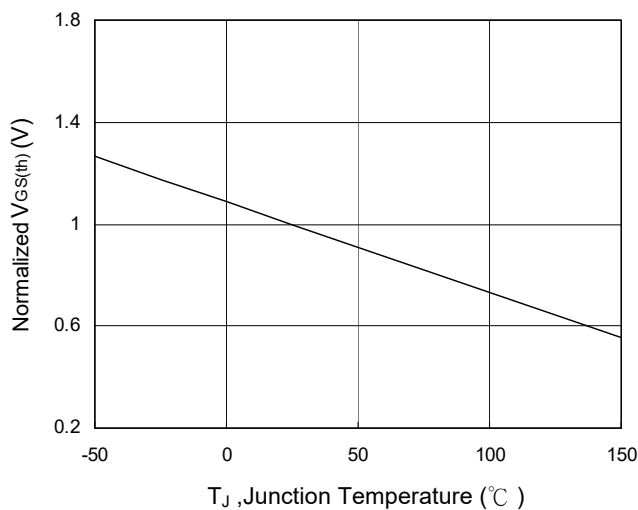


Fig.5 Normalized V_{GS(th)} vs. T_J

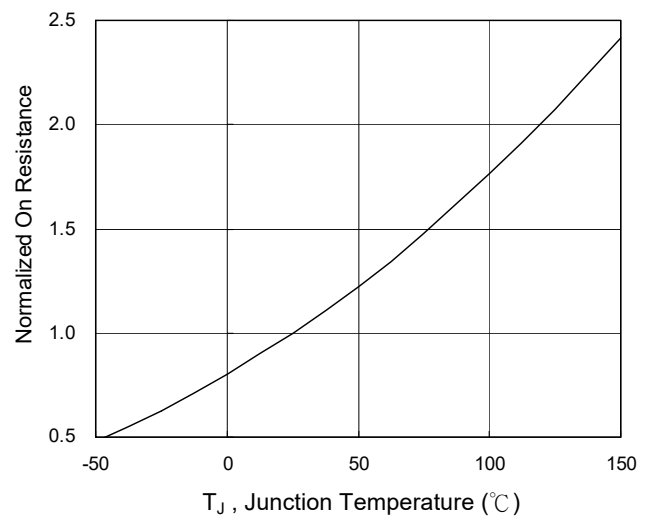


Fig.6 Normalized R_{DSON} vs. T_J

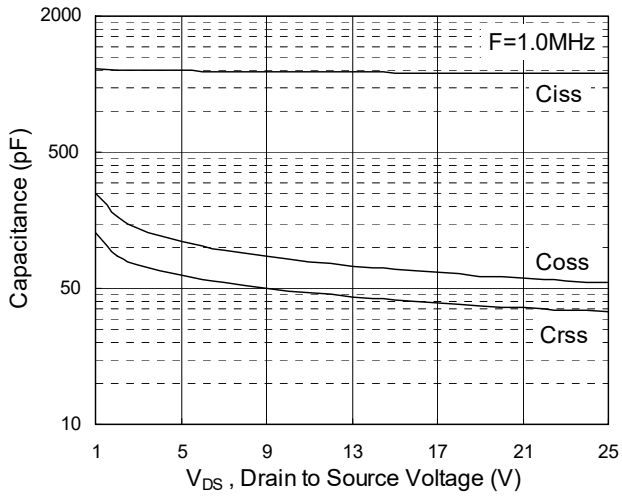


Fig.7 Capacitance

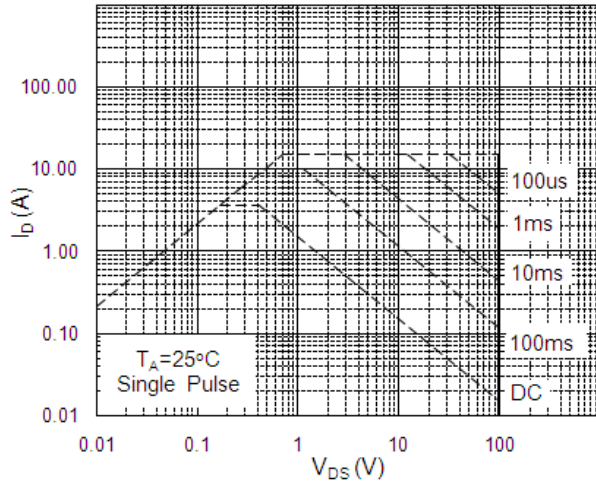


Fig.8 Safe Operating Area

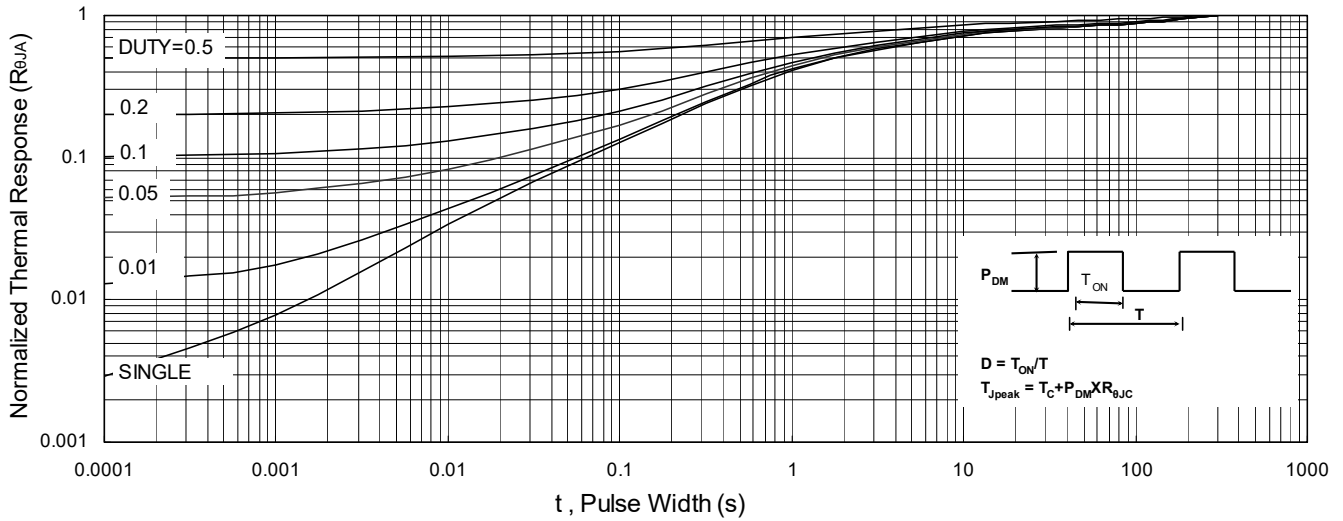


Fig.9 Normalized Maximum Transient Thermal Impedance

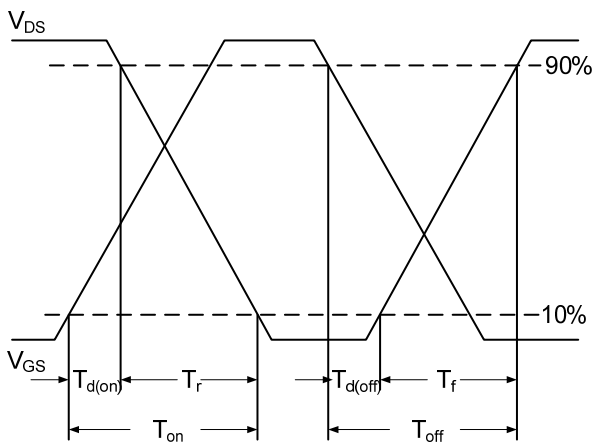


Fig.10 Switching Time Waveform

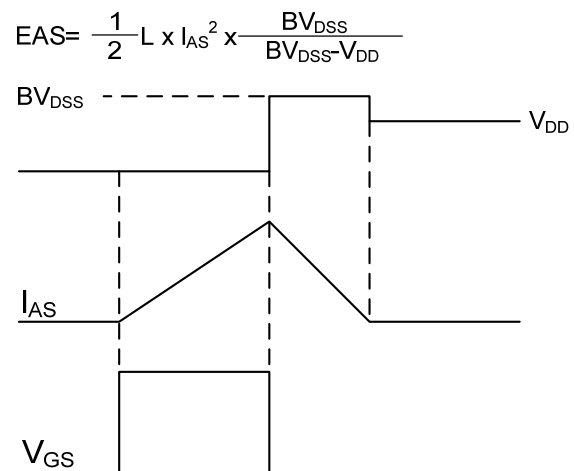


Fig.11 Unclamped Inductive Switching Waveform



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