General Description

WSD4280DN22 combines a P-Channel enhancement mode power MOSFET which is produced with high cell density and DMOS trench technology and a low forward voltage schottky diode. the tiny and thin outline saves PCB consumption.

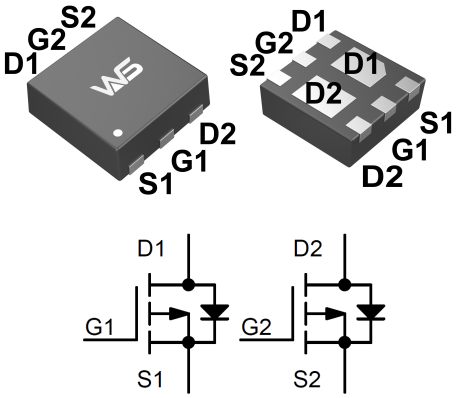
Applications

- Bidirectional blocking switch;
- DC-DC conversion applications;
- Li-battery charging;

Product Summery

V_{DSS}	R_{DSON}(typ.)	I_D
-15V	47mΩ@-4.5V	-4.6A
	61mΩ@-2.5V	
	90mΩ@-1.8V	

DFN2x2C-6_EP2_S Pin Configuration



Absolute Maximum Ratings (T_A = 25℃ Unless Otherwise Noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-15	V
V_{GS}	Gate-Source Voltage	±8	V
I_D@T_c=25℃	Continuous Drain Current, V_{GS} = -4.5V[1]	-4.6	A
I_{DM}	300μS Pulsed Drain Current, (V_{GS} =-4.5V)	-15	A
P_D	Power Dissipation Derating above T_A = 25°C (Note 2)	1.9	W
T_{STG},T_J	Storage Temperature Range	-55 to 150	℃
$R_{\theta JA}$	Thermal Resistance Junction-ambient [1]	65	℃/W
$R_{\theta JC}$	Thermal Resistance Junction-Case[1]	50	℃/W

Note1: Devices mounted on FR4 PCB with minima soldering pad;
Note2: For a single chip.

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=-250uA	-15	---	---	V
$\triangle BV_{DSS}/\triangle T_J$	BVDSS Temperature Coefficient	Reference to 25℃ , I_D=-1mA	---	-0.01	---	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=-4.5V , I_D=-1A	---	47	61	mΩ
		V_{GS}=-2.5V , I_D=-1A	---	61	80	
		V_{GS}=-1.8V , I_D=-1A	---	90	150	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =-250uA	-0.4	-0.62	-1.2	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	3.13	---	mV/℃
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-10V , V_{GS}=0V , T_J=25℃	---	---	-1	uA
		V_{DS}=-10V , V_{GS}=0V , T_J=55℃	---	---	-5	
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±12V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=-5V , I_D=-1A	---	10	---	S
R_g	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz	---	2	---	Ω
Q_g	Total Gate Charge (-4.5V)	V_{DS}=-10V , V_{GS}=-4.5V , I_D=-4.6A	---	9.5	---	nC
Q_{gs}	Gate-Source Charge		---	1.4	---	
Q_{gd}	Gate-Drain Charge		---	2.3	---	
$T_{d(on)}$	Turn-On Delay Time	V_{DD}=-10V , V_{GS}=-4.5V , R_G=1Ω I_D=-3.9A,	---	15	---	ns
T_r	Rise Time		---	16	---	
$T_{d(off)}$	Turn-Off Delay Time		---	30	---	
T_f	Fall Time		---	10	---	
C_{iss}	Input Capacitance	V_{DS}=-10V , V_{GS}=0V , f=1MHz	---	781	---	pF
C_{oss}	Output Capacitance		---	98	---	
C_{rss}	Reverse Transfer Capacitance		---	96	---	

Note :

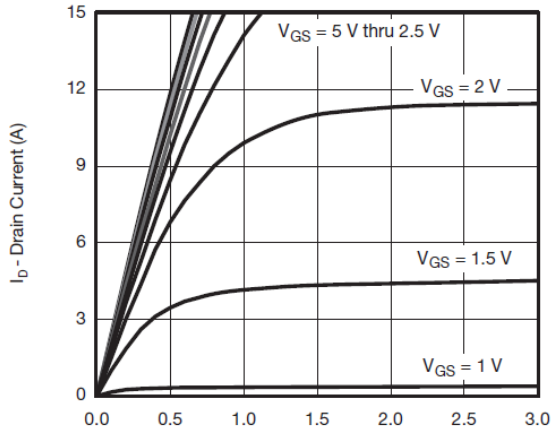
1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper, t≦10sec.

2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

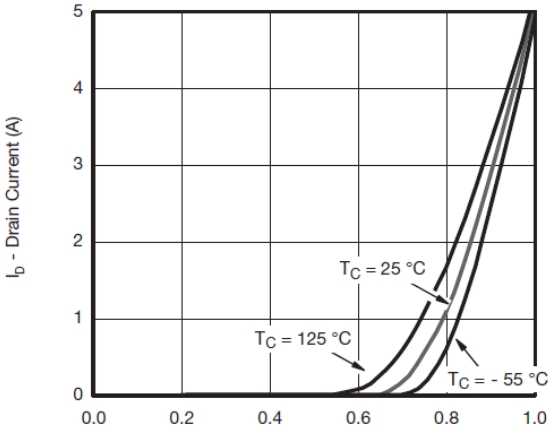
3.The power dissipation is limited by 150℃ junction temperature

4.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

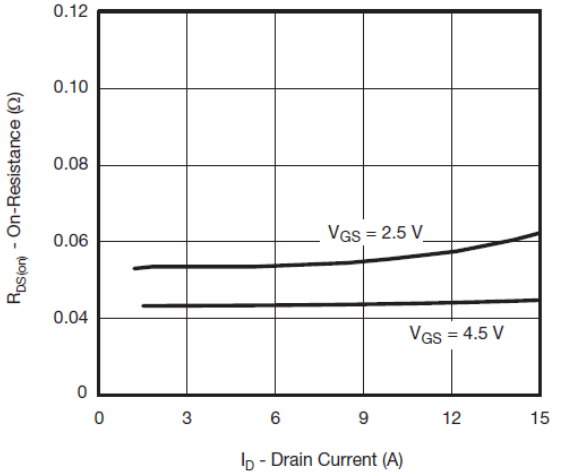
Typical Performance Characteristics of P-Channel MOSFET



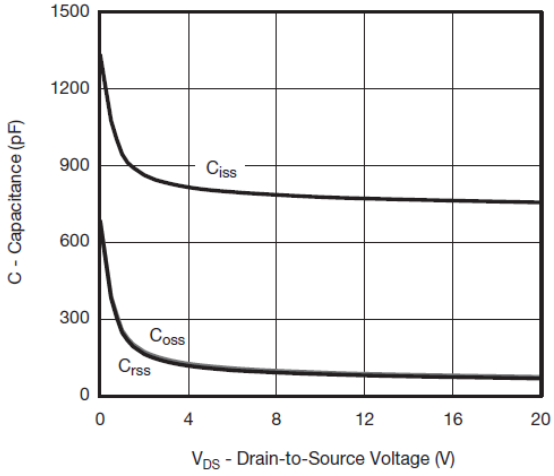
Output Characteristics



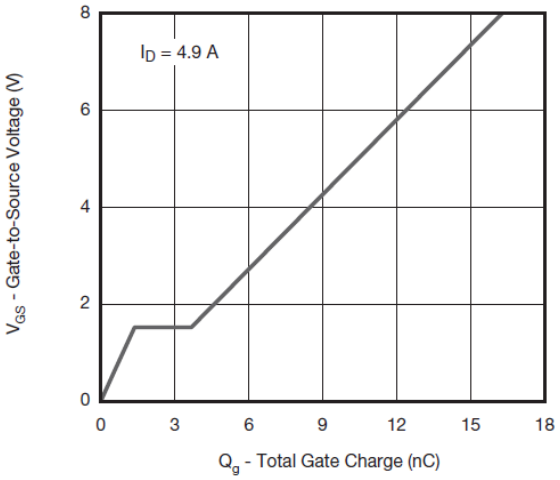
Transfer Characteristics



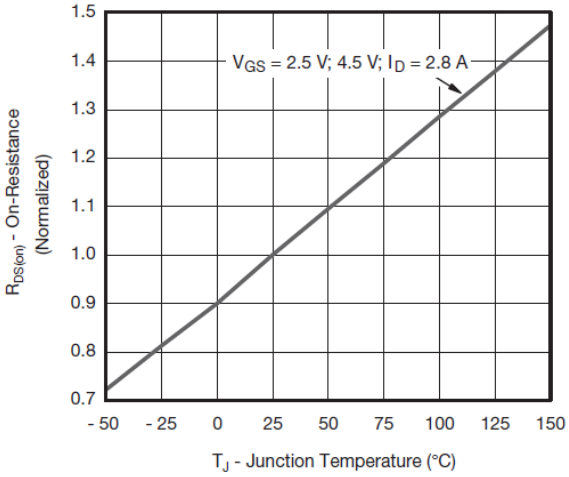
On-Resistance vs. Drain Current and Gate Voltage



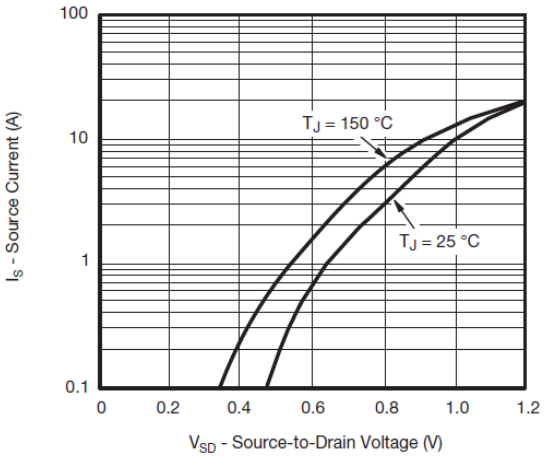
Capacitance



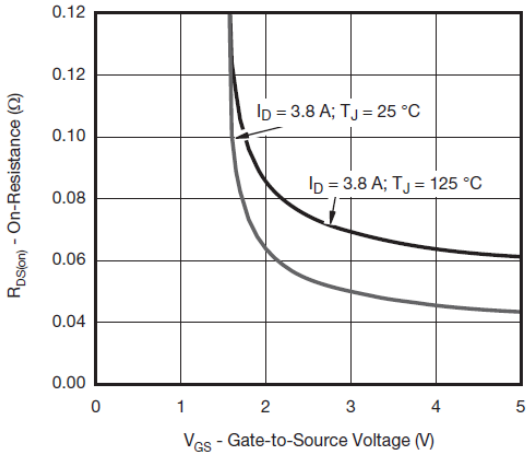
Gate Charge



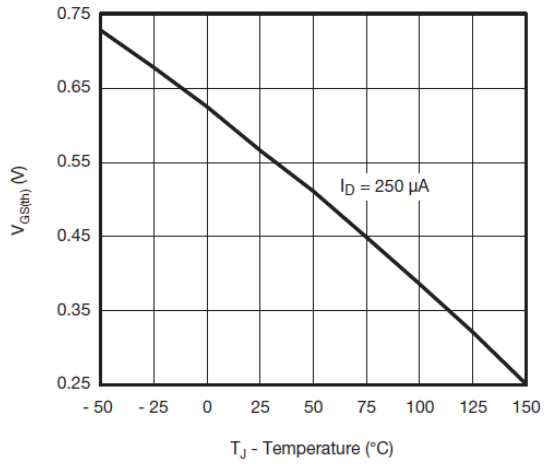
On-Resistance vs. Junction Temperature



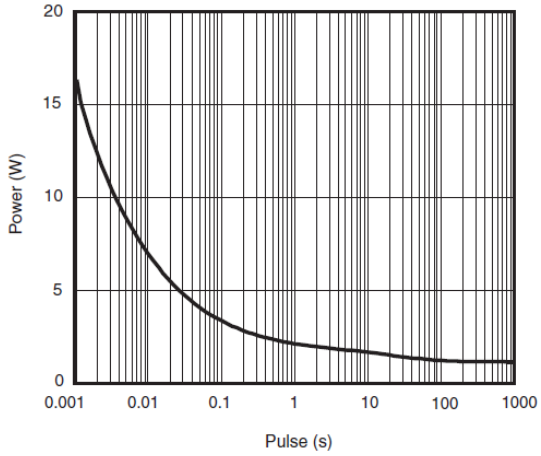
Source-Drain Diode Forward Voltage



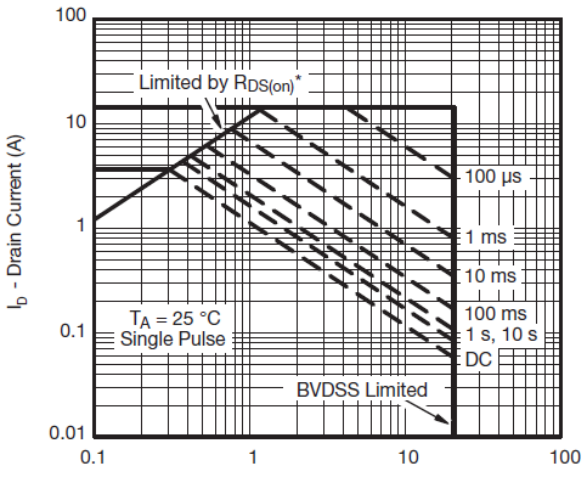
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



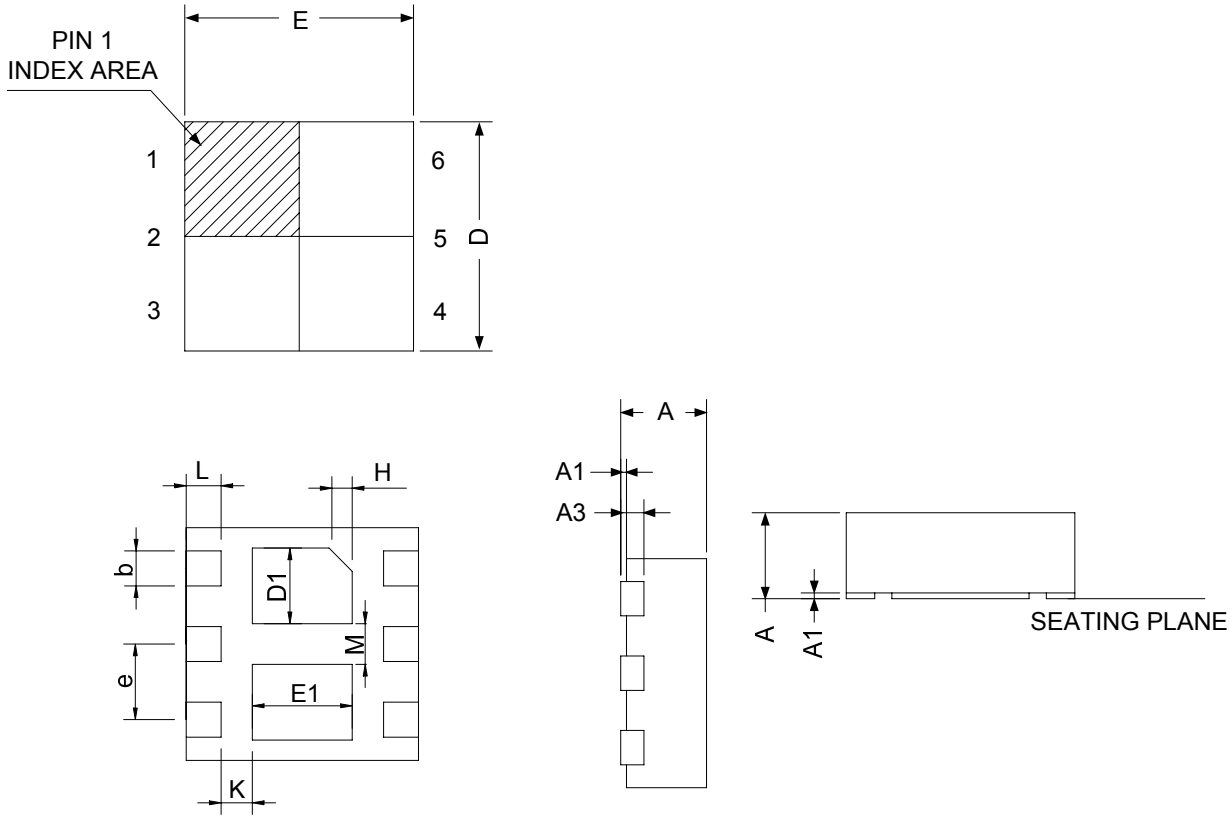
Single Pulse Power, Junction-to-Ambient



* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

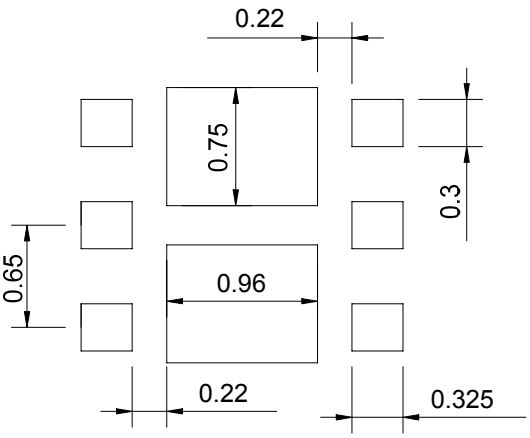
Safe Operating Area, Junction-to-Ambient

Package Information DFN2x2C-6_EP2_S



SYMBOL	DFN2x2C-6_EP2_S			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.200 REF		0.008 REF	
b	0.25	0.35	0.010	0.014
D	1.90	2.10	0.075	0.083
D1	0.55	0.75	0.022	0.030
E	1.90	2.10	0.075	0.083
E1	0.76	0.96	0.030	0.038
e	0.65 BSC		0.026 BSC	
H	0.20 BSC		0.008 BSC	
K	0.17	0.37	0.007	0.015
L	0.25	0.35	0.010	0.014
M	0.25	0.45	0.010	0.018

RECOMMENDED LAND PATTERN



UNIT: mm

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