4 Data Lane 2:1 MIPI Switch

Features

- 10-Channel 2:1 Switch
- Signal Types: MIPI, D-PHY & C-PHY
- Supply Voltage Range(V_{CC}): 1.65V to 5.0V
- Input Signals: 0V to 1.3V
- R_{ON}: 7Ω Typical
- ΔR_{ON}: 0.1Ω Typical
- I_{CC}: 25μA Typical
- -3dB Bandwidth: 3.5 GHz Typical
- Low Crosstalk: −30 dB Typical
- Low Off Isolation: −24 dB Typical
- C_{ON}: 1.5 pF Typical

General Description

The AW35649 is a four-data-lane MIPI D-PHY switch. The AW35649 can also be configured as three-data-lane MIPI C-PHY switch.

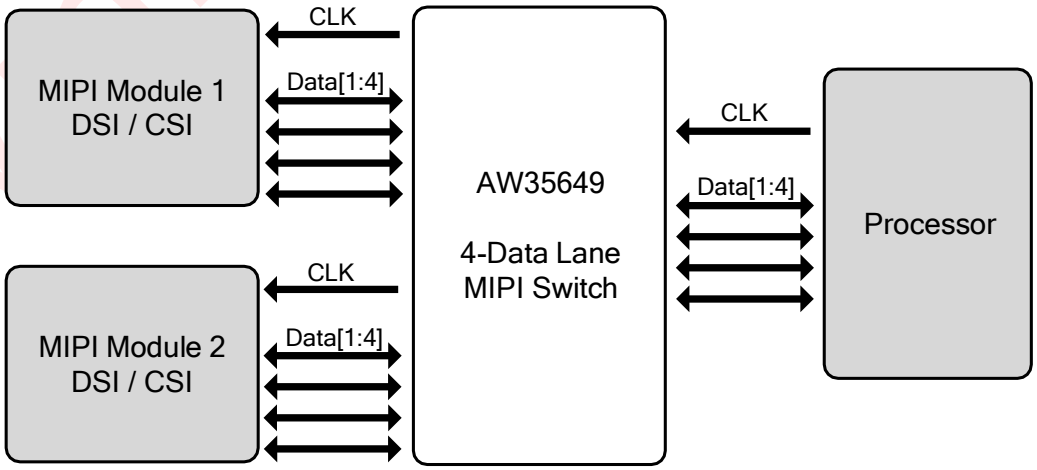
This 10 channel single-pole double-throw switch is optimized for high speed MIPI applications. The AW35649 is designed to facilitate multiple MIPI compliant devices to connect to a CSI or DSI module.

The AW35649 is available in a WLCSP 2.43mmX2.43mmX0.488mm-36B package.

Applications

- Smartphones
- Tablets
- Laptops
- Displays

Typical Application Circuit



Typical Application Circuit of AW35649

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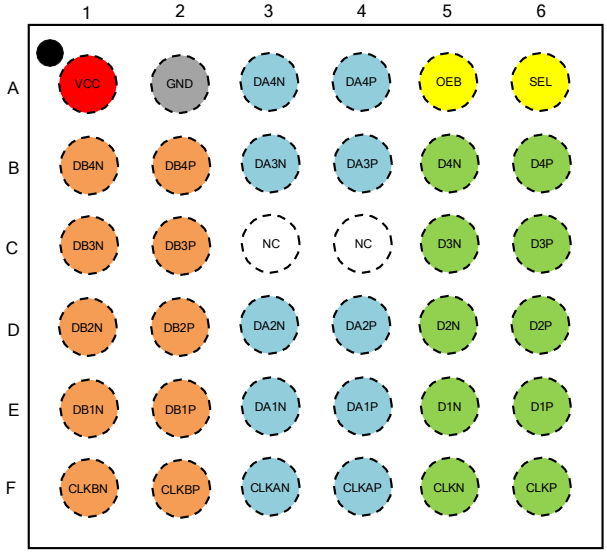
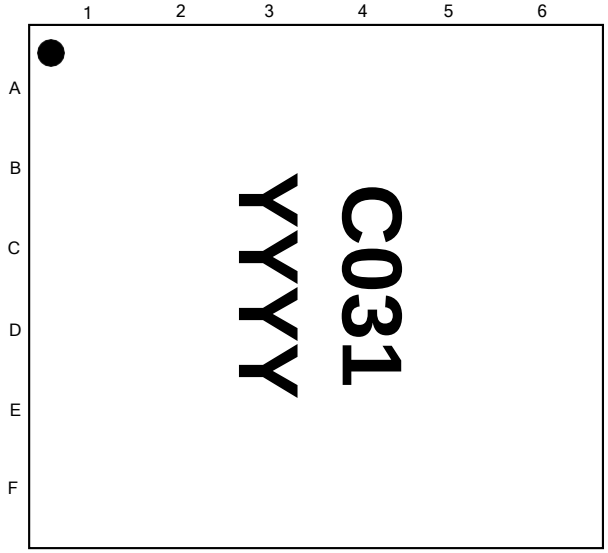
Pin Configuration And Top Mark

AW35649CSR
(Top View)



AW35649CSR Marking
(Top View)



C031 - AW35649CSR
YYYY - Production Tracing Code

Pin Configuration and Top Mark

Pin Definition

PIN	NAME	DESCRIPTION
A1	VCC	Power supply input
A2	GND	Ground
A3	DA4N	A side data port 4, differential -
A4	DA4P	A side data port 4, differential +
A5	OEB	Output enable, active low
A6	SEL	Channel select
B1	DB4N	B side data port 4, differential -
B2	DB4P	B side data port 4, differential +
B3	DA3N	A side data port 3, differential -
B4	DA3P	A side data port 3, differential +
B5	D4N	Common data port 4, differential -
B6	D4P	Common data port 4, differential +

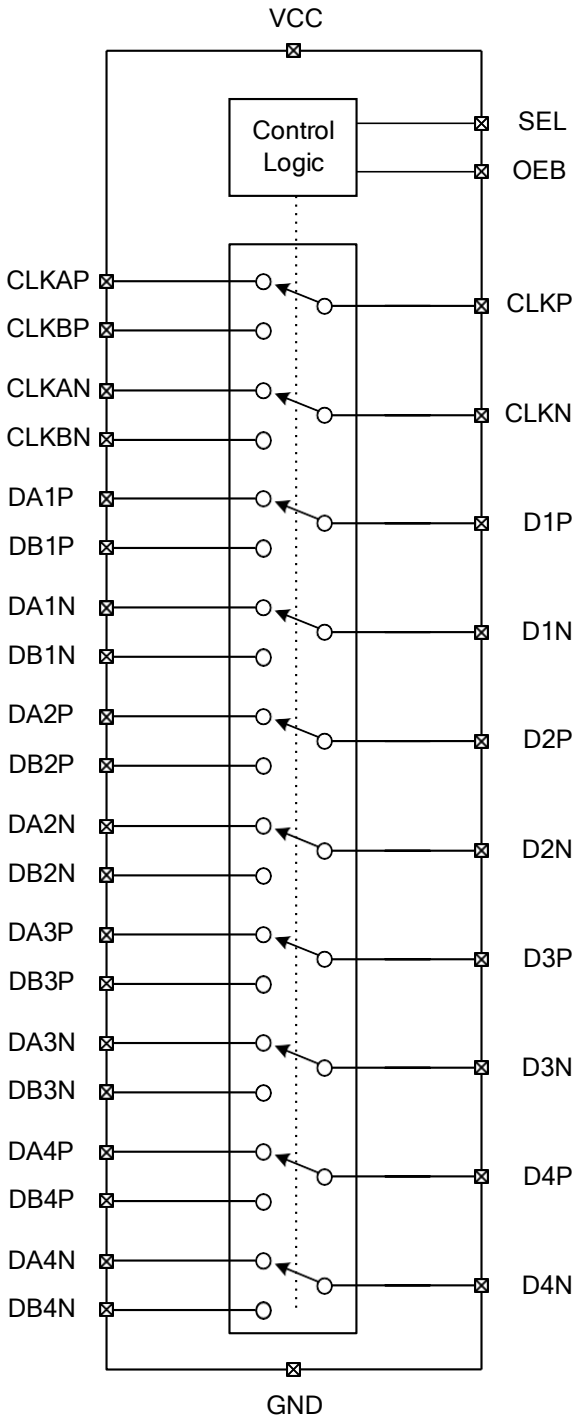
Pin Definition (Continued)

PIN	NAME	DESCRIPTION
C1	DB3N	B side data port 3, differential -
C2	DB3P	B side data port 3, differential +
C3	NC	No connect
C4	NC	No connect
C5	D3N	Common data port 3, differential -
C6	D3P	Common data port 3, differential +
D1	DB2N	B side data port 2, differential -
D2	DB2P	B side data port 2, differential +
D3	DA2N	A side data port 2, differential -
D4	DA2P	A side data port 2, differential +
D5	D2N	Common data port 2, differential -
D6	D2P	Common data port 2, differential +
E1	DB1N	B side data port 1, differential -
E2	DB1P	B side data port 1, differential +
E3	DA1N	A side data port 1, differential -
E4	DA1P	A side data port 1, differential +
E5	D1N	Common data port 1, differential -
E6	D1P	Common data port 1, differential +
F1	CLKBN	B side clock port, differential -
F2	CLKBP	B side clock port, differential +
F3	CLKAN	A side clock port, differential -
F4	CLKAP	A side clock port, differential +
F5	CLKN	Common clock port, differential -
F6	CLKP	Common clock port, differential +

Pin Functions

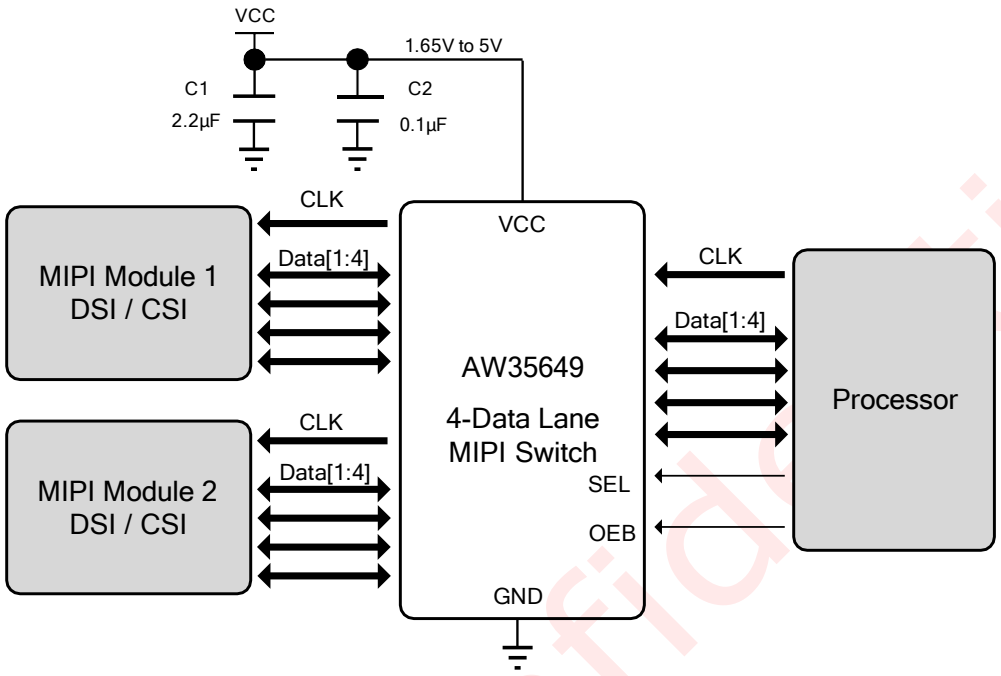
OEB	SEL	Function
H	X	Clock and Data ports High Impedance
L	L	CLKP/N=CLKAP/N, DnP/N=DAnP/N
L	H	CLKP/N=CLKBP/N, DnP/N=DBnP/N

Functional Block Diagram

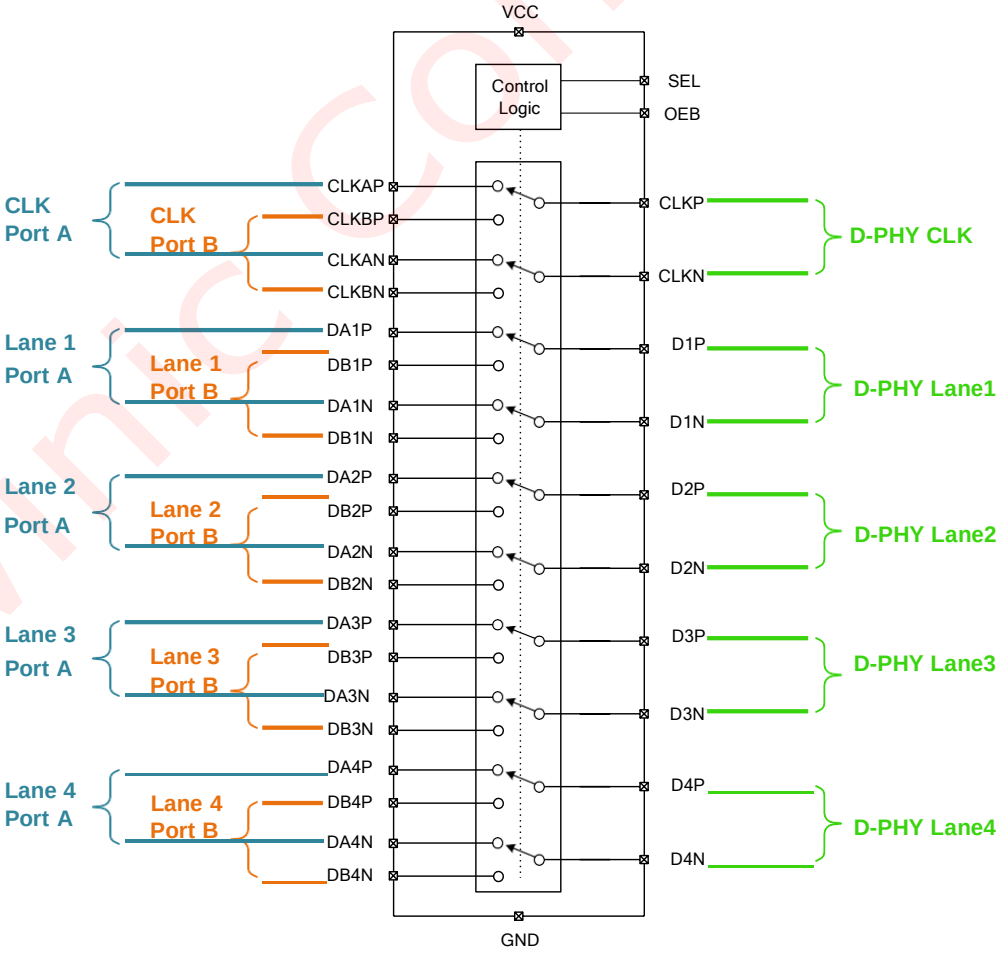


Functional Block Diagram

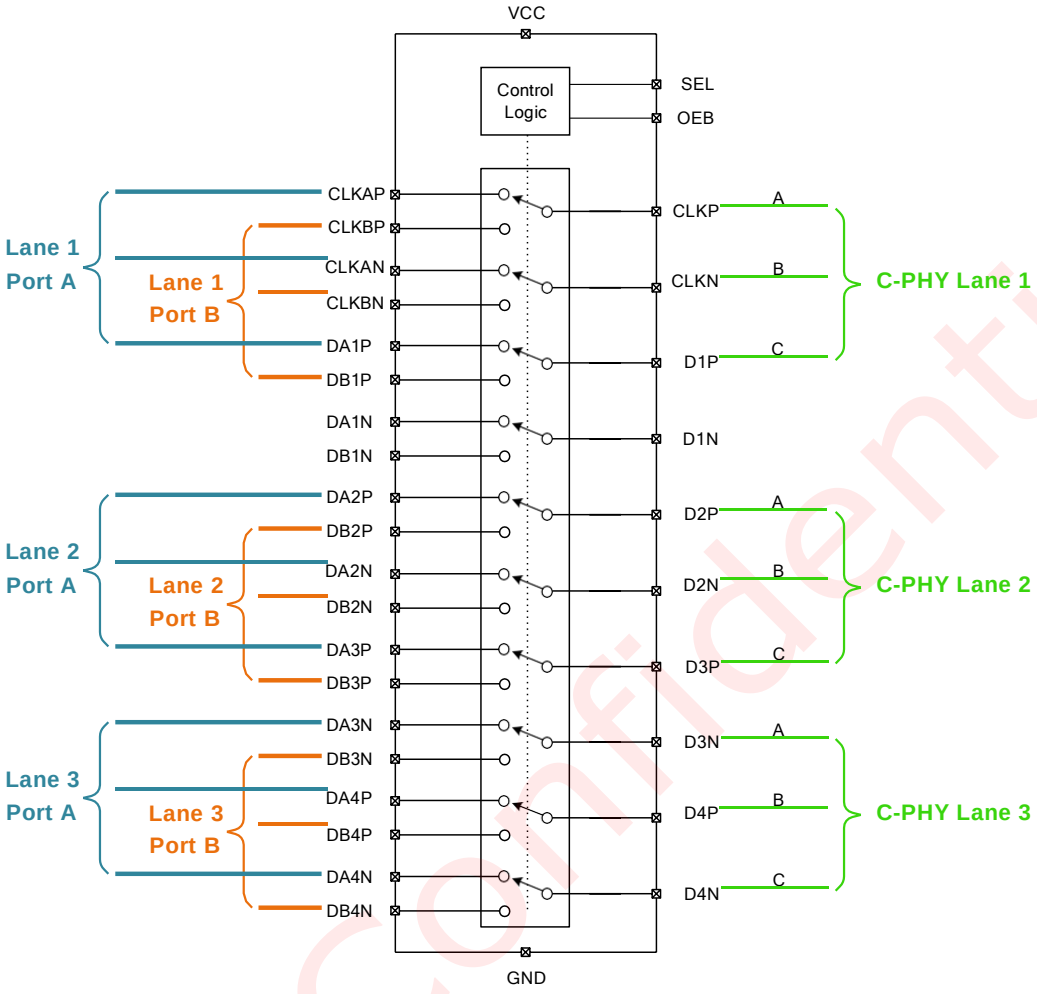
Typical Application Circuits



Typical Application Circuit of AW35649



Recommended D-PHY Configuration of AW35649



Recommended C-PHY Configuration of AW35649

The control inputs OEB,SEL must be held HIGH or LOW, and cannot be left floating

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW35649CSR	-40°C～85°C	WLCSP 2.43mmX2.43mm X0.488mm-36B	C031	MSL1	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS		RANGE
Supply voltage range V_{CC}		-0.3V to 6V
Input/Output DC switch voltage $V_{I/O}$(NOTE2)		-0.3V to 6V
Input voltage range	SEL, OEB	-0.3V to 6V
Junction-to-ambient thermal resistance θ_{JA}		61°C/W
Maximum operating junction temperature T_{JMAX}		150°C
Operating free-air temperature range		-40°C to 85°C
Storage temperature T_{STG}		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C
ESD		
Human Body Model (All pins, per ANSI/ESDA/JEDEC JS-001)		±2kV
Charged Device Model (All pins, per JESD22-C101)		±1kV
Machine Model (All pins, per JESD22-A115C)		±200V
Latch-Up		
Test condition: JEDEC78		±200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: $V_{I/O}$ refers to analog data/clock switch ports

Electrical Characteristics

T_A = -40°C to 85°C unless otherwise noted. Typical values are guaranteed for V_{CC}=3.3V T_A = 25°C.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		1.65	3.3	5.0	V
I_{CC}	Active supply current	OEB=0V, SEL=0V or V_{CC}		25	45	μA
I_{CC_PD}	Standby supply current	OEB=V_{CC}, SEL=0V or V_{CC}			1	μA
$I_{CC\_PD\_1.5}$	Standby supply current	V_{CC}=5V OEB=1.5V, SEL=0V or V_{CC}		1		μA
DC Characteristics						
R_{ON_HS}	On-state resistance for high speed MIPI mode	$V_{I/O}$=0.2V, I_{ON}=8mA V_{CC}=1.65V		7	11	Ω
		$V_{I/O}$=0.2V, I_{ON}=8mA V_{CC}=1.8V to 5.0V		7	11	Ω
R_{ON_LP}	On-state resistance for low power MIPI mode	$V_{I/O}$=1.2V, I_{ON}=8mA V_{CC}=1.65V		8	12	Ω
		$V_{I/O}$=1.2V, I_{ON}=8mA V_{CC}=1.8V to 5.0V		7.5	12	Ω
ΔR_{ON_HS}	On-state resistance match between channels for high speed MIPI mode	$V_{I/O}$=0.2V, I_{ON}=8mA		0.1		Ω
ΔR_{ON_LP}	On-state resistance match between channels for low power MIPI mode	$V_{I/O}$=1.2V, I_{ON}=8mA		0.1		Ω
$R_{ON\_FLAT\_HS}$	ON-state resistance flatness for high speed MIPI mode	$V_{I/O}$=0V to 0.3V, I_{ON}=8mA		0.9		Ω
$R_{ON\_FLAT\_LP}$	ON-state resistance flatness for low power MIPI mode	$V_{I/O}$=0V to 1.3V, I_{ON}=8mA		0.9		Ω
I_{OFF}	Switch off leakage current	V_{CC}=1.65V to 5.0V OEB, SEL=0V or 5.0V Dn,CLKn,DAn,CLKAn,DBn, CLKBn=0V to 1.3V	-0.5		0.5	μA
I_{ON}	Switch on leakage current	V_{CC}=1.65V to 5.0V OEB=0V, SEL=0V or 5.0V Dn,CLKn,DAn,CLKAn,DBn, CLKBn=0V to 1.3V	-0.5		0.5	μA

Electrical Characteristics (Continued)

T_A = -40°C to 85°C unless otherwise noted. Typical values are guaranteed for V_{CC}=3.3V T_A = 25°C.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
Digital Characteristics						
V_{IH}	Input logic high (SEL, OEB)	V_{CC}=1.65V to 5.0V	1.3			V
V_{IL}	Input logic low (SEL, OEB)	V_{CC}=1.65V to 5.0V			0.5	V
I_{LEAK_IN}	Input leakage (SEL, OEB)	SEL,OEB=0V to 5.0V	-0.5		0.5	μA
C_{IN}	Digital Input capacitance (SEL, OEB)	f=1MHz		5		pF
Dynamic Characteristics						
C_{ON}	ON capacitance(NOTE3)	OEB=0V, Dn,CLKn,DAn,DBn,CLKAn, CLKBn=0V or 0.2V f = 1250 MHz, switch ON		1.5		pF
C_{OFF}	OFF capacitance(NOTE3)	OEB=V_{CC}, Dn,CLKn,DAn,DBn,CLKAn, CLKBn=0V or 0.2V f = 1250MHz, switch OFF		1.2		pF
O_{ISO}	Differential off isolation(NOTE3)	R_L = 50Ω, C_L = 0pF $V_{I/O}$=200mV+200mV_{PP} (differential) f = 1250MHz, switch OFF		-24		dB
X_{TALK}	Differential Channel to channel crosstalk(NOTE3)	R_L = 50Ω, C_L = 0pF $V_{I/O}$=200mV+200mV_{PP} (differential) f = 1250MHz, switch ON		-30		dB
BW	-3dB bandwidth(NOTE3)	R_L = 50Ω, C_L = 0pF $V_{I/O}$=200mV+200mV_{PP} (differential), switch ON	2.5	3.5		GHz
I_{LOSS}	Insertion Loss(NOTE3)	R_L = 50Ω, C_L = 0pF $V_{I/O}$=200mV+200mV_{PP} (differential) f = 750MHz, switch ON		-0.7		dB

NOTE3: Guaranteed by characterization

Electrical Characteristics (Continued)

T_A = -40°C to 85°C unless otherwise noted. Typical values are guaranteed for V_{CC}=3.3V T_A = 25°C.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
Dynamic Characteristics						
t_{INIT}	Initialization time (V_{CC} to output)	Dn,CLKn=0.6V DAn,DBn,CLKAn,CLKBn: R_L = 50Ω, C_L = 0pF		1.5	200	μs
t_{EN}	Device turn on time (OEB to output)	Dn,CLKn=0.6V DAn,DBn,CLKAn,CLKBn: R_L = 50Ω, C_L = 0pF		0.5	200	μs
t_{DIS}	Device turn off time (OEB to output)	Dn,CLKn=0.6V DAn,DBn,CLKAn,CLKBn: R_L = 50Ω, C_L = 0pF		150	250	ns
t_{ON}	Switch turn on time (SEL to output)	Dn,CLKn=0.6V DAn,DBn,CLKAn,CLKBn: R_L = 50Ω, C_L = 0pF		800	1600	ns
t_{OFF}	Switch turn off time (SEL to output)	Dn,CLKn=0.6V DAn,DBn,CLKAn,CLKBn: R_L = 50Ω, C_L = 0pF		150	800	ns
t_{BBM}	Break before make time	Dn,CLKn: R_L = 50Ω, C_L = 0pF DAn,DBn,CLKAn,CLKBn =0.6V		400		ns
t_{PD}	Propagation delay(NOTE4)	Dn,CLKn=0.6V DAn,DBn,CLKAn,CLKBn: R_L = 50Ω, C_L = 0pF		67		ps
$t_{SKEW(INTRA)}$	Intrapair skew(NOTE4)	Dn,CLKn=0.3V DAn,DBn,CLKAn,CLKBn: R_L = 50Ω, C_L = 0pF		6		ps
$t_{SKEW(INTER)}$	Interpair skew(NOTE4)	Dn,CLKn=0.3V DAn,DBn,CLKAn,CLKBn: R_L = 50Ω, C_L = 0pF		6		ps

NOTE4: Guaranteed by characterization

Detailed Functional Description

The AW35649 is a four-data-lane MIPI D-PHY switch. This device is an optimized 10-channel (5 differential) single-pole, double-throw switch for use in high speed applications. The AW35649 can also be configured as three-data-lane MIPI C-PHY switch. The AW35649 is designed to facilitate multiple MIPI compliant devices to connect to a single CSI/DSI, C-PHY/D-PHY module.

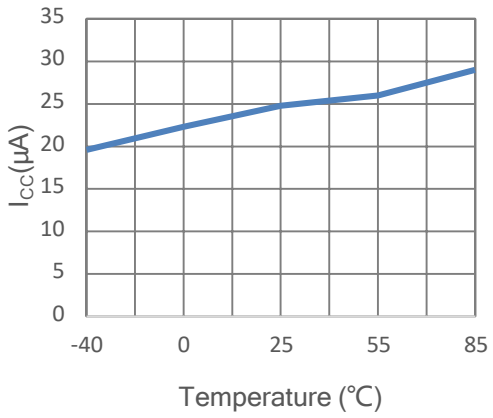
High Impedance Mode

When OEB is logic high, the AW35649 is in high impedance mode, all the clock and data ports are in Hi-Z state.

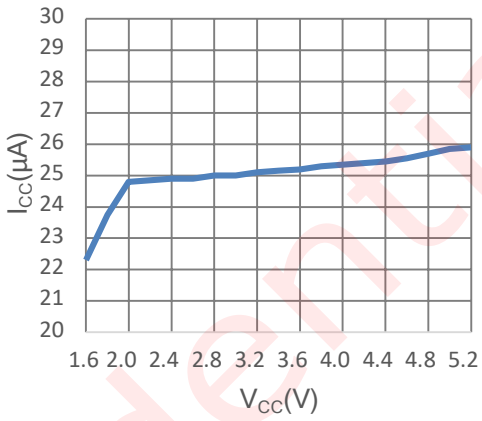
OEB	SEL	Function
H	X	Clock and Data ports High Impedance
L	L	CLKP/N=CLKAP/N, DnP/N=DAnP/N
L	H	CLKP/N=CLKBP/N, DnP/N=DBnP/N

Typical characteristics

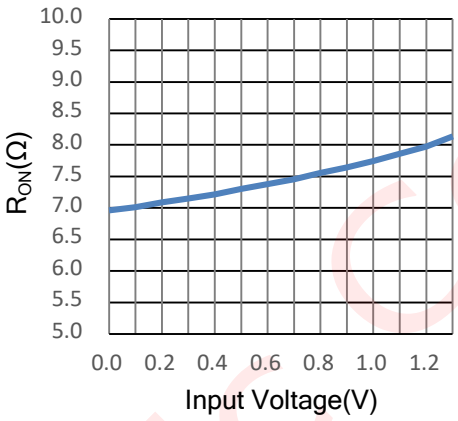
V_{CC}=3.3V, T_A=25°C, unless other noted.



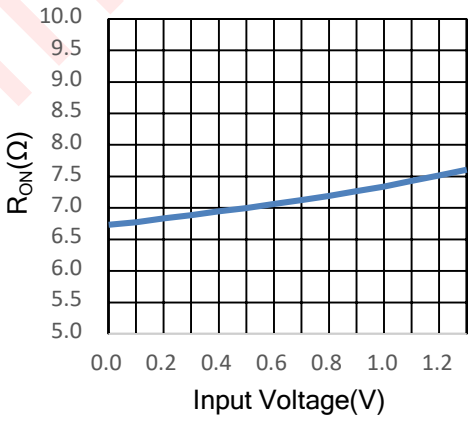
I_{CC} vs. Temp. V_{CC}=3.3V



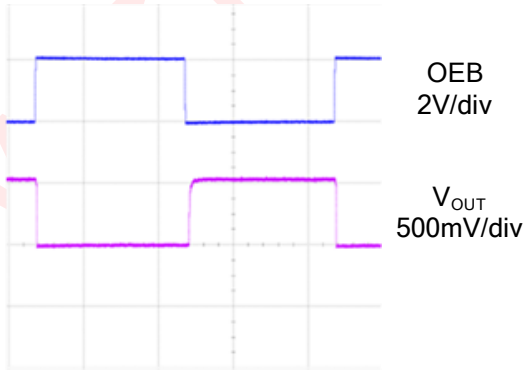
I_{CC} vs. V_{CC} Temp=25℃



R_{ON} vs. Input Voltage. V_{CC}=1.65V



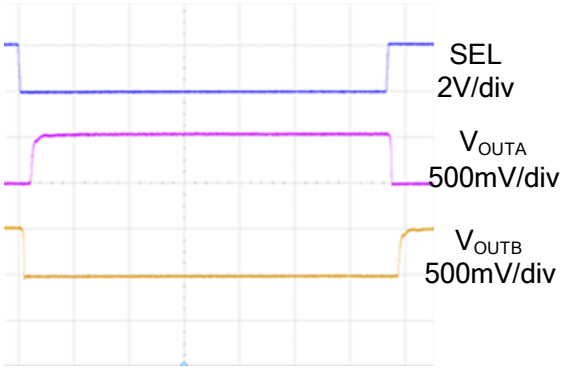
R_{ON} vs. Input Voltage. V_{CC}=1.8V~5V



5μs / div

Timing For OEB

V_{CC}=3.3V $V_{I/O}$=0.6V R_L=50Ω

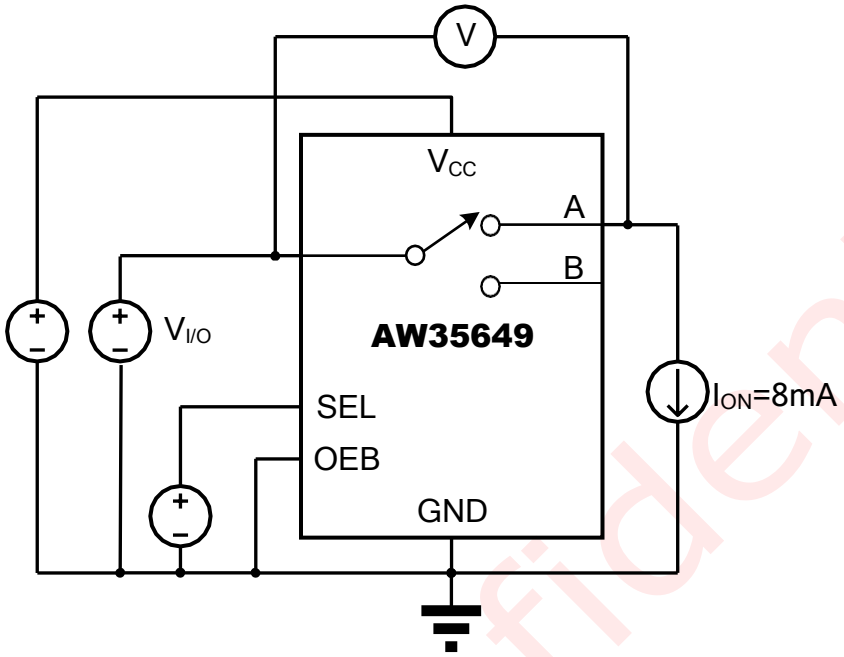


1.5μs / div

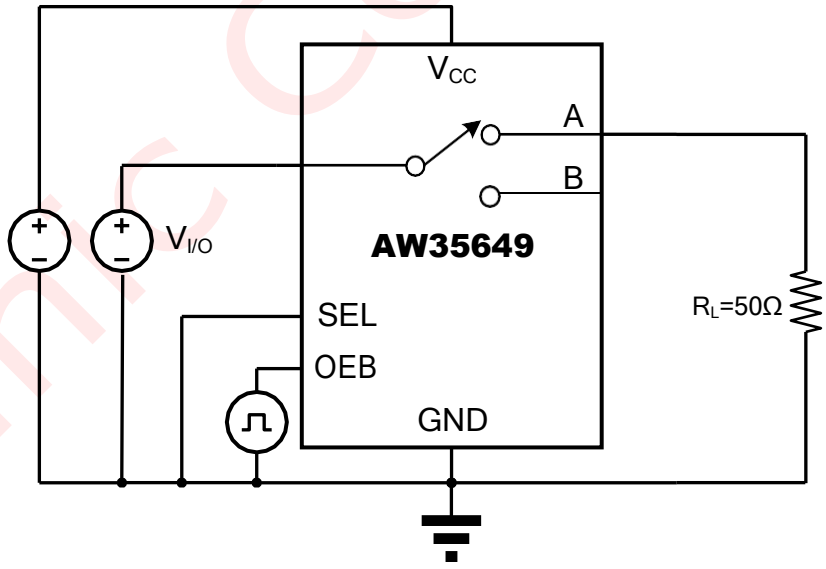
Timing For SEL

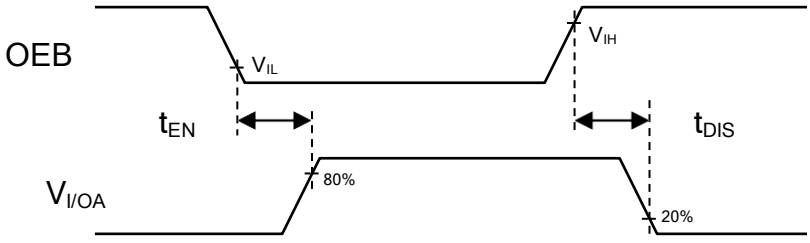
V_{CC}=3.3V $V_{I/O}$=0.6V R_L=50Ω

Parameter Measurement Information

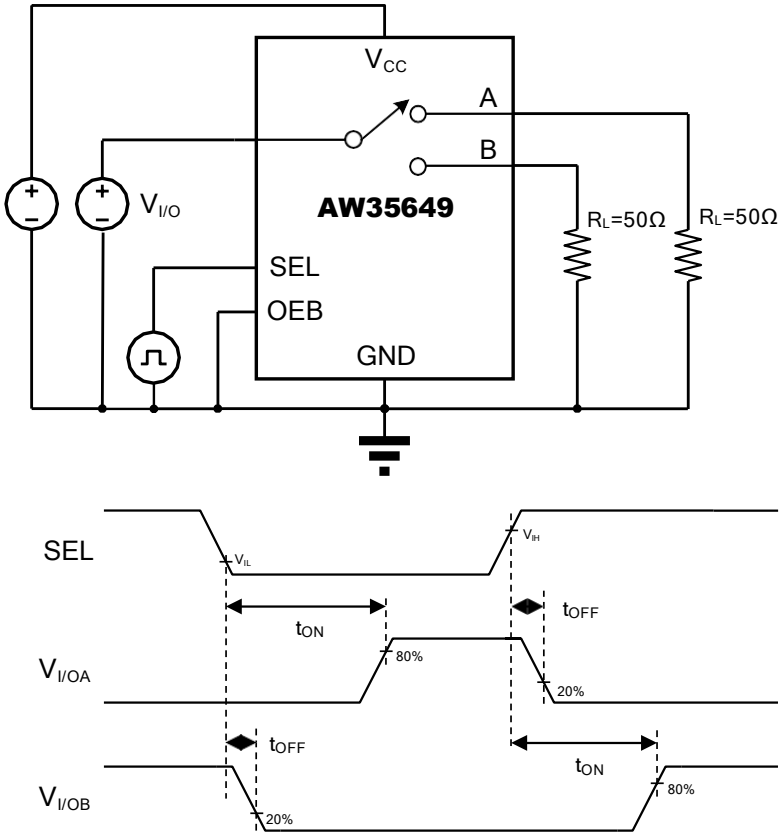


On Resistance

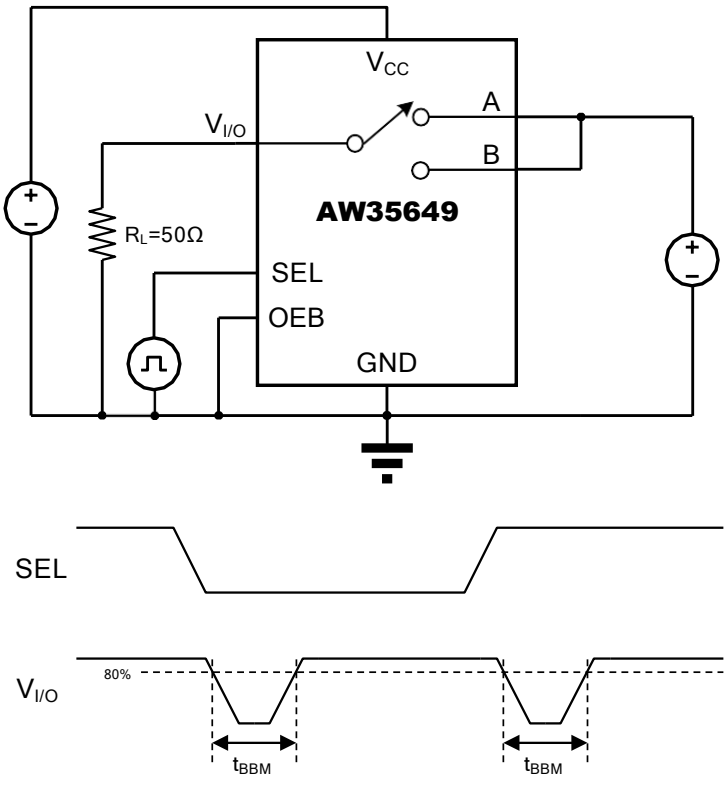




t_{EN} and t_{DIS} Timing For OEB



t_{ON} and t_{OFF} Timing For SEL



t_{BBM} For SEL

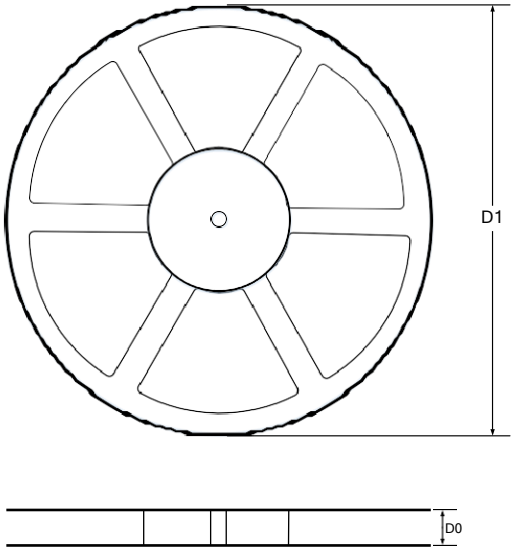
PCB Layout Consideration

To obtain the optimal performance of AW35649, PCB layout should be considered carefully. Here are some guidelines:

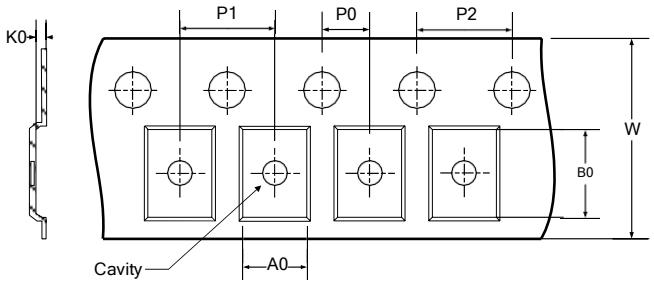
1. Place supply bypass capacitors as close to V_{CC} and GND pin as possible and avoid placing the bypass capacitors near the high-speed traces.
2. The characteristic impedance of the traces must match that of the receiver and transmitter to maintain signal integrity.
3. Route the high-speed signals using a minimum amount of vias and corners which reduces signal reflections and impedance changes. When it becomes necessary to make the traces turn 90°, use an arc instead of making a single 90° turn.
4. Do not route high-speed traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or ICs that use or duplicate clock signals.
5. Avoid stubs on the high-speed signal lines because they cause signal reflections.
6. Route all high-speed signal traces over continuous GND planes, with no interruptions.
7. High speed signal traces must be length matched as much as possible to minimize skew between data and clock lines. Width and spacing between differential traces must be equal line width and line spacing

Tape And Reel Information

REEL DIMENSIONS

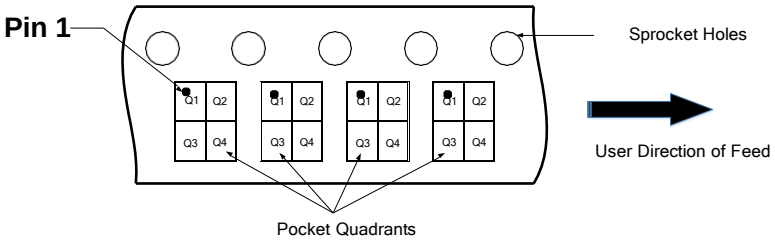


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width B0：Dimension designed to accommodate the component length K0：Dimension designed to accommodate the component thicknessW：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket holeP1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

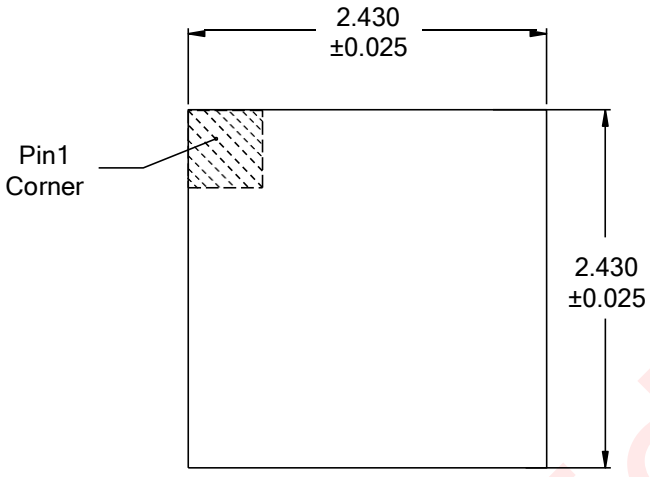


DIMENSIONS AND PIN1 ORIENTATION

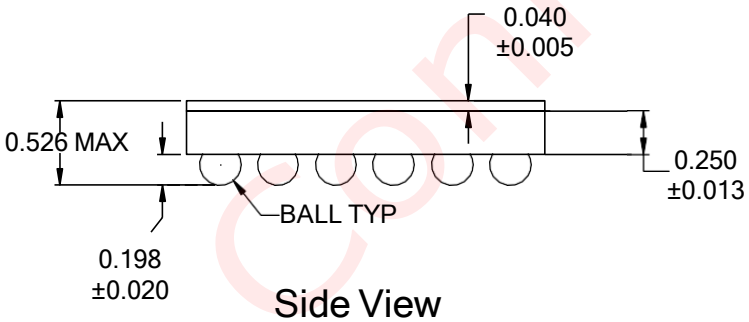
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
179.00	9.00	2.54	2.54	0.76	2.00	4.00	4.00	8.00	Q1

All dimensions are nominal

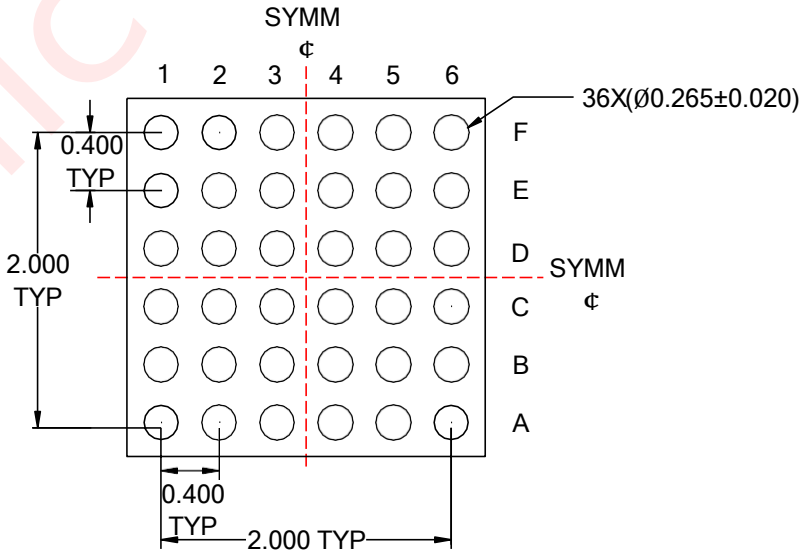
Package Description



Top View



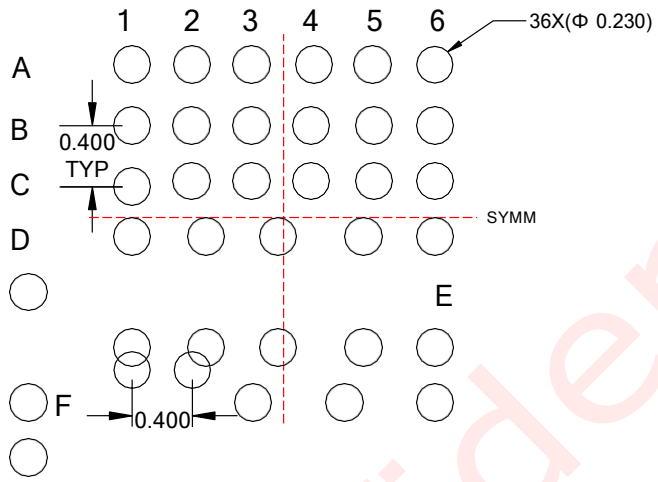
Side View

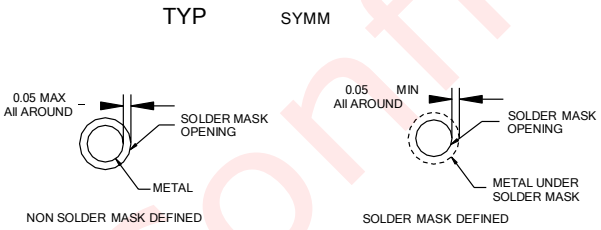


Bottom View

Unit:mm

Land Pattern Data





Unit: mm

Revision History

Version	Date	Change Record
V1.0	Mar 2019	Datasheet V1.0 released
V1.1	Jul 2019	1. Updated Description Diagram. (P13) 2. Updated Description Diagram. (P14)

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