ISL28005

Micropower, Rail-to-Rail Input Current Sense Amplifier with Voltage Output

The ISL28005 is a micropower, unidirectional high-side and low-side current sense amplifier featuring a proprietary rail-to-rail input current sensing amplifier. The ISL28005 is ideal for high-side current sense applications where the sense voltage is usually much higher than the amplifier supply voltage. The device can be used to sense voltages as high as 28V when operating from a supply voltage as low as 2.7V. The micropower ISL28005 consumes only 50µA of supply current when operating from a 2.7V to 28V supply.

The ISL28005 features a common-mode input voltage range from 0V to 28V. The proprietary architecture extends the input voltage sensing range down to 0V, making it an excellent choice for low-side ground sensing applications. The benefit of this architecture is that a high degree of total output accuracy is maintained over the entire 0V to 28V common mode input voltage range.

The ISL28005 is available in fixed (100V/V, 50V/V and 20V/V) gains in the space saving 5 Ld SOT-23 package. The parts operate over the extended temperature range from -40°C to +125°C.

Features

- Low Power Consumption: 50µA,Typical
- Supply Range: 2.7V to 28V
- Wide Common Mode Input: 0V to 28V
- Fixed Gain Versions
  - ISL28005-100: 100V/V
  - ISL28005-50: 50V/V
  - ISL28005-20: 20V/V
- Operating Temperature Range: -40°C to +125°C
- Package: 5 Ld SOT-23

Applications

- Power Management/Monitors
- Power Distribution and Safety
- DC/DC, AC/DC Converters
- Battery Management/Charging
- Automotive Power Distribution

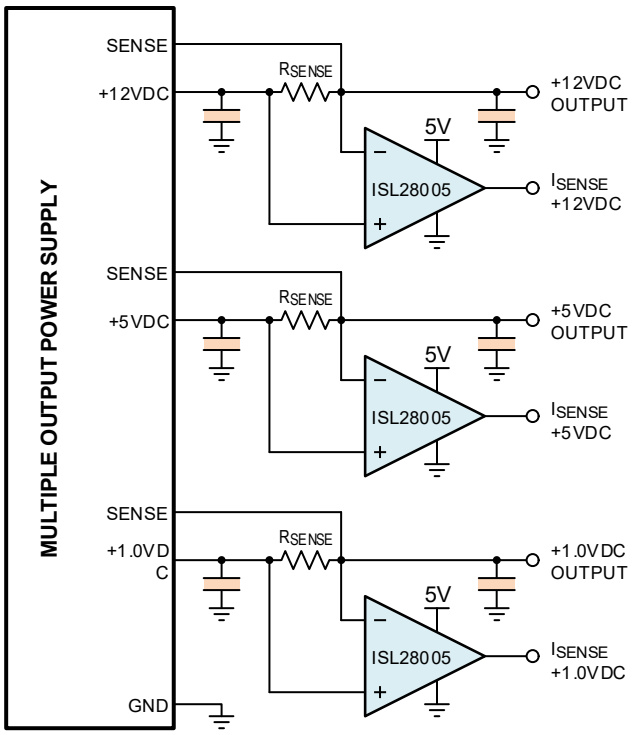


Figure 1. Typical Application

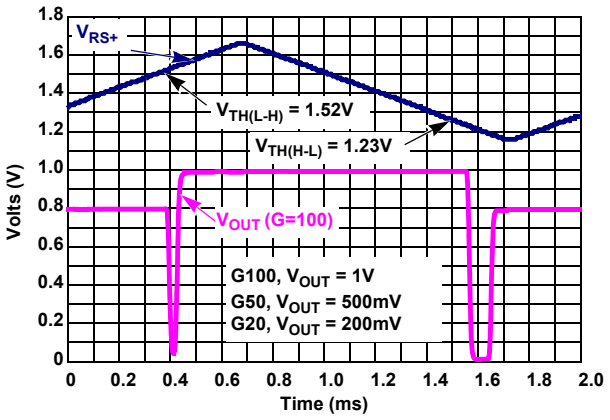


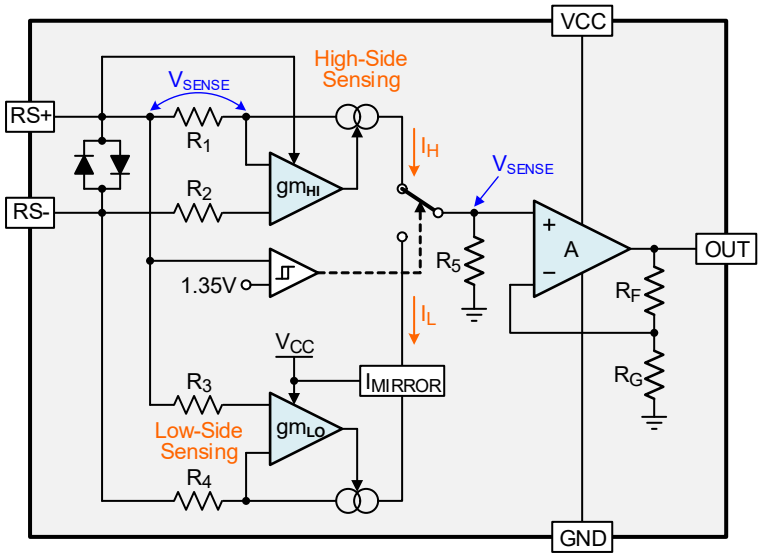
Figure 2. High-Side and Low-Side Threshold Voltage

Contents

1. Overview . . . 3
1.1 Block Diagram . . . 3
2. Pin Information . . . 3
2.1 Pin Assignments . . . 3
2.2 Pin Descriptions . . . 3
3. Specifications . . . 4
3.1 Absolute Maximum Ratings . . . 4
3.2 ESD Ratings . . . 4
3.3 Recommended Operating Conditions . . . 4
3.4 Thermal Specifications . . . 4
3.5 Electrical Specifications . . . 5
4. Typical Performance Graphs . . . 7
4.1 Test Circuits and Waveforms . . . 10
5. Applications Information . . . 11
5.1 Functional Description . . . 11
5.2 Hysteretic Comparator . . . 12
5.3 Typical Application Circuit . . . 13
5.4 Error Sources . . . 13
6. Layout Guidelines . . . 14
6.1 Kelvin Connected Sense Resistor . . . 14
6.2 Overall Accuracy (VOA %) . . . 14
6.3 Power Dissipation . . . 15
7. Package Outline Drawing . . . 16
8. Ordering Information . . . 17
9. Revision History . . . 17

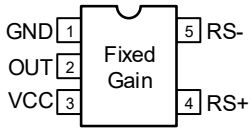
1. Overview

1.1 Block Diagram



2. Pin Information

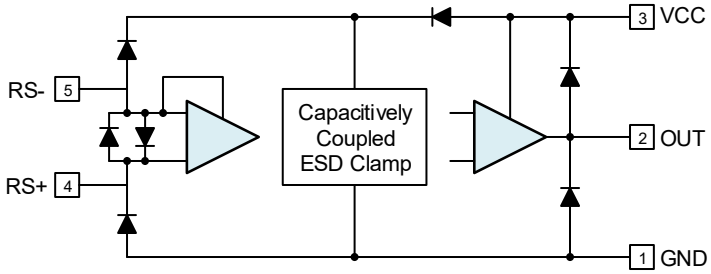
2.1 Pin Assignments



Top View

2.2 Pin Descriptions

Pin Number	Pin Name	Description
1	GND	Power Ground
2	OUT	Amplifier Output
3	VCC	Positive Power Supply
4	RS+	Sense Voltage Non-inverting Input
5	RS-	Sense Voltage Inverting Input



3. Specifications

3.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
Max Supply Voltage		28	V
Max Differential Input Current		20	mA
Max Differential Input Voltage		±0.5	V
Max Input Voltage (RS+, RS-)	GND - 0.5	30	V
Max Input Current for Input Voltage <GND -0.5V		±20	mA
Output Short-Circuit Duration		Indefinite	

3.2 ESD Ratings

ESD Model/Test	Rating	Unit
Human Body Model (Tested per JESD22-A114F)	4	kV
Charged Device Model (Tested per JESD22-C101D)	1.5	kV
Machine Model (Tested per EIA/JESD22-A115-A)	200	V

3.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Ambient Temperature	-40	+125	°C

3.4 Thermal Specifications

Thermal Resistance (Typical)	θ_{JA} (°C/W)[1]	θ_{JC} (°C/W)[2]
5 Ld SOT-23 Package	190	90

1. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See **TB379** for details.
2. For θ_{JC}, the case temperature location is taken at the package top center.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature		+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	see TB493		

3.5 Electrical Specifications

V_{CC} = 12V, V_{RS+} = 0V to 28V, V_{SENSE} = 0V, R_{LOAD} = 1MΩ, T_A = +25°C unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +125°C. Temperature data established by characterization.**

Parameter	Symbol	Conditions	Min[1]	Typ	Max[1]	Unit
Input Offset Voltage[2][3]	V_{OS}	V_{CC} = V_{RS}+ = 12V, V_S = 20mV to = 100mV	-500 **-500**	60	500 **500**	µV
		V_{CC} = 12V, V_{RS}+ = 0.2V, V_S = 20mV, V_S = 100mV	-3 **-3.3**	-1.2	3 **3.3**	mV
Leakage Current	I_{RS}+, I_{RS}-	V_{CC} = 0V, V_{RS+} = 28V		0.041	1.2 **1.5**	µA
Gain = 100 + Input Bias Current	I_{RS}+	V_{RS}+ = 2V, V_{SENSE} = 5mV		4.7	6 **7**	µA
		V_{RS}+ = 0V, V_{SENSE} = 5mV	-500 **-600**	-425		nA
Gain = 50, Gain = 20 +Input Bias Current		V_{RS}+ = 2V, V_{SENSE} = 5mV		4.7	6 **8**	µA
		V_{RS}+ = 0V, V_{SENSE} = 5mV	-700 **-840**	-432		nA
Input Bias Current	I_{RS}-	V_{RS}+ = 2V, V_{SENSE} = 5mV		5	50 **75**	nA
		V_{RS}+ = 0V, V_{SENSE} = 5mV	-125 **-130**	-45		nA
Common Mode Rejection Ratio	CMRR	V_{RS}+ = 2V to 28V	105	115		dB
Power Supply Rejection Ratio	PSRR	V_{CC} = 2.7V to 28V, V_{RS}+ = 2V	90	105		dB
Full-scale Sense Voltage	VF_S	V_{CC} = 28V, V_{RS}+ = 0.2V, 12V	200			mV
Gain[2]	G	ISL28005-100		100		V/V
		ISL28005-50		50		V/V
		ISL28005-20		20		V/V
Gain = 100 Gain Accuracy[4]	G_A	V_{CC} = V_{RS}+ = 12V, V_{SENSE} = 20mV to 100mV	-2 **-3**		2 **3**	%
		V_{CC} = 12V, V_{RS}+ = 0.1V, V_{SENSE} = 20mV to 100mV		-0.25		%
Gain = 50, Gain = 20 Gain Accuracy[4]		V_{CC} = V_{RS}+ = 12V, V_{SENSE} = 20mV to 100mV	-2 **-3**		2 **3**	%
		V_{CC} = 12V, V_{RS}+ = 0.1V, V_{SENSE} = 20mV to 100mV	-3 -4	-0.31	3 4	%

V_{CC} = 12V, V_{RS+} = 0V to 28V, V_{SENSE} = 0V, R_{LOAD} = 1MΩ, T_A = +25°C unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +125°C. Temperature data established by characterization. (Cont.)**

Parameter	Symbol	Conditions	Min[1]	Typ	Max[1]	Unit
Gain = 100 Total Output Accuracy[5]	V_{OA}	V_{CC} = V_{RS}+ = 12V, V_{SENSE} = 100mV	-2.5 **-2.7**		2.5 **2.7**	%
		V_{CC} = 12V, V_{RS}+ = 0.1V, V_{SENSE} = 100mV		-1.25		%
Gain = 50, Gain = 20 Total Output Accuracy[4]		V_{CC} = V_{RS}+ = 12V, V_{SENSE} = 100mV	-2.5 **-2.7**		2.5 **2.7**	%
		V_{CC} = 12V, V_{RS}+ = 0.1V, V_{SENSE} = 100mV	-6 **-7**	-1.41	6 **7**	%
Output Voltage Swing, High V_{CC} - V_{OUT}	V_{OH}	I_O = -500µA, V_{CC} = 2.7V, V_{SENSE} = 100mV V_{RS}+ = 2V		39	50	mV
Output Voltage Swing, Low V_{OUT}	V_{OL}	I_O = 500µA, V_{CC} = 2.7V, V_{SENSE} = 0V, V_{RS}+ = 2V		30	50	mV
Output Resistance	R_{OUT}	V_{CC} = V_{RS}+ = 12V, V_{SENSE} = 100mV I_{OUT} = 10µA to 1mA		6.5		Ω
Short-Circuit Sourcing Current	I_{SC+}	V_{CC} = V_{RS}+ = 5V, R_L = 10Ω		4.8		mA
Short-Circuit Sinking Current	I_{SC-}	V_{CC} = V_{RS}+ = 5V, R_L = 10Ω		8.7		mA
Gain = 100 Supply Current	I_{CC}	V_{RS}+ > 2V, V_{SENSE} = 5mV		50	59 **62**	µA
Gain = 50, 20 Supply Current		V_{RS}+ > 2V, V_{SENSE} = 5mV		50	62 **63**	µA
Supply Voltage	V_{CC}	Guaranteed by PSRR	2.7		28	V
Gain = 100 Slew Rate	SR	Pulse on RS+ pin, V_{OUT} = $8V_{P-P}$ (see Figure 25)	0.58	0.76		V/µs
Gain = 50 Slew Rate		Pulse on RS+ pin, V_{OUT} = $8V_{P-P}$ (see Figure 25)	0.58	0.67		V/µs
Gain = 20 Slew Rate		Pulse on RS+ pin, V_{OUT} = $3.5V_{P-P}$ (see Figure 25)	0.50	0.67		V/µs
Gain = 100 -3dB Bandwidth	BW_{-3dB}	V_{RS}+ = 12V, 0.1V, V_{SENSE} = 100mV		110		kHz
Gain = 50 -3dB Bandwidth		V_{RS}+ = 12V, 0.1V, V_{SENSE} = 100mV		160		kHz
Gain = 20 -3dB Bandwidth		V_{RS}+ = 12V, 0.1V, V_{SENSE} = 100mV		180		kHz
Output Settling Time to 1% of Final Value	t_s	V_{CC} = V_{RS}+ = 12V, V_{OUT} = 10V step, V_{SENSE} > 7mV		15		µs
		V_{CC} = V_{RS}+ = 0.2V, V_{OUT} = 10V step, V_{SENSE} > 7mV		20		µs
Capacitive-Load Stability		No sustained oscillations		300		pF
Power-Up Time to 1% of Final Value	$t_{s\ Power-up}$	V_{CC} = V_{RS}+ = 12V, V_{SENSE} = 100mV		15		µs
		V_{CC} = 12V, V_{RS}+ = 0.2V V_{SENSE} = 100mV		50		µs
Saturation Recovery Time		V_{CC} = V_{RS}+ = 12V, V_{SENSE} = 100mV, overdrive		10		µs

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

2. Definition of terms:

- $V_{SENSE}A = V_{SENSE}$ at 100mV
- $V_{SENSE}B = V_{SENSE}$ at 20mV
- $V_{OUT}A = V_{OUT}$ at $V_{SENSE}A$ = 100mV
- $V_{OUT}B = V_{OUT}$ at $V_{SENSE}B$ = 20mV
- G = $GAIN = \left(\frac{V_{OUT}A - V_{OUT}B}{V_{SENSE}A - V_{SENSE}B}\right)$

3. V_{OS} is extrapolated from the gain measurement. $V_{OS} = V_{SENSE}A - \frac{V_{OUT}A}{G}$

4. % Gain Accuracy = $G_A = \left(\frac{G_{MEASURED} - G_{EXPECTED}}{G_{EXPECTED}}\right) \times 100$

5. Output Accuracy % $V_{OA} = \left(\frac{VOUT_{MEASURED} - VOUT_{EXPECTED}}{-VOUT_{EXPECTED}}\right) \times 100$ where V_{OUT} = VSENSE X GAIN and VSENSE = 100mV

4. Typical Performance Graphs

V_{CC} = 12V, R_L = 1M, unless otherwise specified.

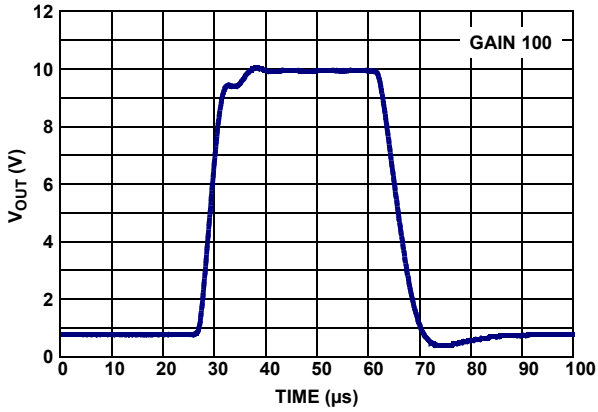


Figure 3. Large Signal Transient Response V_{RS+} = 0.2V, V_{SENSE} = 100mV

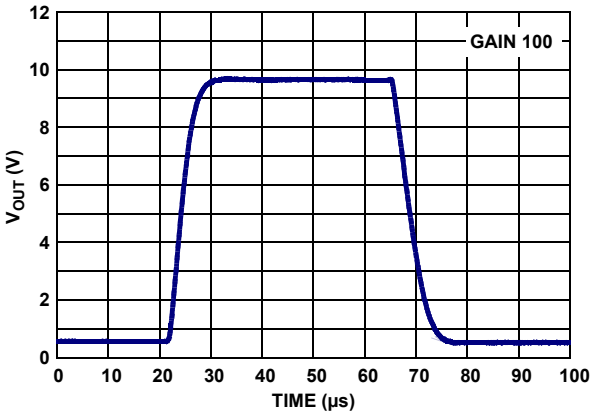


Figure 4. Large Signal Transient Response V_{RS+} = 12V, V_{SENSE} = 100mV

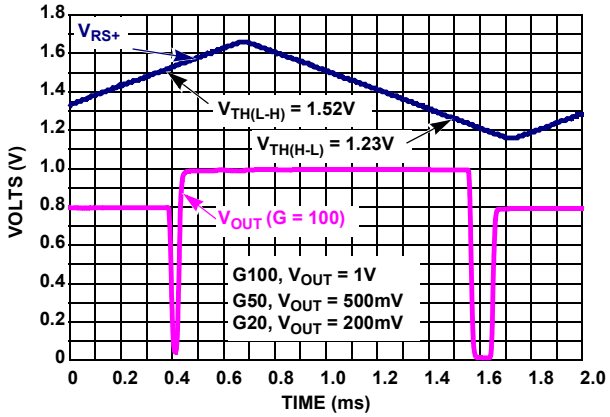


Figure 5. High-Side and Low-Side Threshold Voltage $V_{RS+(L-H)}$ and $V_{RS+(H-L)}$, V_{SENSE} = 10mV

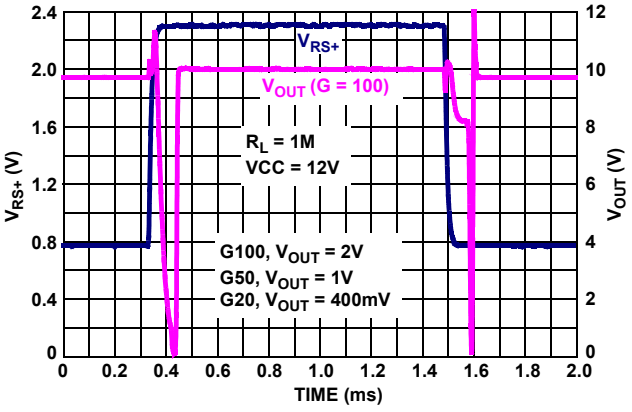


Figure 6. V_{OUT} vs V_{RS+}, V_{SENSE} = 20mV Transient Response

V_{CC} = 12V, R_L = 1M, unless otherwise specified. (Cont.)

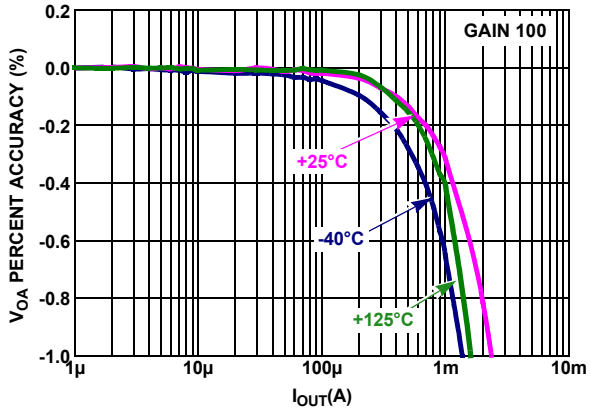


Figure 7. Normalized V_{OA} vs I_{OUT}

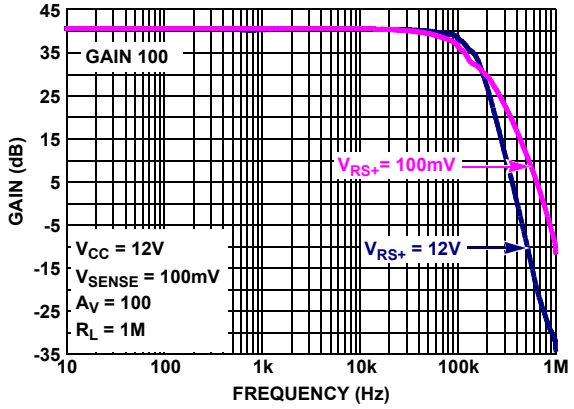


Figure 8. GAIN vs FREQUENCY V_{RS+}= 100mV/12V, V_{SENSE} = 100mV, V_{OUT} = 250mV_{P-P}

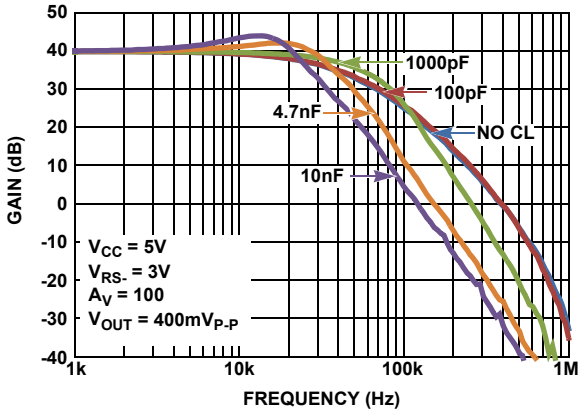


Figure 9. Capacitive Load Drive Gain vs Frequency

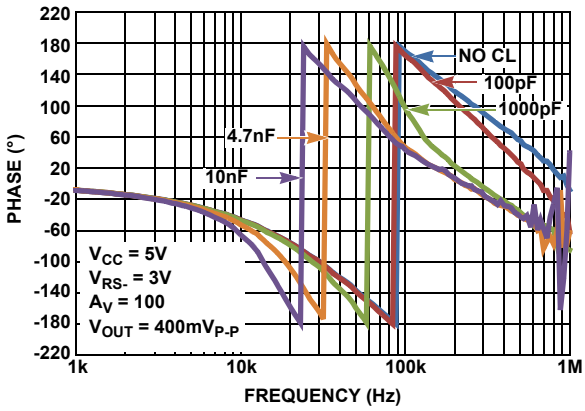


Figure 10. Capacitive Load Drive Phase vs Frequency

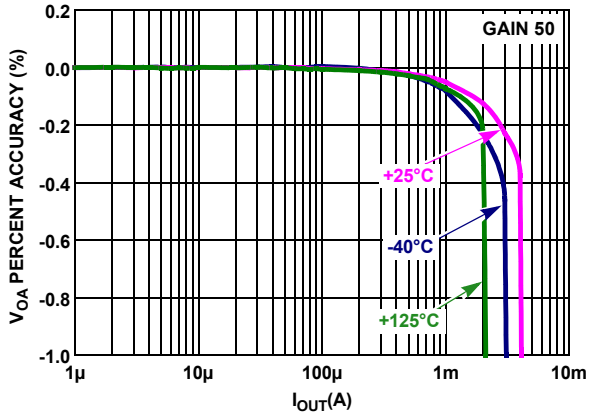


Figure 11. Normalized V_{OA} vs I_{OUT}

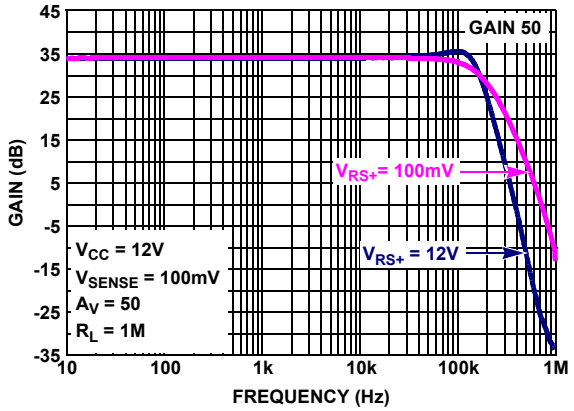


Figure 12. Gain vs Frequency V_{RS+}= 100mV/12V, V_{SENSE} = 100mV, V_{OUT} = 250mV_{P-P}

V_{CC} = 12V, R_L = 1M, unless otherwise specified. (Cont.)

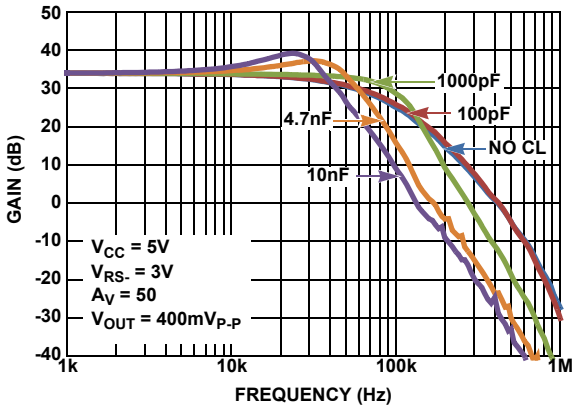


Figure 13. Capacitive Load Drive Gain vs Frequency

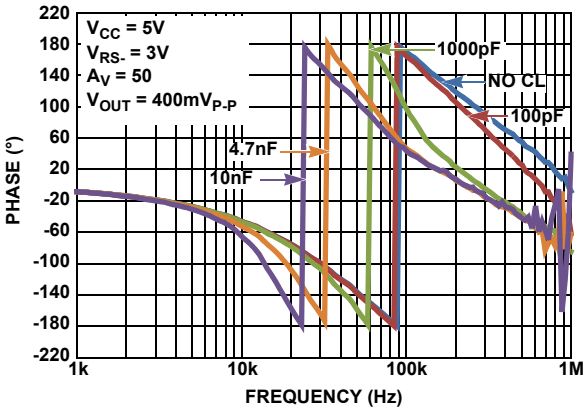


Figure 14. Capacitive Load Drive Phase vs Frequency

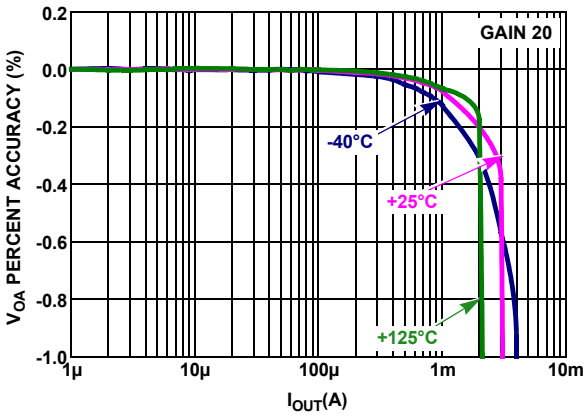


Figure 15. Normalized V_{OA} vs I_{OUT}

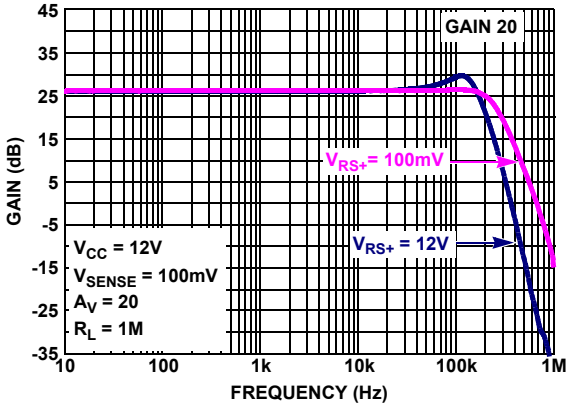


Figure 16. Gain vs Frequency V_{RS+} = 100mV/12V, V_{SENSE} = 100mV, V_{OUT} = 250mV_{P-P}

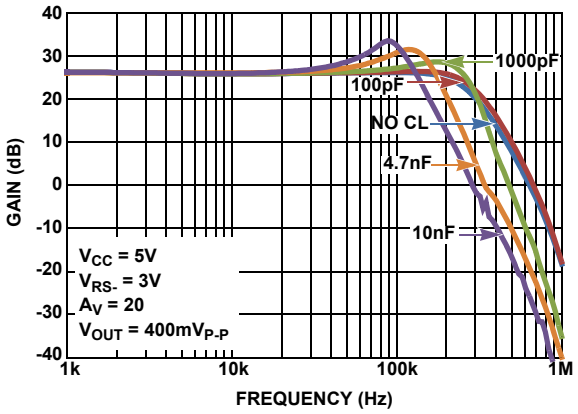


Figure 17. Capacitive Load Drive Gain vs Frequency

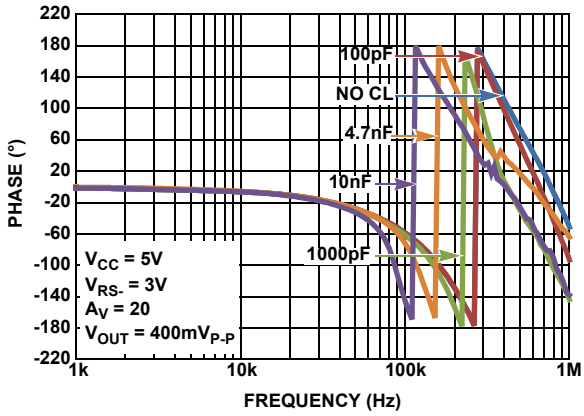


Figure 18. Capacitive Load Drive Phase vs Frequency

V_{CC} = 12V, R_L = 1M, unless otherwise specified. (Cont.)

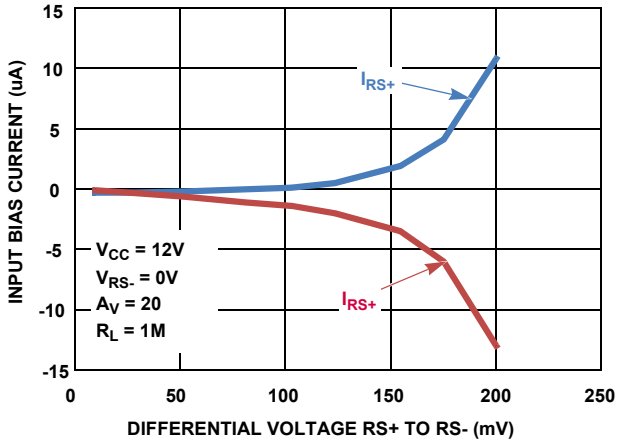


Figure 19. Low-Side Current Sensing Input Bias Currents

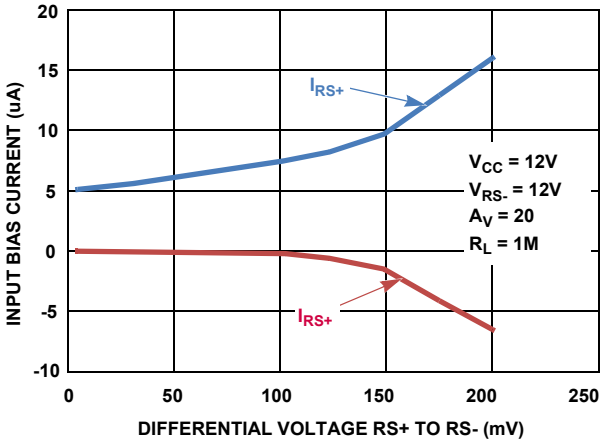


Figure 20. High-Side Current Sensing Input Bias Currents

4.1 Test Circuits and Waveforms

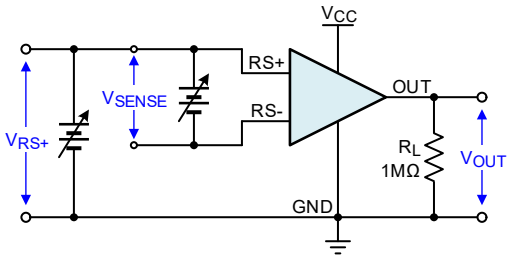


Figure 21. I_{CC}, V_{OS}, V_{OA}, CMRR, PSRR, Gain Accuracy

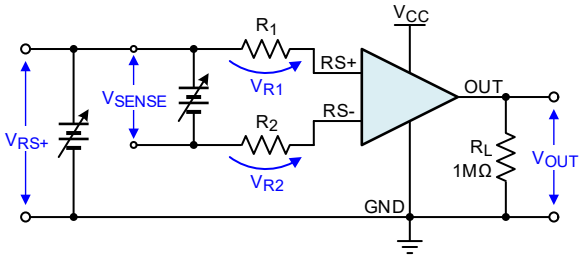


Figure 22. Input Bias Current, Leakage Current

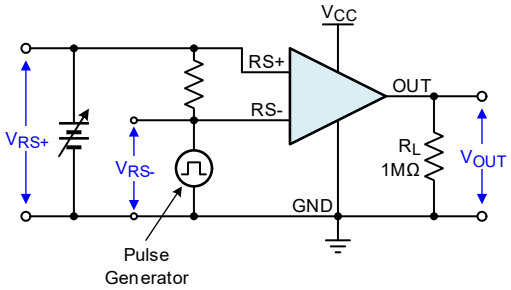


Figure 23. Slew Rate, t_s, Saturation Recovery Time

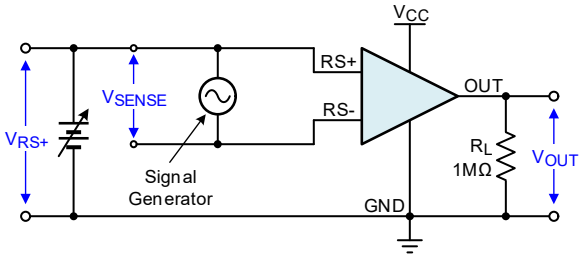


Figure 24. Gain vs Frequency

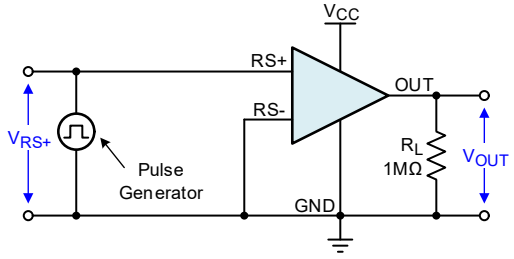


Figure 25. Slew Rate

5. Applications Information

5.1 Functional Description

The ISL28005-20, ISL28005-50 and ISL28005-100 are single supply, uni-directional current sense amplifiers with fixed gains of 20V/V, 50V/V and 100V/V respectively.

The ISL28005 is a 2-stage amplifier. Figure 26 shows the active circuitry for high-side current sense applications where the sense voltage is between 1.35V to 28V. Figure 27 shows the active circuitry for ground sense applications where the sense voltage is between 0V to 1.35V.

The first stage is a bi-level trans-conductance amp and level translator. The gm stage converts the low voltage drop (V_{SENSE}) sensed across an external milli-ohm sense resistor, to a current (at gm = 21.3µA/V). The trans-conductance amplifier forces a current through R_1 resulting to a voltage drop across R_1 that is equal to the sense voltage (V_{SENSE}). The current through R_1 is mirrored across R_5 creating a ground-referenced voltage at the input of the second amplifier equal to V_{SENSE}.

The second stage is responsible for the overall gain and frequency response performance of the device. The fixed gains (20, 50, 100) are set with internal resistors R_f and R_g. The only external component needed is a current sense resistor (typically 0.001Ω to 0.01Ω, 1W to 2W).

The transfer function is given in Equation 1 where I_SR_S is the product of the load current and the sense resistor and is equal to V_{SENSE}.

(EQ. 1) $$V_{OUT} = GAIN \times (I_S R_S + V_{OS})$$

When the sensed input voltage is >1.35V, the gm_{HI} amplifier path is selected and the input gm stage derives its ~2.86µA supply current from the input source through the RS+ terminal. When the sense voltage at R_S+ drops below the 1.35V threshold, the gm_{LO} amplifier is enabled for Low Side current sensing. The gm_{LO} input bias current reverses, flowing out of the RS- pin. Since the gm_{LO} amplifier is sensing voltage around ground, it cannot source current to R5. A current mirror referenced off Vcc supplies the current to the second stage for generating a ground referenced output voltage. See Figure 19 and Figure 20 for typical input bias currents for high-side and low-side current sensing.

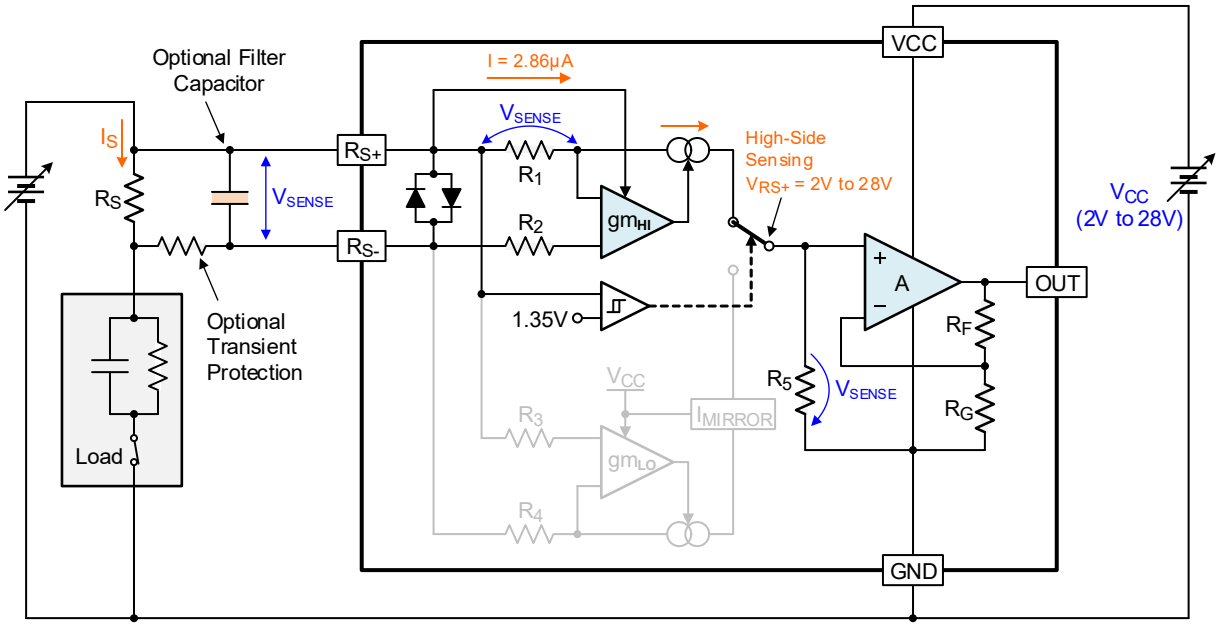


Figure 26. High-Side Current Detection

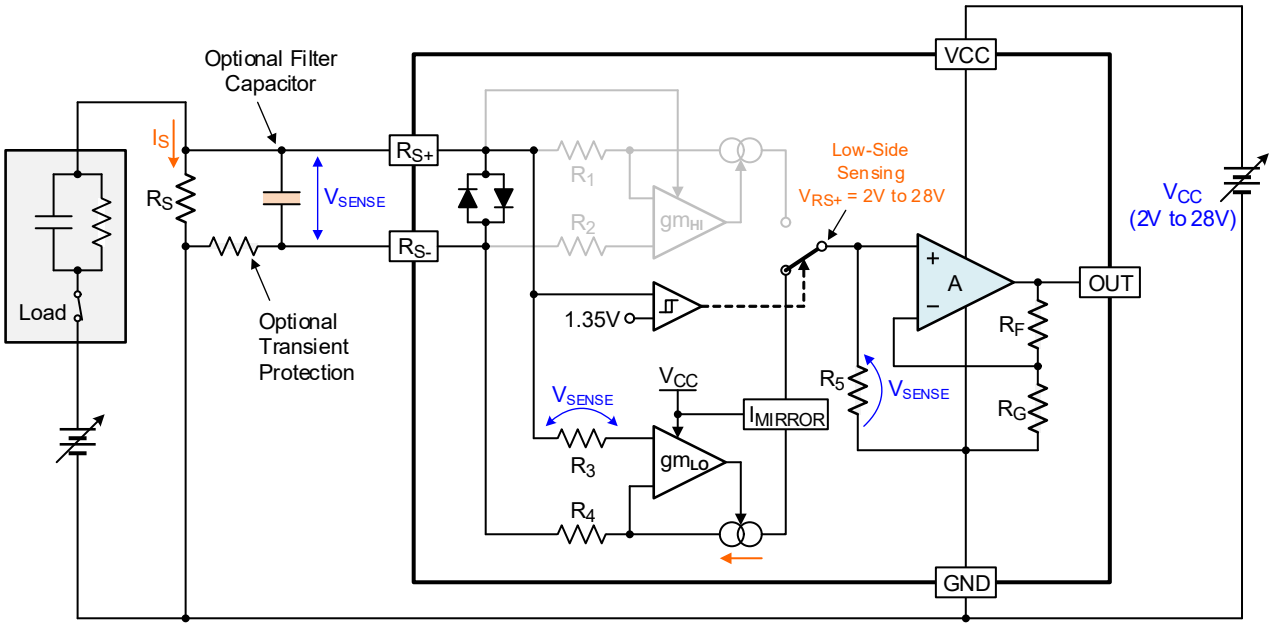


Figure 27. Low-Side Current Detection

5.2 Hysteretic Comparator

The input trans-conductance amps are under control of a hysteretic comparator operating from the incoming source voltage on the RS+ pin (see Figure 28). The comparator monitors the voltage on RS+ and switches the sense amplifier from the low-side gm amp to the high-side gm amplifier whenever the input voltage at R_S+ increases above the 1.35V threshold. Conversely, a decreasing voltage on the RS+ pin, causes the hysteric comparator to switch from the high-side gm amp to the low-side gm amp as the voltage decreases below 1.35V. It is that low-side sense gm amplifier that gives the ISL28005 the proprietary ability to sense current all the way to 0V. Negative voltages on the R_S+ or R_S- are beyond the sensing voltage range of this amplifier.

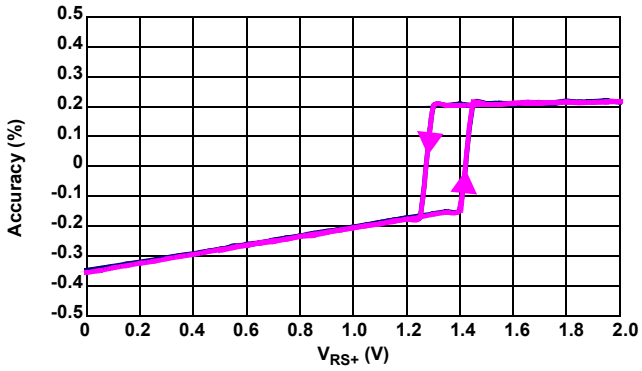


Figure 28. Gain Accuracy vs V_{RS+} = 0V to 2V

5.3 Typical Application Circuit

Figure 29 shows the basic application circuit and optional protection components for switched-load applications. For applications where the load and the power source is permanently connected, only an external sense resistor is needed. For applications where fast transients are caused by hot plugging the source or load, external protection components may be needed. The external current limiting resistor (R_P) in Figure 29 may be required to limit the peak current through the internal ESD diodes to < 20mA. This condition can occur in applications that experience high levels of in-rush current causing high peak voltages that can damage the internal ESD diodes. An R_P resistor value of 100Ω provides protection for a 2V transient with the maximum of 20mA flowing through the input while adding only an additional 13µV (worse case over-temperature) of V_{OS}. See the following formula:

$((R_P \times I_{RS-}) = (100\Omega \times 130nA) = 13\mu V)$

Switching applications can generate voltage spikes that can overdrive the amplifier input and drive the output of the amplifier into the rails, resulting in a long overload recovery time. Capacitors C_M and C_D filter the common mode and differential voltage spikes.

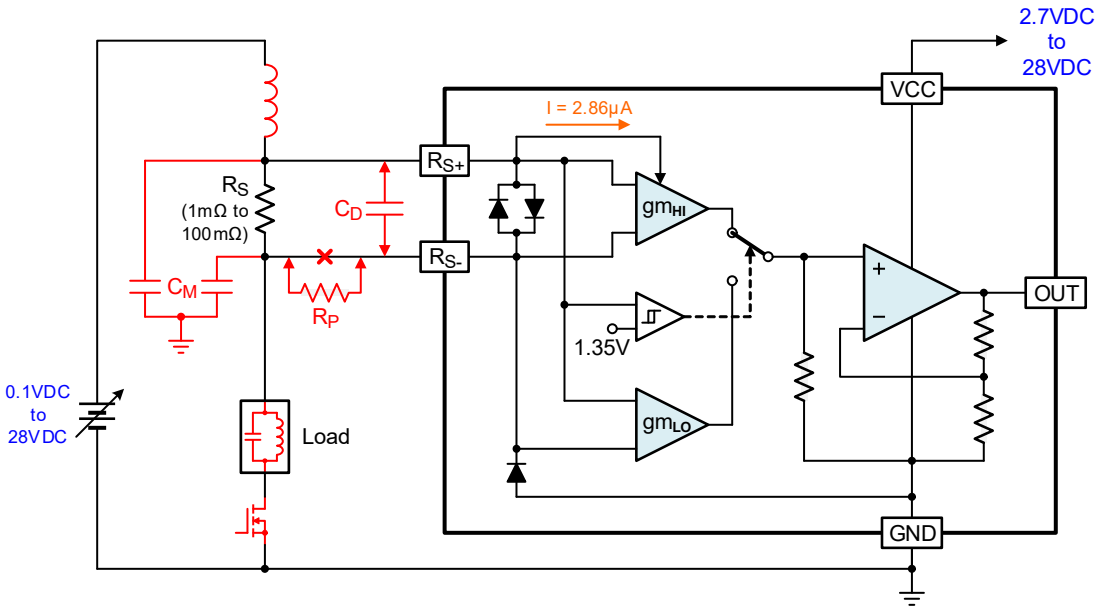


Figure 29. Typical Application Circuit

5.4 Error Sources

There are 3 dominant error sources: gain error, input offset voltage error, and Kelvin voltage error (see Figure 30). The gain error is dominated by the internal resistance matching tolerances. The remaining errors appear as sense voltage errors at the input to the amplifier. They are V_{OS} of the amplifier and Kelvin voltage errors. If the transient protection resistor is added, an additional V_{OS} error can result from the IxR voltage due to input bias current. The limiting resistor should only be added to the R_S- input, due to the high-side gm amplifier (gm_{HI}) sinking several micro amps of current through the RS+ pin.

6. Layout Guidelines

6.1 Kelvin Connected Sense Resistor

The source of Kelvin voltage errors is illustrated in Figure 30. The resistance of 1/2 oz. copper is ~1mΩ per square with a TC of ~3900ppm/°C (0.39%/°C). When you compare this unwanted parasitic resistance with the total of 1mΩ to 10mΩ resistance of the sense resistor, it is easy to see why the sense connection must be chosen very carefully. For example, consider a maximum current of 20A through a 0.005Ω sense resistor, generating a V_{SENSE} = 0.1 and a full scale output voltage of 10V (G = 100). Two side contacts of only 0.25 square per contact puts the V_{SENSE} input about 0.5 x 1mΩ away from the resistor end capacitor. If only 10A the 20A total current flows through the kelvin path to the resistor, you get an error voltage of 10mV (10A x 0.5sq x 0.001Ω/sq. = 10mV) added to the 100mV sense voltage for a sense voltage error of 10% (0.110V - 0.1)/0.1V) x 100.

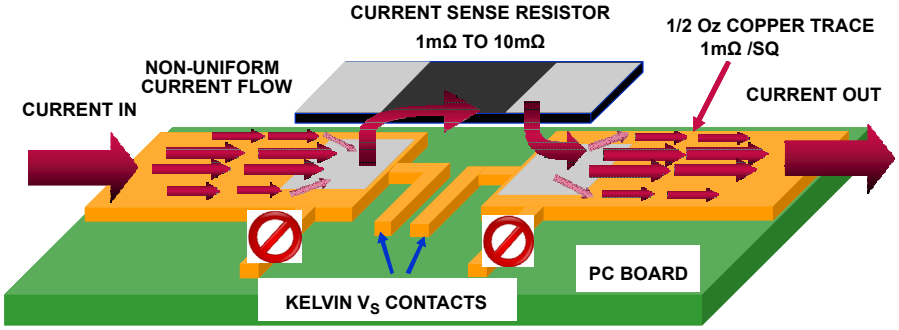


Figure 30. PC Board Current Sense Kelvin Connection

6.2 Overall Accuracy (V_{OA} %)

V_{OA} is defined as the total output accuracy Referred-to-Output (RTO). The output accuracy contains all offset and gain errors, at a single output voltage. Equation 2 is used to calculate the % total output accuracy where V_{OUT} Actual = V_{SENSE} x GAIN.

(EQ. 2) $$V_{OA} = 100 \times \left(\frac{V_{OUT}\text{actual} - V_{OUT}\text{expected}}{V_{OUT}\text{expected}} \right)$$

Example: Gain = 100, For 100mV V_{SENSE} input we measure 10.1V. The overall accuracy (V_{OA}) is 1% as shown in Equation 3.

(EQ. 3) $$V_{OA} = 100 \times \left(\frac{10.1 - 10}{10} \right) = 1\text{percent}$$

6.3 Power Dissipation

It is possible to exceed the +150°C maximum junction temperatures under certain load and power supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related using Equation 4:

(EQ. 4) $$T_{JMAX} = T_{MAX} + \theta_{JA} x PD_{MAXTOTAL}$$

where:

- $P_{DMAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})
- PD_{MAX} for each amplifier can be calculated using Equation 5:

(EQ. 5) $$PD_{MAX} = V_S \times I_{qMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L}$$

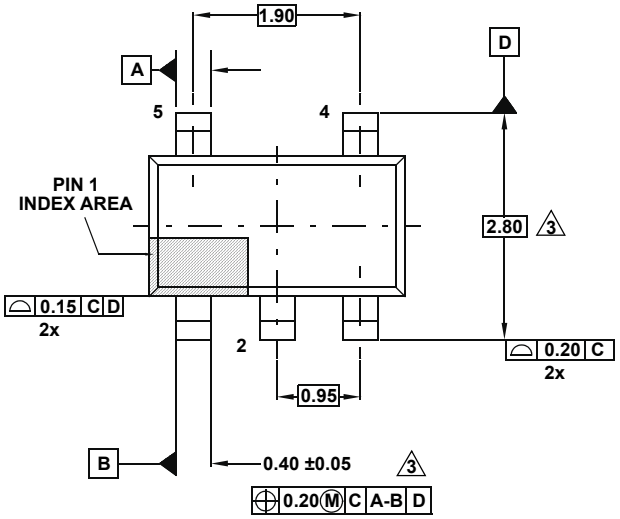
where:

- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- PD_{MAX} = Maximum power dissipation of 1 amplifier
- V_{CC} = Total supply voltage
- I_{qMAX} = Maximum quiescent supply current of 1 amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application
- R_L = Load resistance

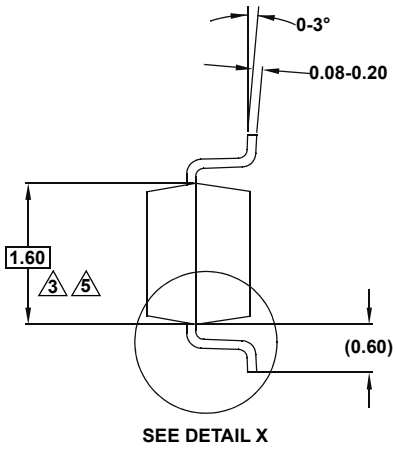
7. Package Outline Drawing

For the most recent package outline drawing, see P5.064A.

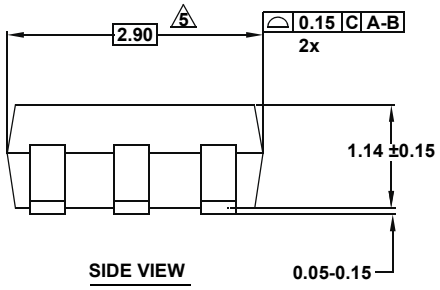
P5.064A
5 Lead Small Outline Transistor Plastic Package
Rev 0, 2/10



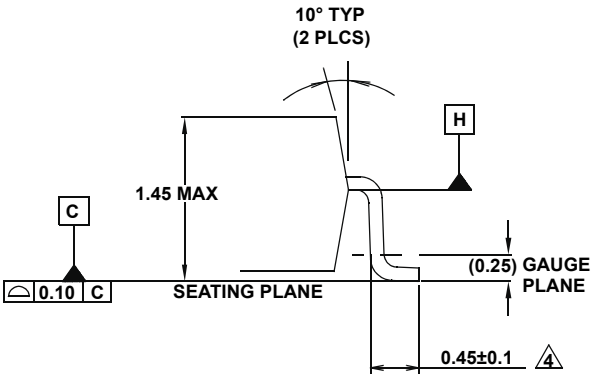
TOP VIEW



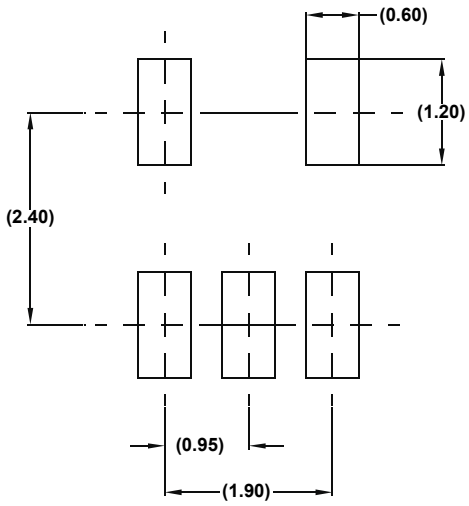
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. Dimension is exclusive of mold flash, protrusions or gate burrs.
4. Foot length is measured at reference to guage plane.
5. This dimension is measured at Datum “H”.
6. Package conforms to JEDEC MO-178AA.

8. Ordering Information

Part Number[1][2]	Gain	Part Marking[3]	Package Description (RoHS Compliant)	PKG. DWG. #	Carrier Type[4]	Temp. Range
ISL28005FH100Z-T7	100V/V	BDEA	5 Ld SOT-23	P5.064A	Reel, 3k	-40 to +125°C
ISL28005FH100Z-T7A					Reel, 250	
ISL28005FH50Z-T7	50V/V	BDDA			Reel, 3k	
ISL28005FH50Z-T7A					Reel, 250	
ISL28005FH20Z-T7	20V/V	BDCA			Reel, 3k	
ISL28005FH20Z-T7A					Reel, 250	
ISL28005FH-100EVAL1Z	100V/V Evaluation Board					
ISL28005FH-50EVAL1Z	50V/V Evaluation Board					
ISL28005FH-20EVAL1Z	20V/V Evaluation Board					

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. For Moisture Sensitivity Level (MSL), see the ISL28005 product page. For more information about MSL, see TB363.
3. The part marking is located on the bottom of the part.
4. See TB347 for details about reel specifications.

9. Revision History

Revision	Date	Change
6.01	Mar 3, 2022	Corrected the Output Resistance units from W back to ohms on page 6.
6.00	Feb 10, 2022	Applied New Template. Removed Related Literature and About Intersil sections. Updated Ordering Information table formatting. Updated Figures 1, Block Diagram. Pin Configuration, and figure in Pin description table. Updated Figure 21 through Figure 27, and Figure 29.
5.00	Oct 24, 2013	Added eight new Typical Performance Curves 1. Av = 100 Capacitive Load Drive Gain vs Freq 2. Av = 100 Capacitive Load Drive Phase vs Freq 3. Av = 50 Capacitive Load Drive Gain vs Freq 4. Av = 50 Capacitive Load Drive Phase vs Freq 5. Av = 20 Capacitive Load Drive Gain vs Freq 6. Av = 20 Capacitive Load Drive Phase vs Freq 7. High Side Operation Input Bias Currents 8. Low Side Operation Input Bias Currents Under Electrical Specifications Table: Changed parameter from Is to Icc to clarify supply current.
4.00	Apr 11, 2011	Corrected location of the load in Figure 27. Moved Load from the ground side of the input sense circuit to the high side of the voltage source. Updated note in Min Max column of spec table from "Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested." to "Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design."
3.00	Sep 2, 2010	Added -T7A tape and reel package options to Ordering Information Table for all packages.

Revision	Date	Change
2.00	May 12, 2010	Added Note 4 to Part Marking Column in Ordering Information table. Corrected hyperlinks in Notes 1 and 3 in Ordering Information table. Corrected ISL28005 hyperlink in “About Intersil” on page 15. Added Eval boards to ordering info. Added “Related Literature” on page 1 Updated Package Drawing Number in the Ordering Information table from MDP0038 to P50.64A. Revised package outline drawing from MDP0038 to P5.064A. MDP0038 package contained 2 packages for both the 5 and 6 Ld SOT-23. MDP0038 was obsoleted and the packages were separated and made into 2 separate package outline drawings; P5.064A and P6.064A. Changes to the 5 Ld SOT-23 were to move dimensions from table onto drawing, add land pattern and add JEDEC reference number.
1.00	Feb 3, 2010	-Page1: Edited last sentence of paragraph 2. Moved order of GAIN listings from 20, 50, 100 to 100, 50, 20 in the 3rd paragraph. Under Features ....removed "Low Input Offset Voltage 250µV,max" Under Features .... moved order of parts listing from 20, 50, 100 (from top to bottom) to 100, 50, 20. -Page 3: Removed coming soon on ISL28005FH50Z and ISL28005FH20Z and changes the order or listing them to 100, 50, 20. -Page 5: VOA test. Under conditions column ...deleted “20mV to”. It now reads ... Vsense = 100mV SR test. Under conditions column ..deleted what was there. It now reads ... Pulse on RS+pin, See Figure 25 -Page 6: ts test. Removed Gain = 100 and Gain = 100V/V in both description and conditions columns respectively. -Page 9 Added Figure 25 and adjusted figure numbers to account for the added figure.
0.00	Dec14, 2009	Initial Release

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/