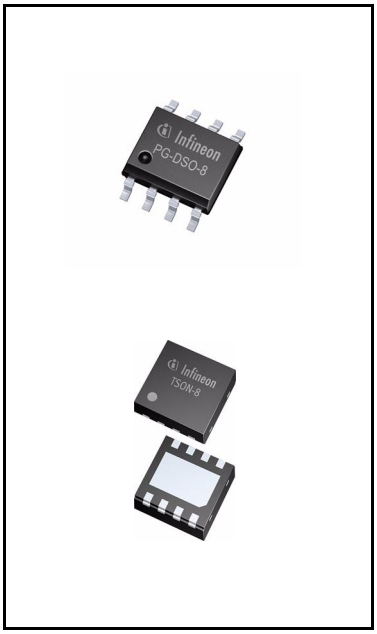
TLE8457C / TLE8457D

LIN Transceiver with integrated voltage regulator

AEC Qualified

RoHS



1 Overview

Features

- Single-wire LIN transceiver for transmission rates up to 20 kBit/s
- Compliant to ISO 17987-4, LIN specification 2.2 A and SAE J2602
- 5 V or 3.3 V low drop-out linear voltage regulator with 70 mA current capability
- Stable with ceramic output capacitor of 1 µF
- Ultra low current consumption in sleep mode of max. 16 µA
- Ultra low current consumption in standby mode of typical 20 µA
- Very low leakage current on the BUS pin
- V_{CC} undervoltage detection with RESET output
- TxD protected with dominant time-out function
- BUS short to V_{BAT} protection and BUS short to GND handling
- Overtemperature protection and supply undervoltage detection
- Very high ESD robustness: ±8 kV according to IEC61000-4-2
- Optimized for high electromagnetic compatibility (EMC);
  Very low emission and high immunity to interference
- Available in standard PG-DSO-8 and leadless PG-TSON-8 packages
- PG-TSON-8 package supports automated optical inspection (AOI)
- Green Product (RoHS compliant)

Potential applications

- LIN slave satellite modules
- Window lifters
- Rain and light sensors
- Sun roof control modules
- Wiper modules
- Ambient lighting

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

Description

The TLE8457C / TLE8457D is a monolithic integrated LIN transceiver and low drop-out voltage regulator. The device is designed to supply a microcontroller and peripherals with up to 70 mA, provide protection through V_{CC} undervoltage reset, while also offering bi-directional bus communication compliant to LIN specification 2.2 A and SAE J2602. With the ultra low quiescent current consumption of typical 20 µA in standby mode the TLE8457C / TLE8457D is especially suited for applications that are permanently supplied by the battery.

Based on the Infineon BiCMOS technology the TLE8457C / TLE8457D provide excellent ESD robustness together with a very high level of electromagnetic compatibility (EMC). The TLE8457C / TLE8457D is AEC qualified and tailored to withstand the harsh conditions of the automotive environment.

Type	LDO V_{CC} output voltage	Package	Marking	Init timeout feature[1)]
TLE8457CSJ	5 V	PG-DSO-8	8457C	No
TLE8457CLE	5 V	PG-TSON-8	8457C	No
TLE8457DSJ	3.3 V	PG-DSO-8	8457D	No
TLE8457DLE	3.3 V	PG-TSON-8	8457D	No

1) “Init timeout feature” is only available with TLE8457A & TLE8457B.

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2 Block diagram

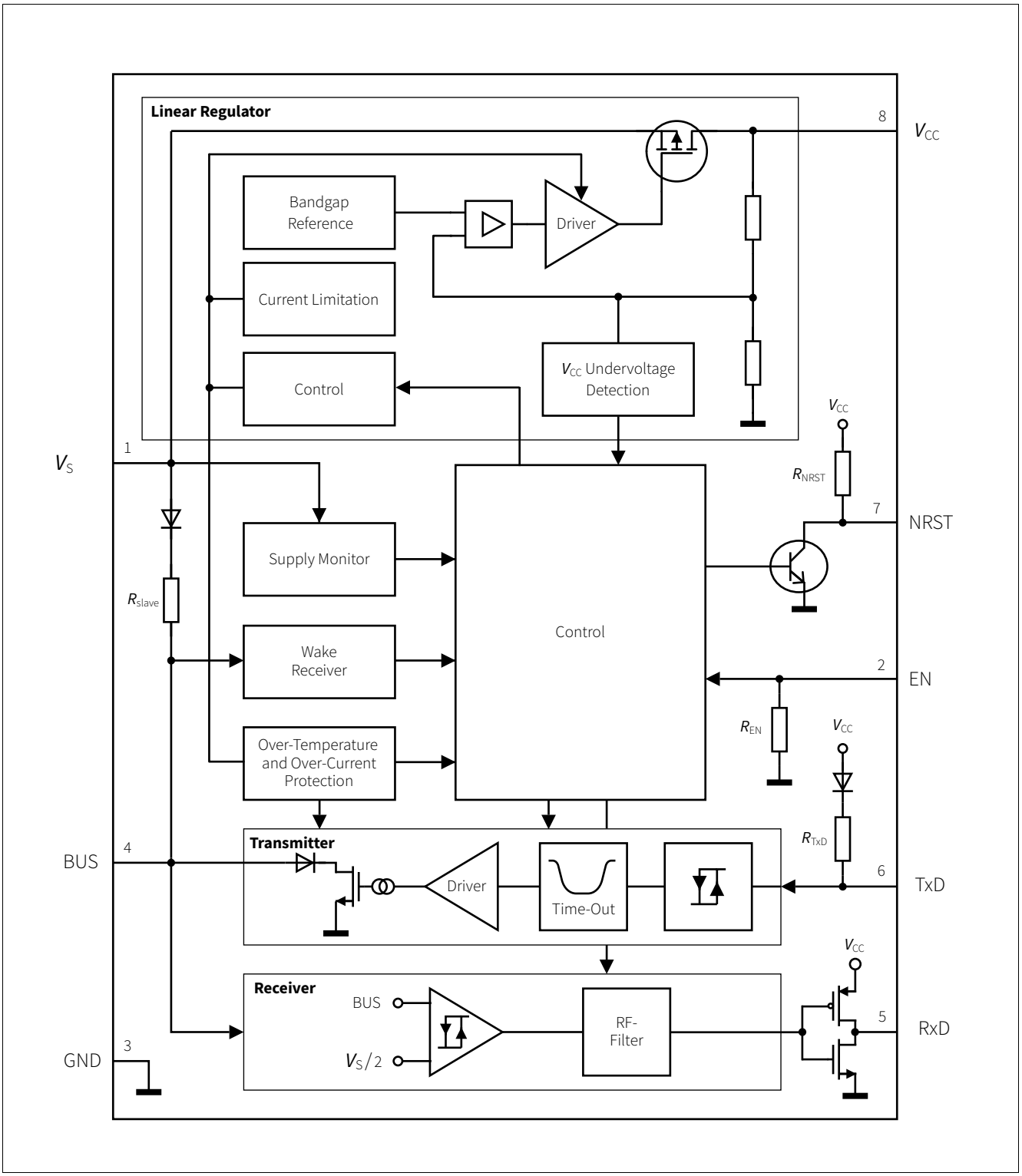

Figure 1 Block diagram

3 Pin configuration

3.1 Pin assignment

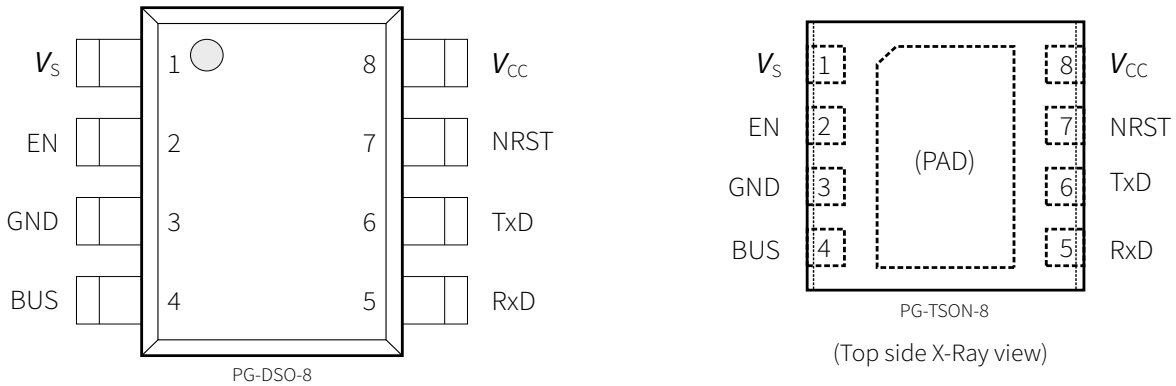

Figure 2 Pin configuration

3.2 Pin definitions and functions

Pin	Symbol	Function
1	VS	**Battery supply voltage;** Decoupling capacitor required
2	EN	**Enable input;** Integrated pull-down resistor Logic “high” to select normal operation mode
3	GND	**Ground**
4	BUS	**BUS input/output;** Integrated LIN slave termination
5	RxD	**Receive data output;** Monitors the LIN bus signal in normal operation mode Indicates a wake-up event in standby mode
6	TxD	**Transmit data input;** Integrated pull-up resistor Logic “low” to drive a dominant signal on the LIN bus
7	NRST	**Undervoltage reset output;** Integrated pull-up resistor Logical “low” during reset
8	VCC	**Voltage regulator output;** Output capacitor requirements specified in functional device characteristics
PAD[1)]	–	Connect to PCB heat sink area. Do not connect to other potential than GND

1) Only available with PG-TSON8 package.

4 Functional description

4.1 Operating modes

The operation mode of the TLE8457C / TLE8457D is controlled with the EN and TxD input pins (see **Figure 3** and **Table 2**). The TLE8457C / TLE8457D has 3 major operation modes:

- Normal operation mode
- Standby mode
- Sleep mode

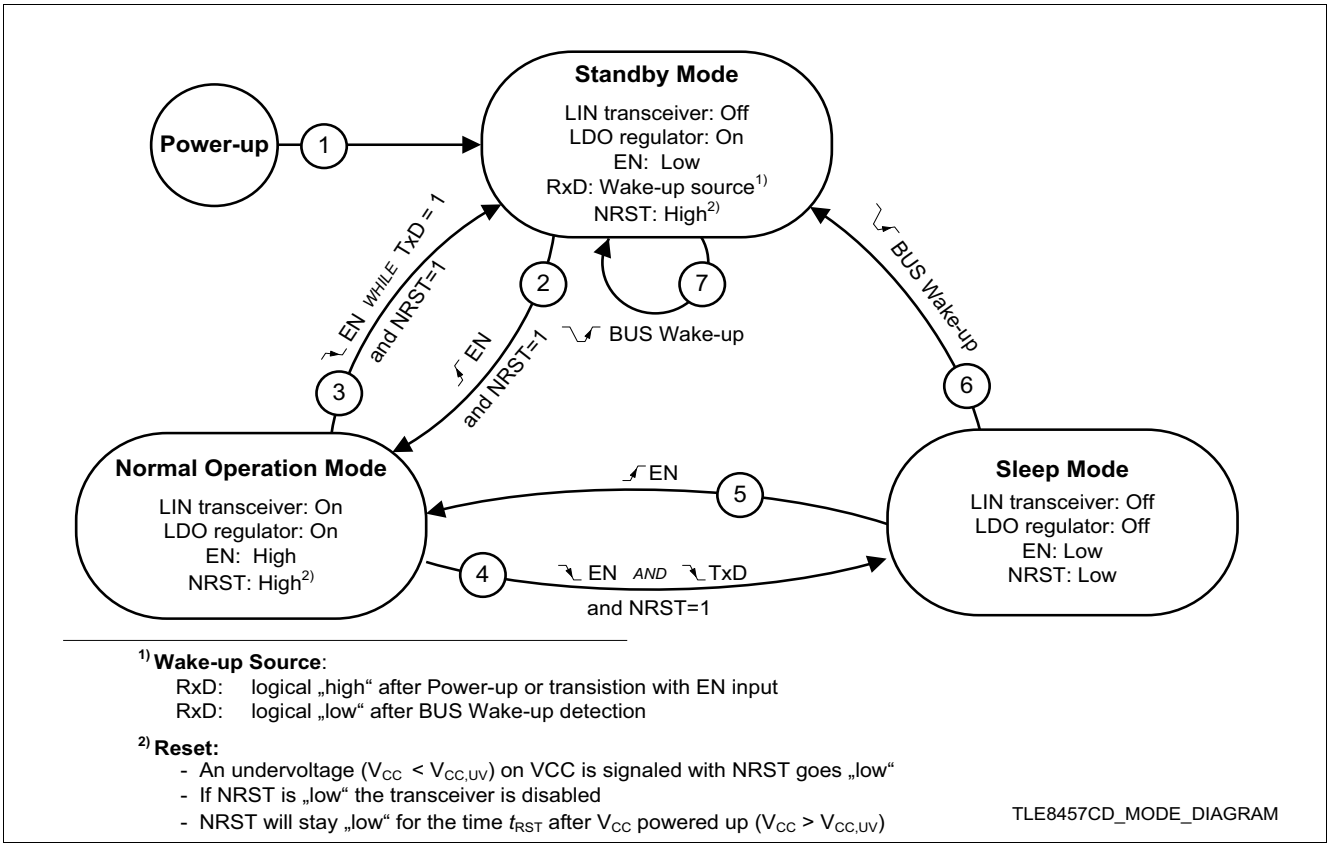

Figure 3 Operation mode state diagram

Table 1 Operation mode transitions

No.	Reason for transition	Comment
1	Power-on detection	The V_S supply voltage rise above the $V_{S,PON}$ power-on reset level.
2	Mode change with EN input	Triggered by logic “high” level. V_{CC} has to be in the functional range.
3	Mode change with EN and TxD inputs	Triggered by logic “low” level on EN while TxD is held “high”. V_{CC} has to be in the functional range.
4	Mode change with EN and TxD inputs	Triggered by logic “low” level on EN and TxD. V_{CC} has to be in the functional range.
5	Mode change with EN input	Triggered by logic “high” level.

Table 1 Operation mode transitions (cont'd)

No.	Reason for transition	Comment
6	Bus wake-up detection	RxD is set "low" for signalling the bus wake-up event to the microcontroller.
7	Bus wake-up detection in standby mode	RxD is set "low" for signalling the bus wake-up event to the microcontroller. Operating mode is not changed.

Table 2 Operating mode control

Mode	Control		Functionality			Comments
	EN	TxD	V_{CC}	NRST	RxD	
Sleep	Low	Low	Off	Low	Floating	–
Standby	Low	High[1)]	On	High[2)]	Low High	RxD "low" after a bus wake-up RxD "high" after power-up or reset
Normal operation	High	Low High	On	High[2)]	Low High	RxD reflects the signal on the bus TxD driven by the microcontroller

1) The TxD input has a pull-up structure to V_{CC} and is per default set to logic "high" if left open.

2) NRST is logic "low" during V_{CC} undervoltage and while issuing a reset pulse to the microcontroller.

4.1.1 Normal operation mode

In normal operation mode both the voltage regulator and the LIN transceiver are active. The TLE8457C / TLE8457D supports data transmission rates up to 20 kBit/s. Data from the microcontroller is transmitted to the LIN bus via the TxD input, while the receiver detects the data stream on the LIN bus and forwards it to the RxD output.

After entering normal operation mode the TLE8457C / TLE8457D requires a logic “high” signal for the time $t_{to,rec}$ on the TxD input before releasing the data communication. The transmitter remains deactivated as long as the signal on the TxD input pin remains logic “low”, preventing possible bus communication disturbance (see **Figure 4**).

From normal operation mode the TLE8457C / TLE8457D can be set to standby mode or sleep mode.

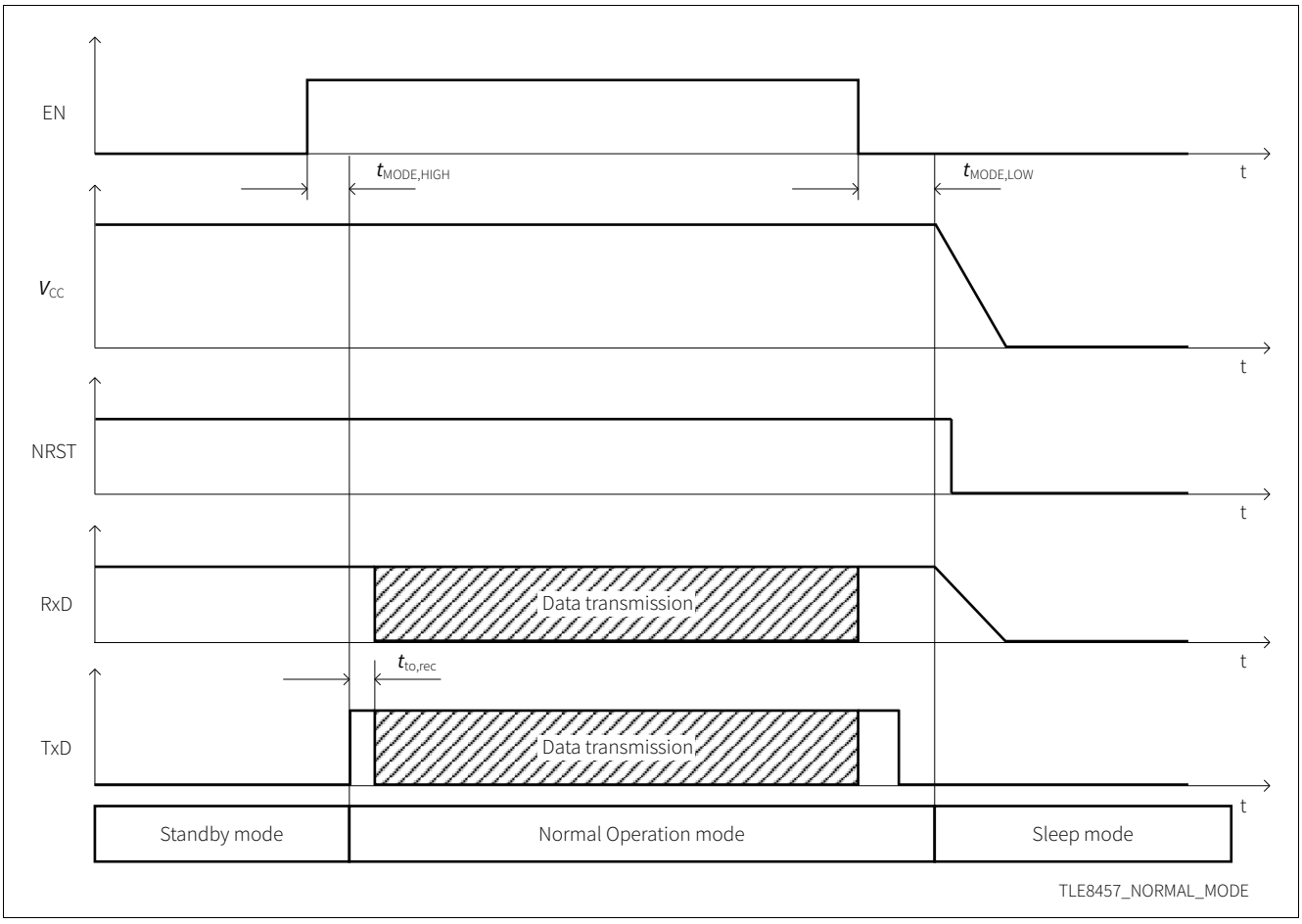

Figure 4 Entering normal operation mode, transition to sleep mode

4.1.2 Standby mode

Standby mode is a low power mode with ultra low quiescent current consumption while the voltage regulator remains active, supplying for example a microcontroller in stop mode. No LIN bus communication is possible, the transmitter and the receiver are disabled. The low power receiver is still active and the device can wake up by a message from the LIN bus.

For changing the operation mode from standby mode to sleep mode, the device has to be set to normal operation mode first, then to sleep mode (see **Figure 4**).

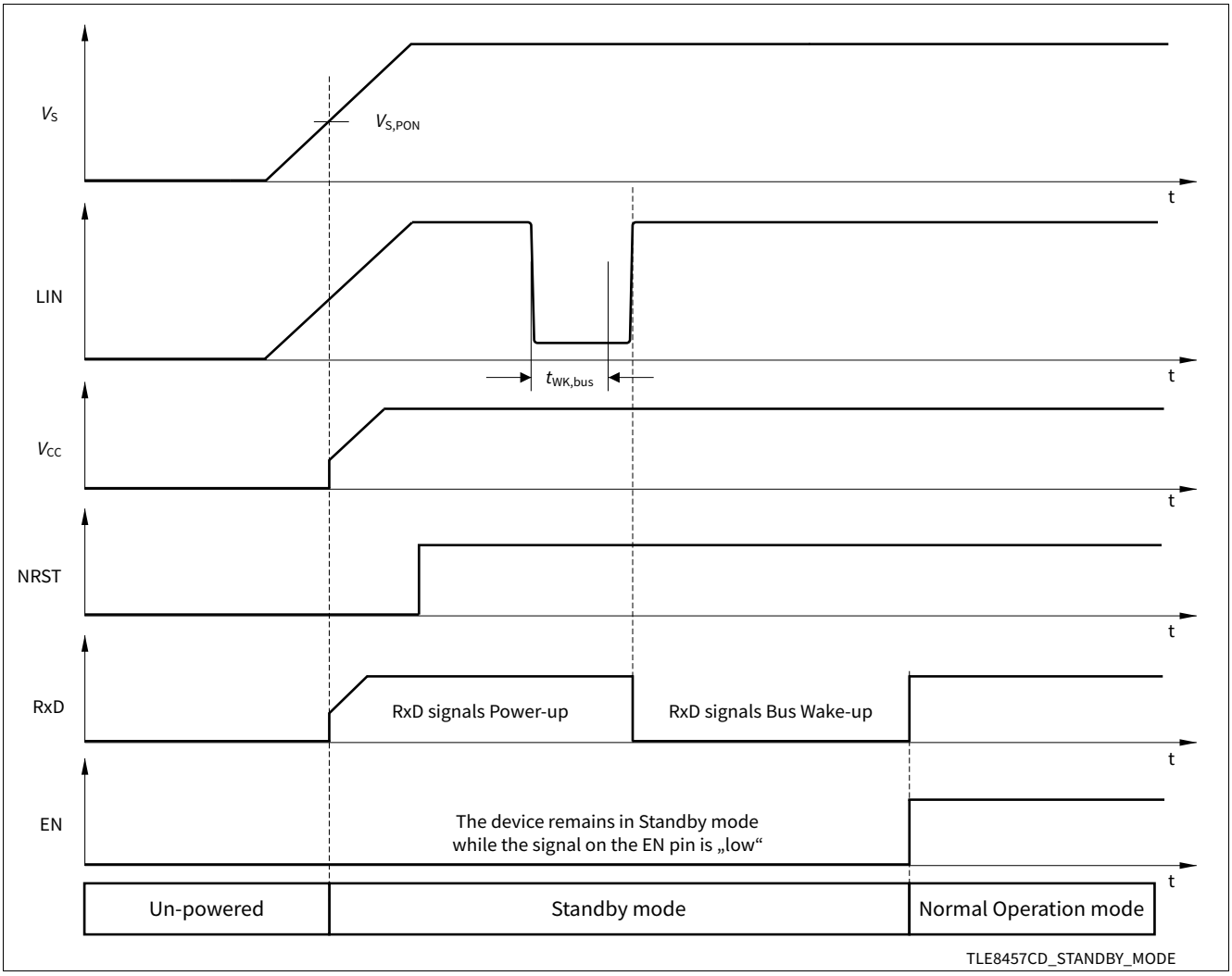

Figure 5 Entering standby mode after power-up

In standby mode the TLE8457C / TLE8457D indicates wake-up information on the RxD output. After a power-up and reset event, the RxD output will be “high”. If the TLE8457C / TLE8457D is in standby mode after bus wake-up detection, the RxD output will be “low”.

4.1.3 Sleep mode

Sleep mode is a low power mode with quiescent current consumption reduced to a minimum while the device can still wake up by a message from the LIN bus. Both the transceiver and the voltage regulator are switched off.

4.1.4 Bus wake-up event

A bus wake-up event, also called remote wake-up, causes a transition from a low power mode to standby mode. A falling edge on the LIN bus, followed by a dominant BUS signal for the time $t_{WK,bus}$ results in a bus wake-up event. The mode change to standby mode becomes active with the following rising edge on the LIN bus, when BUS voltage exceeds $V_{BUS,wk}$. The TLE8457C / TLE8457D remains in low power mode until it detects a state change on the LIN bus from dominant to recessive (see **Figure 6**). In standby mode a logic “low” signal on the RxD output indicates a bus wake-up event.

In case the TLE8457C / TLE8457D detects a bus wake-up event while already being in standby mode, the wake-up event will be signalled with a logic “low” level on RxD and override the previous wake source (see **Figure 5**).

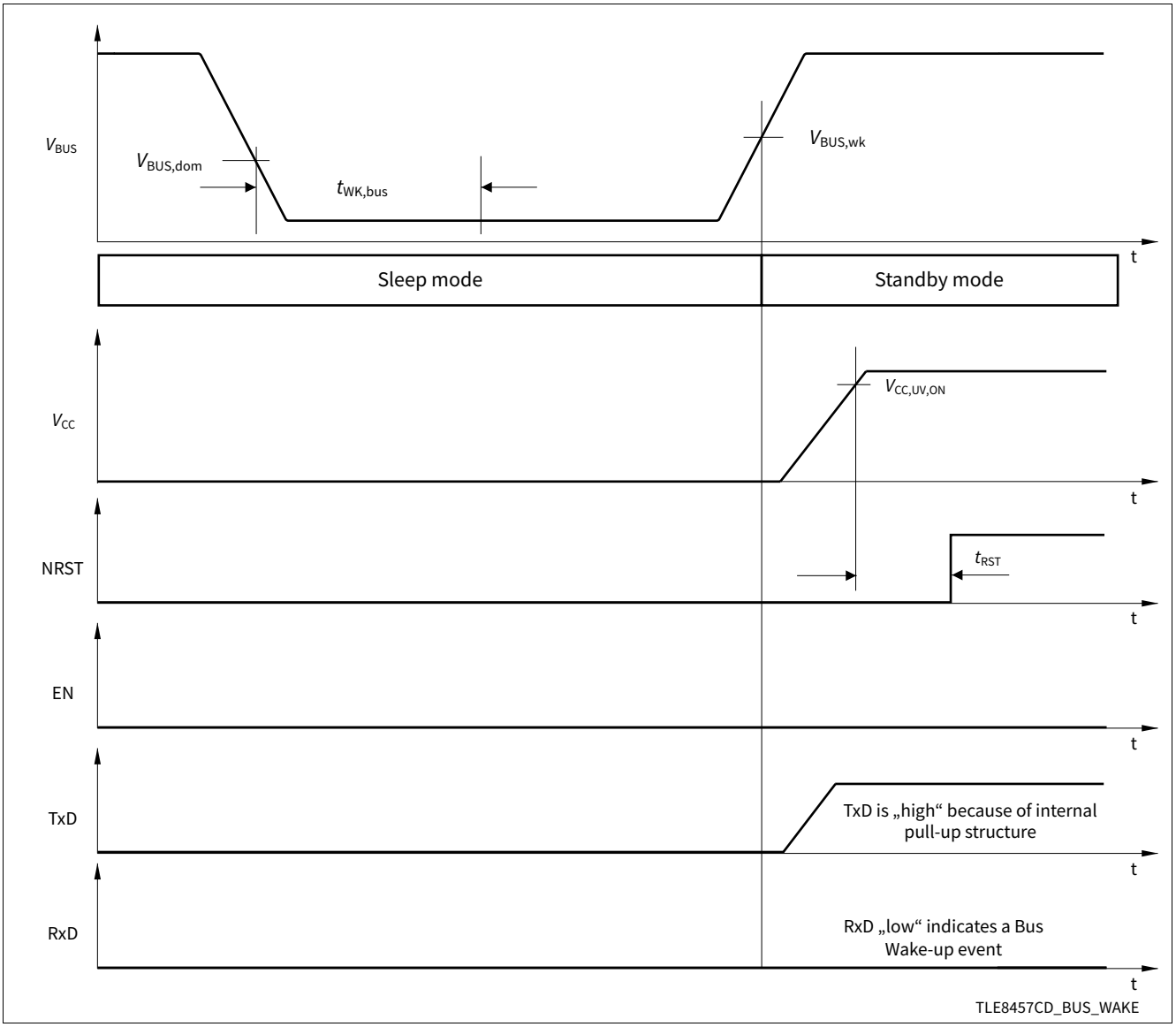

Figure 6 Bus wake-up behavior

4.1.5 Mode transition via EN pin

The EN input is used for operation mode control of the TLE8457C / TLE8457D. By setting the EN input logic “high” for the time $t_{MODE,HIGH}$ while being in standby mode, a transition to normal operation mode will be triggered.

If the voltage level at the EN input is set logic “high” while the TLE8457C / TLE8457D is in sleep mode, a transition to normal mode is initiated.

From normal operation mode the TLE8457C / TLE8457D can be set to either sleep mode or standby mode. If the EN input is set “low” for the time $t_{MODE,LOW}$ while the TxD input is held at logic “high”, the mode will change to standby mode. For a transition to sleep mode, the TxD must be set to logic “low” before the time $t_{MODE,LOW}$ elapses after EN goes “low” (see **Figure 7**). It is recommended to program a short delay time from when EN is set “low” until TxD is set “low”, to prevent driving the BUS dominant through mode transition to sleep mode.

The EN input has an integrated pull-down resistor to ensure the device remains in a low power mode if the EN input is left open. The EN input has an integrated hysteresis (see **Figure 7**).

The TLE8457C / TLE8457D changes the operation modes regardless of the signal on the BUS pin. In the case of a short circuit failure between the LIN bus and GND, resulting in a permanent dominant signal, the TLE8457C / TLE8457D can be set to sleep mode.

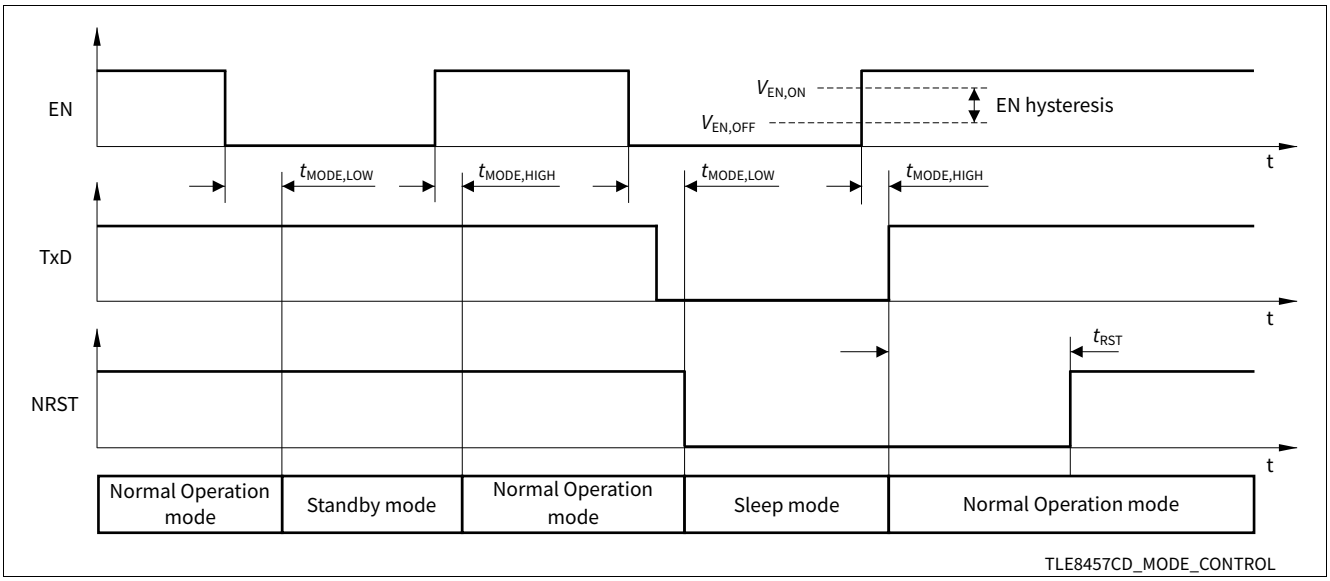

Figure 7 Operation mode control

The EN input is blocked while the TLE8457C / TLE8457D is in normal operation mode or standby mode and NRST is “low”, indicating an undervoltage on V_{cc}. After the NRST output goes “high”, mode control with the EN input is released again.

4.2 Power supplies

The TLE8457C / TLE8457D is designed for being supplied by the battery line through an external reverse polarity protection diode at the V_S pin (see **Figure 16**). An input capacitor is needed for damping input line transients.

4.2.1 Power-up and power-down

During power-up the TLE8457C / TLE8457D will enter standby mode when the V_S supply reaches the power-on reset level $V_{S,PON}$. The voltage regulator output V_{CC} will track the V_S supply voltage until V_{CC} reaches its nominal voltage level. As V_{CC} reaches the undervoltage level $V_{CC,UV}$, the NRST output will stay logic “low” for the reset

time t_{RST} and then be set logic “high”. As NRST goes “high”, the EN input will become active and the TLE8457C / TLE8457D can change operating mode accordingly (see **Table 2**).

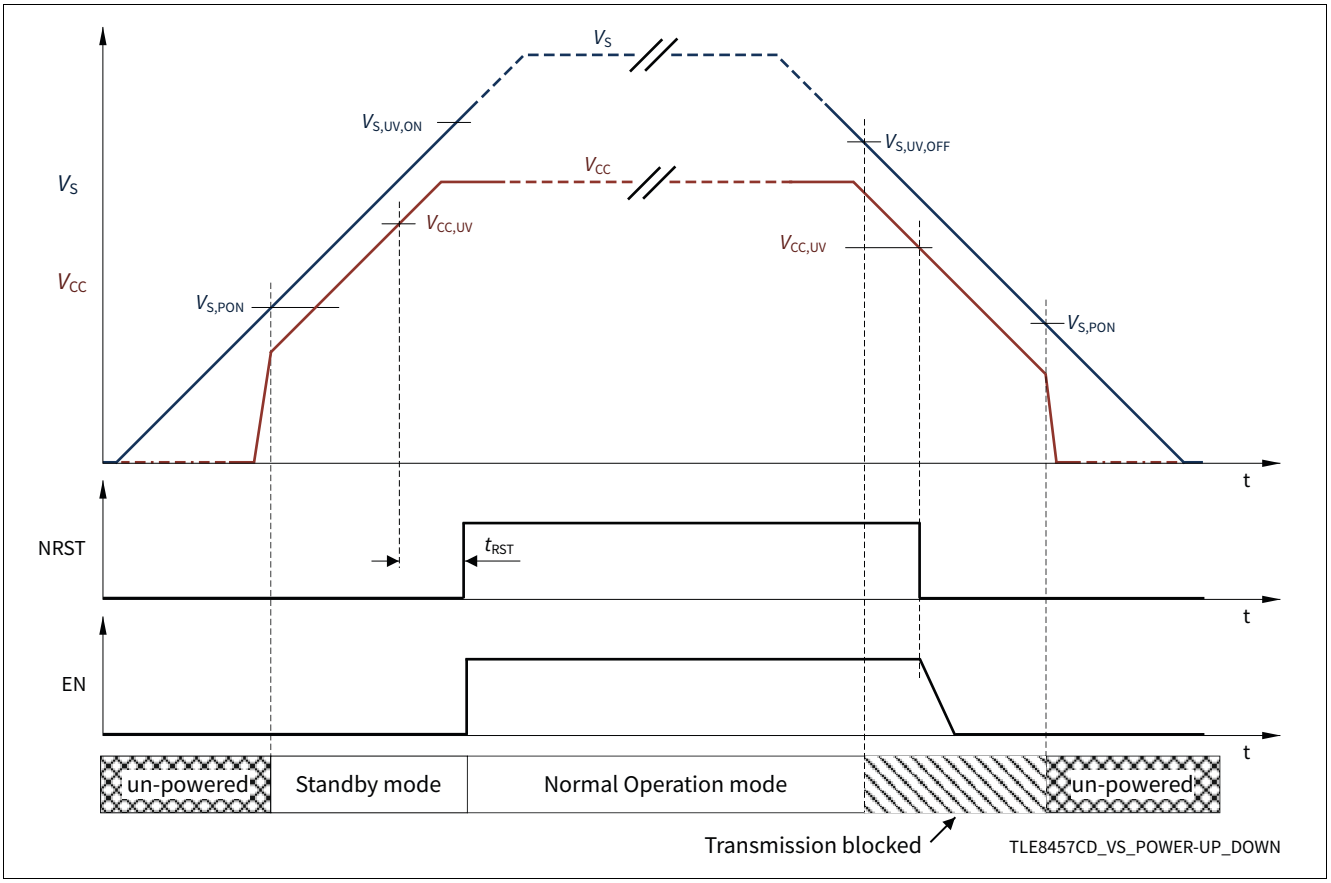

Figure 8 Power-up and power-down behavior

While powering down while in normal operation mode the TLE8457C / TLE8457D will block the LIN transmitter as the V_S supply voltage falls below $V_{S,UV,OFF}$. The voltage regulator will start tracking the V_S supply voltage when falling below $V_{CC} + V_{DR}$. As V_{CC} falls below the undervoltage level $V_{CC,UV}$, the NRST output will be set logic “low”. When the V_S supply voltage falls below the power-on-reset level $V_{S,PON}$ the voltage regulator will be disabled and the TLE8457C / TLE8457D will be considered unpowered.

4.2.2 V_S undervoltage detection

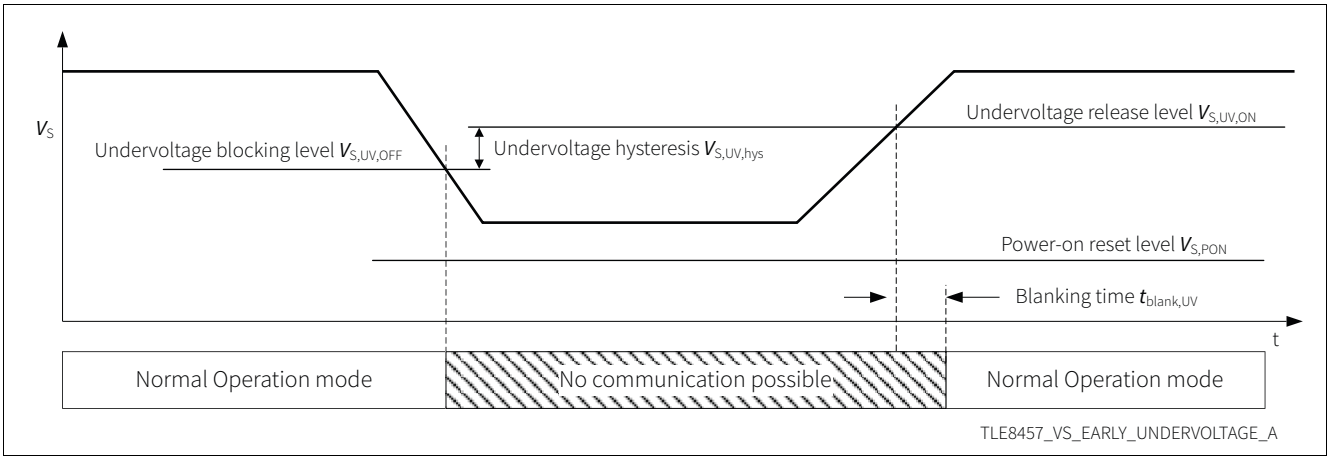

Figure 9 V_S early undervoltage detection

The TLE8457C / TLE8457D has an undervoltage detection on the supply pin V_S with two different thresholds:

- In normal operation mode the TLE8457C / TLE8457D blocks the communication between the LIN bus and the microcontroller when detecting an early undervoltage event. The RxD output will be set “high”. However, no mode change will occur. After V_S rises above the undervoltage release level $V_{S,UV,REL}$, the bus communication interface will be released as soon as the signal on the TxD input goes “high” (see **Figure 9**).
- When the power supply V_S drops below the power-on reset level $V_{S,PON}$ the TLE8457C / TLE8457D not only blocks the transceiver communication, it also changes the operation mode to standby mode after recovery of V_S, see **Figure 10**. In standby mode the TLE8457C / TLE8457D indicates a power-up event on the RxD pin. The power-on reset detection is active in all operation modes.

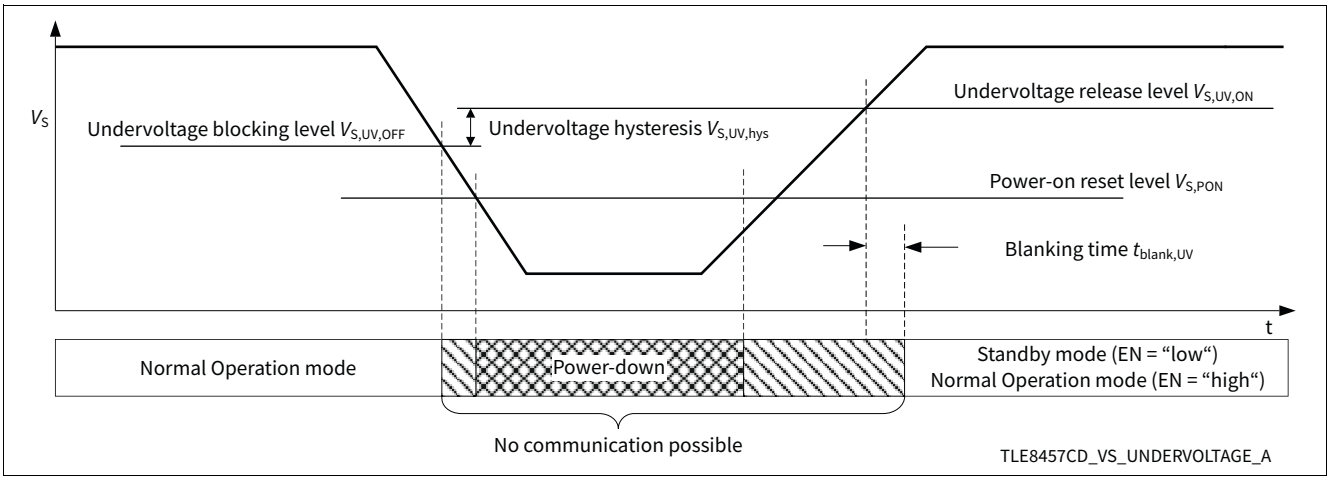

Figure 10 V_S undervoltage detection

4.3 Voltage regulator

The TLE8457C / TLE8457D has an integrated voltage regulator dedicated for supplying microcontrollers and/or on-board sensors under harsh automotive environment conditions. It can supply a load current up to 70 mA with an output voltage tolerance within ± 2%. Because of the ultra low current consumption, the TLE8457C / TLE8457D is perfectly suited for applications permanently connected to the battery supply. Additionally, in sleep mode, the voltage regulator is switched off and an even lower quiescent current can be achieved.

The voltage regulator output is protected against undervoltage, overcurrent, overtemperature and power-up failures. In case the load current rises above the functional range, for example during V_{CC} short circuits, the output current is limited to $I_{CC,lim}$. Therefore the V_{CC} output voltage will drop. A reset pulse will be issued if V_{CC} falls below the undervoltage reset threshold.

The V_{CC} supply output provides a stable supply voltage with output capacitors down to 1 µF, including low ESR multi-layer ceramic capacitors.

4.3.1 V_{CC} undervoltage detection

The TLE8457C / TLE8457D has an undervoltage detection feature on the voltage regulator V_{CC} output. If the V_{CC} voltage falls below the undervoltage threshold $V_{CC,UV}$ for longer than detection time $t_{det,RST}$, the NRST output will be set logic “low” and the transceiver will be deactivated.

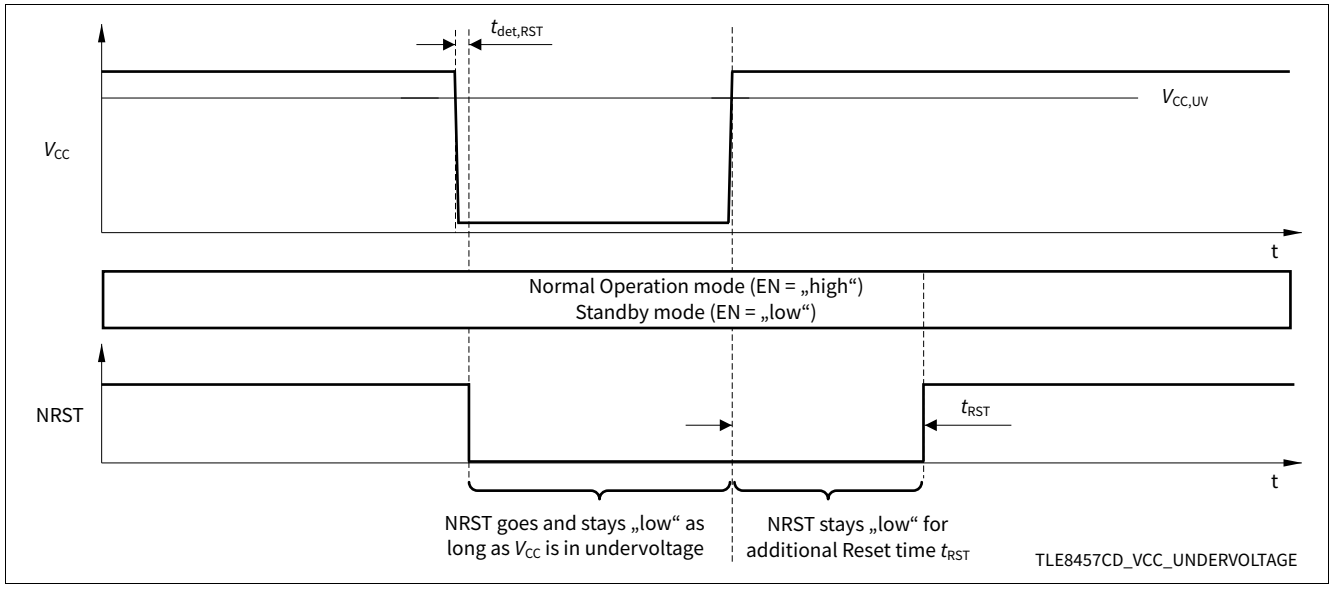

Figure 11 V_{CC} undervoltage detection

4.3.2 Reset output

The NRST output is used for issuing reset pulses, for example to an external microcontroller. In case of voltage regulator undervoltage or overtemperature events, the NRST output will go “low” and the transceiver is deactivated. The NRST output will stay “low” until a complete recovery from the failure is achieved. After the additional time t_{RST} has elapsed NRST will go “high” (see **Figure 11**).

While NRST is “low” mode transition is blocked.

The NRST pin has an internal pull up to V_{CC}. If needed in the application, an additional external pull-up resistor can be implemented.

4.4 LIN transceiver

The LIN interface is a single wire, bi-directional bus, used for in-vehicle networks. The integrated LIN transceiver of the TLE8457C / TLE8457D is the interface between the microcontroller and the physical LIN bus (see **Figure 16**). Data from the microcontroller is driven to the LIN bus via the TxD input. The transmit data stream on the TxD input is converted to a LIN bus signal with optimized slew rates in order to minimize the electromagnetic emission of the LIN network. The RxD output reads back the information from the LIN bus to the microcontroller. The receiver has an integrated filter network for noise suppression from the LIN bus and to increase the electromagnetic immunity level of the transceiver.

The LIN specification defines two valid bus levels (see **Figure 12**):

- Dominant state with the LIN bus voltage level near GND, actively driven by a transceiver.
- Recessive state with the LIN bus voltage pulled up to the supply voltage V_S through the bus termination.

By setting the TxD input of the TLE8457C / TLE8457D to a logic “low” signal, the transceiver generates a dominant level on the BUS interface pin. The receiver reads back the signal on the LIN bus and indicates the dominant LIN bus signal with a logic “low” on the RxD output to the microcontroller. By setting the TxD input “high”, the transceiver sets the LIN interface pin to the recessive level. At the same time the recessive level on the LIN bus is indicated by a logic “high” signal on the RxD output.

Every LIN network consists of a master node and one or more slave nodes. To configure the TLE8457C / TLE8457D for master node applications, a termination resistor of 1 kΩ and a diode must be connected between the LIN bus and the power supply V_S (see **Figure 16**).

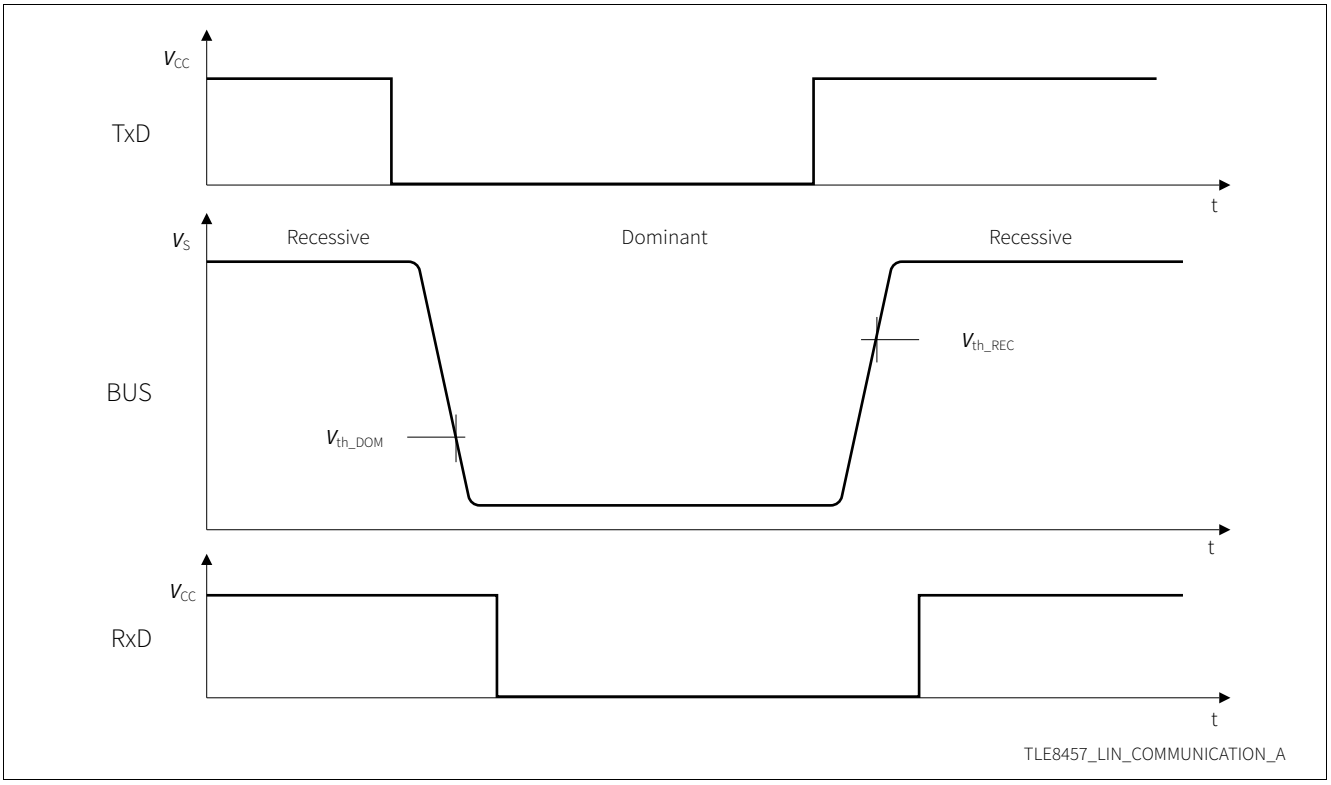

Figure 12 LIN bus signals

4.4.1 TxD time-out

The TxD time-out feature protects the LIN bus against permanent blocking in the case where the logical signal on the TxD input is continuously “low”, caused by a malfunctioning microcontroller or a short circuit on the printed circuit board for example. In normal operation mode, a logic “low” signal on the TxD input for time t > t_{TxD} disables the transmitter’s output driver stage (see **Figure 13**). The receiver will remain active and the data on the BUS is still monitored on the RxD output.

The TLE8457C / TLE8457D will release the output stage after a TxD time-out event first when detecting a logic “high” signal on the respective TxD input for the duration of $t_{to,rec}$.

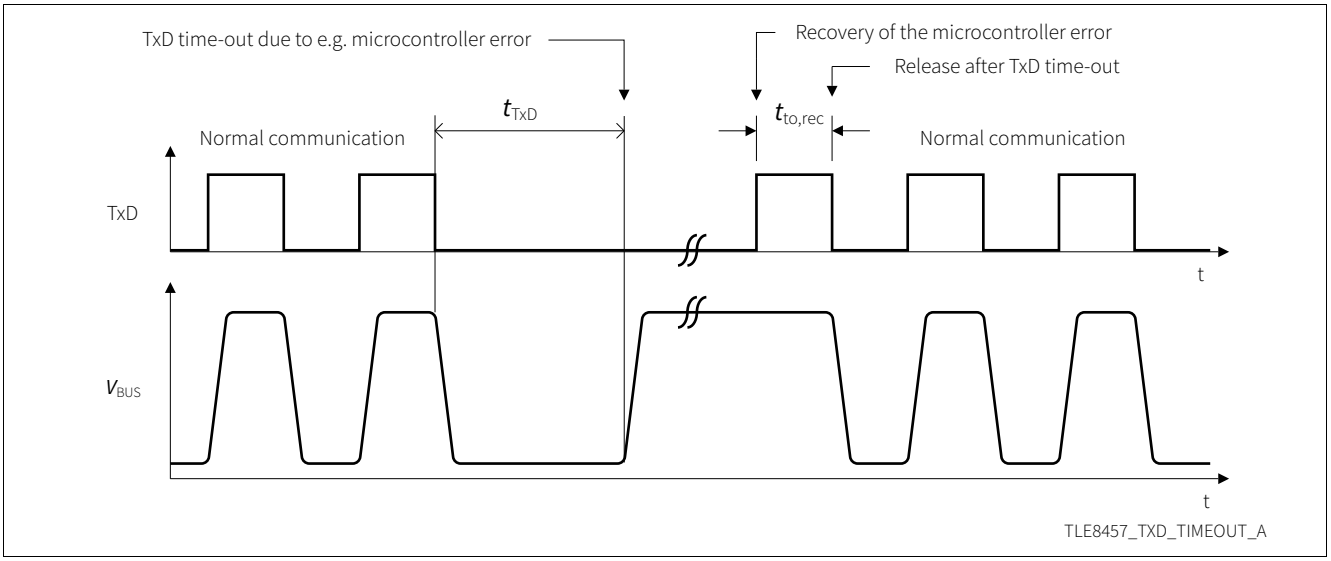

Figure 13 TxD time-out

4.4.2 Short-circuit

The BUS pin of TLE8457C / TLE8457D can withstand short-circuits to either GND or to the power supply V_S. The integrated overtemperature protection may disable the transmitter if a permanent short circuit on the BUS pin causes the TLE8457C / TLE8457D to overheat.

4.5 Overtemperature protection

The TLE8457C / TLE8457D has two independent overtemperature detectors for protecting the device against thermal overstress, namely on the voltage regulator pass element and on the LIN bus transmitter. In the case where the junction temperature at the LIN transmitter increases above the thermal shut-down level T_{JSD}, it will be disabled until the junction temperature of the transmitter cools down below $T_J < T_{JSD} - \Delta T$. No other effect, nor mode change, will occur. After the LIN transmitter overtemperature recovery, the TxD input requires a logic “high” signal before restarting data transmission.

If an overtemperature event is detected on the voltage regulator, it will be disabled and the NRST output will be set “low”. During the overtemperature condition no functionality of the TLE8457C / TLE8457D is available. After the junction temperature cools down below $T_J < T_{JSD} - \Delta T$, the voltage regulator is reactivated and NRST will be set “high” after delay time t_{RST}.

Note: The overtemperature detection of the LIN transmitter and the voltage regulator are working independently. Therefore either only the LIN transmitter or only the voltage regulator or both can be switched off, depending on the circumstance. An example of only LIN transmitter overtemperature could be bus short-circuit or severe electromagnetical injection.

5 General product characteristics

5.1 Absolute maximum ratings

Table 3 Absolute maximum ratings voltages, currents and temperatures[1)]

All voltages with respect to ground; positive current flowing into pin; unless otherwise specified

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltage							
Supply input voltage	V_S	-0.3	–	45	V	LIN Spec 2.2A (Par. 11)	P_5.1.1
Bus input voltage	V_{BUS}	-27	–	40	V	–	P_5.1.2
Logic voltages at EN and TxD	$V_{logic,in}$	-0.3	–	7.0	V	–	P_5.1.3
Logic voltages at RxD and NRST	$V_{logic,out}$	-0.3	–	V_{CC} + 0.3	V	–	P_5.1.4
Voltage regulator output	V_{CC}	-0.3	–	7.0	V	–	P_5.1.5
Currents							
Output current at RxD	I_{RxD}	-15	–	15	mA	–	P_5.1.6
Output current at NRST	I_{NRST}	–	–	10	mA	–	P_5.1.7
Temperature							
Junction temperature	T_j	-40	–	150	°C	–	P_5.1.8
Storage temperature	T_s	-55	–	150	°C	–	P_5.1.9
ESD susceptibility							
Electrostatic discharge voltage at V_S and BUS vs. GND	V_{ESD}	-8	–	8	kV	Human body model (100 pF via 1.5 kΩ)[2)]	P_5.1.10
Electrostatic discharge voltage all other pins	V_{ESD}	-2	–	2	kV	Human body model (100 pF via 1.5 kΩ)[2)]	P_5.1.11
Electrostatic discharge voltage corner pins	V_{ESD}	-750	–	750	V	Charged device model[3)]	P_5.1.12
Electrostatic discharge voltage at all other pins	V_{ESD}	-500	–	500	V	Charged device model[3)]	P_5.1.13

1) Not subject to production test, specified by design.
2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS-001 (1.5 kΩ, 100 pF).
3) ESD susceptibility, charged device model “CDM” EIA / JESD 22-C101 or ESDA STM5.3.1.

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as ‘outside’ normal operating range. Protection functions are not designed for continuous repetitive operation.*

5.2 Functional range

Table 4 Operating range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply voltage							
Supply voltage range for normal operation	$V_{S(nor)}$	5.5	–	28	V	LIN Spec 2.2A Param. 10	P_5.2.12
Extended Supply Voltage Range for Operation	$V_{S(ext)}$	3.0	–	40	V	Parameter deviations possible	P_5.2.22
Stability requirement on V_{CC}							
Output capacitor range	C_{VCC}	1.0	–	–	µF	1)3)	P_5.2.3
Output capacitor ESR	ESR(C_{VCC})	–	–	5.0	Ω	2)3)	P_5.2.4
Thermal parameter							
Junction temperature	T_j	-40	–	150	°C	3)	P_5.2.5

1) The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%.
2) Relevant ESR value at f = 10 kHz.
3) Not subject to production test, specified by design.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

5.3 Thermal characteristics

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, please visit **www.jedec.org**.*

Table 5 Thermal resistance[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Thermal resistance, PG-DSO-8 package version							
Junction to ambient	R_{thJA}	–	130	–	K/W	[2)]	P_5.3.1
Thermal resistance, PG-TSON-8 package version							
Junction to ambient	R_{thJA}	–	60	–	K/W	[2)]	P_5.3.2
Junction to ambient		–	190	–	K/W	Footprint only[3)]	P_5.3.5
Junction to ambient		–	70	–	K/W	300 mm^2 heatsink on PCB[3)]	P_5.3.6
Thermal shutdown junction temperature							
Thermal shutdown temperature	T_{JSD}	160	180	200	°C	T_{JSD} increasing	P_5.3.3
Thermal shutdown hysteresis	ΔT	–	10	–	K	T_{JSD} decreasing	P_5.3.4

1) Not subject to production test, specified by design.

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (IC+package) was simulated on a 76.2 × 114.3 × 1.5 mm^3 board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted to the first inner copper layer.

3) Specified R_{thJA} value is according to Jedec JESD51-3 at natural convection on FR4 1s0p board; The product (IC+package) was simulated on a 76.2 × 114.3 × 1.5 mm^3 board with 1 inner copper layer (1 × 70 µm Cu).

6 Electrical characteristics

6.1 Functional device characteristics

Table 6 Electrical characteristics

5.5 V < V_S < 28 V; R_{LIN} = 500 Ω; -40 °C < T_j < 150°C;
all voltages with respect to ground; positive current flowing into pin[1]; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current Consumption							
Current consumption at V_S, transmitter in recessive state	$I_{S,rec}$	0.1	0.3	0.7	mA	I_{CC} = 50 µA; without R_{LIN}; TxD = “high”; V_{BUS} = V_S; NRST=”high”	P_6.1.1
Current consumption at V_S, transmitter in dominate state	$I_{S,dom}$	0.1	1.0	3.0	mA	I_{CC} = 50 µA; without R_{LIN}; TxD = “low”; V_{BUS} = 0 V; NRST=”high”	P_6.1.2
Current consumption at V_S, dominate state	I_{S,dom_max}	70	71	73	mA	I_{CC} = 70 mA; without R_{LIN}; TxD = “low”; V_{BUS} = 0 V; NRST=”high”	P_6.1.3
Current consumption at V_S in standby mode $I_{S,standby} = I_S - I_{CC}$	$I_{S,standby}$	–	20	40	µA	Standby mode; I_{CC} = 50 µA; V_S = V_{BUS} = 13.5 V; NRST = TxD = “high”	P_6.1.4
Current consumption at V_S in sleep mode	$I_{S,Sleep}$	–	7	16	µA	Sleep mode; V_S = 13.5 V; V_{BUS} = V_S; V_{CC} = 0 V	P_6.1.5
Current consumption at V_S in sleep mode. BUS shorted to GND	I_{S,SC_GND}	250	–	800	µA	Sleep Mode; V_S = 13.5 V; V_{BUS} = 0 V; V_{CC} = 0 V	P_6.1.6
Power-up and power-down							
Power-on reset level, V_S on	$V_{S,PON}$	–	–	3.0	V	–	P_6.1.7
Undervoltage threshold, V_S on	$V_{S,UV,ON}$	4.7	5.15	5.5	V	Rising edge	P_6.1.8
Undervoltage threshold, V_S off	$V_{S,UV,OFF}$	4.4	4.85	5.2	V	Falling edge	P_6.1.9
Undervoltage hysteresis on V_S $V_{S,UV,hys} = V_{S,UV,ON} - V_{S,UV,OFF}$	$V_{S,UV,hys}$	200	300	–	mV	2)	P_6.1.10
Undervoltage blanking time	$t_{BLANK,UV}$	–	10	–	µs	2)	P_6.1.11
Enable input: EN							
“High” level input voltage	$V_{EN,ON}$	2	–	–	V	–	P_6.1.12
“Low” level input voltage	$V_{EN,OFF}$	–	–	0.8	V	–	P_6.1.13
Input hysteresis	$V_{EN,hys}$	50	200	–	mV	–	P_6.1.14
Pull-down resistance	R_{EN}	15	30	60	kΩ	–	P_6.1.15
Delay time for mode change, EN → “low”	$t_{MODE,LOW}$	10	–	50	µs	–	P_6.1.16

Table 6 Electrical characteristics (cont'd)

5.5 V < V_S < 28 V; R_{LIN} = 500 Ω; -40 °C < T_j < 150°C;
all voltages with respect to ground; positive current flowing into pin[1]; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Delay time for mode change, EN → "high"	$t_{MODE,HIGH}$	–	–	5	µs	[2]	P_6.1.17
Input capacitance	C_{i_EN}	–	5	–	pF	[2]	P_6.1.83
Reset Output: NRST							
"High" level leakage current	$I_{NRST,H}$	–	–	5	µA	[2]	P_6.1.19
"Low" level output voltage	V_{NRST}	–	–	0.4	V	I_{NRST} = 1.5 mA; V_{CC} > 1 V;	P_6.1.20
Reset time	t_{RST}	4	10	16	ms	–	P_6.1.21
Internal pull-up resistance	R_{NRST}	5	10	20	kΩ	–	P_6.1.22
Voltage regulator output, 5 V versions (TLE8457Cxx): V_{CC}							
Output voltage	V_{CC}	4.9	5.0	5.1	V	0.05 mA < I_{CC} < 70 mA; 5.8 V < V_S < 28 V	P_6.1.23
Output voltage drop $V_{DR} = V_S - V_{CC}$ [3]	V_{DR}	–	250	650	mV	I_{CC} < 70 mA	P_6.1.24
Output voltage drop, 50 mA $V_{DR} = V_S - V_{CC}$	$V_{DR,50}$	–	180	480	mV	I_{CC} < 50 mA	P_6.1.25
Output voltage drop, 20 mA $V_{DR} = V_S - V_{CC}$	$V_{DR,20}$	–	80	200	mV	I_{CC} < 20 mA	P_6.1.26
Output current limitation	$I_{CC,lim}$	-150	–	-70	mA	0 V < V_{CC} < 4.8 V	P_6.1.27
Load regulation	$\Delta V_{CC,lo}$	–	25	50	mV	0.05 mA < I_{CC} < 70 mA; V_S = 13.5 V	P_6.1.28
Line regulation	$\Delta V_{CC,li}$	–	25	50	mV	I_{CC} = 1 mA; 5.8 V < V_S < 28 V	P_6.1.29
Power supply ripple rejection	PSRR	50	60	–	dB	[2] I_{CC} = 50 mA; f = 100 Hz; V_r = 0.5 V_{pp}; V_S = 13.5 V	P_6.1.30
Undervoltage reset threshold	$V_{CC,UV}$	4.27	4.4	4.5	V	V_{CC} decreasing	P_6.1.31
Undervoltage reset hysteresis	$V_{CC,UV,hy}$	50	100	–	mV	–	P_6.1.32
Undervoltage detection time	$t_{det,RST}$	1	–	20	µs	[2] V_{CC} = 3.5 V C_{NRST} = 20 pF	P_6.1.33
Voltage regulator output, 3.3 V versions (TLE8457Dxx): V_{CC}							
Output voltage	V_{CC}	3.234	3.300	3.366	V	0.05 mA < I_{CC} < 70 mA; 4.066 V < V_S < 28 V	P_6.1.34
Output voltage drop $V_{DR} = V_S - V_{CC}$	V_{DR}	–	380	770	mV	I_{CC} < 70 mA	P_6.1.35
Output voltage drop, 50 mA $V_{DR} = V_S - V_{CC}$	$V_{DR,50}$	–	280	550	mV	I_{CC} < 50 mA	P_6.1.36
Output voltage drop, 20 mA $V_{DR} = V_S - V_{CC}$	$V_{DR,20}$	–	110	220	mV	I_{CC} < 20 mA	P_6.1.37

Table 6 Electrical characteristics (cont'd)

5.5 V < V_S < 28 V; R_{LIN} = 500 Ω; -40 °C < T_j < 150°C;
all voltages with respect to ground; positive current flowing into pin[1]; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output current limitation	$I_{CC,lim}$	-150	–	-70	mA	0 V < V_{CC} < 3.1 V	P_6.1.38
Load regulation	$\Delta V_{CC,lo}$	–	25	50	mV	0.05 mA < I_{CC} < 70 mA; V_S = 13.5 V	P_6.1.39
Line regulation	$\Delta V_{CC,li}$	–	25	50	mV	I_{CC} = 1 mA; 4.066 V < V_S < 28 V	P_6.1.40
Power supply ripple rejection	PSRR	50	60	–	dB	[2] I_{CC} = 50 mA; f = 100 Hz; V_r = 0.5 V_{pp}; V_S = 13.5 V	P_6.1.41
Undervoltage reset threshold	$V_{CC,UV}$	2.82	2.90	2.96	V	V_{CC} decreasing	P_6.1.42
Undervoltage reset hysteresis	$V_{CC,UV,hy}$	33	66	–	mV	–	P_6.1.43
Undervoltage detection time	$t_{det,RST}$	1	–	20	µs	[2] V_{CC} = 2.31 V C_{NRST} = 20 pF	P_6.1.44
Receiver output: RxD							
"High" level output voltage	$V_{RxD,H}$	0.8 × V_{CC}	–	–	V	I_{RxD} = -2 mA; V_{BUS} = V_S	P_6.1.45
"Low" level output voltage	$V_{RxD,L}$	–	–	0.2 × V_{CC}	V	I_{RxD} = 2 mA; V_{BUS} = 0 V	P_6.1.46
Transmission input: TxD							
"High" level input voltage range	$V_{TxD,H}$	0.7 × V_{CC}	–	–	V	Recessive state	P_6.1.47
"Low" level input voltage range	$V_{TxD,L}$	–	–	0.3 × V_{CC}	V	Dominant state	P_6.1.48
Input hysteresis	$V_{TxD,hys}$	200	–	–	mV	–	P_6.1.49
Pull-up resistance	R_{TxD}	15	30	60	kΩ	–	P_6.1.50
TxD time-out	t_{TxD}	8	18	28	ms	–	P_6.1.51
TxD recessive release time	$t_{to,rec}$	–	–	10	µs	[2]	P_6.1.52
Input capacitance	C_{i_TxD}	–	5	–	pF	[2]	P_6.1.93
BUS receiver: BUS							
Receiver threshold voltage, recessive to dominant edge	V_{th_dom}	0.4 × V_S	0.44 × V_S	–	V	V_S < 18 V;	P_6.1.53
Receiver dominant state	V_{BUSdom}	-27	–	0.4 × V_S	V	LIN Spec 2.2A (Par. 17)[4]	P_6.1.54
Receiver threshold voltage, dominant to recessive edge	V_{th_rec}	–	0.56 × V_S	0.6 × V_S	V	V_S < 18 V;	P_6.1.55
Receiver recessive state	V_{BUSrec}	0.6 × V_S	–	40	V	LIN Spec 2.2A (Par. 18)[5]	P_6.1.56
Receiver center voltage	V_{BUS_CNT}	0.475 × V_S	0.5 × V_S	0.525 × V_S	V	LIN Spec 2.2A (Par. 19)[6] V_S < 18V;	P_6.1.57

Table 6 Electrical characteristics (cont'd)

5.5 V < V_S < 28 V; R_{LIN} = 500 Ω; -40 °C < T_j < 150°C;
all voltages with respect to ground; positive current flowing into pin[1]; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Receiver hysteresis	V_{HYS}	0.07 × V_S	0.12 × V_S	0.175 × V_S	V	LIN Spec 2.2A (Par. 20)[7] V_S < 18 V;	P_6.1.58
Wake-up threshold voltage	$V_{BUS,wk}$	0.4 × V_S	0.5 × V_S	0.6 × V_S	V	–	P_6.1.59
BUS transmitter: BUS							
BUS recessive output voltage	$V_{BUS,ro}$	0.8 × V_S	–	V_S	V	TxD = "high"; Open load	P_6.1.60
BUS short-circuit current	I_{BUS_LIM}	40	85	125	mA	V_{BUS} = 18 V; LIN Spec 2.2A (Par. 12);	P_6.1.61
Leakage current	$I_{BUS\_NO\_GND}$	-1	-0.5	–	mA	V_S = 0 V; V_{BUS} = -12 V; LIN Spec 2.2A (Par. 15)	P_6.1.62
Leakage current	$I_{BUS\_NO\_BAT}$	–	1	5	µA	V_S = 0 V; V_{BUS} = 18 V; LIN Spec 2.2A (Par. 16)	P_6.1.63
Leakage current	$I_{BUS\_PAS\_dom}$	-1	-0.5	–	mA	V_S = 18 V; V_{BUS} = 0 V; LIN Spec 2.2A (Par. 13)	P_6.1.64
Leakage current	$I_{BUS\_PAS\_rec}$	–	1	5	µA	V_S = 8 V; V_{BUS} = 18 V; Driver stage "off"; TxD = "high"; LIN Spec 2.2A (Par. 14)	P_6.1.65
Forward voltage serial diode	$V_{SerDiode}$	0.4	–	1.0	V	$I_{SerDiode}$ = - 75 µA LIN Spec 2.2A (Par.21)	P_6.1.66
BUS pull-up resistance	R_{slave}	20	40	60	kΩ	LIN Spec 2.2A (Par. 26)	P_6.1.67
BUS dominant output voltage maximum load	$V_{BUS,do}$	–	–	1.4	V	V_{TxD} = 0 V; R_{LIN} = 500 Ω; V_S = 5.5 V;	P_6.1.68
BUS dominant output voltage maximum load	$V_{BUS,do}$	–	–	2.0	V	V_{TxD} = 0 V; R_{LIN} = 500 Ω; V_S = 18 V;	P_6.1.98
Input capacitance	C_{i_BUS}		–	30	pF	[2]	P_6.1.95
Dynamic transceiver characteristics: BUS							
Dominant time for bus wake-up	$t_{WK,bus}$	30	–	150	µs	–	P_6.1.69
Propagation delay: LIN bus dominant to RxD "low"	t_{rx_pdft}	1	3.5	6	µs	LIN Spec 2.2A (Par. 31) C_{RxD} = 20 pF	P_6.1.70
LIN bus recessive to RxD "high"	t_{rx_pdr}	1	3.5	6	µs		
Receiver delay symmetry	t_{rx_sym}	-2	–	2	µs	LIN Spec 2.2A (Par. 32) t_{rx_sym} = t_{rx_pdf} - t_{rx_pdr}; C_{RxD} = 20 pF	P_6.1.71

Table 6 Electrical characteristics (cont'd)

5.5 V < V_S < 28 V; R_{LIN} = 500 Ω; -40 °C < T_j < 150°C;
all voltages with respect to ground; positive current flowing into pin[1]; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Duty cycle D1 (for worst case at 20 kBit/s) D1 = $t_{bus\_rec(min)}$ / 2 × t_{bit}	*D1*	0.396	–	–		Duty cycle 1 [8] $TH_{Rec(max)}$ = 0.744 × V_S; $TH_{Dom(max)}$ = 0.581 × V_S; V_S = 7.0 … 18 V; t_{bit} = 50 µs; LIN Spec 2.2A (Par. 27)	P_6.1.72
Duty cycle D1 V_S supply 5.5 V to 7.0 V (for worst case at 20 kBit/s) D1 = $t_{bus\_rec(min)}$ / 2 × t_{bit}	*D1*	0.396	–	–		Duty cycle 1 [8] $TH_{Rec(max)}$ = 0.760 × V_S; $TH_{Dom(max)}$ = 0.593 × V_S; 5.5 V < V_S < 7.0 V; t_{bit} = 50 µs	P_6.1.73
Duty cycle D2 (for worst case at 20 kBit/s) D2 = $t_{bus\_rec(max)}$ / 2 × t_{bit}	*D2*	–	–	0.581		Duty cycle 2 [8] $TH_{Rec(min)}$ = 0.422 × V_S; $TH_{Dom(min)}$ = 0.284 × V_S; V_S = 7.6 … 18 V; t_{bit} = 50 µs; LIN Spec 2.2A (Par. 28)	P_6.1.74
Duty cycle D2 V_S supply 6.1 V to 7.6 V (for worst case at 20 kBit/s) D2 = $t_{bus\_rec(max)}$ / 2 × t_{bit}	*D2*	–	–	0.581		Duty cycle 2 [8] $TH_{Rec(min)}$ = 0.41 × V_S; $TH_{Dom(min)}$ = 0.275 × V_S; 6.1 V < V_S < 7.6 V; t_{bit} = 50 µs;	P_6.1.75
Duty cycle D3 V_S supply 7.0 V to 18.0 V (for worst case at 10.4 kBit/s) D3 = $t_{bus\_rec(min)}$ / 2 × t_{bit}	*D3*	0.417	–	–		Duty cycle 3 [8] $TH_{Rec(max)}$ = 0.778 × V_S; $TH_{Dom(max)}$ = 0.616 × V_S; V_S = 7.0 … 18 V; t_{bit} = 96 µs; LIN Spec 2.2A (Par. 29)	P_6.1.76
Duty cycle D3 V_S supply 5.5 V to 7.0 V (for worst case at 10.4 kBit/s) D3 = $t_{bus\_rec(min)}$ / 2 × t_{bit}	*D3*	0.417	–	–		Duty cycle 3 [8] $TH_{Rec(max)}$ = 0.797 × V_S; $TH_{Dom(max)}$ = 0.630 × V_S; 5.5 V < V_S < 7.0 V; t_{bit} = 96 µs;	P_6.1.77

Table 6 Electrical characteristics (cont'd)

5.5 V < V_S < 28 V; R_{LIN} = 500 Ω; -40 °C < T_j < 150°C;
all voltages with respect to ground; positive current flowing into pin[1]; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Duty cycle D4 V_S supply 7.6 V to 18.0 V (for worst case at 10.4 kBit/s) D4 = $t_{bus\_rec(max)}$ / 2 × t_{bit}	*D4*	–	–	0.590		Duty cycle 4 [8] $TH_{Rec(min)}$ = 0.389 × V_S; $TH_{Dom(min)}$ = 0.251 × V_S; V_S = 7.6 … 18 V; t_{bit} = 96 µs; LIN Spec 2.2A (Par. 30)	P_6.1.78
Duty cycle D4 V_S supply 6.1 V to 7.6 V (for worst case at 10.4 kBit/s) D4 = $t_{bus\_rec(max)}$ / 2 × t_{bit}	*D4*	–	–	0.590		Duty cycle 4 [8] $TH_{Rec(min)}$ = 0.378 × V_S; $TH_{Dom(min)}$ = 0.242 × V_S; 6.1 V < V_S < 7.6 V; t_{bit} = 96 µs;	P_6.1.79

1) Load current on V_{CC} specified positive direction out of pin.
2) Not subject to production test, specified by design.
3) Measured when the output voltage V_{CC} has dropped 100 mV from the nominal value obtained at V_S = 13.5 V.
4) Minimum limit specified by design.
5) Maximum limit specified by design.
6) $V_{BUS\_CNT} = (V_{th\_dom} + V_{th\ rec}) / 2$.
7) $V_{HYS} = V_{th\_rec} - V_{th\_dom}$.
8) BUS load according to LIN Spec 2.2A:
   Load 1 = 1 nF / 1 kΩ = C_{BUS} / R_{LIN}
   Load 2 = 6.8 nF / 660 Ω = C_{BUS} / R_{LIN}
   Load 3 = 10 nF / 500 Ω = C_{BUS} / R_{LIN}

6.2 Diagrams

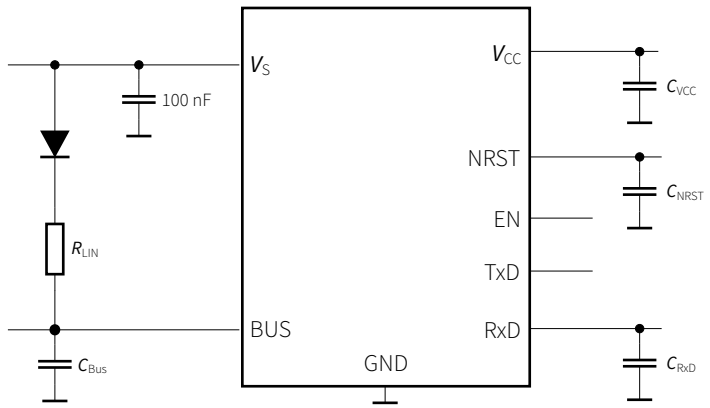

Figure 14 Simplified test circuit for dynamic transceiver characteristics

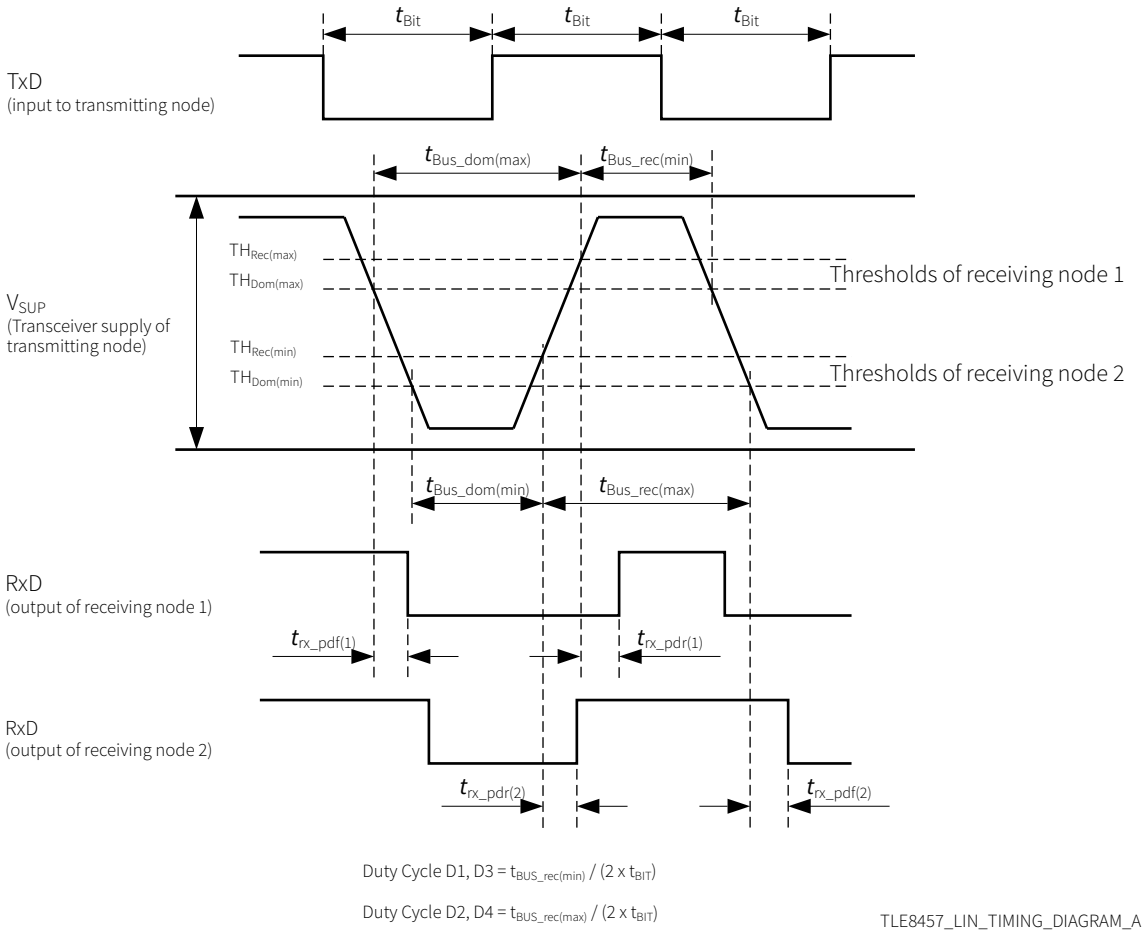

Figure 15 Timing diagram for dynamic transceiver characteristics

7 Application information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

7.1 Application example

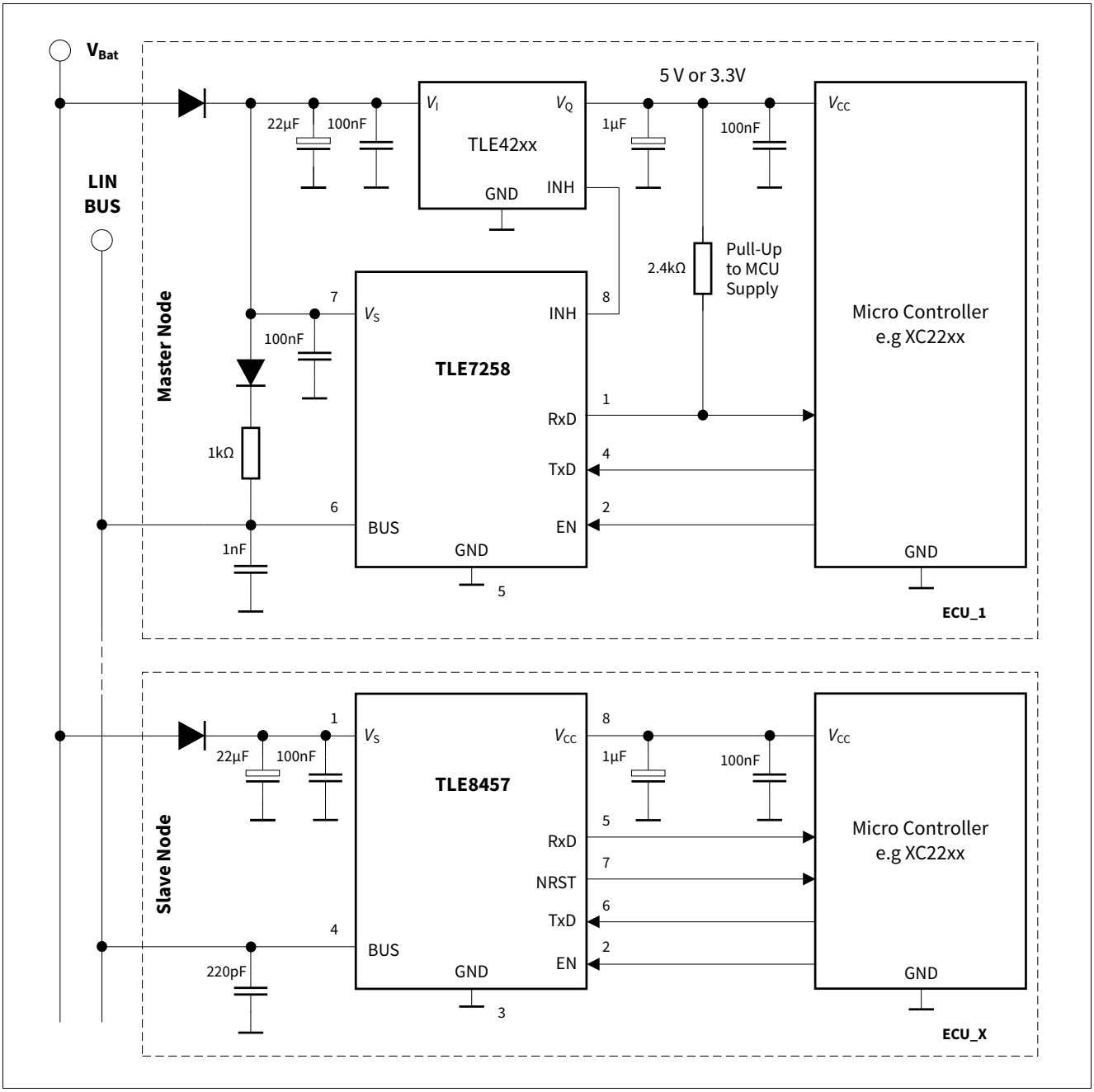

Figure 16 Simplified application circuit

7.2 ESD robustness according to IEC61000-4-2

Test for ESD robustness according to IEC61000-4-2 (150 pF, 330 Ω) have been performed. The results and test conditions are available in a separate test report.

Table 7 ESD robustness according to IEC61000-4-2

Performed Test	Results	Unit	Remarks
Electrostatic discharge voltage at pin V_S, BUS versus GND	+8	kV	[1)]Positive pulse
Electrostatic discharge voltage at pin V_S, BUS versus GND	-8	kV	[1)]Negative pulse

1) ESD susceptibility according LIN EMC 1.3 Test Specification, Section 4.3. (IEC 61000-4-2) - Tested by external test house.

7.3 Transient robustness according to ISO 7637-2

Test for transient robustness according to ISO 7637-2 have been performed. The results and test conditions are available in a separate test report.

Table 8 Automotive transient robustness according to ISO 7637-2

Performed Test	Results	Unit
Pulse 1	-100	V
Pulse 2	+75	V
Pulse 3a	-150	V
Pulse 3b	+100	V

7.4 LIN physical layer compatibility

As the LIN physical layer is independent from higher LIN layers (for example LIN protocol layer), all nodes with a LIN physical layer corresponding to this revision can be mixed with LIN physical layer nodes, which are according to older revisions (LIN 1.0, LIN 1.1, LIN 1.2, LIN 1.3, LIN 2.0, LIN 2.1 and LIN 2.2), without any restrictions.

8 Package information

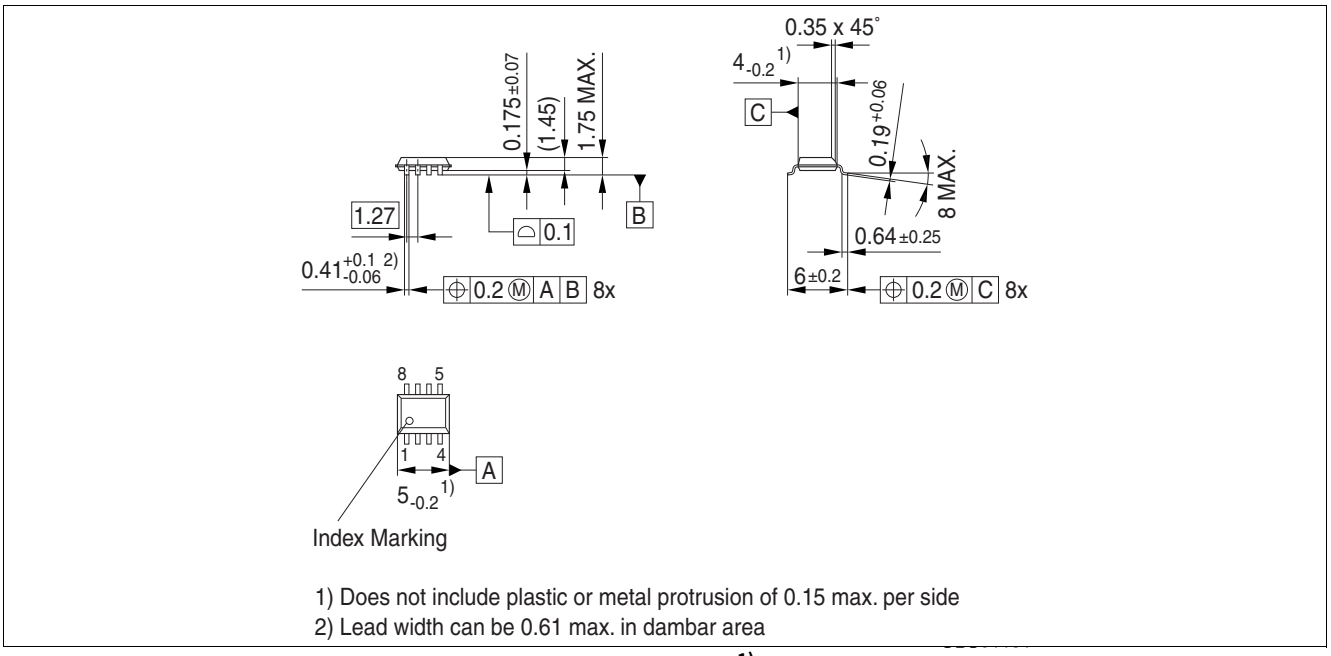

Figure 17 PG-DSO-8 (Plastic dual small outline PG-DSO-8)[1)]

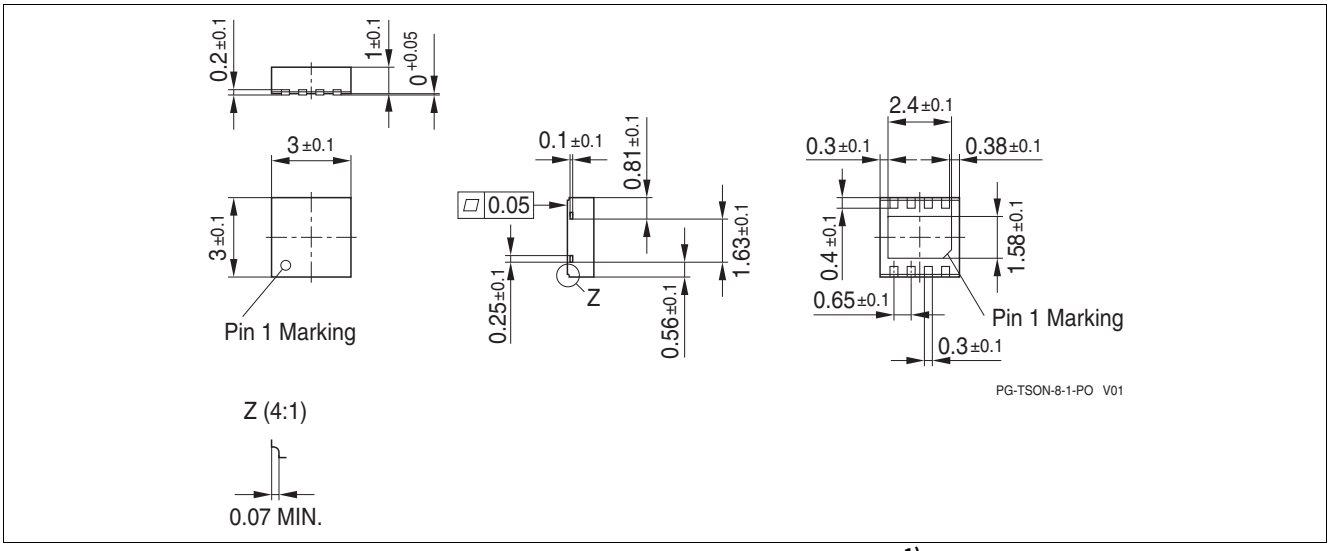

Figure 18 PG-TSON-8 (Plastic thin small outline nonleaded PG-TSON-8)[1)]

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

1) Dimensions in mm

9 Revision history

Revision	Date	Changes
1.1	2018-10-15	Data Sheet updated: • Updated to new layout style • Editorial changes
1.0	2018-01-22	Data Sheet created

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