CS53L30

Ultra Low Power, 4-Channel Microphone A/D Converter With TDM Interface

Product Overview

The CS53L30 is an ultra low power, high performance, quad-channel A/D converter designed to enable enhanced voice processing features in smartphones, tablets and other consumer electronics applications. With a small form factor and consuming less than 2.5 mW of power per channel, the CS53L30 enhances voice processing features such as noise suppression, acoustic echo cancellation and multi-channel beamforming, and offers improved performance in voice capture processing involving voice control and recognition.

The CS53L30 integrates a flexible input front end that can accommodate a combination of digital microphone, analog microphone and line inputs in fully differential, pseudo-differential and single-ended configurations. The analog microphone input path includes a +10 or +20 dB boost and a –6 to +12 dB programmable gain amplifier (PGA), as well as a dedicated mic-bias generator for each of the four microphone channels for improved channel-to-channel separation which enhances the performance of beamforming algorithms. Digital signal processing features like high-pass filters, noise gates and volume controls provide further pre-conditioning, which are essential to improve voice-processing performance.

A single CS53L30 can output its four channels of audio data up to 48 kHz sample rate over two I²S ports or a single TDM port. For applications that require additional mic inputs, up to four CS53L30s can be used together to output up to 16 channels of data over a single TDM line for seamless system integration. The CS53L30 has a multi-device synchronization protocol to align all audio channels and minimize interchannel phase mismatch.

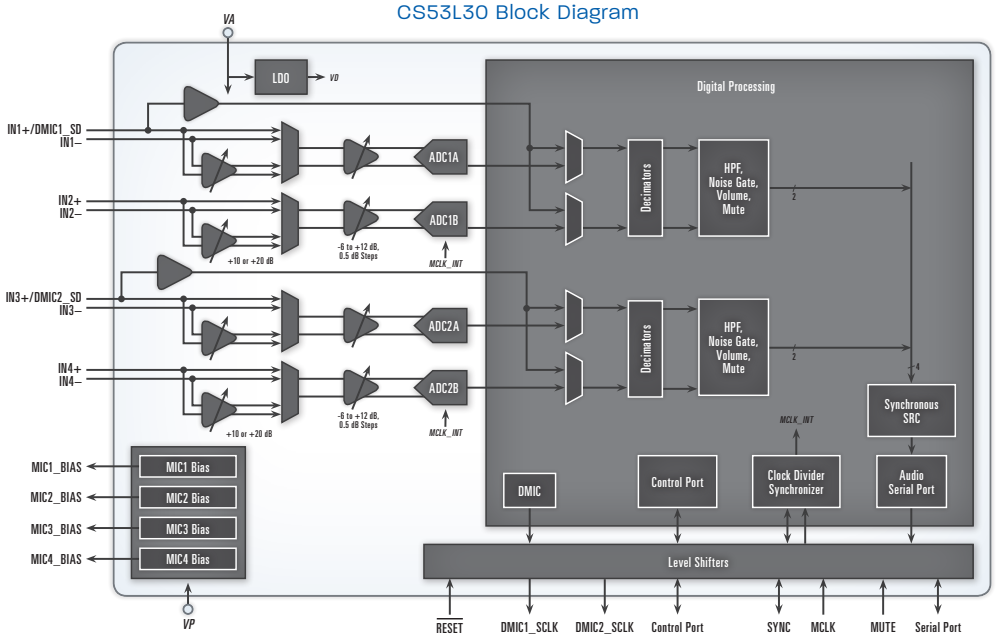
The CS53L30 can operate as a serial port clock master or slave. In master mode, clock dividers are used to generate the internal master clock and audio clocks from either the 6/12 MHz, 6.144/12.288 MHz, 5.6448/11.2896 MHz, or 19.2 MHz master clock.

The CS53L30 can be controlled through a high speed I²C™ control port and is powered by a 1.8 V nominal analog supply and a typical 3.6 V battery supply. The CS35L30 is available in a 30-ball, 0.4 mm pitch WLCSP package and a 32-pin, 5 X 5-mm QFN package.

Target Applications

The CS53L30 is ideally suited for mic-array type systems such as voice-recognition, advanced headsets, mobile computing devices, voice recorders, digital video cameras and smart TV and set-top-boxes.

CS53L30 Block Diagram



Features/Benefits

- Ultra low power consumption
  - <2.5 mW mono analog mic record at 8 kHz
  - <4.5 mW stereo analog mic record at 16 kHz
- High analog performance
  - 91 dB A-weighted dynamic range at 0 dB gain
  - –84 dB THD+N at 0 dB gain
  - Dedicated mic-bias generator for each of the four input channels
- Flexible analog input front end
  - Supports up to four line/mic inputs in fully differential, pseudo-differential and single-ended configuration
  - Four analog programmable gain amplifiers
    - –6 to +12 dB, in 0.5-dB steps
    - +10 or +20 dB boost for mic input
- Digital microphone (DMIC) interface
  - Supports up to four DMIC channels
  - Two DMIC SCLK generators
- Serial port interface
  - Two I^2S output ports or single TDM output port
  - Up to four CS53L30s can be used together to output up to 16 channels of data over a single TDM line
  - Multi-device synchronization protocol ensures minimal interchannel phase mismatch
- Digital signal processing
  - Volume control, mute, programmable high-pass filter and noise gate
- Flexible clocking
  - Native support for both audio and USB clocks with no PLL required
  - Master or slave mode
- Mute pin for quick mic mute and programmable quick power down
- High speed 400 kHz I^2C™ control port
- 30-ball WLCSP or 32-pin QFN package

CDB53L30 Evaluation Board

The CDB53L30 evaluation board is a convenient platform for evaluating the CS53L30 low-power, quad-channel microphone ADC with TDM output. It supports multiple power supply and signal I/O configurations, including the option to connect directly to the CS53L30 from an external system such as a host processor (while bypassing the onboard control circuitry). The CDB53L30 has two CS53L30 devices, providing the ability to evaluate the multichip synchronization protocol. To evaluate the synchronization protocol using four devices, two CDB53L30s can be linked using the SYNC I/O header. The CDB53L30 also serves as the component and layout reference for the CS53L30

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