40ns、微功耗、推挽输出比较器

特性

- 低传播延迟：**40ns**
- 低静态电流
  每通道 **40μA**
- 输入共模扩展范围扩展到任一电源轨之上 **200mV**
- 低输入偏移电压：**1mV**
- 输出电源范**+2.7V** 至 **+5.5V**
- 温度范围： **-40°C** 至 **+125°C**

应用范围

- 检测设备
- 测试和测量
- 高速采样系统
- 电信
- 便携式通信

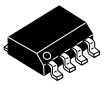
说明

HT3201 和 HT3202 是单通道和双通道比较器，此比较器能够在极小型封装内提供高速 (40ns) 和低功耗 (40μA) 的最终组合，此封装具有诸如轨到轨输入、低偏移电压 (1mV)、和高输出驱动电流等特性。 在对响应时间要求严格的多种应用中也可轻松执行此器件。 HT320x 系列产品可提供单通道 (HT3201) 和双通道 (HT3202) 版本，这两个版本的器件都带有推挽输出。 HT3201 采用 SOT23-5 封装。 HT3202 采用 SOIC-8 和 MSOP-8 封装。 所有器件可在扩展的工业温度范围，即 -40°C 至 +125°C，内运行。

订购信息

SOT23-5 T SUFFIX
HT3201ARTZ

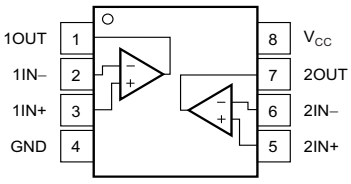
MSOP8 M SUFFIX
HT3202ARMZ



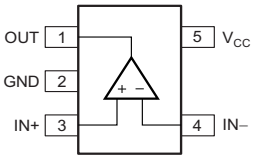
SOP−8 R SUFFIX
HT3202ARZ

T_A = -40° to 125°C for all packages.

SOIC-8 AND MSOP-8
(TOP VIEW)



SC70-5 AND SOT23-5
(TOP VIEW)



ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		VALUE	UNIT
Supply voltage		7	V
Signal input terminals	Voltage(2)	–0.5 to (V_{CC}) + 0.5	V
	Current(2)	±10	mA
Output short circuit(3)		100	mA
Operating temperature range		–55 to +125	°C
Storage temperature range, T_{stg}		–65 to +150	°C
Junction temperature, T_J		+150	°C
Electrostatic discharge (ESD) ratings HT3201	Human body model (HBM)	2000	V
Electrostatic discharge (ESD) ratings HT3202	Human body model (HBM)	1000	V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal.
(3) Short-circuit to ground.

ELECTRICAL CHARACTERISTICS: V_{CC} = 5.0 V

At T_A = +25°C and V_{CC} = 5.0 V, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{IO}	Input offset voltage		$V_{CM} = V_{CC} / 2$		1	5	mV
			T_A = –40°C to +125°C			6	mV
dV_{OS}/dT	Input offset voltage drift		T_A = –40°C to +125°C		1	10	µV/°C
PSRR	Power-supply rejection ratio		$V_{CM} = V_{CC} / 2$, V_{CC} = 2.5 V to 5.5 V	65	85		dB
	Input hysteresis				1.2		mV
INPUT BIAS CURRENT							
I_{IB}	Input bias current		$V_{CM} = V_{CC} / 2$		1	50	pA
			T_A = –40°C to +125°C			5	nA
I_{IO}	Input offset current		$V_{CM} = V_{CC} / 2$		1	50	pA
			T_A = –40°C to +125°C			2.5	nA
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range		T_A = –40°C to +125°C	(V_{EE}) – 0.2		(V_{CC}) + 0.2	V
CMRR	Common-mode rejection ratio		–0.2 V < V_{CM} < 5.2 V	60	70		dB
INPUT IMPEDANCE							
	Common-mode				10^{13} || 2		Ω || pF
	Differential				10^{13} || 4		Ω || pF
SWITCHING CHARACTERISTICS							
t_{pd}	Propagation delay time	Low to high	Input overdrive = 20 mV, C_L = 15 pF		47	50	ns
			Input overdrive = 100 mV, C_L = 15 pF		43	50	ns
			T_A = –40°C to +125°C			55	ns
		High to low	Input overdrive = 20 mV, C_L = 15 pF		45	50	ns
			Input overdrive = 100 mV, C_L = 15 pF		42	50	ns
			T_A = –40°C to +125°C			55	ns
	Propagation delay skew		Input overdrive = 20mV, C_L = 15 pF		2		ns
	Propagation delay matching (HT3202)	High to low, Low to High	Input overdrive = 20 mV, C_L = 15 pF			5	ns
t_r	Rise time		10% to 90%		2.9		ns
t_f	Fall time		10% to 90%		3.7		ns
OUTPUT							
V_{OL}	Voltage output swing	From lower rail	I_{SINK} = 4 mA		175	190	mV
			T_A = –40°C to +125°C			225	mV
V_{OH}		From upper rail	I_{SOURCE} = 4 mA		120	140	mV
			T_A = –40°C to +125°C			170	mV
I_{SC}	Short-circuit current (per comparator)		I_{SC} sinking	40	48		mA
			T_A = –40°C to +125°C		See Typical Curve		mA
			I_{SC} sourcing	52	60		mA
			T_A = –40°C to +125°C		See Typical Curve		mA
POWER SUPPLY							
V_{CC}	Specified voltage			2.7		5.5	V
I_Q	Quiescent current				40	50	µA
			T_A = –40°C to +125°C			65	µA
TEMPERATURE							
	Specified range			–40		+125	°C
	Storage range			–65		+150	°C

ELECTRICAL CHARACTERISTICS: V_{CC} = 2.7 V

At T_A = +25°C and V_{CC} = 2.7 V, unless otherwise noted.

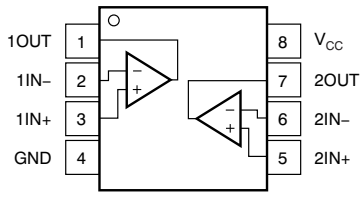
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{IO}	Input offset voltage		V_{CM} = V_{CC} / 2		1	5	mV
			T_A = –40°C to +125°C			6	mV
dV_{OS}/dT	Input offset voltage drift		T_A = –40°C to +125°C		1	10	µV/°C
PSRR	Power-supply rejection ratio		V_{CM} = V_{CC} / 2, V_{CC} = 2.5 V to 5.5 V	65	85		dB
	Input hysteresis				1.2		mV
INPUT BIAS CURRENT							
I_{IB}	Input bias current		V_{CM} = V_{CC} / 2		1	50	pA
			T_A = –40°C to +125°C			5	nA
I_{IO}	Input offset current		V_{CM} = V_{CC} / 2		1	50	pA
			T_A = –40°C to +125°C			2.5	nA
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range		T_A = –40°C to +125°C	(V_{EE}) – 0.2		(V_{CC}) + 0.2	V
CMRR	Common-mode rejection ratio		–0.2 V < V_{CM} < 2.9 V	56	68		dB
INPUT IMPEDANCE							
	Common-mode				10^{13} || 2		Ω || pF
	Differential				10^{13} || 4		Ω || pF
SWITCHING CHARACTERISTICS							
t_{pd}	Propagation delay time	Low to high	Input overdrive = 20 mV, C_L = 15 pF		47	50	ns
			Input overdrive = 100 mV, C_L = 15 pF		42	50	ns
			T_A = –40°C to +125°C			55	ns
		High to low	Input overdrive = 20 mV, C_L = 15 pF		40	50	ns
			Input overdrive = 100 mV, C_L = 15 pF		38	50	ns
			T_A = –40°C to +125°C			55	ns
	Propagation delay skew		Input overdrive = 20mV, C_L = 15 pF		2		ns
	Propagation delay matching (HT3202)	High to low, Low to High	Input overdrive = 20 mV, C_L = 15 pF			5	ns
t_r	Rise time		10% to 90%		4.8		ns
t_f	Fall time		10% to 90%		5.2		ns
OUTPUT							
V_{OL}	Voltage output swing	From lower rail	I_{SINK} = 4 mA		230	260	mV
			T_A = –40°C to +125°C			325	mV
V_{OH}		From upper rail	I_{SOURCE} = 4 mA		210	250	mV
			T_A = –40°C to +125°C			350	mV
I_{SC}	Short-circuit current (per comparator)		I_{SC} sinking	13	19		mA
			T_A = –40°C to +125°C		See Typical Curve		mA
			I_{SC} sourcing	15	21		mA
			T_A = –40°C to +125°C		See Typical Curve		mA
POWER SUPPLY							
V_{CC}	Specified voltage			2.7		5.5	V
I_Q	Quiescent current				36	46	µA
			T_A = –40°C to +125°C			60	µA
TEMPERATURE							
	Specified range			–40		+125	°C
	Storage range			–65		+150	°C

THERMAL INFORMATION

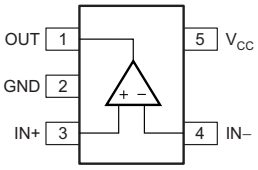
THERMAL METRIC(1)		HT3201		HT3202		UNITS
		DBV (SOT23)	DCK (SC70)	D (SOIC)	DGK (MSOP)	
		5 PINS	5 PINS	8 PINS	8 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	237.8	281.9	146.3	201.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	108.7	97.6	97.2	92.5	
θ_{JB}	Junction-to-board thermal resistance	64.1	68.3	84.2	123.3	
ψ_{JT}	Junction-to-top characterization parameter	12.1	2.6	45.5	23.0	
ψ_{JB}	Junction-to-board characterization parameter	63.3	67.3	83.7	121.6	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	

PIN CONFIGURATIONS

D AND DGK PACKAGES
SOIC-8 AND MSOP-8
(TOP VIEW)



DCK AND DBV PACKAGES
SC70-5 AND SOT23-5
(TOP VIEW)



PIN DESCRIPTIONS: D, DGK

NAME	NO.	DESCRIPTION
1IN–	2	Negative input, comparator 1
1IN+	3	Positive input, comparator 1
1OUT	1	Output, comparator 1
2IN–	6	Negative input, comparator 2
2IN+	5	Positive input, comparator 2
2OUT	7	Output, comparator 2
GND	4	Negative supply, ground
V_{CC}	8	Positive supply

PIN DESCRIPTIONS: DCK, DBV

NAME	NO.	DESCRIPTION
OUT	1	Output
GND	2	Negative supply, ground
IN+	3	Positive input
V_{CC}	5	Positive supply
IN–	4	Negative input

TYPICAL CHARACTERISTICS

At T_A = +25°C, V_{CC} = +5 V, and input overdrive (V_{OD}) = 20 mV, unless otherwise noted.

OFFSET VOLTAGE DISTRIBUTION

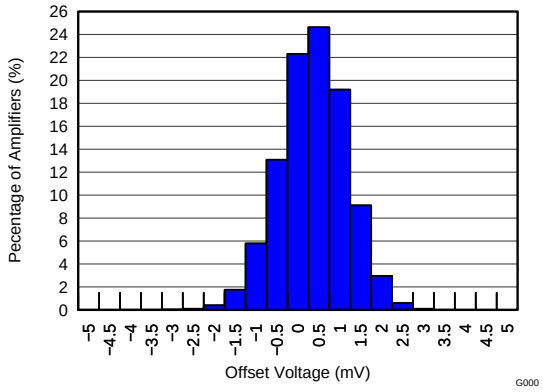


Figure 1.

HYSTERESIS DISTRIBUTION

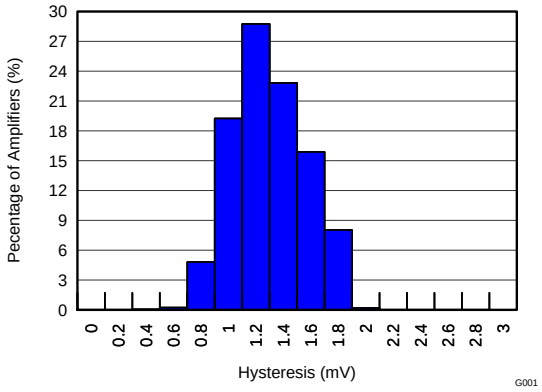


Figure 2.

OFFSET VOLTAGE vs TEMPERATURE

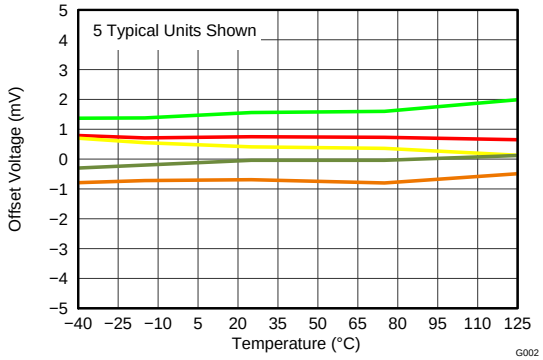


Figure 3.

OFFSET VOLTAGE vs COMMON-MODE VOLTAGE

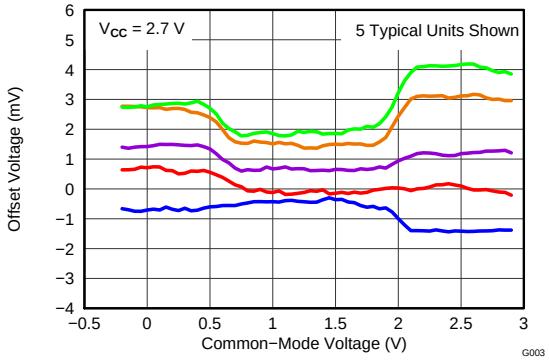


Figure 4.

OFFSET VOLTAGE vs COMMON-MODE VOLTAGE

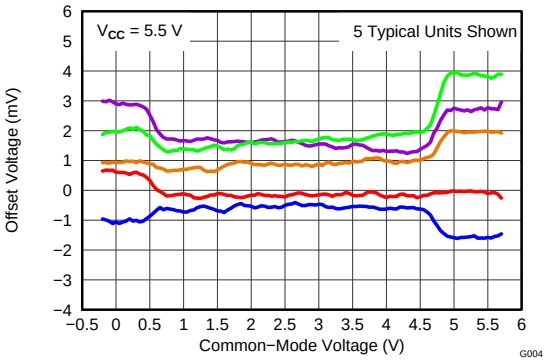


Figure 5.

OFFSET VOLTAGE vs POWER SUPPLY

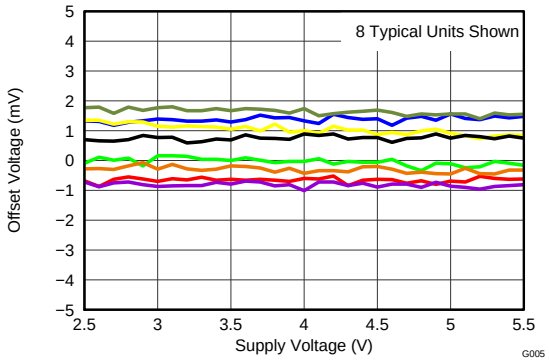


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{CC} = +5 V, and input overdrive (V_{OD}) = 20 mV, unless otherwise noted.

COMMON-MODE REJECTION RATIO AND POWER-SUPPLY REJECTION RATIO vs TEMPERATURE

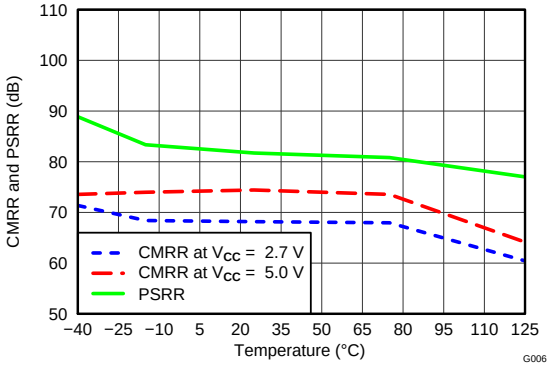


Figure 7.

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs TEMPERATURE

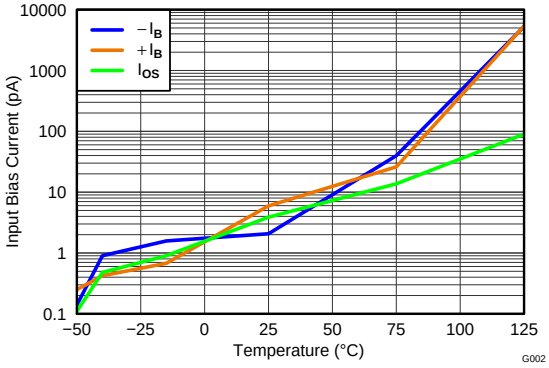


Figure 8.

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs COMMON-MODE INPUT VOLTAGE

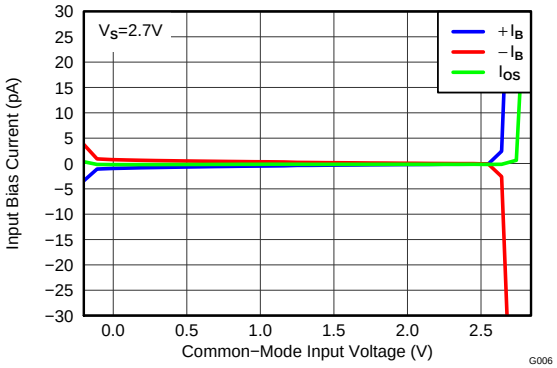


Figure 9.

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs COMMON-MODE INPUT VOLTAGE

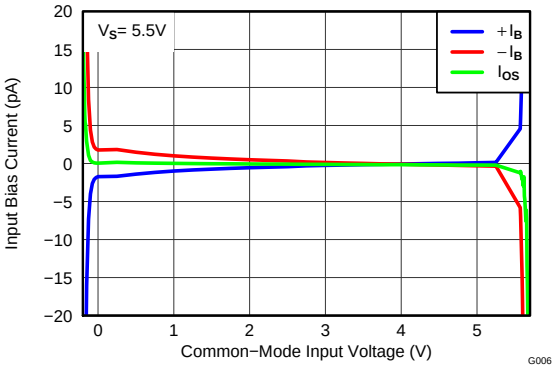


Figure 10.

QUIESCENT CURRENT DISTRIBUTION

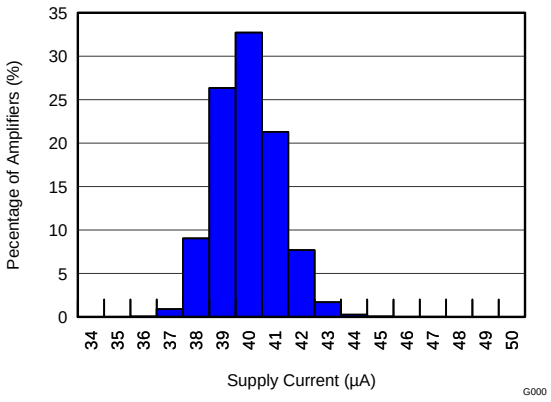


Figure 11.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

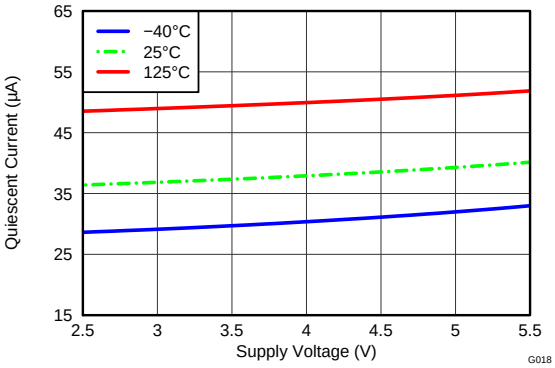


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{CC} = +5 V, and input overdrive (V_{OD}) = 20 mV, unless otherwise noted.

QUIESCENT CURRENT vs SWITCHING FREQUENCY

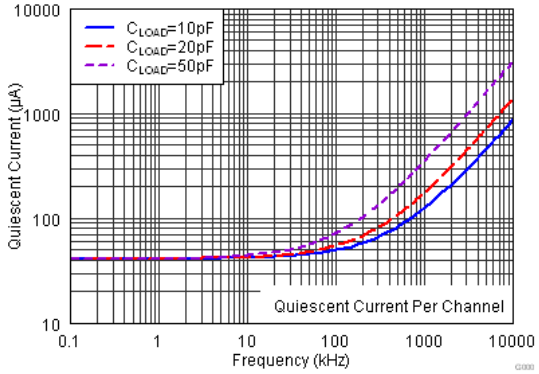


Figure 13.

SHORT-CIRCUIT CURRENT vs TEMPERATURE

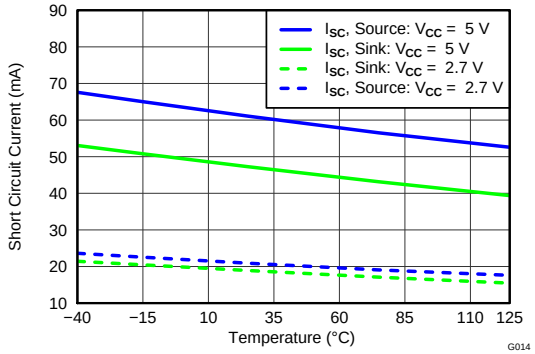


Figure 14.

OUTPUT VOLTAGE vs OUTPUT CURRENT

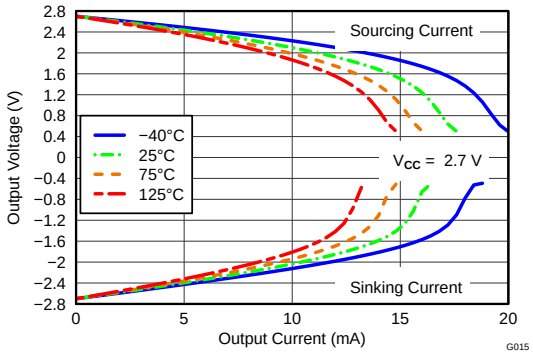


Figure 15.

OUTPUT VOLTAGE vs OUTPUT CURRENT

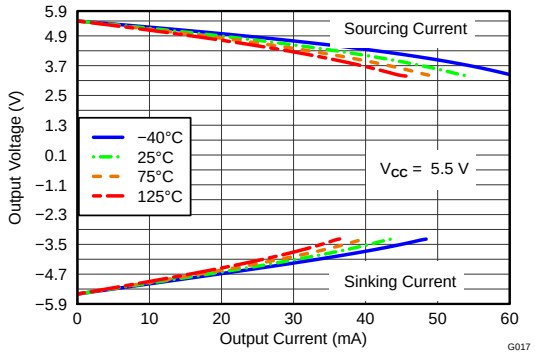


Figure 16.

PROPAGATION DELAY FALLING EDGE

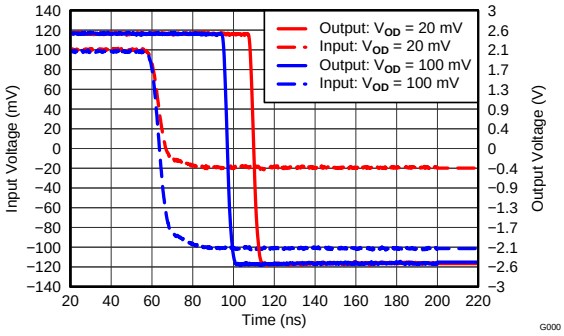


Figure 17.

PROPAGATION DELAY RISING EDGE

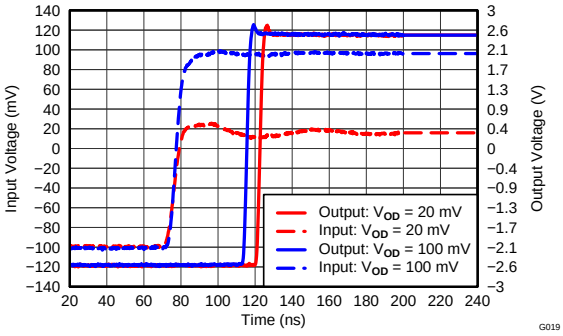


Figure 18.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{CC} = +5 V, and input overdrive (V_{OD}) = 20 mV, unless otherwise noted.

PROPAGATION DELAY vs INPUT OVERDRIVE

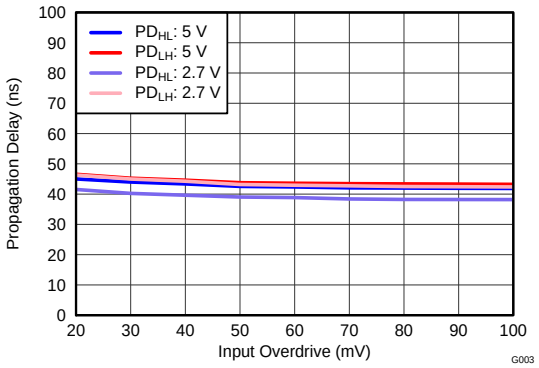


Figure 19.

PROPAGATION DELAY vs TEMPERATURE

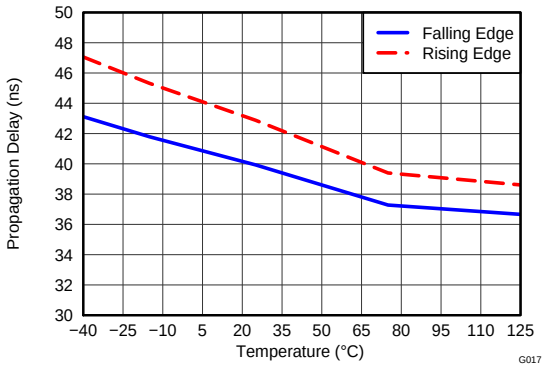


Figure 20.

PROPAGATION DELAY vs COMMON-MODE VOLTAGE

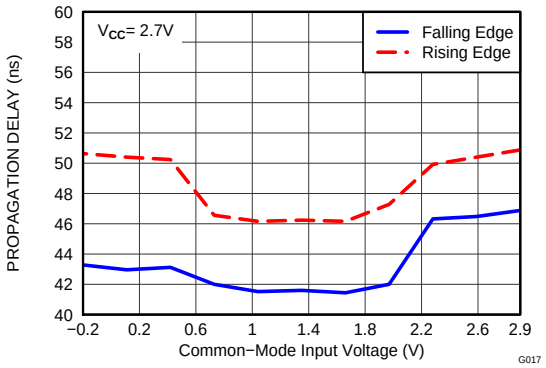


Figure 21.

PROPAGATION DELAY vs COMMON-MODE VOLTAGE

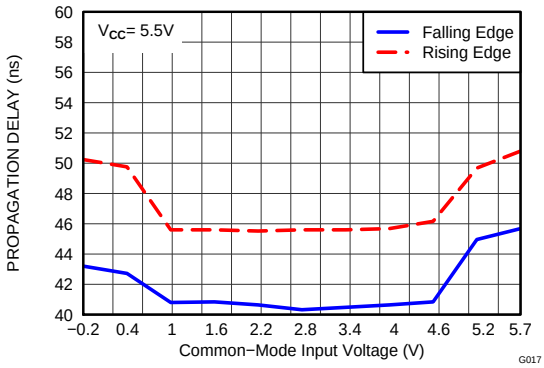


Figure 22.

PROPAGATION DELAY vs SUPPLY VOLTAGE

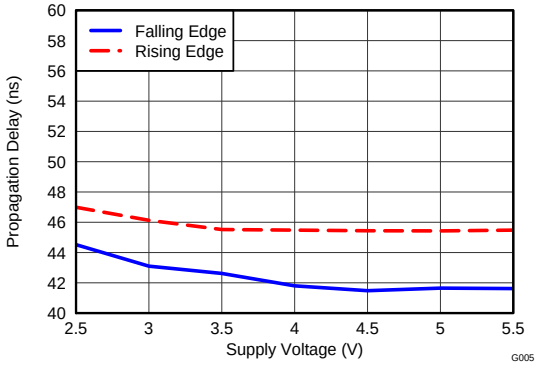


Figure 23.

PROPAGATION DELAY vs CAPACITIVE LOAD

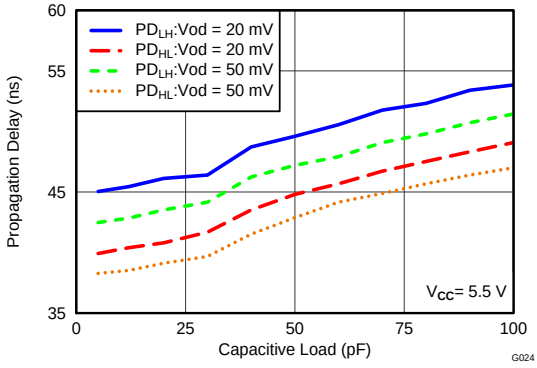


Figure 24.

APPLICATION INFORMATION

The HT3201 and HT3202 are single- and dual-supply (respectively), push-pull comparators featuring 40 ns of propagation delay on only 40 µA of supply current. This combination of fast response time and minimal power consumption make the HT3201 and HT3202 excellent comparators for portable, battery-powered applications as well as fast-switching threshold detection such as pulse-width modulation (PWM) output monitors and zero-cross detection.

COMPARATOR INPUTS

The HT3201 and HT3202 are rail-to-rail input comparators, with an input common-mode range that exceeds the supply rails by 200 mV for both positive and negative supplies. The devices are specified from 2.7 V to 5.5 V, with room temperature operation from 2.5 V to 5.5 V. The HT3201 and HT3202 are designed to prevent phase inversion when the input pins exceed the supply voltage. Figure 25 shows the HT320x response when input voltages exceed the supply, resulting in no phase inversion.

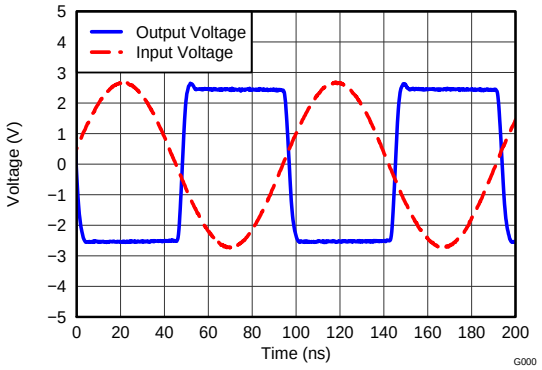


Figure 25. No Phase Inversion: Comparator Response to Input Voltage (Prop Delay Included)

The electrostatic discharge (ESD) protection input structure of two back-to-back diodes and 1-kΩ series resistors are used to limit the differential input voltage applied to the precision input of the comparator by clamping input voltages that exceed V_{CC} beyond the specified operating conditions. If potential overvoltage conditions that exceed absolute maximum ratings are present, the addition of external bypass diodes and resistors is recommended, as shown in Figure 26. Large differential voltages greater than the supply voltage should be avoided to prevent damage to the input stage.

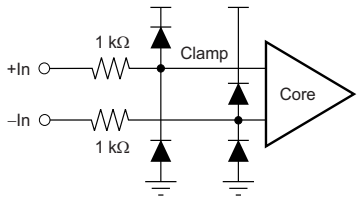


Figure 26. HT3201 equivalent input structure

EXTERNAL HYSTERESIS

The HT3201 and HT3202 have a hysteresis transfer curve (shown in Figure 27) that is a function of the following three components:

- V_{TH}: the actual set voltage or threshold trip voltage
- V_{OS}: the internal offset voltage between V_{IN+} and V_{IN-}. This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond in order to change output states.
- V_{HYST}: internal hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

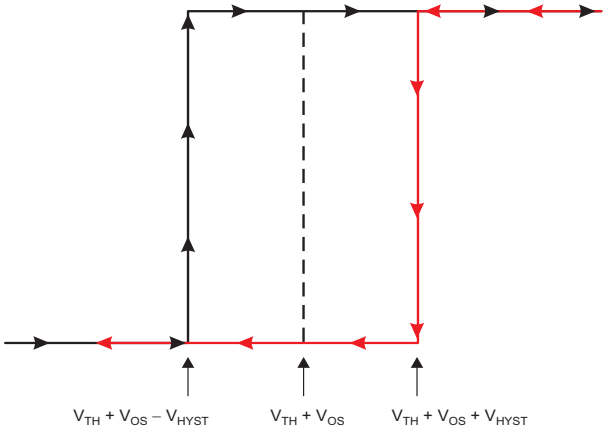


Figure 27. HT3201 Hysteresis Transfer Curve

Inverting Comparator With Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V_{CC}), as shown in Figure 28. When V_{IN} at the inverting input is less than V_A, the output voltage is high (for simplicity assume V_O switches as high as V_{CC}). The three network resistors can be represented as R1 || R3 in series with R2. The lower input trip voltage (V_{A1}) is defined by Equation 1:

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \parallel R3) + R2} \quad (1)$$

When V_{IN} is greater than [$V_A \times (V_{IN} > V_A)$], the output voltage is low, very close to ground. In this case, the three network resistors can be presented as R2 || R3 in series with R1. The upper trip voltage (V_{A2}) is defined by Equation 2:

$$V_{A2} = V_{CC} \times \frac{R2 \parallel R3}{R1 + (R2 \parallel R3)} \quad (2)$$

The total hysteresis provided by the network is defined by Equation 3:

$$\Delta V_A = V_{A1} - V_{A2} \quad (3)$$

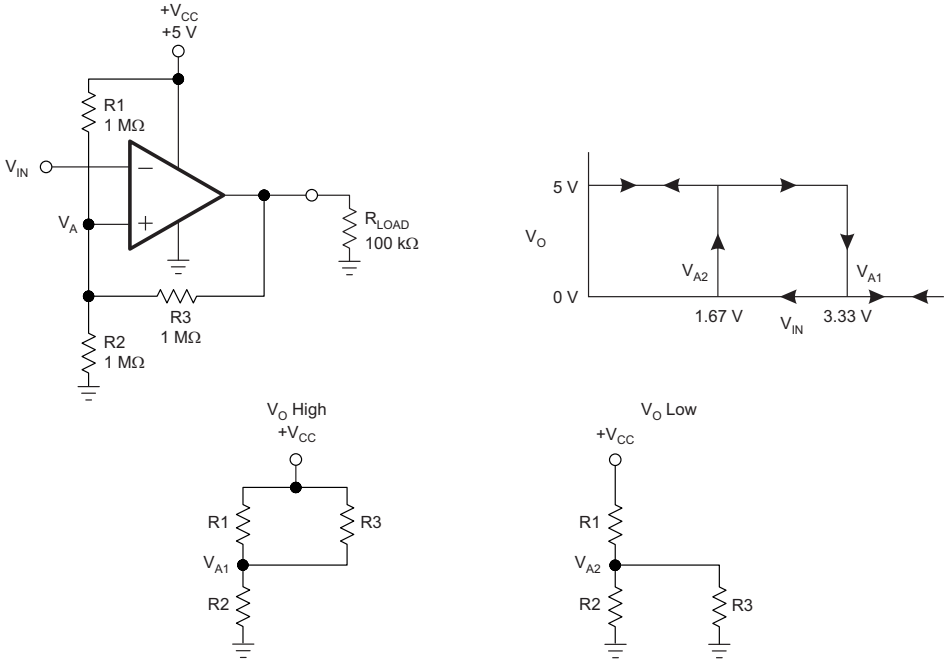


Figure 28. HT3201 in Inverting Configuration with Hysteresis

Noninverting Comparator with Hysteresis

A noninverting comparator with hysteresis requires a two-resistor network, as shown in Figure 29, and a voltage reference (V_{REF}) at the inverting input. When V_{IN} is low, the output is also low. For the output to switch from low to high, V_{IN} must rise up to V_{IN1}. V_{IN1} is calculated by Equation 4:

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} \times V_{REF} \quad (4)$$

When V_{IN} is high, the output is also high. In order for the comparator to switch back to a low state, V_{IN} must equal V_{REF} before V_A is again equal to V_{REF}. V_{IN} can be calculated by Equation 5:

$$V_{IN2} = \frac{V_{REF}\,(R1 + R2) - V_{CC} \times R1}{R2} \quad (5)$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}, as defined by Equation 6.

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2} \quad (6)$$

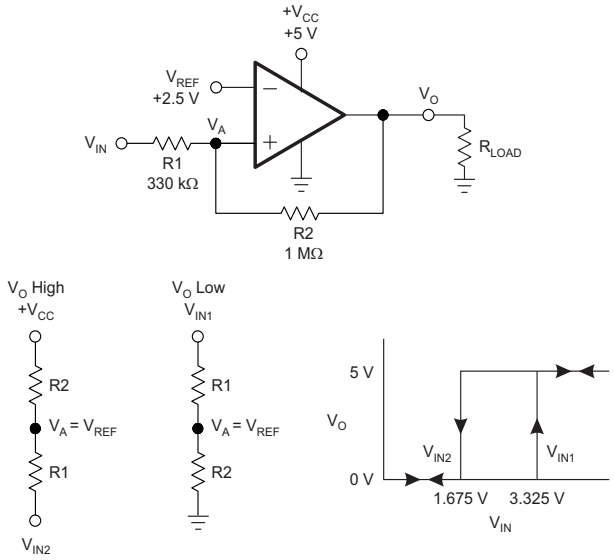


Figure 29. HT3201 in Noninverting Configuration with Hysteresis

CAPACITIVE LOADS

The HT3201 and HT3202 feature a push-pull output. When the output switches, there is a direct path between V_{CC} and ground, causing increased output sinking or sourcing current during the transition. Following the transition the output current decreases and supply current returns to 40 µA, thus maintaining low power consumption. Under reasonable capacitive loads, the HT3201 and HT3202 maintain specified propagation delay (see the Typical Characteristics), but excessive capacitive loading under high switching frequencies may increase supply current, propagation delay, or induce decreased slew rate.

CIRCUIT LAYOUT

The HT3201 and HT3202 are fast-switching, high-speed comparators and require high-speed layout considerations. For best results, the following layout guidelines should be maintained:

1. Use a printed circuit board (PCB) with a good, unbroken low-inductance ground plane.
2. Place a decoupling capacitor (0.1-μF ceramic, surface-mount capacitor) as close as possible to V_{CC}.
3. On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep inputs away from the output.
4. Solder the device directly to the PCB rather than using a socket.
5. For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000 pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to propagation delay when the impedance is low. The topside ground plane runs between the output and inputs.
6. The ground pin ground trace runs under the device up to the bypass capacitor, shielding the inputs from the outputs.

APPLICATIONS CIRCUITS

One of the benefits of ac coupling a single-supply comparator circuit is that it can block dc offsets induced by ground-loop offsets that could potentially produce either a false trip or a common-mode input violation. Figure 30 shows the HT3201 configured as an ac-coupled comparator.

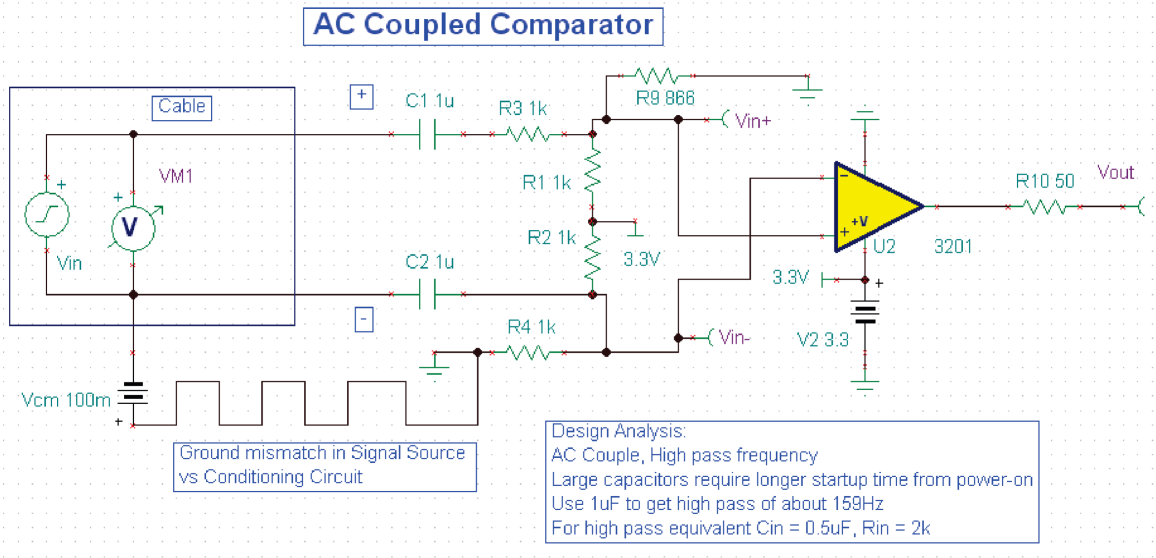


Figure 30. HT3201 Configured as an AC-Coupled Comparator

Figure 31 shows a single-supply current monitor configured as a difference amplifier with a gain of 50. The OPA320 was chosen for this circuit because of its gain bandwidth (20 MHz), which allows higher speed triggering and monitoring of the current across the shunt resistor followed by the fast response of the HT3201.

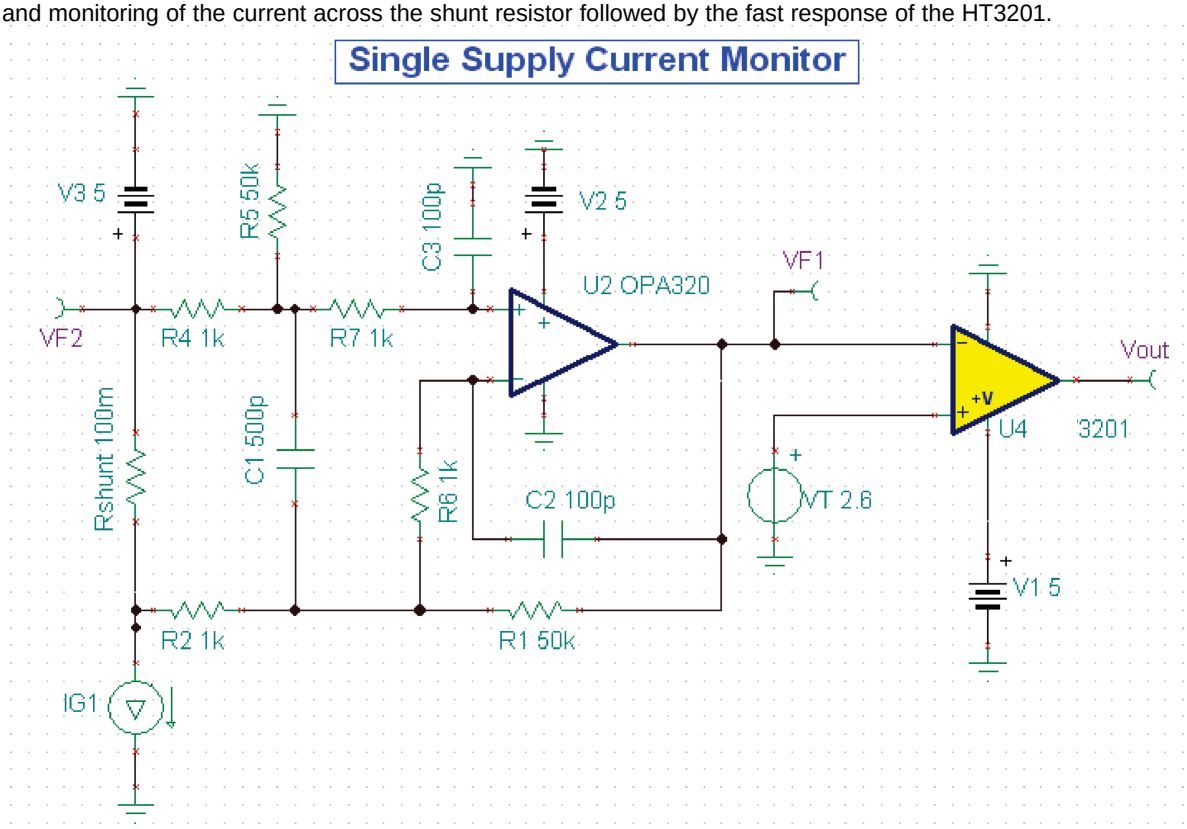


Figure 31. HT3201 and OPA320 Configured as a Fast-Response Output Current Monitor

Figure 32 shows the TMP20 and HT3201 designed as a high-speed temperature switch. The TMP20 is an analog output temperature sensor where output voltage decreases with temperature. The comparator output is tripped when the output reaches a critical trip threshold.

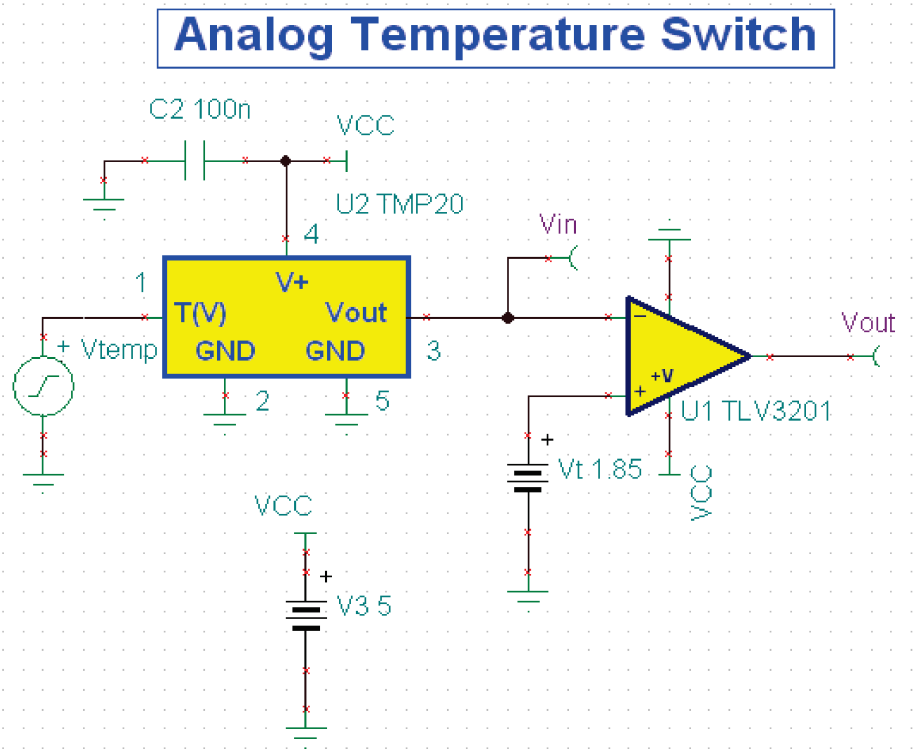
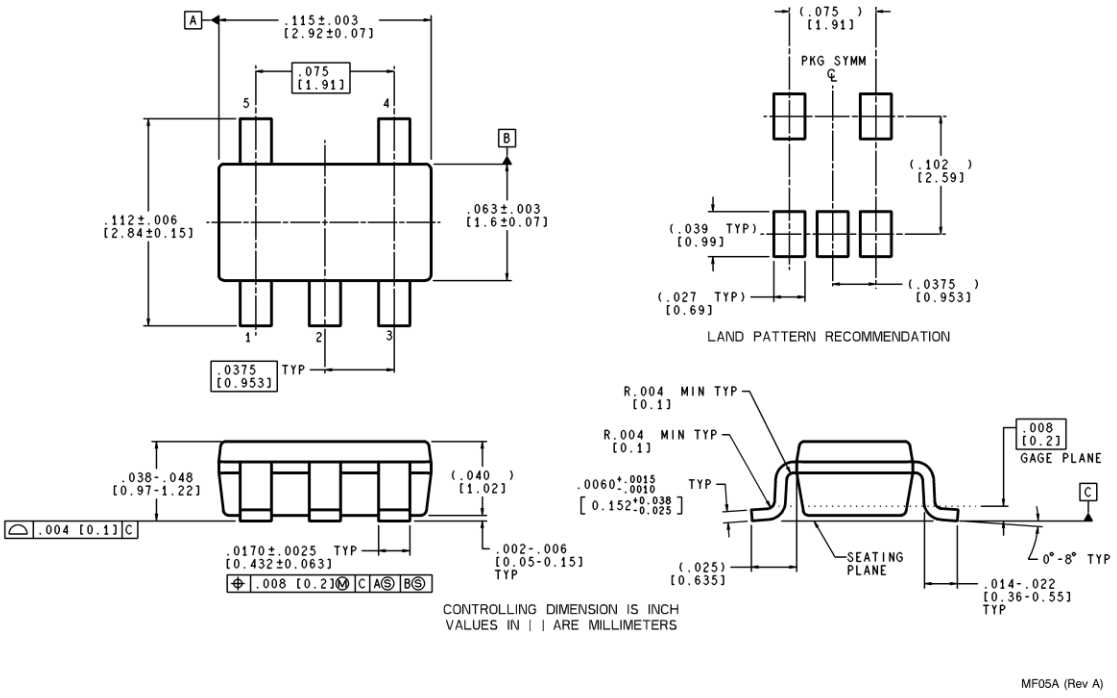


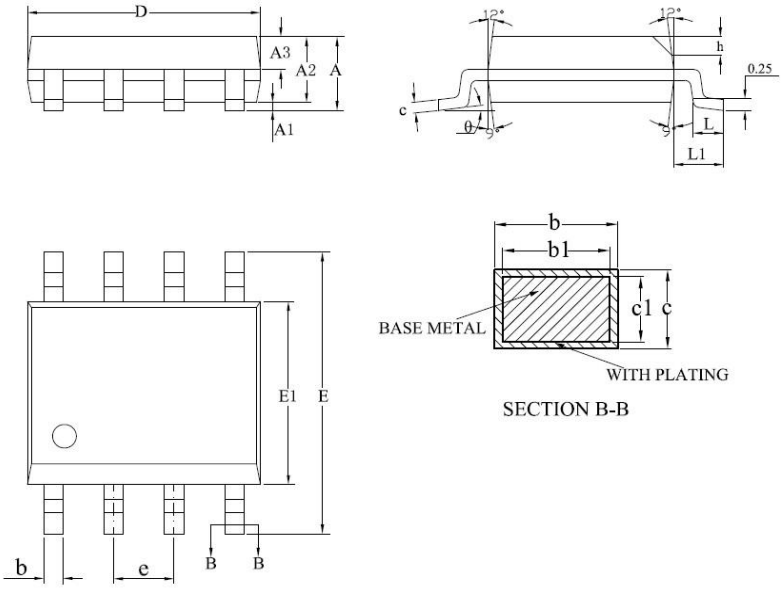
Figure 32. HT3201 and TMP20 Configured as a Precision Analog Temperature Switch

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



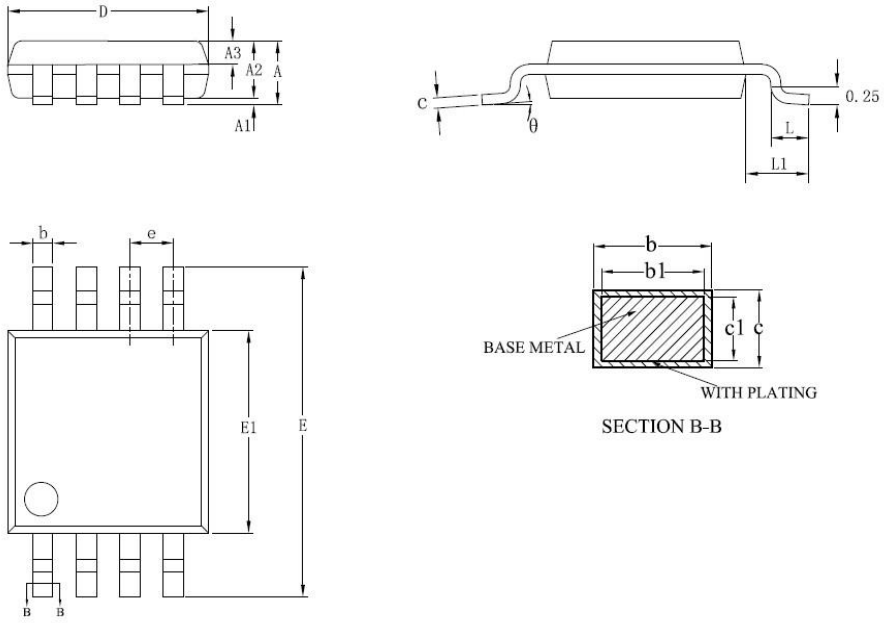
5-Pin SOT23-5
NS Package Number MF05A

SOIC-8



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

MSOP-8



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.10
A1	0.05	—	0.15
A2	0.75	0.85	0.95
A3	0.30	0.35	0.40
b	0.28	—	0.36
b1	0.27	0.30	0.33
c	0.15	—	0.19
c1	0.14	0.15	0.16
D	2.90	3.00	3.10
E	4.70	4.90	5.10
E1	2.90	3.00	3.10
e	0.65BSC		
L	0.40	—	0.70
L1	0.95REF		
θ	0	—	8°