500 mA Low-Dropout Linear Regulator

Features

- Input voltage range: 1.9V to 5V
- Fixed outputs of 1.0V, 1.2V, 1.5V, 1.8V, 2.5V, 2.8V, 3.0V, 3.3V
- Rated output current: 500mA
- Quiescent current: typical 54μA
- Typical 0.1μA shutdown current
- Typical 200mV dropout voltage at 300mA load
- Power supply rejection ratio: typical 72dB (I_{OUT}=30mA, freq=1kHz,1.8V output)
- Noise: typical 85μVrms (I_{OUT}=30mA, BW=10Hz to 100kHz, 1.8V output)
- Built-in output short protection: typical 60mA when output short to ground
- Output auto discharge function
- DFN 1mm X1mm X0.37mm-4L package

Applications

Battery-powered equipment

Smart phone

Digital camera

STB

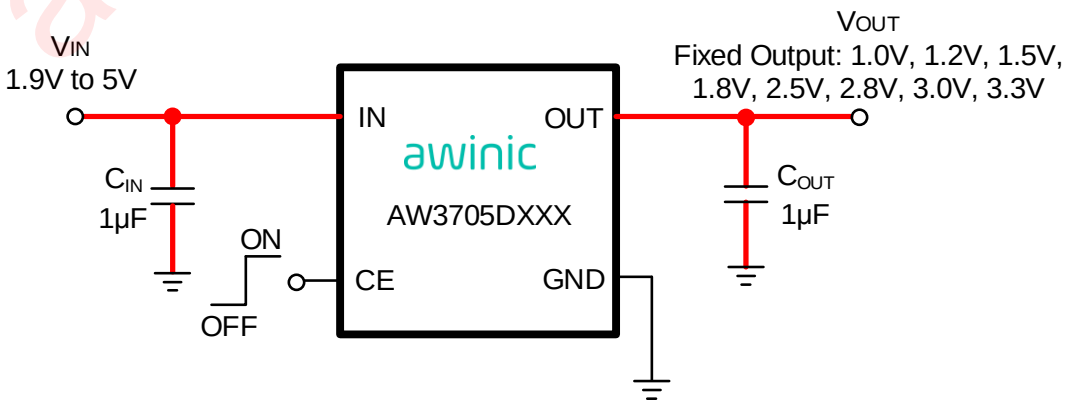
General Description

AW3705DXXX is a low dropout voltage regulator featuring low ON resistance, high PSRR, low Noise, good load/line transient response and smooth soft-start.

AW3705DXXX integrates current limit, short circuit protection, thermal shutdown, sufficiently protecting IC from being damaged.

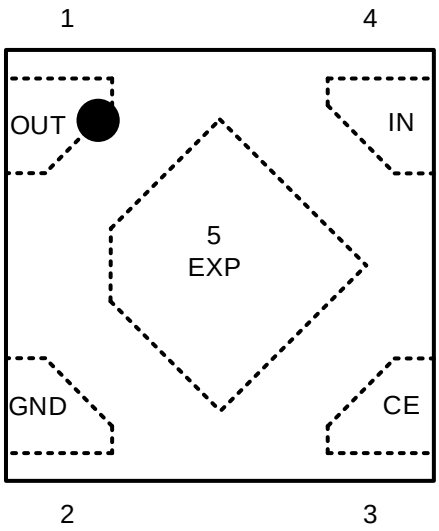
AW3705DXXX is designed to work with a 1μF or more input ceramic capacitor and a 1μF or more output ceramic capacitor. The low power dissipation and good dynamic response make AW3705DXXX very suitable for hand-held communication equipment. Tiny package makes high density mounting of the IC on boards possible.

Typical Application Circuit

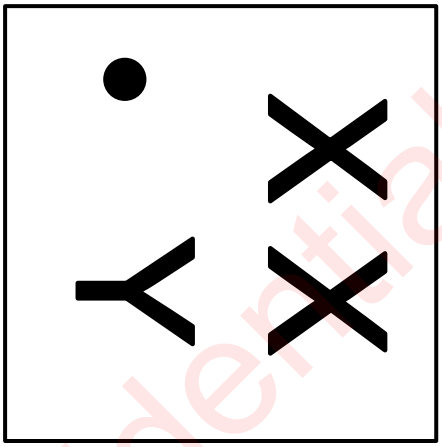


Pin Configuration And Top Mark

AW3705DXXXDNR
(Top View)



AW3705DXXXDNR Marking
(Top View)



XX – AW3705DXXXDNR
Y – Production Tracing Code

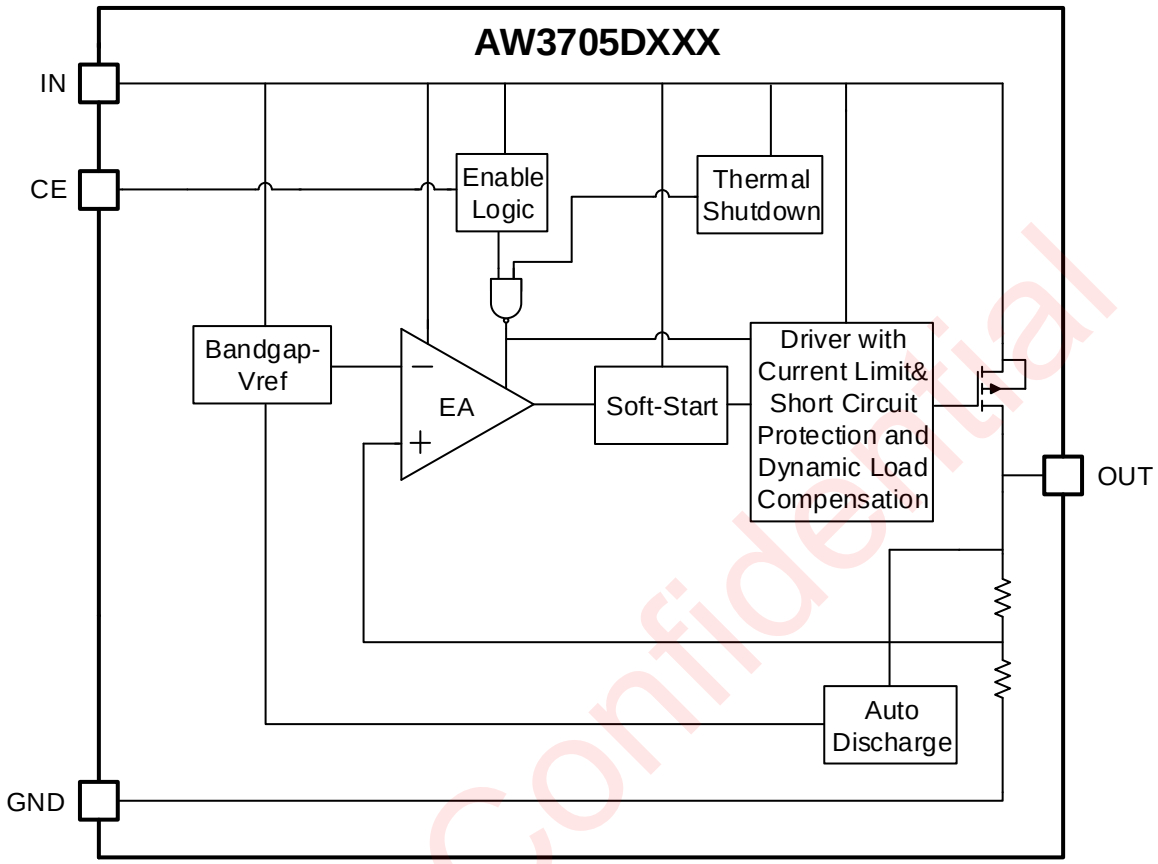
Pin Definition

No.	NAME	DESCRIPTION
1	OUT	Regulated output voltage pin. Put a 1μF or more ceramic capacitor at the output pin.
2	GND	Ground.
3	CE	Chip enable pin. Built-in pull-down resistor. (High Active)
4	IN	Input supply pin. Add a 1μF or more bypass capacitor at the power supply.
5	EXP	Expose pad should be tied to ground plane for better power dissipation.

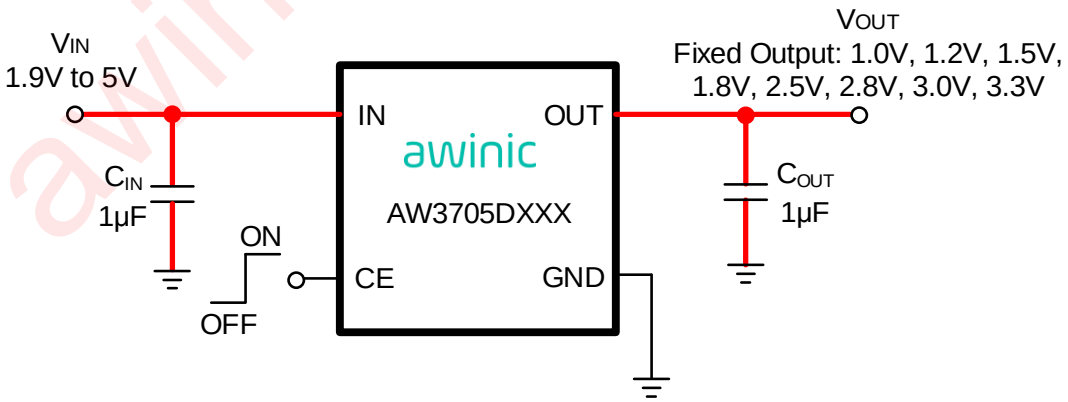
Device Comparison Table

Part Number	$V_{OUT(SET)}$	Rated Current	CE Active	Auto Discharge
AW3705D100DNR	1.0V	500mA	High	YES
AW3705D120DNR	1.2V	500mA	High	YES
AW3705D150DNR	1.5V	500mA	High	YES
AW3705D180DNR	1.8V	500mA	High	YES
AW3705D250DNR	2.5V	500mA	High	YES
AW3705D280DNR	2.8V	500mA	High	YES
AW3705D300DNR	3.0V	500mA	High	YES
AW3705D330DNR	3.3V	500mA	High	YES

Functional Block Diagram



Typical Application Circuits



AW3705DXXX Application circuit

Notice for typical application circuits:

Capacitance of C_{IN} and C_{OUT} should be 1µF or more.

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW3705D100 DNR	-40°C～85°C	DFN 1mmX1mm -4L	AC	MSL1	ROHS+HF	3000 units/Tape and Reel
AW3705D120 DNR	-40°C～85°C	DFN 1mmX1mm -4L	AG	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW3705D150 DNR	-40°C～85°C	DFN 1mmX1mm -4L	AM	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW3705D180 DNR	-40°C～85°C	DFN 1mmX1mm -4L	AS	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW3705D250 DNR	-40°C～85°C	DFN 1mmX1mm -4L	BG	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW3705D280 DNR	-40°C～85°C	DFN 1mmX1mm -4L	BM	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW3705D300 DNR	-40°C～85°C	DFN 1mmX1mm -4L	BQ	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW3705D330 DNR	-40°C～85°C	DFN 1mmX1mm -4L	BW	MSL1	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS	RANGE
Input voltage range V_{BUS}	-0.3V to 6V
Enable control voltage range	-0.3V to 6V
Output voltage range	-0.3V to 6V
Junction-to-ambient thermal resistance θ_{JA}（NOTE2）	250°C/W
Operating free-air temperature range	-40°C to 85°C
Maximum operating junction temperature T_{JMAX}	150°C
Storage temperature T_{STG}	-65°C to 150°C
Lead temperature (soldering 10 seconds)	260°C
ESD	
HBM (Human body model)(NOTE3)	±2kV
CDM(Charged device model)(NOTE4)	±1.5kV
MM(Machine Model)(NOTE5)	±200V
Latch-Up	
Latch-Up(NOTE6)	+IT：200mA -IT：-200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: Thermal resistance from junction to ambient is highly dependent on PCB layout.

NOTE3: All pins. Test Condition: ESDA/JEDEC JS-001-2017.

NOTE4: All pins. Test Condition: ESDA/JEDEC JS-002-2014.

NOTE5: All pins. Test Condition: JESD22 A115C.

NOTE6: Test Condition: JESD78E.

Electrical Characteristics

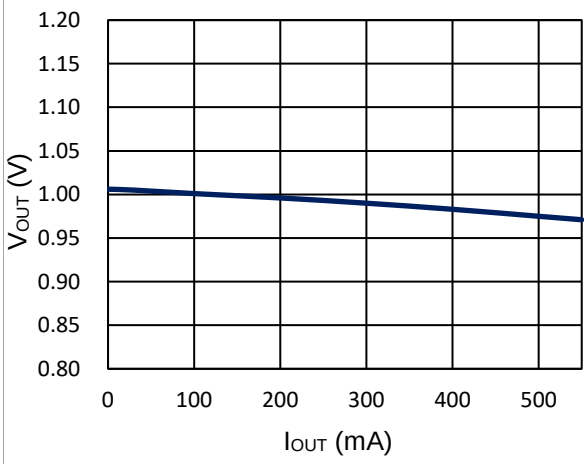
V_{IN}=$V_{OUT(SET)}$+1V, V_{CE}>1.2V, I_{OUT}=1mA, C_{IN}=C_{OUT}=1μF, T_A=25°C (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage Range		1.9		5	V
V_{OUT_ACC}	Output Voltage Accuracy		-3		3	%
$LOAD_{Reg}$	Load Regulation	1mA≤I_{OUT}≤500mA		30	68	mV
$LINE_{Reg}$	Line Regulation	$V_{OUT(SET)}$+0.5V≤V_{IN}≤5V		0.06	0.15	%/V
$V_{dropout}$	Dropout Voltage	I_{OUT}=300mA (for AW3705D180DNR)		200		mV
I_{SD}	Shutdown Current	V_{CE}<0.4V		0.1	1	μA
I_Q	Quiescent Current	I_{OUT}=0mA		54	80	μA
V_{CEH}	CE Input Voltage “H”	-40°C ≤T_A≤85°C	1.2			V
V_{CEL}	CE Input Voltage “L”	-40°C ≤T_A≤85°C			0.4	V
PSRR	Power Supply Ripple Rejection	I_{OUT}=30mA, f=1kHz (for AW3705D180DNR)		72		dB
V_N	Output Voltage Noise	I_{OUT}=30mA, BW=10Hz to 100kHz		45* $V_{OUT(SET)}$		μVrms
I_{CL}	Output Current Limit	V_{OUT}=90%*$V_{OUT(SET)}$	550	850		mA
I_{SC}	Short Current Limit	V_{OUT}<10%*$V_{OUT(SET)}$		60		mA
VTC	Output Voltage Temperature Coefficient	-40°C ≤T_A≤85°C		±80		ppm/°C
R_{DISC}	Auto Discharge Resistance	V_{CE}<0.4V, I_{OUT}=0mA		160		Ω
T_{SDH}	Thermal Shutdown Threshold	Temperature Rising		150		°C
T_{SDL}	Thermal Shutdown Reset Threshold	Temperature Falling		130		°C

Typical Characteristics

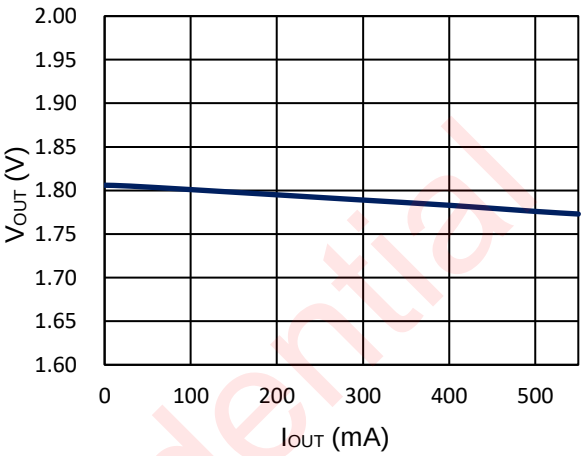
$V_{IN}=V_{OUT(SET)}+1V$, $V_{CE}>1.2V$, $I_{OUT}=1mA$, $C_{IN}=C_{OUT}=1\mu F$, $T_A=25°C$, In Typical Application Circuit , unless other noted.

AW3705D100DNR



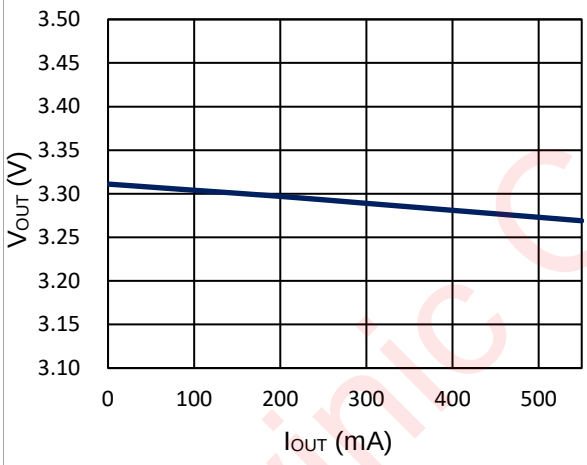
Output Voltage vs Output Current

AW3705D180DNR



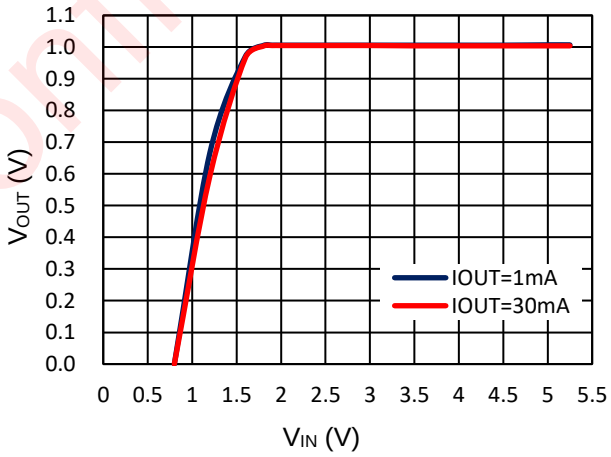
Output Voltage vs Output Current

AW3705D330DNR



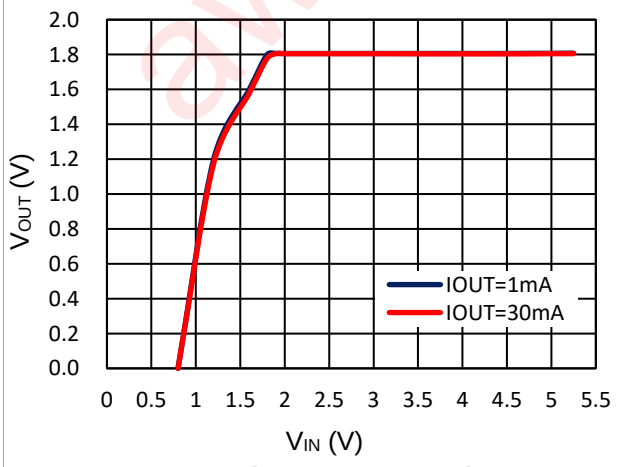
Output Voltage vs Output Current

AW3705D100DNR



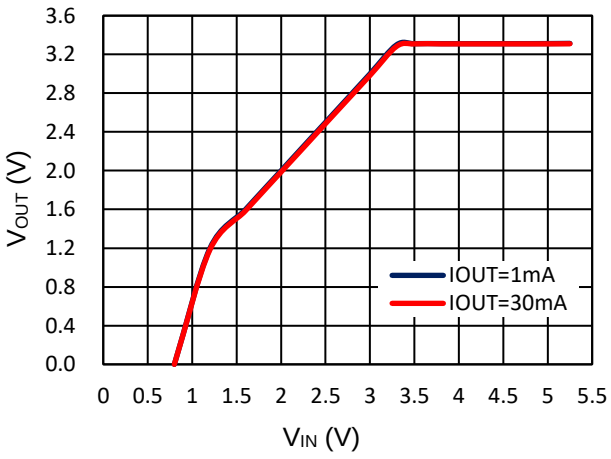
Output Voltage vs Input Voltage

AW3705D180DNR



Output Voltage vs Input Voltage

AW3705D330DNR

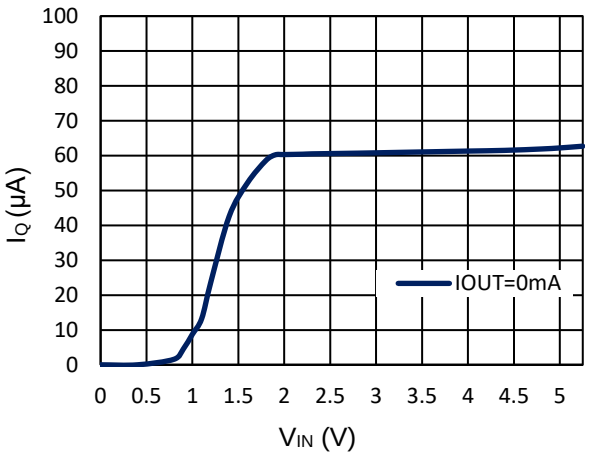


Output Voltage vs Input Voltage

Typical Characteristics (Continued)

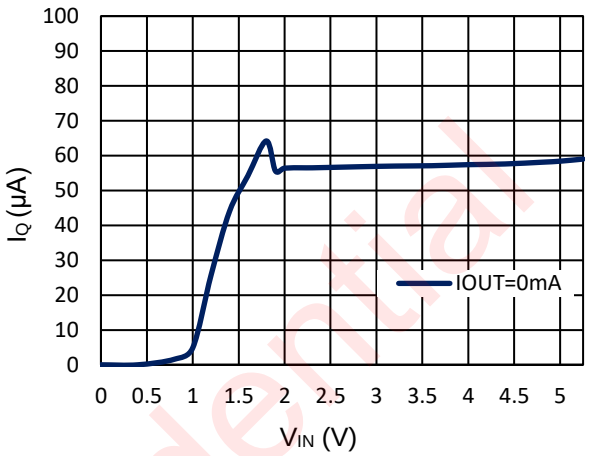
V_{IN}=$V_{OUT(SET)}$+1V, V_{CE}>1.2V , I_{OUT}=1mA , C_{IN}=C_{OUT}=1μF, T_A=25°C, In Typical Application Circuit , unless other noted.

AW3705D100DNR



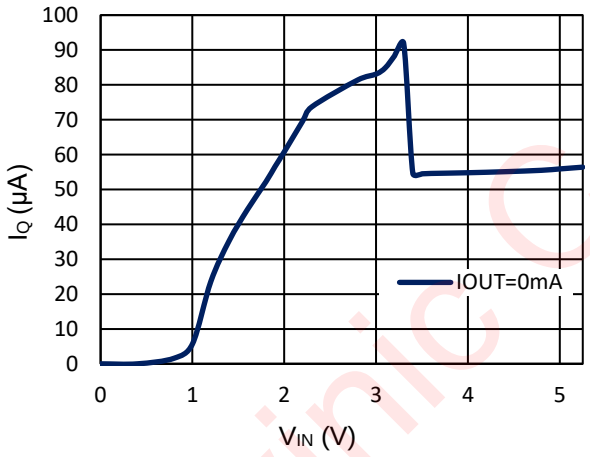
Quiescent Current vs Input Voltage

AW3705D180DNR



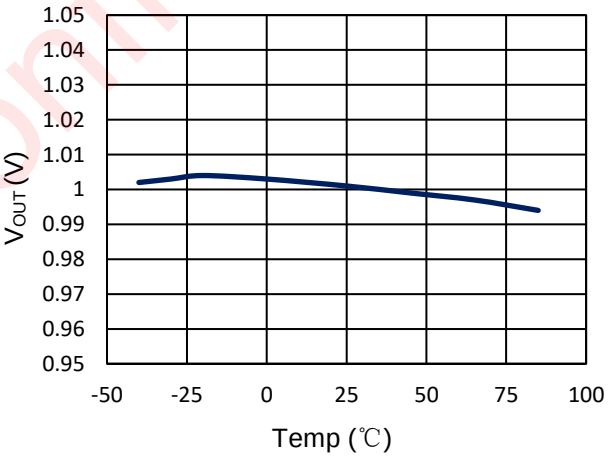
Quiescent Current vs Input Voltage

AW3705D330DNR



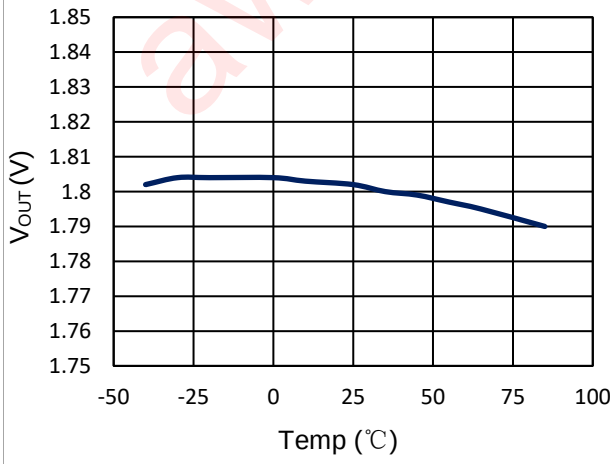
Quiescent Current vs Input Voltage

AW3705D100DNR



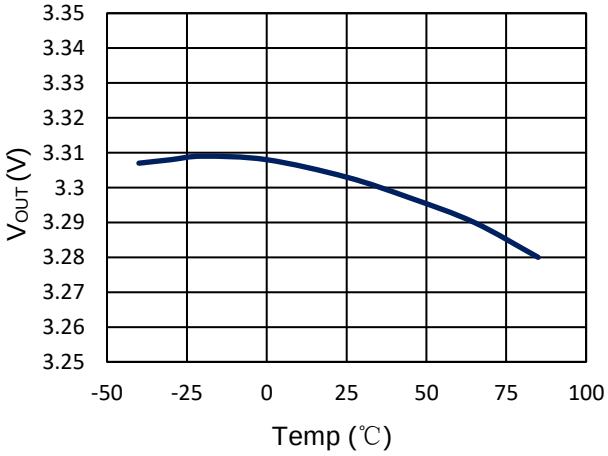
Output Voltage vs Temperature

AW3705D180DNR



Output Voltage vs Temperature

AW3705D330DNR

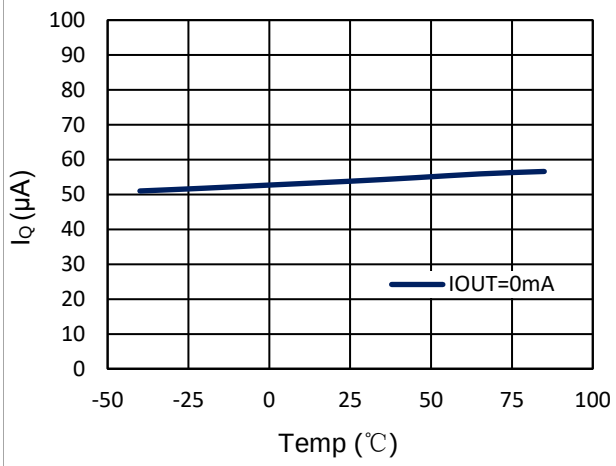


Output Voltage vs Temperature

Typical Characteristics (Continued)

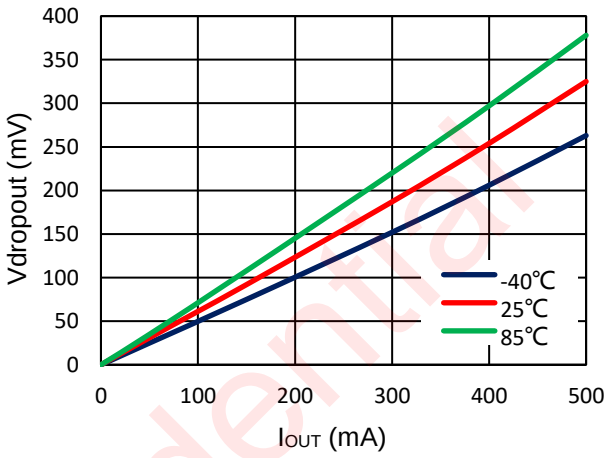
$V_{IN}=V_{OUT(SET)}+1V$, $V_{CE}>1.2V$, $I_{OUT}=1mA$, $C_{IN}=C_{OUT}=1\mu F$, $T_A=25°C$, In Typical Application Circuit , unless other noted.

AW3705D180DNR



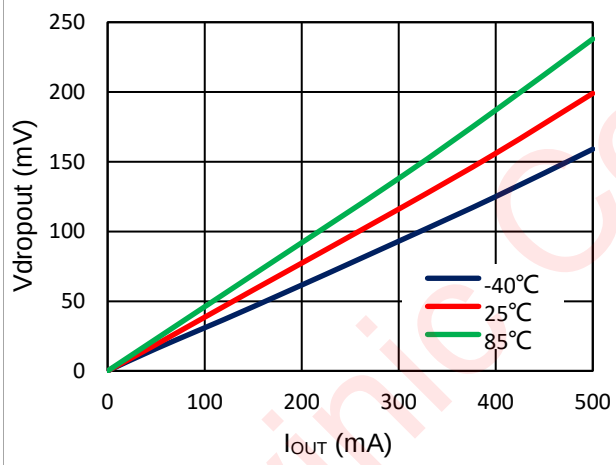
Quiescent Current vs Temperature

AW3705D180DNR



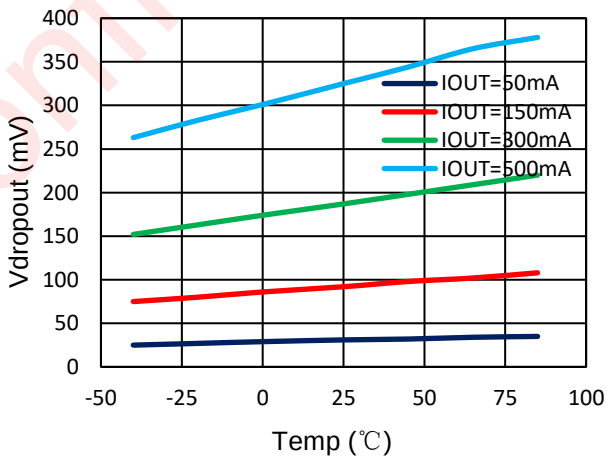
Dropout Voltage vs Output Current

AW3705D330DNR



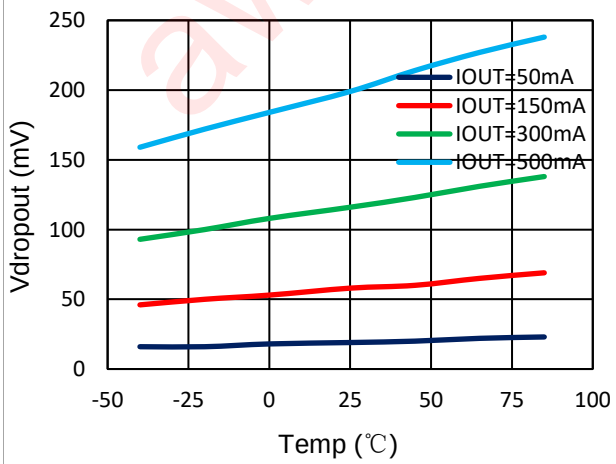
Dropout Voltage vs Output Current

AW3705D180DNR



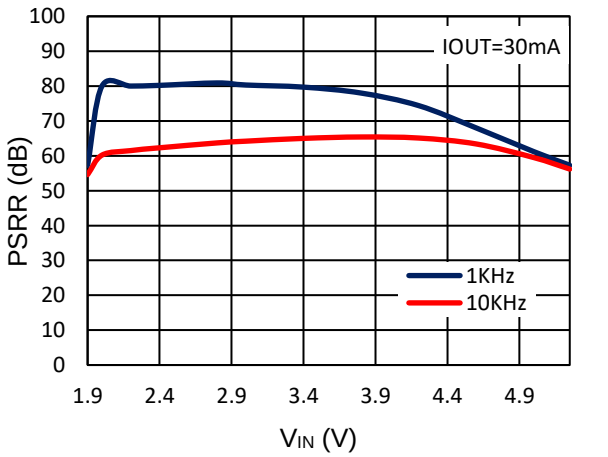
Dropout Voltage vs Temperature

AW3705D330DNR



Dropout Voltage vs Temperature

AW3705D100DNR

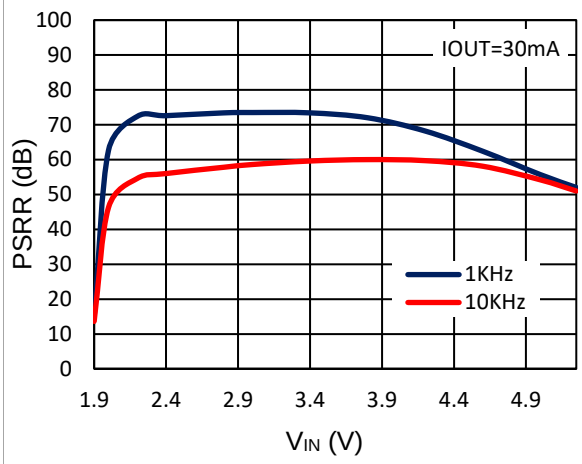


PSRR vs Input Voltage

Typical Characteristics (Continued)

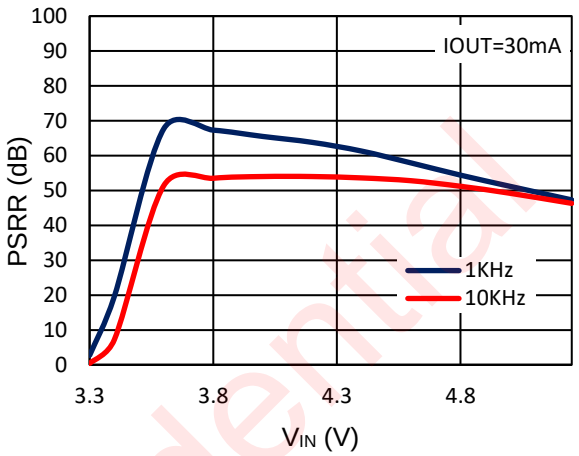
V_{IN}=$V_{OUT(SET)}$+1V, V_{CE}>1.2V , I_{OUT}=1mA , C_{IN}=C_{OUT}=1μF, T_A=25°C, In Typical Application Circuit , unless other noted.

AW3705D180DNR



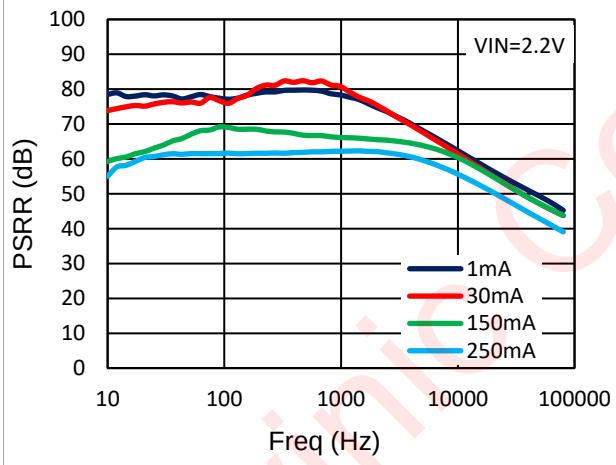
PSRR vs Input Voltage

AW3705D330DNR



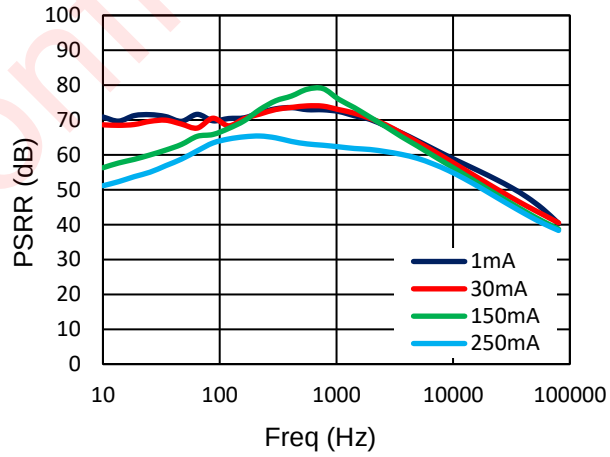
PSRR vs Input Voltage

AW3705D100DNR



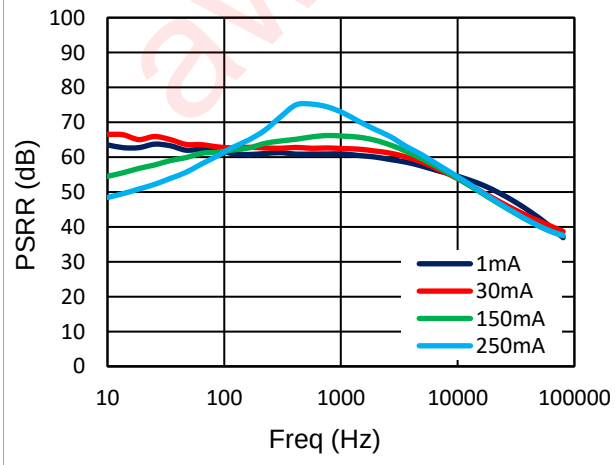
PSRR vs Frequency

AW3705D180DNR



PSRR vs Frequency

AW3705D330DNR

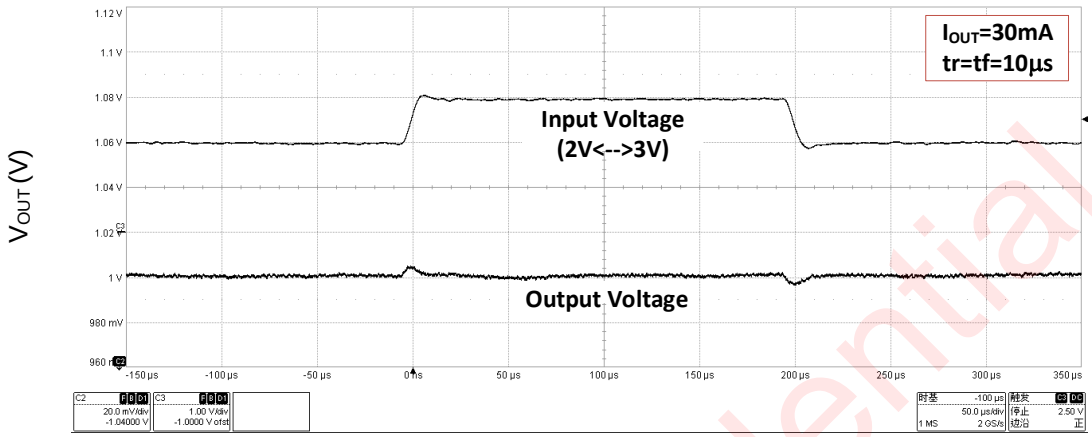


PSRR vs Frequency

Typical Characteristics (Continued)

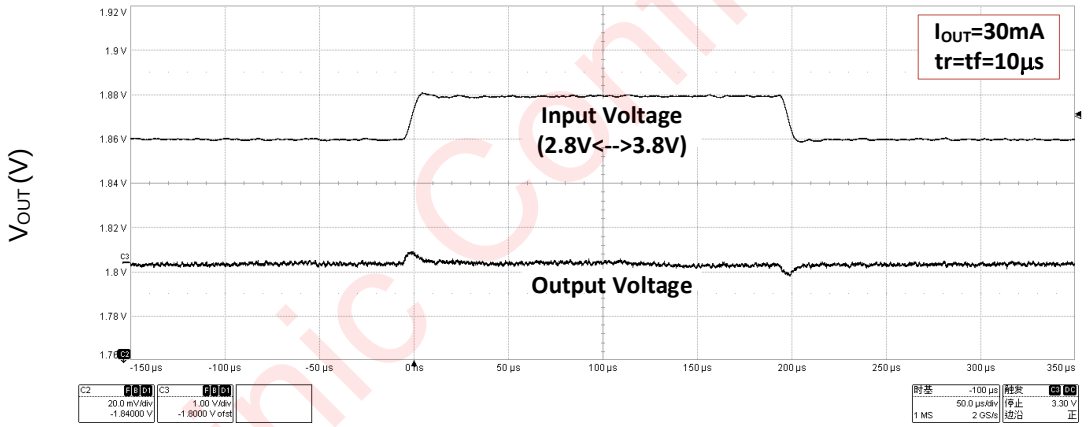
$V_{IN}=V_{OUT(SET)}+1V$, $V_{CE}>1.2V$, $I_{OUT}=1mA$, $C_{IN}=C_{OUT}=1\mu F$, $T_A=25°C$, In Typical Application Circuit , unless other noted.

AW3705D100DNR



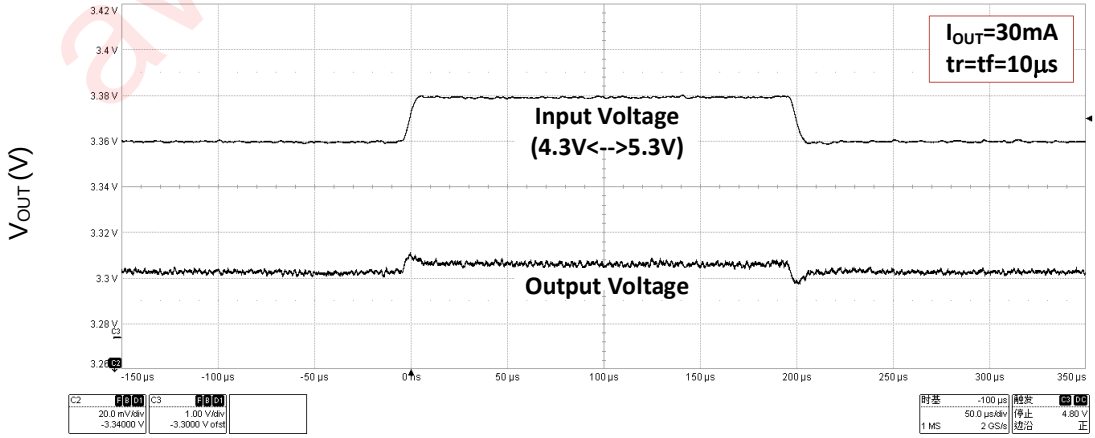
Input Transient Response

AW3705D180DNR



Input Transient Response

AW3705D330DNR

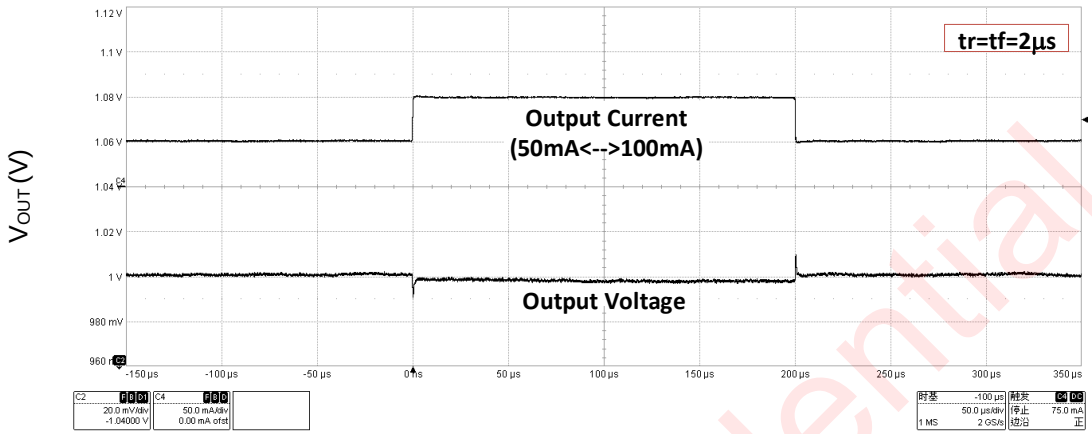


Input Transient Response

Typical Characteristics (Continued)

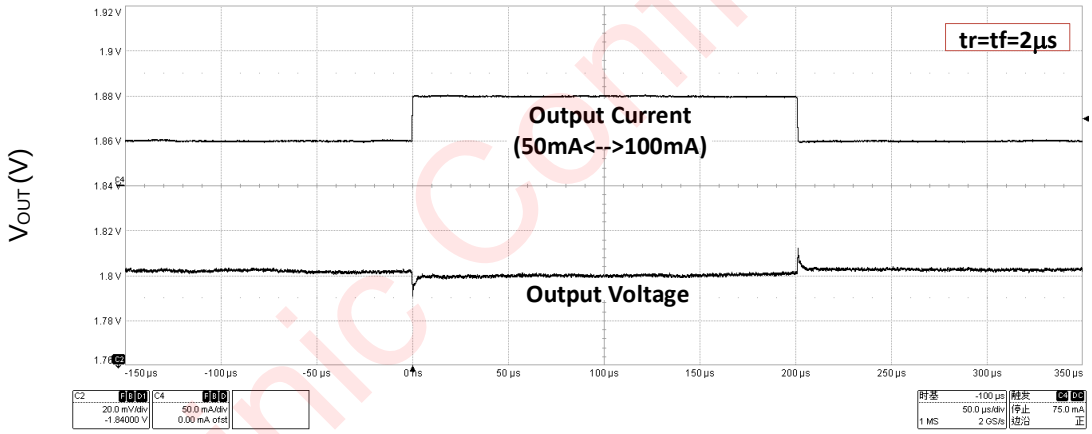
$V_{IN}=V_{OUT(SET)}+1V$, $V_{CE}>1.2V$, $I_{OUT}=1mA$, $C_{IN}=C_{OUT}=1\mu F$, $T_A=25°C$, In Typical Application Circuit , unless other noted.

AW3705D100DNR



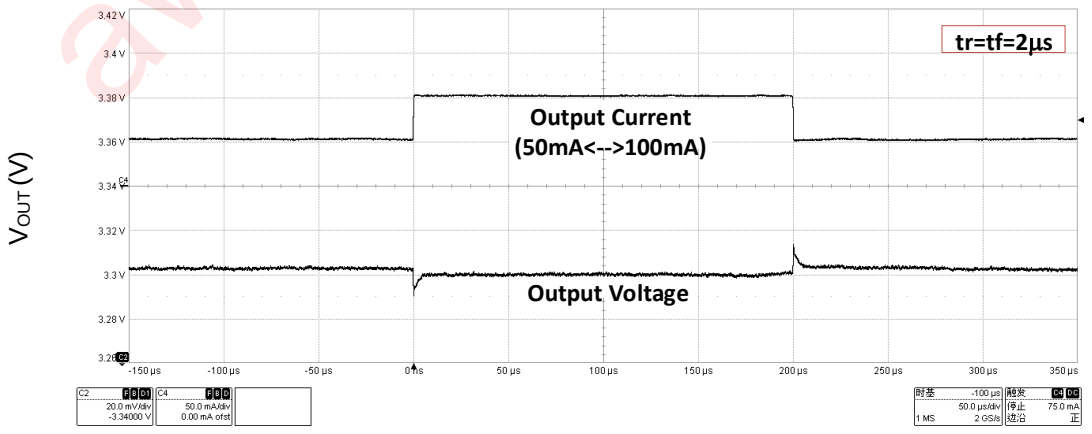
Load Transient Response

AW3705D180DNR



Load Transient Response

AW3705D330DNR

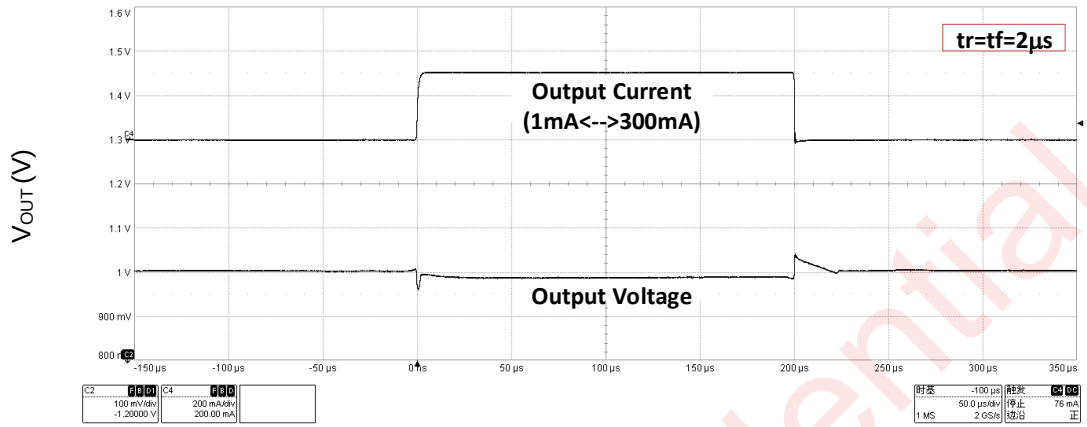


Load Transient Response

Typical Characteristics (Continued)

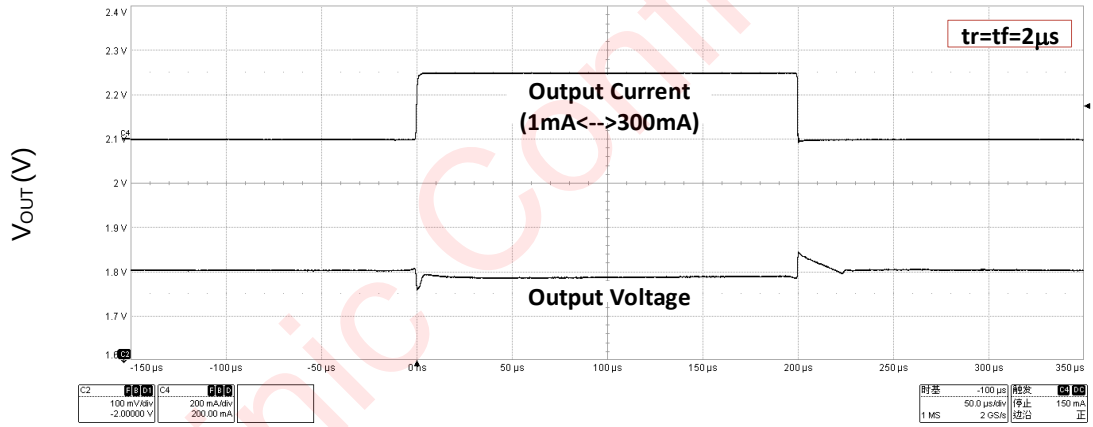
$V_{IN}=V_{OUT(SET)}+1V$, $V_{CE}>1.2V$, $I_{OUT}=1mA$, $C_{IN}=C_{OUT}=1\mu F$, $T_A=25°C$, In Typical Application Circuit , unless other noted.

AW3705D100DNR



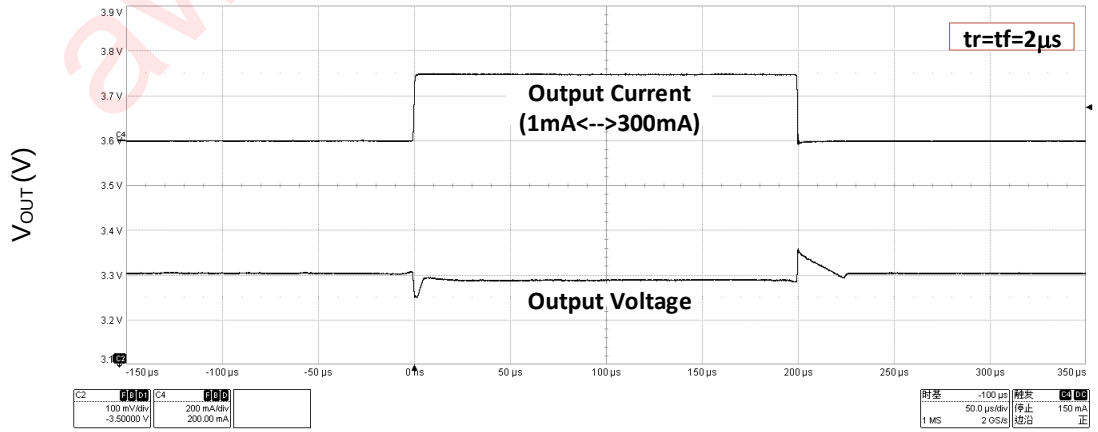
Load Transient Response

AW3705D180DNR



Load Transient Response

AW3705D330DNR

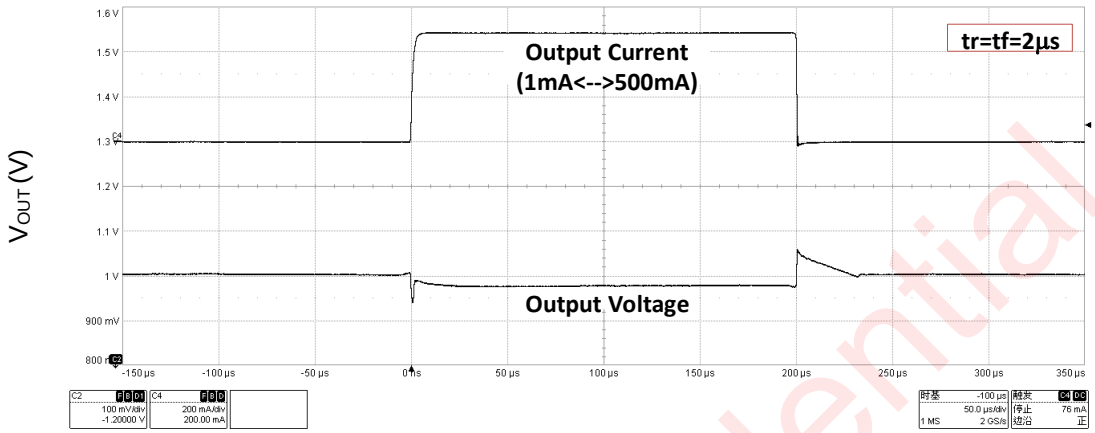


Load Transient Response

Typical Characteristics (Continued)

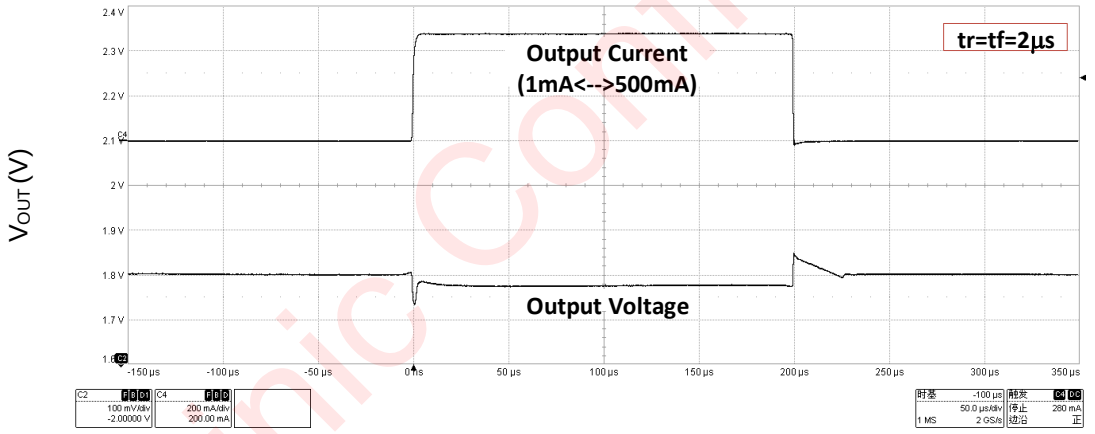
$V_{IN}=V_{OUT(SET)}+1V$, $V_{CE}>1.2V$, $I_{OUT}=1mA$, $C_{IN}=C_{OUT}=1\mu F$, $T_A=25°C$, In Typical Application Circuit , unless other noted.

AW3705D100DNR



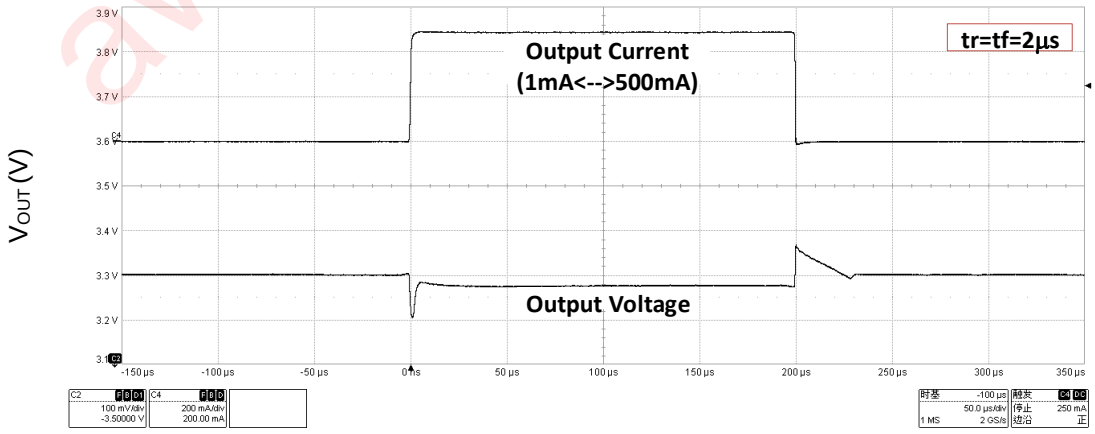
Load Transient Response

AW3705D180DNR



Load Transient Response

AW3705D330DNR

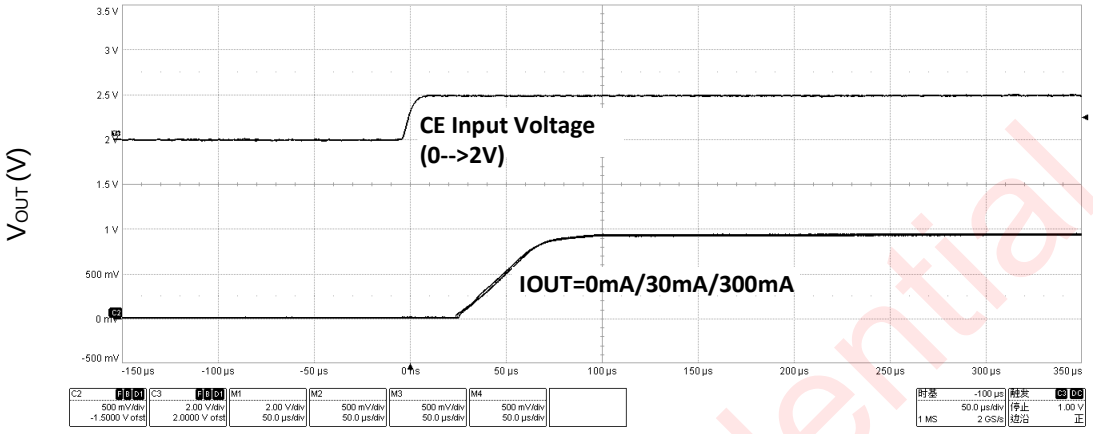


Load Transient Response

Typical Characteristics (Continued)

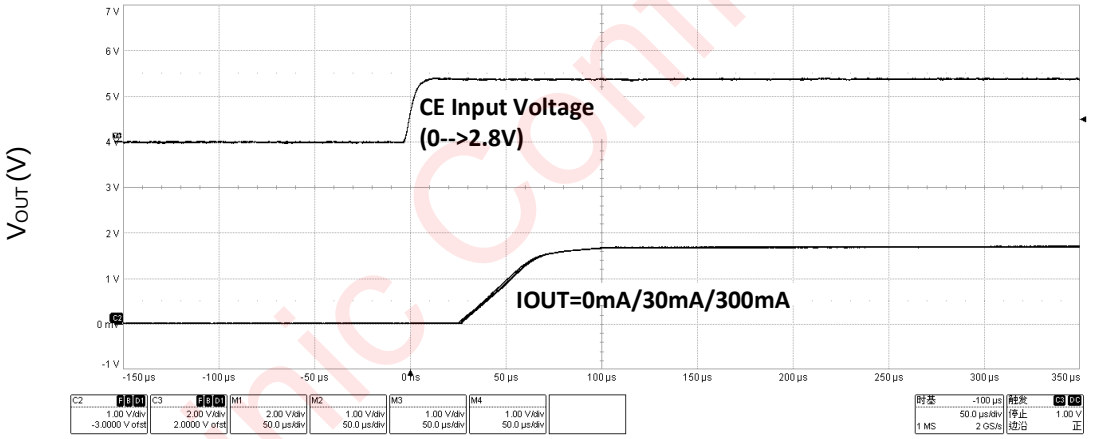
$V_{IN}=V_{OUT(SET)}+1V$, $V_{CE}>1.2V$, $I_{OUT}=1mA$, $C_{IN}=C_{OUT}=1\mu F$, $T_A=25°C$, In Typical Application Circuit , unless other noted.

AW3705D100DNR



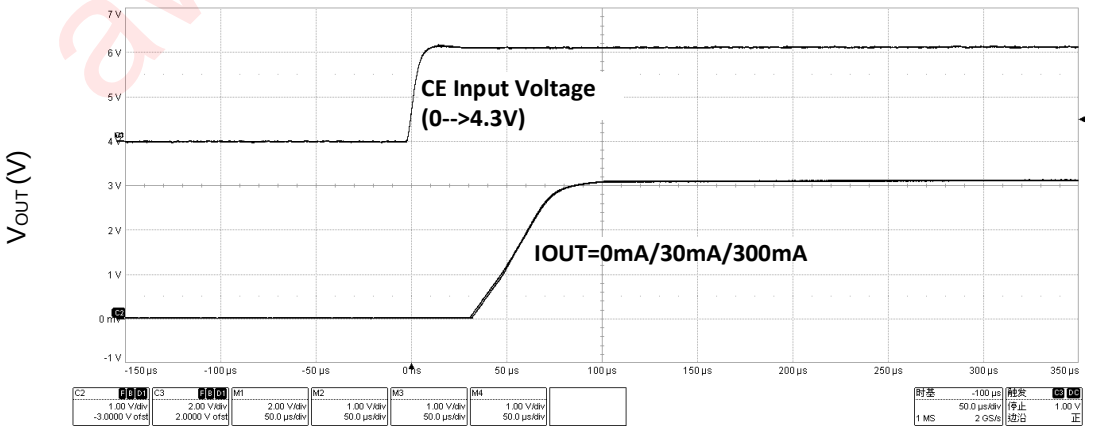
Turn On Speed with CE pin

AW3705D180DNR



Turn On Speed with CE pin

AW3705D330DNR

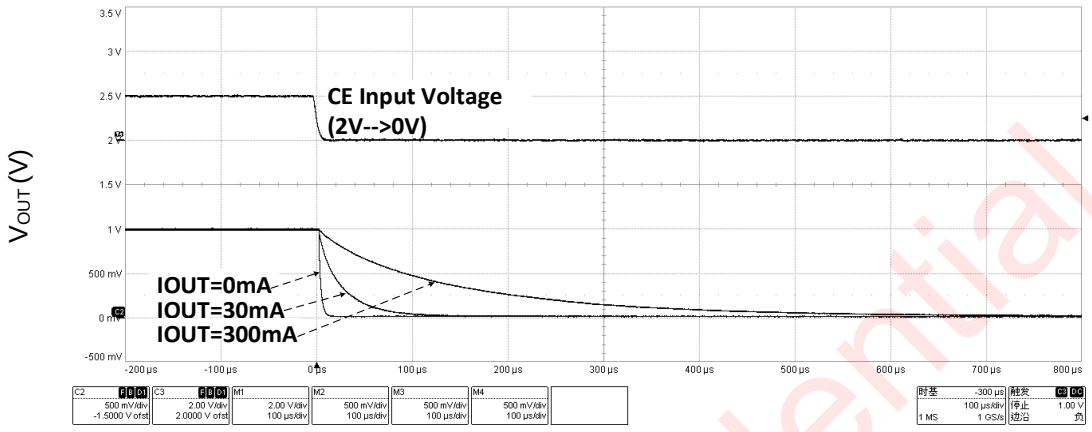


Turn On Speed with CE pin

Typical Characteristics (Continued)

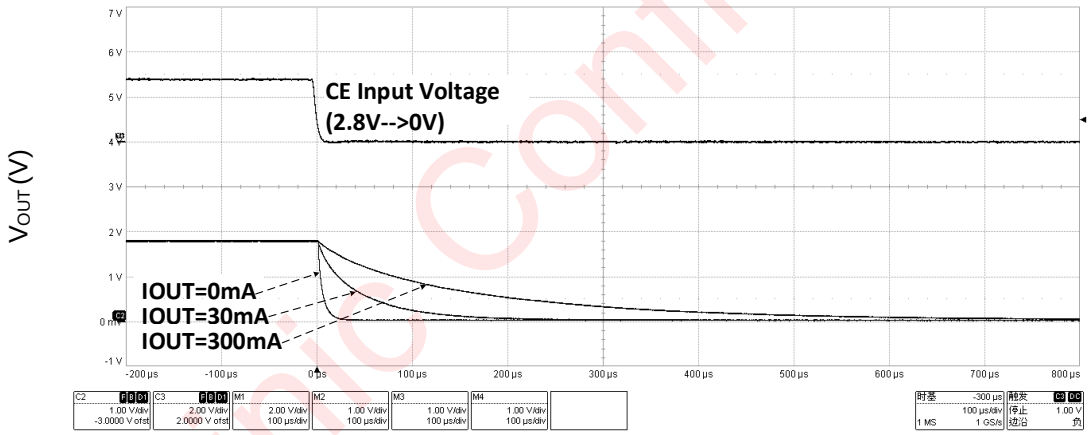
V_{IN}=$V_{OUT(SET)}$+1V, V_{CE}>1.2V , I_{OUT}=1mA , C_{IN}=C_{OUT}=1μF, T_A=25°C, In Typical Application Circuit , unless other noted.

AW3705D100DNR



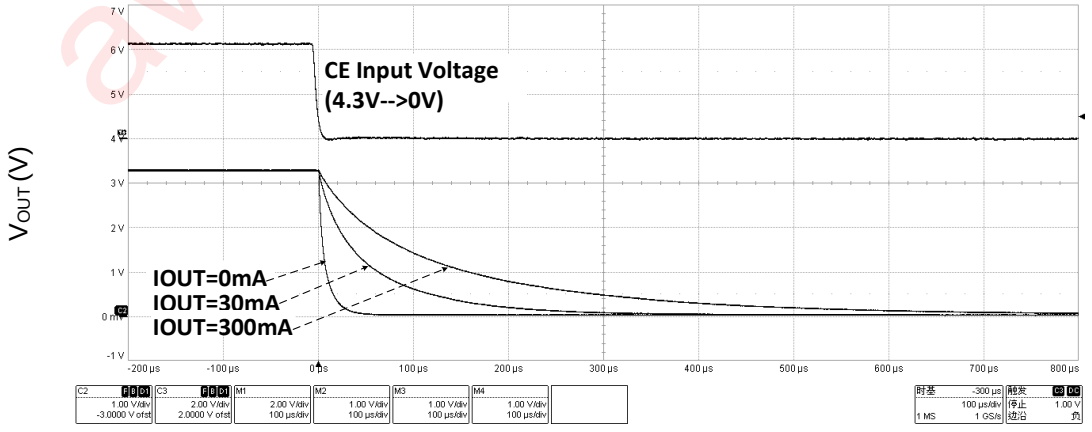
Turn Off Speed with CE pin

AW3705D180DNR



Turn Off Speed with CE pin

AW3705D330DNR



Turn Off Speed with CE pin

Detailed Functional Description

AW3705DXXX is a low dropout voltage regulator. After powered on, with CE pin assertion, feedback voltage signal from the integrated resistor network and a voltage related to the voltage reference are transmit to positive input terminal and negative input terminal of an error amplifier (EA) respectively. The output signal of EA is used to control the open-state of power MOSFET. After soft-start, feedback voltage signal compares with the established reference voltage, making output voltage stable and accurate. AW3705DXXX integrates function of adaptive dynamic bias compensation. It means, as load current increases, bias currents for EA also increase, making LDO obtain excellent dynamic response performance.

Enable Operation

AW3705DXXX uses CE pin to realize enable operation. Applying proper value of voltage to CE pin can make IC enable/disable.

If the voltage of CE pin is less than 0.4V, AW3705DXXX is guaranteed to be disabled. In this state, function modules of IC and power MOSFET are turned off. And the auto discharge function is open making output discharge through a 160Ω resistor to Ground. In disable state, AW3705DXXX only consumes a typical 10nA current.

If the voltage of CE pin is more than 1.2V, AW3705DXXX is guaranteed to be enabled. In this state, the auto discharge MOSFET is closed, and AW3705DXXX regulates output voltage to the designed value of voltage.

A 4MΩ resistor to Ground is built-in at CE pin, making sure that the IC is disabled when CE pin floats. If Enable function is not required, CE pin should be connected directly to IN pin.

Output Current Limit

AW3705DXXX integrates output current limit function, protecting IC from excessive current.

When the load is excessively heavy, AW3705DXXX limits the current flowing through the IC to a typical 800mA current. This value is specially designed, so that IC is protected properly and the output capability of 500mA is not influenced either.

Meanwhile, AW3705DXXX integrates fold-back current limit function, lowering the system dissipation when output overload or short to Ground.

Thermal Shutdown

AW3705DXXX integrates thermal shutdown function, protect IC from excessively high temperature.

When the chip temperature exceeds 150°C, AW3705DXXX detects it as an over-temperature event, triggering thermal shutdown, which will turn off the main function module, including power MOSFET. This inhibits increase of chip's temperature. IC would keep the protection-state on until the chip's temperature falls below to 130°C. At this moment, the over-temperature protection-state is released, IC resumes to work again.The hysteresis avoids IC's turning off and on frequently around the the Thermal Shutdown threshold.

Auto Discharge

AW3705DXXX makes output voltage decrease quickly when in disable state or thermal shutdown state, benefit from integrating auto discharge function.

Application Information

Capacitors Selection

IN pin: Input Capacitor C_{IN}

AW3705DXXX advises to use a 1μF or more X5R or X7R ceramic capacitor at IN pin as shown in Typical Application Circuit.

OUT pin: Output Capacitor C_{OUT}

AW3705DXXX advises to use a 1μF or more X5R or X7R ceramic capacitor at OUT pin as shown in Typical Application Circuit.

NOTE: For the application with fast load transient, capacitance of the input capacitor is recommended to be equal or larger to the sum of the capacitance at the output node for the best load transient performance.

Recommended Components List

Component	PART No.	DESCRIPTION	MFR	TYP.	UNIT
C_{IN}	GRM155R61A105KE15	10V, X5R, 0402	MURATA	1	μF
C_{OUT}	GRM155R61A105KE15	10V, X5R, 0402	MURATA	1	μF

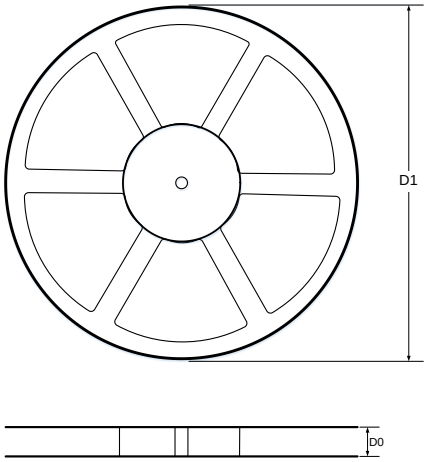
PCB Layout Consideration

To obtain the optimal performance, guidelines below for PCB layout of AW3705DXXX should be obeyed:

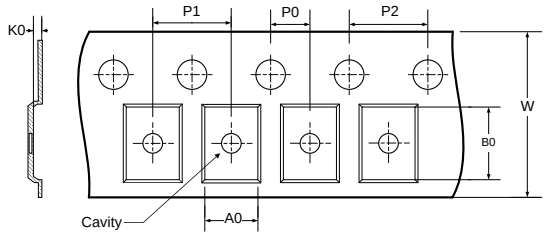
1. All peripheral components should be placed as close to the chip as possible. C_{IN} and C_{OUT} should be close to IN and OUT pins respectively. Avoid connecting device and chip pins with two different layers of copper, use the same layer of copper instead.
2. IN and OUT pin are the large current input and output of the chip, make IN, OUT, and meanwhile GND lines sufficient.
3. The connection lines between the planes of C_{IN} or C_{OUT} and respective chip pin should be as short and wide as possible, to reduce noise and EMI interference.
4. The exposed plane of chip and GND pins must be connected to the large-area ground layer of PCB directly, meanwhile place sufficient vias below the exposed plane. Thus we can decrease the thermal resistor on the board to optimize heat-diffusion performance.

Tape And Reel Information

REEL DIMENSIONS

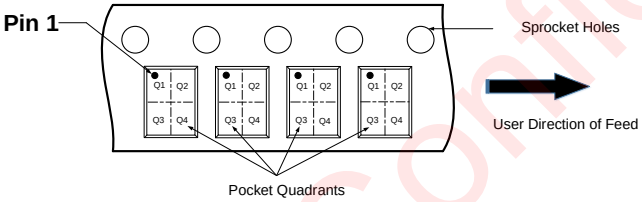


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

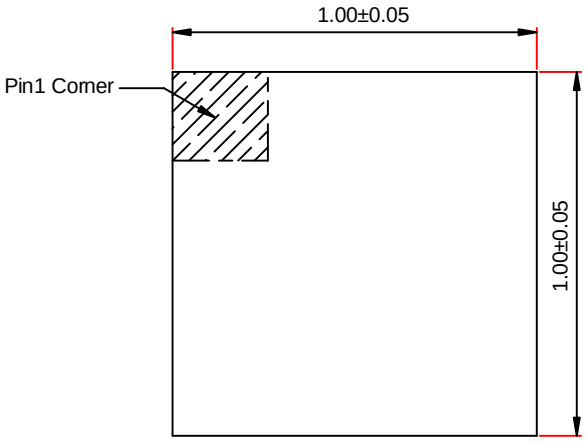


DIMENSIONS AND PIN1 ORIENTATION

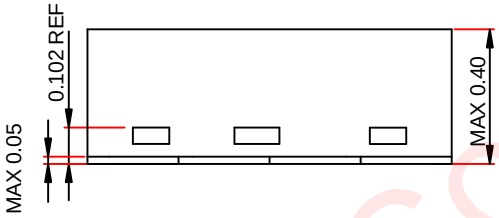
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	1.14	1.17	0.56	2	4	4	8	Q1

All dimensions are nominal

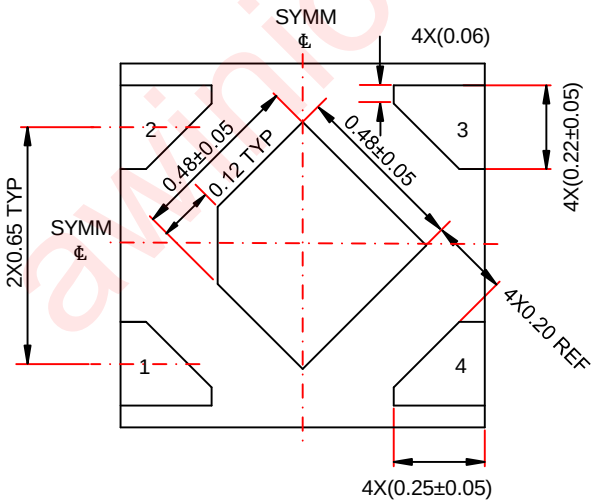
Package Description



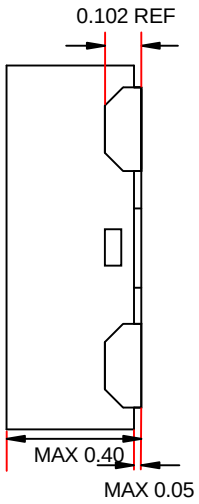
Top View



Side View



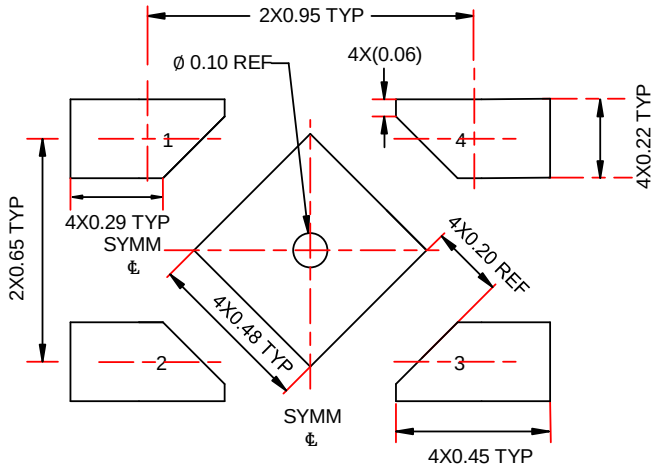
Bottom View

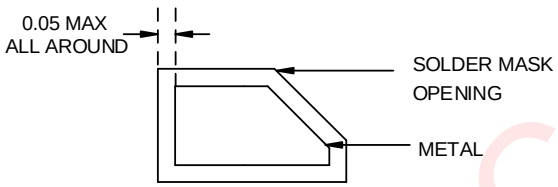


Side View

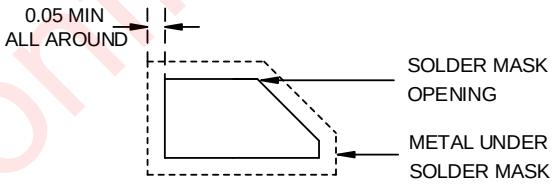
Unit:mm

Land Pattern Data





NON SOLDER MASK DEFINED



SOLDER MASK DEFINED

UNIT : mm

Revision History

Version	Date	Change Record
V1.0	Sept 2018	Officially released

Disclaimer

All trademarks are the property of their respective owners. Information in this document is believed to be accurate and reliable. However, Shanghai AWINIC Technology Co., Ltd (AWINIC Technology) does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

AWINIC Technology reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. Customers shall obtain the latest relevant information before placing orders and shall verify that such information is current and complete. This document supersedes and replaces all information supplied prior to the publication hereof.

AWINIC Technology products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an AWINIC Technology product can reasonably be expected to result in personal injury, death or severe property or environmental damage. AWINIC Technology accepts no liability for inclusion and/or use of AWINIC Technology products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications that are described herein for any of these products are for illustrative purposes only. AWINIC Technology makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

All products are sold subject to the general terms and conditions of commercial sale supplied at the time of order acknowledgement.

Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Reproduction of AWINIC information in AWINIC data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. AWINIC is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of AWINIC components or services with statements different from or beyond the parameters stated by AWINIC for that component or service voids all express and any implied warranties for the associated AWINIC component or service and is an unfair and deceptive business practice. AWINIC is not responsible or liable for any such statements.

