0.1-6GHz DPDT Antenna Cross Switch

Features

- Broadband frequency range: 0.1 to 6.0GHz
- Wide VDD range: 1.65V to 3.3V
- GPIO interface for 1.0V to VDD positive control voltage
- Low insertion loss: 0.35dB typical @ 2.7GHz
- Max input RF power of 39dBm
- Excellent linearity and harmonic performance
- No DC blocking capacitors in typical application
- Small FCLGA (1.1mm x 1.5mm x 0.47 mm -10L) package

Applications

- Cellular 2G/3G/4G/5G TRX
- Antenna switching
- Other RF front-end modules

General Description

The AW12022FLR is a Silicon-On-Insulator(SOI) DPDT switch with low insertion loss and high Isolation. It can be used to support band switching and mode switching for cellular 4G/5G, data cards and tablets.

The symmetrical design of internal ports makes it convenient for PCB routing and adjustment of receiving and transmitting signals. The band/mode switching is realized by the GPIO pin as referenced in the chip block diagram and the control logic. The chip allows power-supply voltages from 1.65V to 3.3V and the positive control voltages from 1V to VDD.

The AW12022FLR is provided in a compact FCLGA 1.1mm x 1.5mm x 0.47mm -10L package.
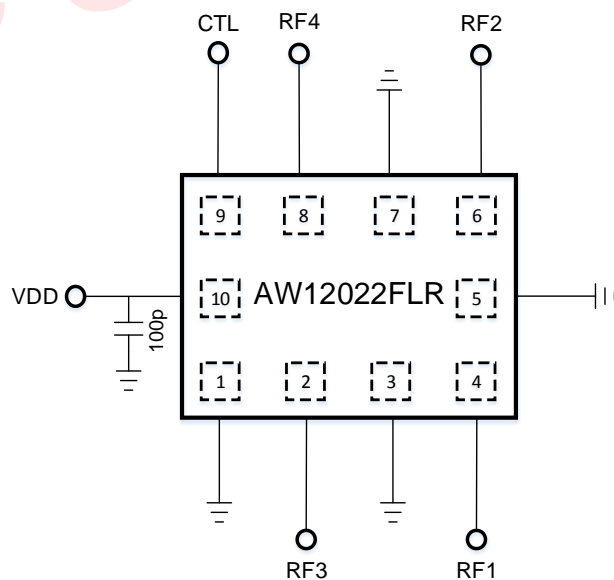
Typical Application Circuit

Figure 1　Typical Application Circuit Of AW12022FLR

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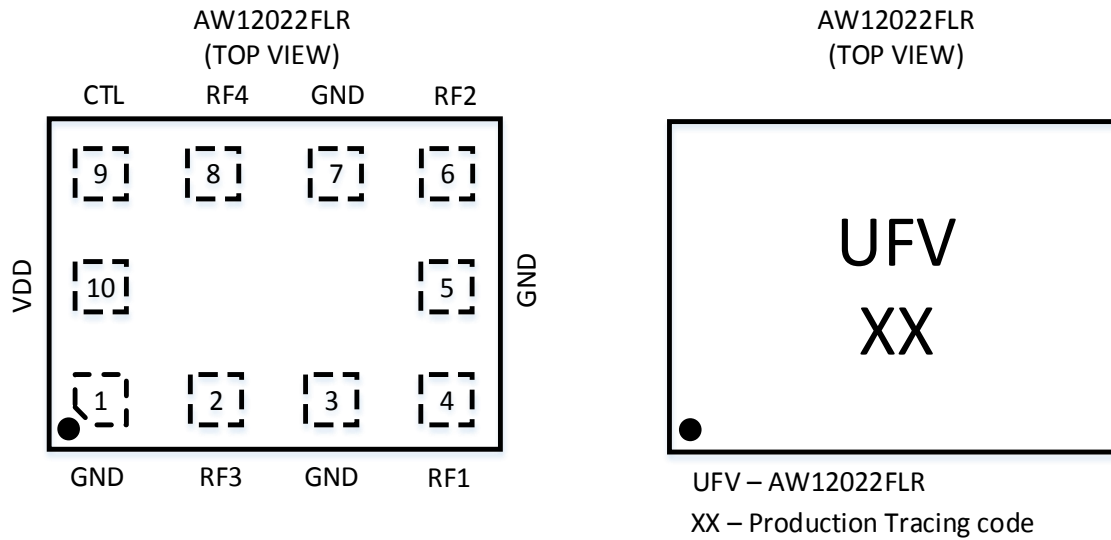
Pin Configuration And Top Mark

AW12022FLR
(TOP VIEW)

AW12022FLR
(TOP VIEW)

UFV
XX

UFV – AW12022FLR

XX – Production Tracing code

Figure 2   Pin Configuration And Top Mark

Pin Definition

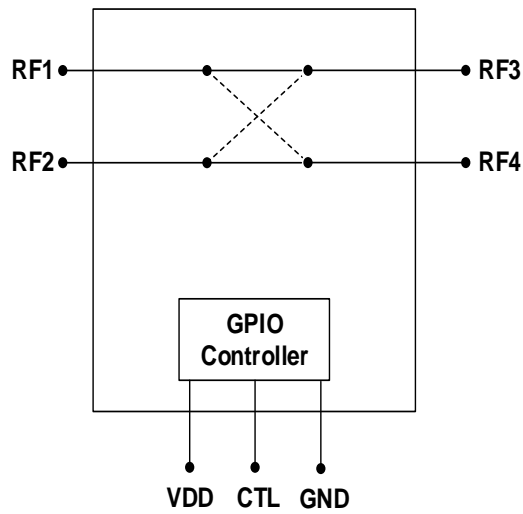| No.	NAME	DESCRIPTION
1	GND	Ground
2	RF3	RF I/O path 3
3	GND	Ground
4	RF1	RF I/O path 1
5	GND	Ground
6	RF2	RF I/O path 2
7	GND	Ground
8	RF4	RF I/O path 4
9	CTL	DC control voltage
10	VDD	DC power supply

Functional Block Diagram

Figure 3   Functional Block Diagram

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW12022FLR	-40°C～85°C	FCLGA 1.1mm x 1.5mm x 0.47 mm -10L	UFV	MSL3	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS		RANGE
Supply Voltage Range VDD		1.65V to 3.3V
Control Voltage Range	CTL	0V to 3.3V
RF input power		39.3dBm
Operating Free-air Temperature Range		-40°C to 85°C
Storage Temperature T_{STG}		-65°C to 150°C
Lead Temperature (Soldering 10 Seconds)		260°C
ESD (NOTE 2)		
HBM (ESDA/JEDEC JS-001)		±1000V
CDM (ESDA/JEDEC JS-002)		±500V

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

Test method: ESDA/JEDEC JS-001

Electrical Characteristics

VDD=1.8V, CTL=0/1.8V, PIN=0dBm, T_A =+25℃, Z_0=50Ω. (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DC Specifications						
VDD	Supply Voltage			1.8		V
IDD	Supply Current	VDD=1.8V		45		μA
IDD	Supply Current	VDD=2.8V		85		μA
VCTL_H VCTL_L	Control Voltage High Low			1.8 0		V
ICTL	Control Current	VCTL = 1.8V		0.1		μA
t_{ON}	Turn-on Switching Time	50% of final control voltage to 90% of final RF power		2		μs
RF Specifications						
IL	Insertion loss	699-960MHz 1710-2200MHz 2300-2690MHz 3300-4200MHz 4400-5000MHz 5150-5925MHz		0.27 0.31 0.35 0.41 0.49 0.57		dB dB dB dB dB dB
ISO	Isolation	699-960MHz 1710-2200MHz 2300-2690MHz 3300-4200MHz 4400-5000MHz 5150-5925MHz		33 25 22 20 18 17		dB dB dB dB dB dB
VSWR	Voltage Standing Wave Ratio	699-960MHz 1710-2200MHz 2300-2690MHz 3300-4200MHz 4400-5000MHz 5150-5925MHz		1.06 1.1 1.1 1.2 1.2 1.3		:1 :1 :1 :1 :1 :1
H2	Second Harmonics	35dBm, GSM LB, CW		-72		dBm
H2	Second Harmonics	33dBm, GSM HB, CW		-70		dBm
H3	Third Harmonics	35dBm, GSM LB, CW		-58		dBm
H3	Third Harmonics	33dBm, GSM HB, CW		-61		dBm
$P_{0.1dB}$	0.1dB Compression Point	0.1GHz–6GHz		39		dBm
IIP3	3rd Order Input Intercept Point	F1=2535MHz, 20dBm F2=2415MHz, -15dBm F0=2655MHz		81		dBm

Timing Diagram (Power ON And OFF Sequence)

It is very important that the user adheres to the correct power-on/off sequence in order to avoid damaging the device. The control signal CTL should be set to 0V unless VDD is set in the operating voltage range.

Power ON:
1) Apply voltage supply --- VDD
2) Set Controls---CTL
3) Apply RF input

Change switch position from one RF port to another:
1) Remove RF input
2) Change control voltages CTL to set the switch to desired RF port
3) Apply RF input

Power OFF:
1) Remove RF input
2) Remove control voltages-CTL
3) Remove VDD input

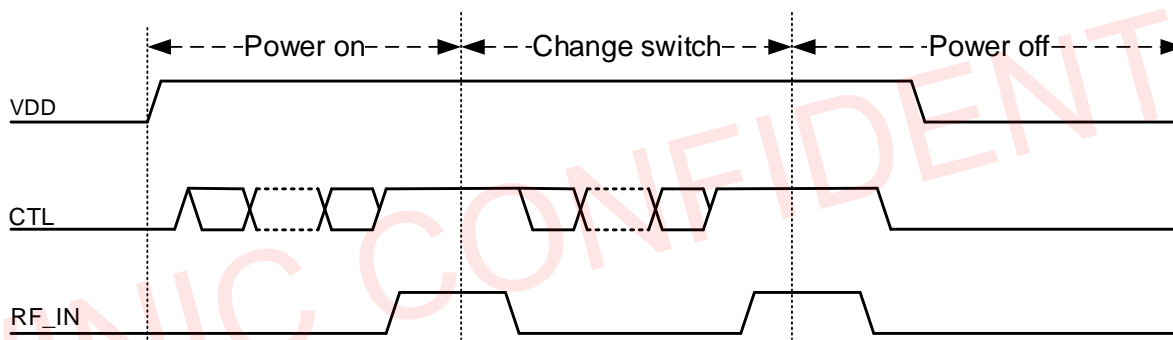**Figure 4   Power On/Change Switch/Power Off Sequence**

AW12022FLR Control Logic

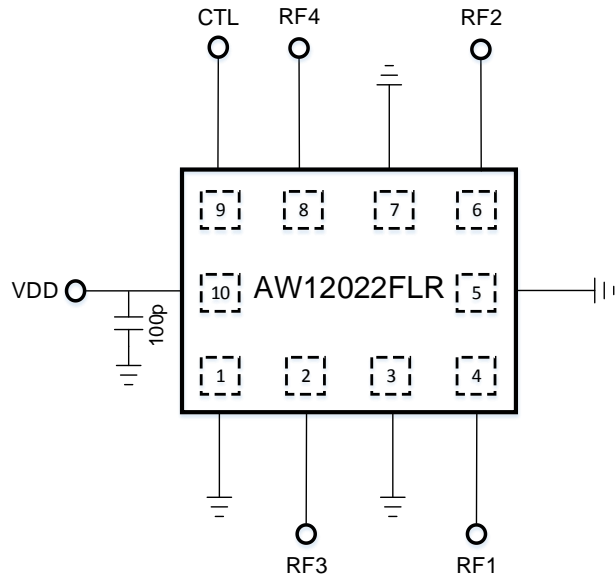| State	Active Path	CTL
1	RF1 to RF4; RF2 to RF3	1
0	RF2 to RF4; RF1 to RF3	0

Application Circuits

Figure 5   AW12022FLR EVB Schematic

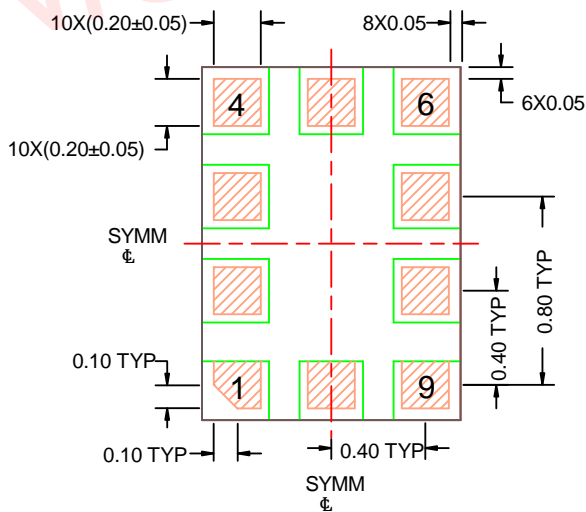## Package Outline Dimensions

1.10±0.05

Pin1 Corner

1.50±0.05

TOP VIEW

0.47±0.05

0.31 REF

0.16±0.04

SIDE VIEW

10X(0.20±0.05)

8X0.05

6X0.05

10X(0.20±0.05)

| 4 | | 6 |

SYMM ℄

0.80 TYP

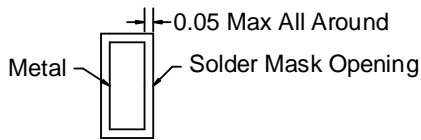0.40 TYP

0.10 TYP

| 1 | | 9 |

0.10 TYP

0.40 TYP

SYMM ℄
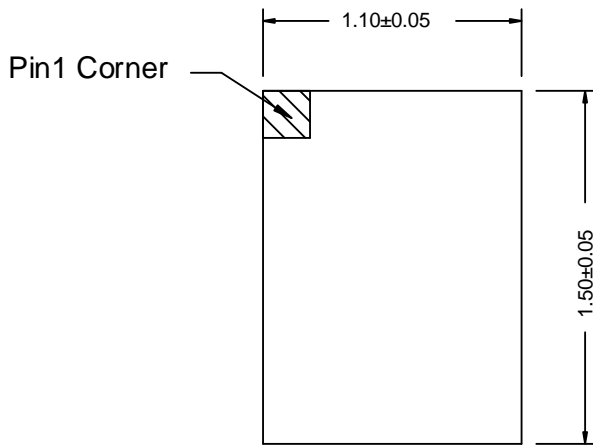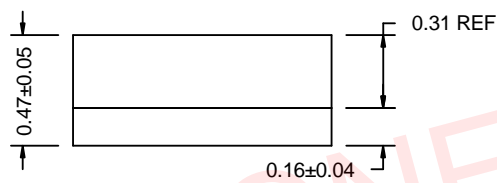
☐ Solder mask opening

▨ LGA pad

Unit: mm

BOTTOM VIEW

Land Pattern Data

1.00 REF

| 1 | 10 | 9 |

0.40 TYP

SYMM ℄

1.40 REF

10X0.20 TYP

| 4 | 5 | 6 |

0.40 TYP

SYMM ℄

10X0.20 TYP

0.05 Max All Around

Metal — Solder Mask Opening

Non-solder Mask Defined

0.05 Min All Around

Metal Under Solder Mask
Solder Mask Opening
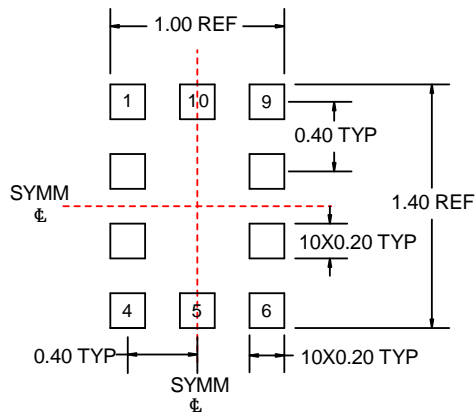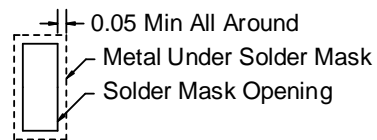
Solder Mask Defined

Unit: mm

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shanghai awinic technology co., ltd.

Tape And Reel Information

REEL DIMENSIONS

TAPE DIMENSIONS

A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
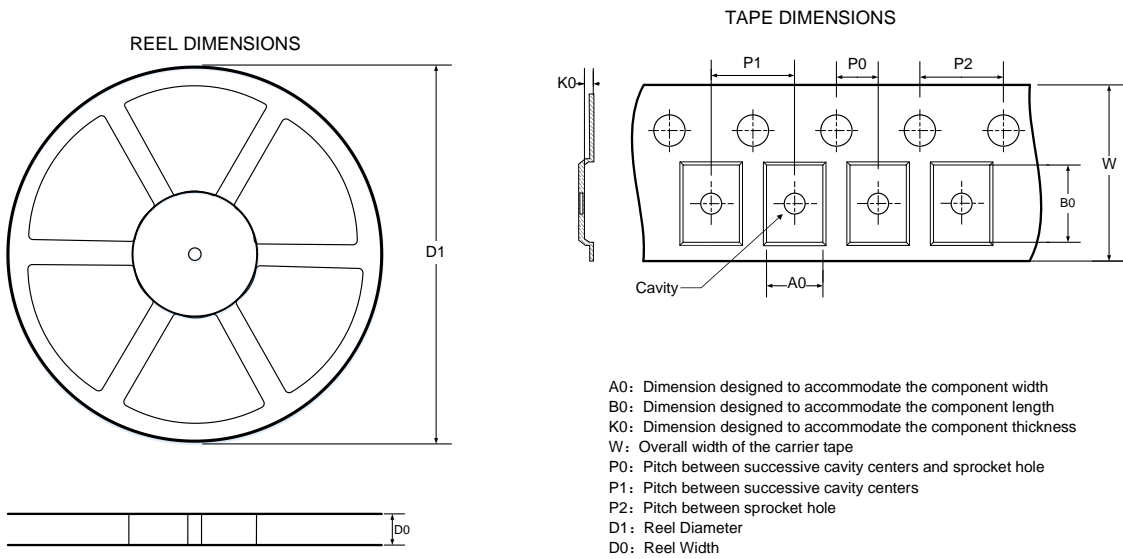K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Pin 1

Sprocket Holes

User Direction of Feed

Pocket Quadrants
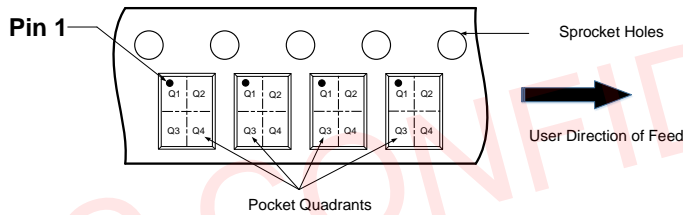
DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
180	9.5	1.3	1.7	0.6	2	4	4	8	Q1

All dimensions are nominal

Revision History

Version	Date	Change Record
V0.9	May 2020	Officially Released
V1.0	Jul. 2020	Update electrical characteristics
V1.1	Jul. 2020	Update electrical characteristics

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