

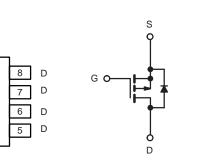
# P-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY						
V <sub>DS</sub> (V)	$R_{DS(on)}\left(\Omega\right)$	I <sub>D</sub> (A) <sup>d</sup>	Q <sub>g</sub> (Typ.)			
- 30	0.0125 at V <sub>GS</sub> = - 10 V	- 11.6	22 nC			
	$0.0180$ at $V_{GS} = -4.5 \text{ V}$	- 10	22 110			

SO-8

Top View

S



#### P-Channel MOSFET

#### **FEATURES**

- Halogen-free According to IEC 61249-2-21 **Available**
- TrenchFET® Power MOSFET
- 100 % R<sub>g</sub> Tested
  100 % UIS Tested

## COMPLIANT HALOGEN **FREE**

#### **APPLICATIONS**

- · Load Switches
  - Notebook PCs
  - Desktop PCs

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V <sub>DS</sub>	- 30	V	
Gate-Source Voltage		V <sub>GS</sub>	± 20	v
	T <sub>C</sub> = 25 °C		- 11.6	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	T <sub>C</sub> = 70 °C		- 10.5	
Continuous Diam Current (1) = 150 °C)	T <sub>A</sub> = 25 °C	l lo	- 8.7 <sup>a, b</sup>	
	T <sub>A</sub> = 70 °C		- 7.7 <sup>a, b</sup>	A
Pulsed Drain Current		I <sub>DM</sub>	- 40	A
Continuous Source Drain Diada Current	T <sub>C</sub> = 25 °C	I-	- 4.6	
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	I <sub>S</sub>	2.0 <sup>a, b</sup>	
Avalanche Current	1 04 11	I <sub>AS</sub>	- 20	
Single-Pulse Avalanche Energy	L = 0.1 mH	E <sub>AS</sub>	20	mJ
	T <sub>C</sub> = 25 °C		5.6	
Maximum Davian Dissination	T <sub>C</sub> = 70 °C	D .	3.6	w
Maximum Power Dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	2.5 <sup>a, b</sup>	VV
	T <sub>A</sub> = 70 °C		1.6 <sup>a, b</sup>	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>a, c</sup>	t ≤ 10 s	R <sub>thJA</sub>	39	50	°C/W	
Maximum Junction-to-Foot	Steady State	R <sub>thJF</sub>	18	22		

- a. Surface mounted on 1" x 1" FR4 board.
- b. t = 10 s.
- c. Maximum under Steady State conditions is 85 °C/W. d. Based on  $T_{\rm C}$  = 25 °C.



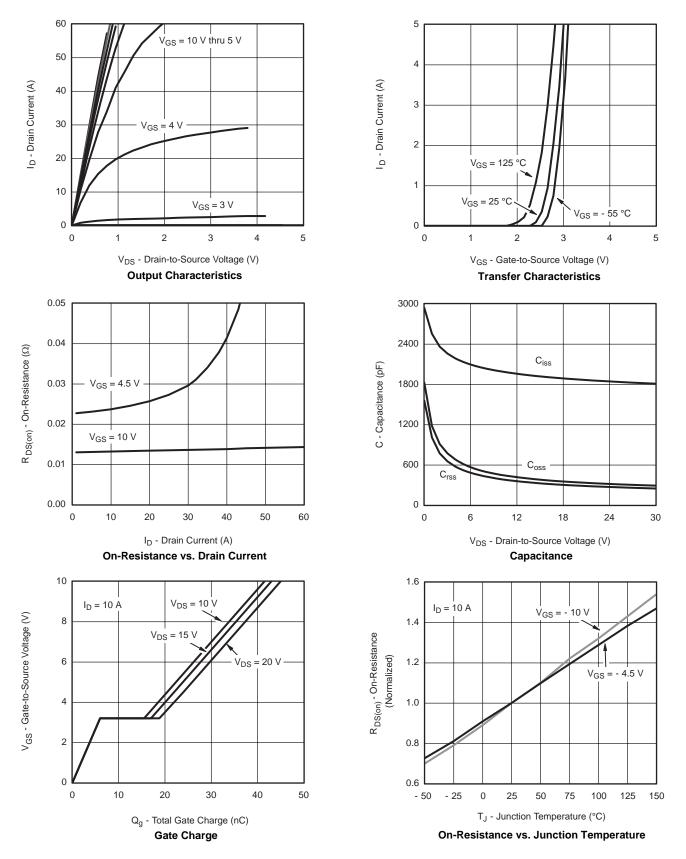
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	- 30			V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$			- 31		m\//9C	
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	,		5.5		mV/°C	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	- 1.0		- 3.0	V	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 25 \text{ V}$			± 100	nA	
Zoro Coto Voltago Proin Current	I <sub>DSS</sub>	V <sub>DS</sub> = - 30 V, V <sub>GS</sub> = 0 V			- 1	μА	
Zero Gate Voltage Drain Current		V <sub>DS</sub> = - 30 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			- 5		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge -10 \text{ V}, V_{GS} = -10 \text{ V}$	- 30			Α	
Davis Ossans Os Otata Basista and	Б	V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 10 A		0.011	0.0125		
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 7 A		0.012	0.018	Ω	
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = - 10 V, I <sub>D</sub> = - 10 A		23		S	
Dynamic <sup>b</sup>							
Input Capacitance	C <sub>iss</sub>			1960		pF	
Output Capacitance	C <sub>oss</sub>	$V_{DS} = -15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		380			
Reverse Transfer Capacitance	C <sub>rss</sub>			325			
Tatal Cata Channa	$Q_g$ $V_{DS} = -15 \text{ V}, V_{GS} = -10 \text{ V}, I_D = -10 \text{ A}$	$V_{DS} = -15 \text{ V}, V_{GS} = -10 \text{ V}, I_{D} = -10 \text{ A}$		43	65		
Total Gate Charge			22	33	nC		
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS} = -15 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -10 \text{ A}$		6		nC	
Gate-Drain Charge	$Q_{gd}$			11			
Gate Resistance	$R_g$	f = 1 MHz	0.3	1.3	2.5	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			11	22		
Rise Time	t <sub>r</sub>	$V_{DD}$ = - 15 V, $R_L$ = 3 $\Omega$		13	25		
Turn-Off DelayTime	t <sub>d(off)</sub>	$I_D \cong -5 \text{ A}, V_{GEN} = -10 \text{ V}, R_g = 1 \Omega$		32	50		
Fall Time	t <sub>f</sub>			9	18	ne	
Turn-On Delay Time	t <sub>d(on)</sub>			44	70	ns	
Rise Time	t <sub>r</sub>	$V_{DD}$ = - 15 V, $R_L$ = 3 $\Omega$		100	160		
Turn-Off DelayTime	t <sub>d(off)</sub>	$I_D \cong$ - 5 A, $V_{GEN}$ = - 4.5 V, $R_g$ = 1 $\Omega$		28	50		
Fall Time	t <sub>f</sub>			15	30		
Drain-Source Body Diode Characterist	ics						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			- 4.6	۸	
Pulse Diode Forward Current	I <sub>SM</sub>				- 50	Α	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = - 2 A, V <sub>GS</sub> = 0 V		- 0.75	- 1.2	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>			28	45	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	I = 2 A dl/dt = 100 A/vo T = 25 °C		20	40	nC	
Reverse Recovery Fall Time	t <sub>a</sub>	$I_F = -2 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 \text{ °C}$		13		20	
Reverse Recovery Rise Time	t <sub>b</sub>	]		15		ns	

#### Notes:

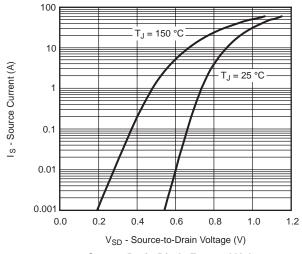
- a. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

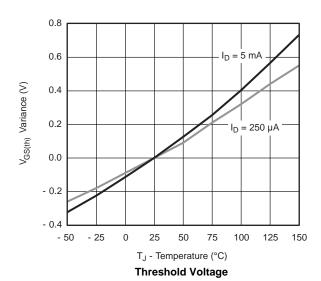


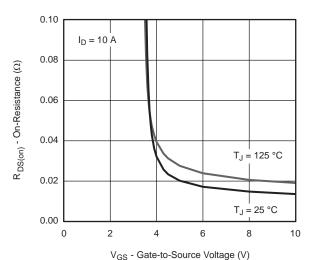




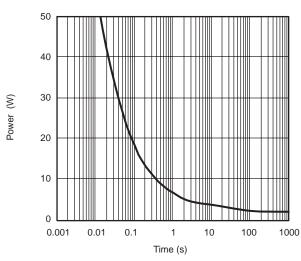


#### Source-Drain Diode Forward Voltage

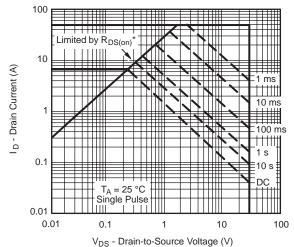




On-Resistance vs. Gate-to-Source Voltage



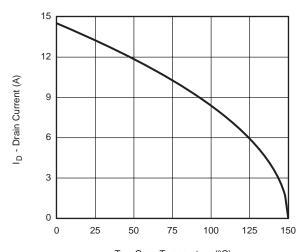
Single Pulse Power, Junction-to-Ambient



\* V<sub>GS</sub> > minimum V<sub>GS</sub> at which R<sub>DS(on)</sub> is specified

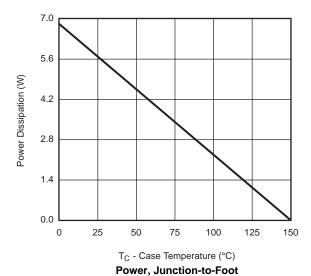
Safe Operating Area

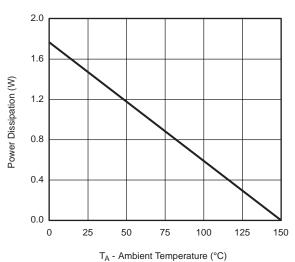




 $T_{\mbox{\scriptsize C}}$  - Case Temperature (°C)

#### **Current Derating\***

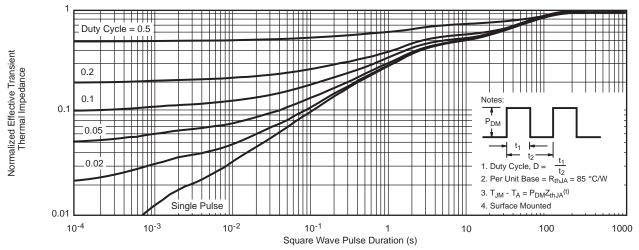




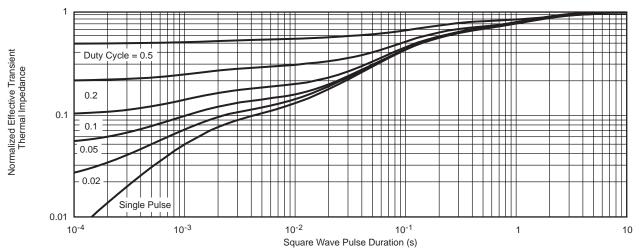
Power Derating, Junction-to-Ambient

<sup>\*</sup> The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package





Normalized Thermal Transient Impedance, Junction-to-Ambient

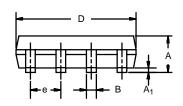


Normalized Thermal Transient Impedance, Junction-to-Foot



**SOIC (NARROW): 8-LEAD**JEDEC Part Number: MS-012







	MILLIM	IETERS	INCHES			
DIM	Min	Max	Min	Max		
Α	1.35	1.75	0.053	0.069		
A <sub>1</sub>	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
E	3.80	4.00	0.150	0.157		
е	1.27	1.27 BSC		0.050 BSC		
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
FCN: C-06527-Rev I 11-Sen-06						

ECN: C-06527-Rev. I, 11-Sep-06

DWG: 5498



### **RECOMMENDED MINIMUM PADS FOR SO-8**



Recommended Minimum Pads Dimensions in Inches/(mm)

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