

## Low-Power DC to 150 MHz 1:9 Fanout Buffer IC

### Features

- 1:9 LVCMOS Output Fanout Buffer from DC to 150 MHz
- Low Additive Phase Jitter of 60 fs RMS
- 8 mA Output Drive Strength
- Low Power Consumption for Portable Applications
- Low Input-Output Delay
- Output-Output Skew <250 ps
- 2.5V to 3.3V,  $\pm 10\%$  Operation
- 1.8V  $\pm 5\%$  Operation up to 67 MHz
- Operating Temperature Range:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C
- Available in 16-Pin QFN Package

### General Description

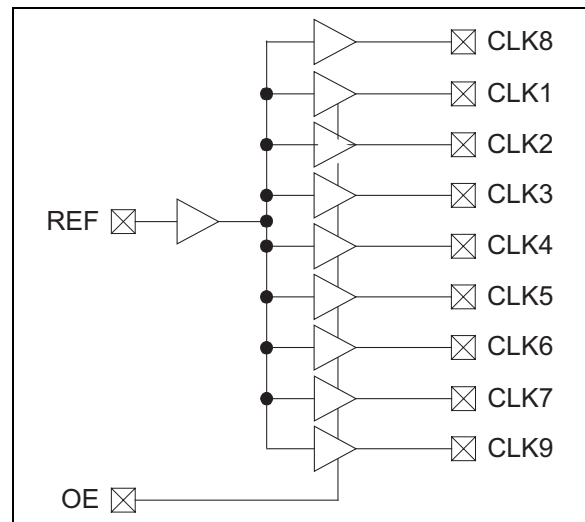
The PL133-97 is an advanced fanout buffer designed for high performance, low-power, small form factor applications. The PL133-97 accepts a reference clock input from DC to 150 MHz and provides nine outputs of the same frequency.

The PL133-97 is offered in a small 3 mm x 3 mm QFN-16L package and it offers the best phase noise, additive jitter performance, and lowest power consumption of any comparable IC.

The PL133-97 outputs can be disabled to a high impedance (tri-state) by pulling low the OE pin. When the OE pin is high, the outputs are enabled and follow the REF input signal. When the OE pin is left open, a pull-up resistor on the chip will default the OE pin to logic 1 so the outputs are enabled.

CLK8 is a free running output that remains enabled when the OE pin is pulled low.

### Functional Block Diagram



# PL133-97

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

Supply Voltage to Ground Potential .....	-0.5V to +4.6V
DC Input Voltage .....	$V_{SS} - 0.5V$ to +4.6V
Static Discharge Voltage (Per MIL-STD-883, Method 3015).....	>2000V

### Operating Ratings †

Supply Voltage, $V_{DD}$ .....	1.71V to 3.63V
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† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

### Electrical Characteristics:

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Low Voltage	$V_{IL}$	—	—	$0.3 \times V_{DD}$	V	Note 1
Input High Voltage	$V_{IH}$	$0.7 \times V_{DD}$	—	—	V	Note 1
Input Low Current	$I_{IL}$	—	—	50	$\mu A$	$V_{IN} = 0V$
Input High Current	$I_{IH}$	—	—	100	$\mu A$	$V_{IN} = V_{DD}$
Supply Current	$I_{DD}$	—	—	32	mA	66.67 MHz with unloaded outputs
Output Low Voltage	$V_{OL}$	—	—	0.5	V	$I_O = 8 \text{ mA}, V_{DD} = 3.3V$
		—	—	0.5		$I_O = 6 \text{ mA}, V_{DD} = 2.5V$
		—	—	0.5		$I_O = 4 \text{ mA}, V_{DD} = 1.8V$
Output High Voltage	$V_{OH}$	$V_{DD} - 0.5$	—	—	V	$I_O = -8 \text{ mA}, V_{DD} = 3.3V$
		$V_{DD} - 0.5$	—	—		$I_O = -6 \text{ mA}, V_{DD} = 2.5V$
		$V_{DD} - 0.5$	—	—		$I_O = -4 \text{ mA}, V_{DD} = 1.8V$
OE Pin Pull-Up Resistance	$R_{PU}$	—	120	—	k $\Omega$	—
Load Capacitance	$C_L$	—	—	30	pF	Load Capacitance, below 100 MHz, $V_{DD} > 2.25V$
		—	—	10		Load Capacitance between 100 MHz and 134 MHz, $V_{DD} > 2.25V$
		—	—	5		Load Capacitance, above 134 MHz, $V_{DD} > 2.25V$
		—	—	15		Load Capacitance, below 67 MHz, $1.71V < V_{DD} < 2.25V$
Input Capacitance	$C_{IN}$	—	—	7	pF	—
Power-Up Time	$t_{PU}$	0.05	—	50	ms	Power-up time for all $V_{DD}$ to reach minimum specified voltage (power ramps must be monotonic)

**Note 1:** REF input has a threshold voltage of  $V_{DD}/2$ .

## SWITCHING CHARACTERISTICS [Note 2](#)

### Electrical Characteristics:

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Operating Frequency	f	DC	—	160	MHz	$V_{DD} = 3.3V, 2.5V$
		DC	—	67	MHz	$V_{DD} = 1.8V$
Duty Cycle = $t_2 \div t_1$	—	40	50	60	%	Measured at $V_{DD}/2$ , Input = 50%
Rise Time	$t_3$	—	—	1.5	ns	Measured between 0.8V and 2.0V
Fall Time	$t_4$	—	—	1.5	ns	Measured between 0.8V and 2.0V
Output to Output Skew <a href="#">Note 1</a>	$t_5$	—	—	250	ps	All outputs equally loaded
Propagation Delay, REF Rising Edge to CLKX Rising Edge <a href="#">Note 1</a>	$t_6$	1	5	9.2	ns	Measured at $V_{DD}/2$

**Note 1:** Parameter is guaranteed by design and characterization.

**2:** All parameters are specified with loaded outputs.

## NOISE CHARACTERISTICS

### Electrical Characteristics:

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Additive Phase Jitter	—	—	60	—	fs	$V_{DD} = 3.3V$ , Frequency = 100 MHz Integration range 12 kHz - 20 MHz

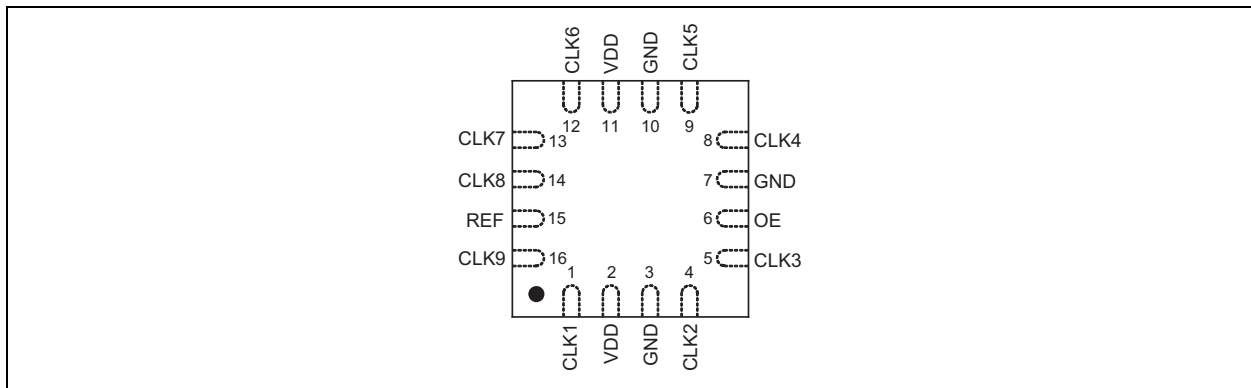
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## TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
<b>Temperature Ranges</b>						
Ambient Operating Temperature ( $T_A$ )	$T_A$	0	—	+70	°C	Commercial
		-40	—	+85		Industrial
Junction Temperature	$T_J$	—	—	+150	°C	—
Storage Temperature Range	$T_S$	-65	—	+150	°C	—
<b>Package Thermal Resistance</b>						
16-Lead QFN	$R_{\theta JA}$	—	82.5	—	°C/W	—

**Note 1:** The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e.,  $T_A$ ,  $T_J$ ,  $\theta_{JA}$ ). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +150°C rating. Sustained junction temperatures above +150°C can impact the device reliability.

## 2.0 PIN DESCRIPTIONS



**FIGURE 2-1:** Pin Configuration, 16-Lead QFN Package.

The descriptions of the pins are listed in [Table 2-1](#).

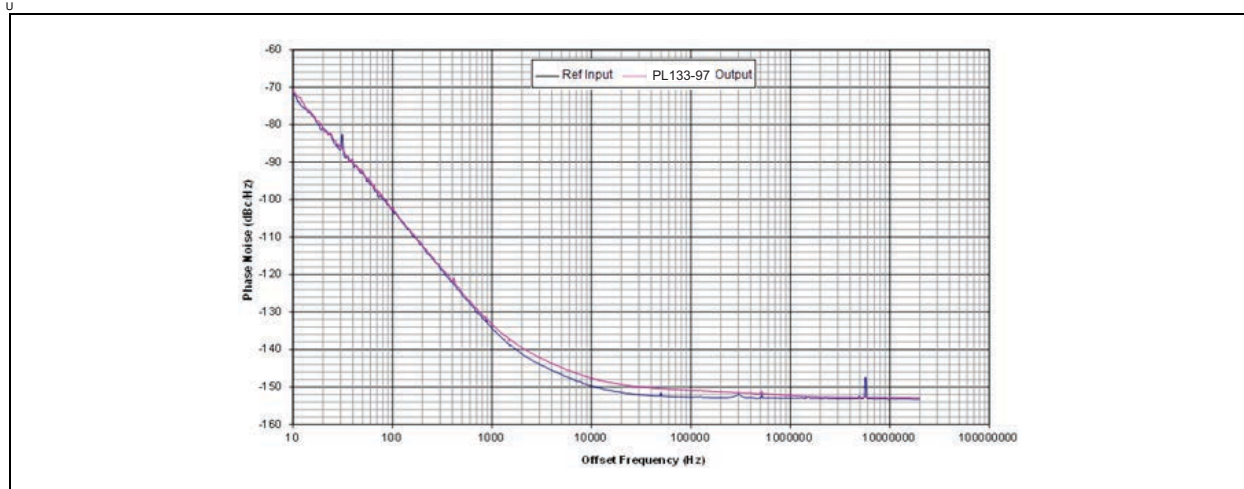
**TABLE 2-1: PIN FUNCTION TABLE**

Pin Number	P8in Name	Type	Description
15	REF	I	Input reference frequency
1	CLK1	O	Buffered clock output
4	CLK2	O	Buffered clock output
5	CLK3	O	Buffered clock output
8	CLK4	O	Buffered clock output
9	CLK5	O	Buffered clock output
12	CLK6	O	Buffered clock output
13	CLK7	O	Buffered clock output
14	CLK8	O	Buffered clock output, free running, does not disable with OE
16	CLK9	O	Buffered clock output
2, 11	VDD	P	VDD connection
3, 7, 10	GND	P	GND connection
6	OE	I	Output enable control input with 130 kΩ pull-up
ePAD	—	—	Center Pad for thermal relief. Connect to GND

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## 3.0 NOMINAL PERFORMANCE CHARACTERISTICS

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.



**FIGURE 3-1:** PL133-97 Additive Phase Jitter:  $V_{DD} = 3.3V$ , CLK-100 MHz, Integration Range 12 kHz - 20 MHz.

When a buffer is used to pass a signal then the buffer will add a little bit of its own noise. The phase noise on the output of the buffer will be a little bit more than the phase noise in the input signal. The noise added by the buffer to the input signal is quantified by the additive phase jitter defined by the following formula:

### EQUATION 3-1:

$$\text{AdditivePhaseJitter} = \sqrt{(\text{OutputPhaseJitter})^2 - (\text{InputPhaseJitter})^2}$$

4.0 SWITCHING WAVEFORMS

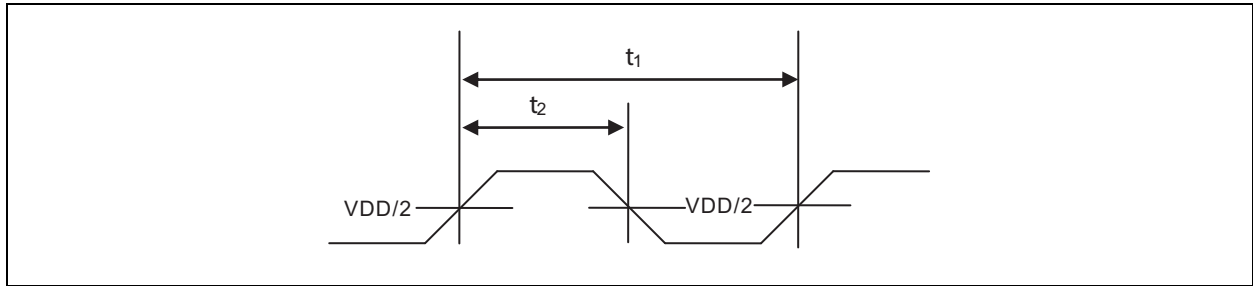


FIGURE 4-1: Duty Cycle Timing.

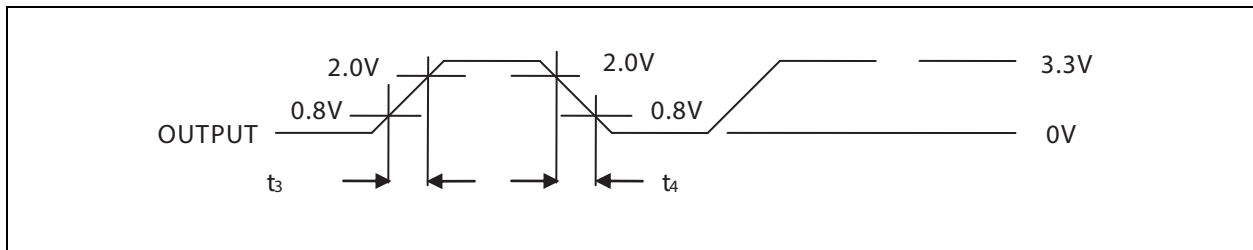


FIGURE 4-2: All Outputs Rise/Fall Time.

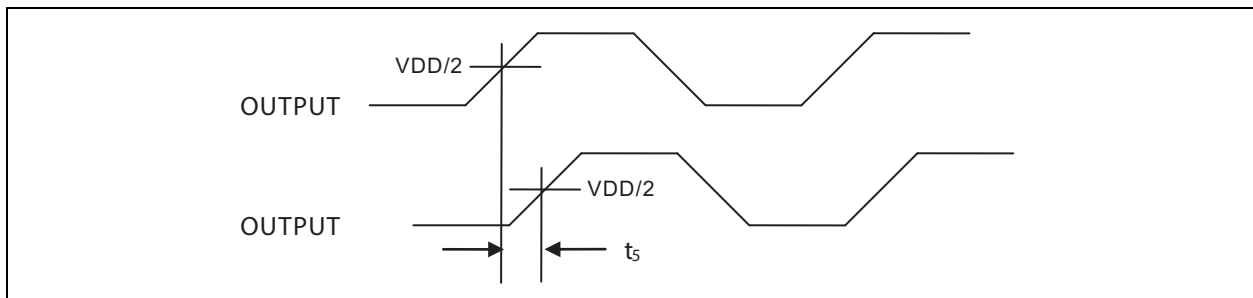


FIGURE 4-3: Output to Output Skew.

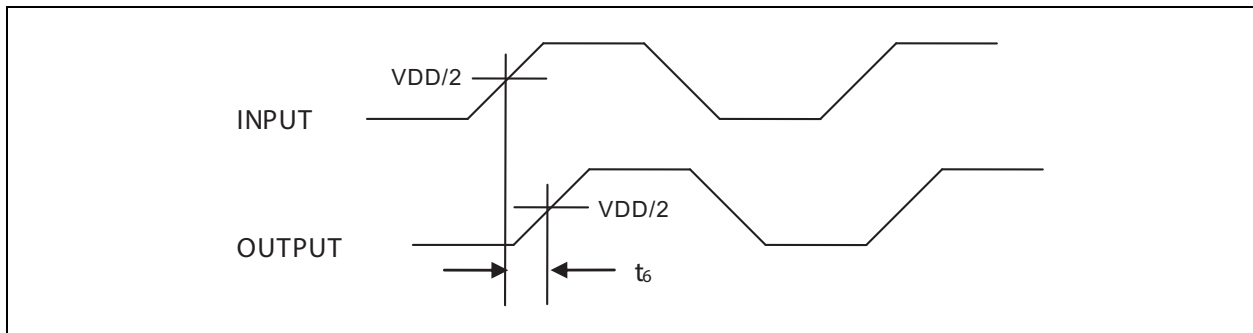
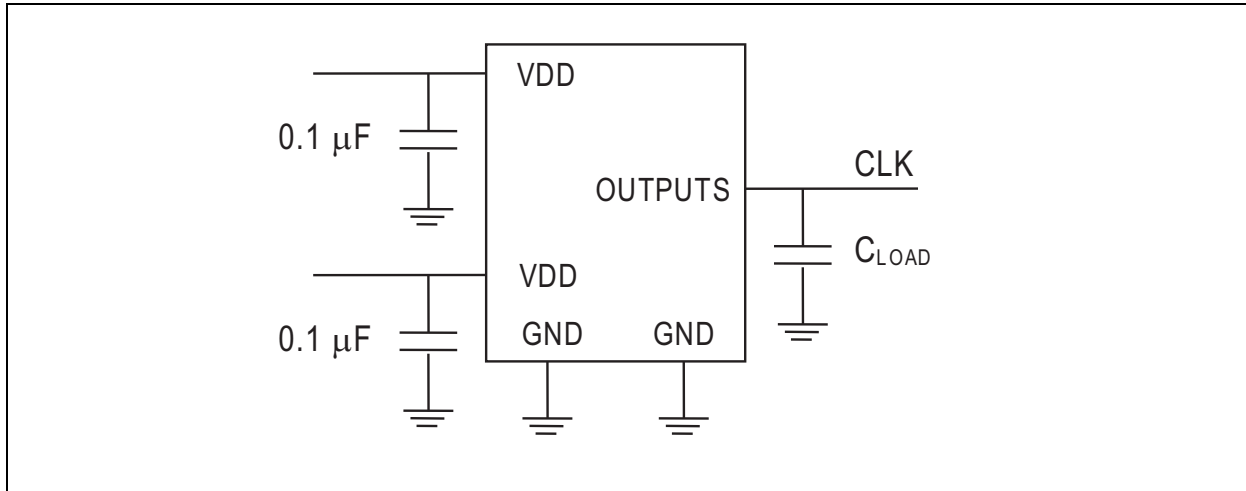


FIGURE 4-4: Input-Output Propagation Delay.

## 5.0 TEST CIRCUIT



**FIGURE 5-1:** Test Circuit.



## 6.0 LAYOUT RECOMMENDATIONS

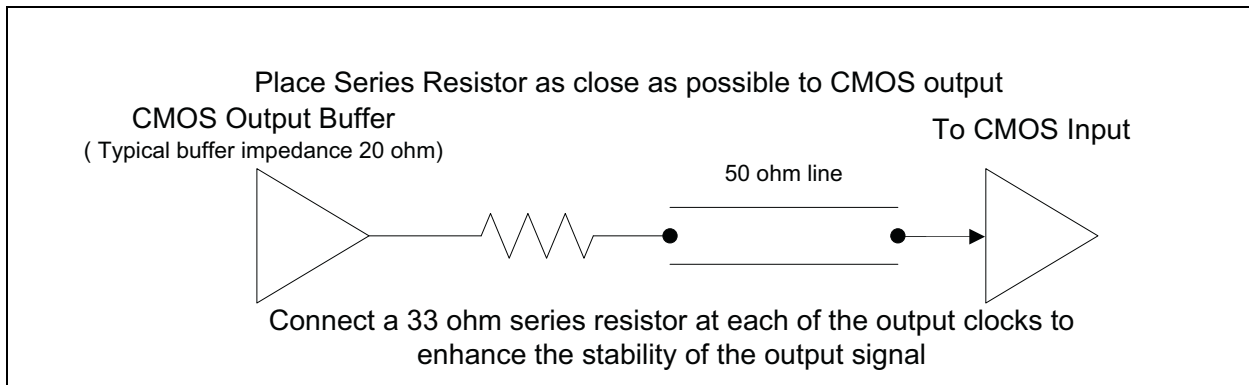
The following guidelines are to assist you with a performance optimized PCB design:

### 6.1 Signal Integrity and Termination Considerations

- Keep traces short
- Trace = Inductor. With a capacitive load this equals ringing
- Long trace = Transmission Line. Without proper termination this will cause reflections ringing and waveforms degradations.
- Use stripline or microstrip with defined impedance for long traces (> 1 inch)
- Match traces on one side of the board to avoid reflections bouncing back and forth.

### 6.2 Decoupling and Power Supply Considerations

- Place decoupling capacitors as close as possible to the VDD pin(s) to limit noise from the power supply
- Addition of a ferrite bead in series with VDD can help prevent noise from other board sources
- Value of decoupling capacitor is frequency dependant. Typical values to use are 0.1  $\mu\text{F}$  for designs using frequencies <50 MHz and 0.01  $\mu\text{F}$  for designs using frequencies >50 MHz



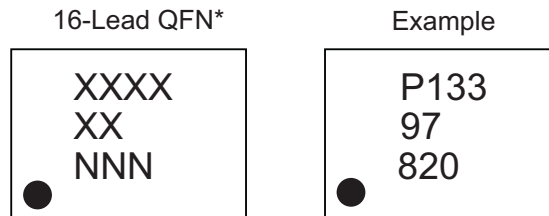
**FIGURE 6-1:** Typical CMOS Termination.

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## 7.0 PACKAGING INFORMATION

### 7.1 Package Marking Information



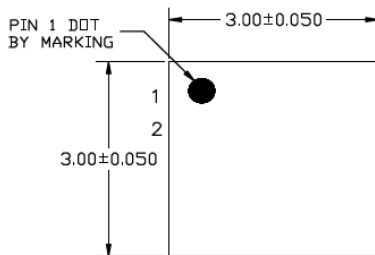
<b>Legend:</b>	XX...X	Product code, customer-specific information, or frequency in MHz without printed decimal point
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
<b>Note:</b>	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar ( ) and/or Overbar ( ) symbol may not be to scale.	

## 16-Lead QFN Package Outline and Recommended Land Pattern

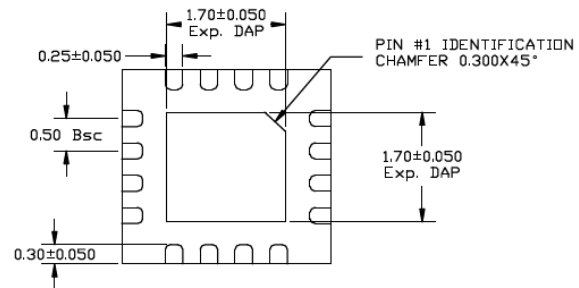
**TITLE**

16 LEAD QFN 3x3mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

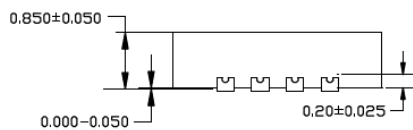
<b>DRAWING #</b>	QFN33-16LD-PL-3	<b>UNIT</b>	MM
<b>Lead Frame</b>	NiPdAu	<b>Lead Finish</b>	NiPdAu



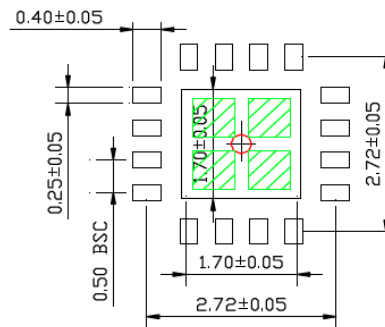
**TOP VIEW**  
NOTE: 1, 2, 3



**BOTTOM VIEW**  
NOTE: 1, 2, 3



**SIDE VIEW**  
NOTE: 1, 2, 3



**RECOMMENDED LAND PATTERN**  
NOTE: 4, 5

**NOTE:**

1. MAX PACKAGE WARPAGE IS 0.05mm.
2. MAX ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED.
4. RED CIRCLE IN LAND PATTERN INDICATES THERMAL VIA. SIZE SHOULD BE 0.30-0.35mm IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE.
5. GREEN RECTANGLES (SHADED AREA) INDICATE SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.60x0.60mm IN SIZE, 0.20mm SPACING.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

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## APPENDIX A: REVISION HISTORY

### Revision A (April 2022)

- Converted Micrel document PL133-97 to Microchip data sheet DS20006672A.
- Minor text changes throughout.

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NOTES:

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>PART NO.</u>	<u>X</u>	<u>XX</u>	<u>X</u>
Device	Package	Temperature Range	Media Type
<p><b>Device:</b> PL133-97: Low-Power DC to 150 MHz 1:9 Fanout Buffer IC</p> <p><b>Package:</b> Q = 16-Lead QFN Package (RoHS Compliant)</p> <p><b>Temperature Range:</b> C = 0°C to +70°C (Commercial) I = -40°C to +85°C (Industrial)</p> <p><b>Media Type:</b> (blank) = 20/Bag R = 3,000/Reel</p>		<p><b>Examples:</b></p> <p>a) PL133-97QC Low-Power DC to 150 MHz 1:9 Fanout Buffer IC, QFN Package, 0°C to +70°C, 20/Bag</p> <p>b) PL133-97QC-R Low-Power DC to 150 MHz 1:9 Fanout Buffer IC, QFN Package, 0°C to +70°C, 3,000/Reel</p> <p>c) PL133-97QI Low-Power DC to 150 MHz 1:9 Fanout Buffer IC, QFN Package, -40°C to +85°C, 20/Bag</p> <p>b) PL133-97QI-R Low-Power DC to 150 MHz 1:9 Fanout Buffer IC, QFN Package, -40°C to +85°C, 3,000/Reel</p>	
		<p><b>Note 1:</b> Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.</p>	

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NOTES:



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