A Product Line of
Diodes Incorporated

PI6ULS5V9306

Dual Bidirectional I2C-Bus and SMBus Voltage-Level Translator

Features

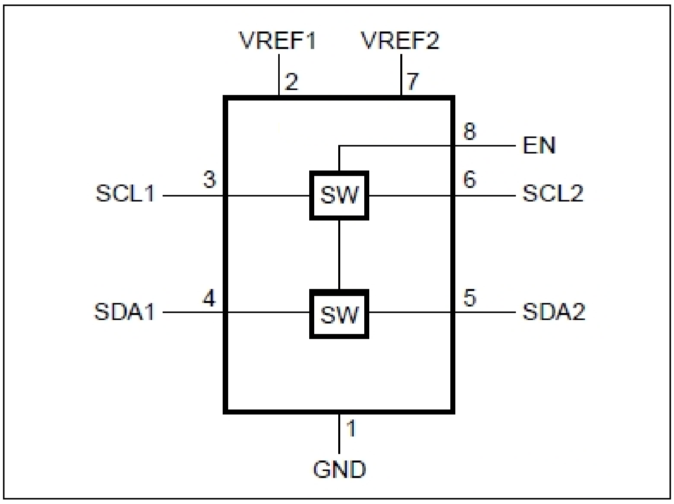
- 2-bit Bidirectional Translator for SDA and SCL Lines in Mixed-Mode I2C-Bus Applications
- Standard-Mode, Fast-Mode, and Fast-Mode Plus I2C-Bus and SMBus Compatible
- Less than 1.5ns Maximum Propagation Delay to Accommodate Standard Mode and Fast Mode I2C-Bus Devices and Multiple Masters
- Allows Voltage Level Translation Between:
    - 0.9V VREF1 and 1.8V, 2.5V, 3.3V, or 5V VREF2
    - 1.2V VREF1 and 1.8V, 2.5V, 3.3V, or 5V VREF2
    - 1.5V VREF1 and 2.5V, 3.3V, or 5V VREF2
    - 1.8V VREF1 and 3.3V or 5V VREF2
    - 2.5V VREF1 and 5V VREF2
    - 3.3V VREF1 and 5V VREF2
- Provides Bidirectional Voltage Translation with no Direction Pin
- Low 3.5Ω ON-State Connection Between Input and Output Ports Provides Less Signal Distortion
- Open-Drain I2C-Bus I/O Ports (SCL1, SDA1, SCL2, and SDA2)
- 5V Tolerant I2C-Bus I/O Ports to Support Mixed-Mode Signal Operation
- High-Impedance SCL1, SDA1, SCL2, and SDA2 Pins for EN = LOW
- Lock-up Free Operation for Isolation when EN = LOW
- Flow through Pinout for Ease of Printed-Circuit Board Trace Routing
- ESD Protection Exceeds 4KV HBM per JESD22-A114
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. “Green” Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/
- Package: TDFN2x3-8(ZE), MSOP-8(U), SOIC-8(W)

Description

The DIODES™ PI6ULS5V9306 is a dual bidirectional I^{2}C-bus and SMBus voltage-level translator with an enable (EN) input. It is operational from 0.9V to 3.3V (VREF1) and 1.8V to 5V (VREF2).

The PI6ULS5V9306 allows bidirectional voltage translations between 1.0V and 5V without the use of a direction pin. The low ON-state resistance (Ron) of the switch allows connections to be made with minimal propagation delay. When EN is HIGH, the translator switch is on, and the SCL1 and SDA1 I/O are connected to the SCL2 and SDA2 I/O respectively, allowing bidirectional data flow between ports. When EN is LOW, the translator switch is off, and a high-impedance state exists between ports.

Block Diagram

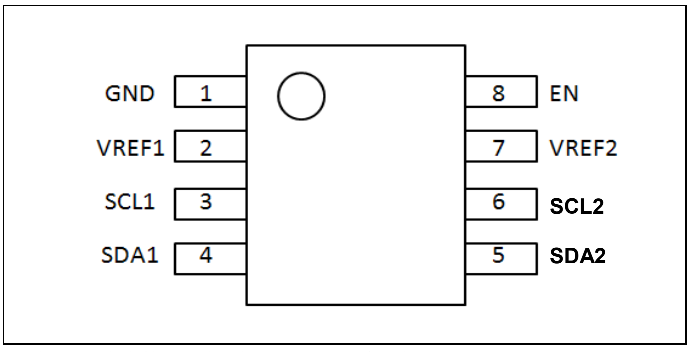


Function Table

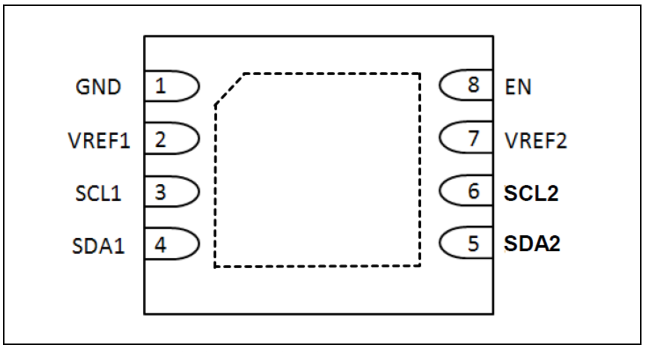
EN	Function
H	SCL1 = SCL2; SDA1 = SDA2
L	disabled

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated’s definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green” products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Configuration



MSOP-8(U)/SOIC-8(W) (Top View)



TDFN2x3-8(ZE) (Top View)

Pin Description

Pin#	Name	Description
1	GND	Ground (0V)
2	VREF1	Low-voltage side reference supply voltage for SCL1 and SDA1
3	SCL1	Serial clock, low-voltage side; connect to VREF1 through a pullup resistor
4	SDA1	Serial data, low-voltage side; connect to VREF1 through a pullup resistor
5	SDA2	Serial data, high-voltage side; connect to VREF2 through a pullup resistor
6	SCL2	Serial clock, high-voltage side; connect to VREF2 through a pullup resistor
7	VREF2	High-voltage side reference supply voltage for SCL2 and SDA2
8	EN	Switch enable input; connect to VREF2 and pullup through a high resistor

Maximum Ratings

Storage Temperature	-65°C to +150°C
Reference Voltage (2)	-0.5V to +6.0V
Reference Bias Voltage	-0.5V to+6.0V
DC Input Voltage	-0.5V to +6.0V
Control Input Voltage (EN)	-0.5V to+6.0V
Channel Current (DC)	128mA
Input Clamping Current	-50mA
ESD: HBM Mode	4000V
Junction Temperature under Bias (T_J)	125°C

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operation Conditions

V_{CC} = 2.7V to 5.5V; GND = 0V; T_A = -40°C to +85°C; unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{I/O}$	Voltage on an Input/Output Pin	SCL1, SDA1, SCL2, SDA2	0	—	5	V
V_{REF1}	Reference Voltage(1)	VREF1	0.9	—	3.3	V
V_{REF2}	Reference Bias Voltage(2)	VREF2	1.8	—	5	V
$V_{I(EN)}$	Input Voltage on Pin EN	—	0	—	5	V
$I_{(pass)}$	Pass Switch Current	—	—	—	64	mA
T_A	Ambient Temperature	—	-40	—	85	°C

DC Electrical Characteristics

T_A = -40°C to +85°C; unless otherwise specified.

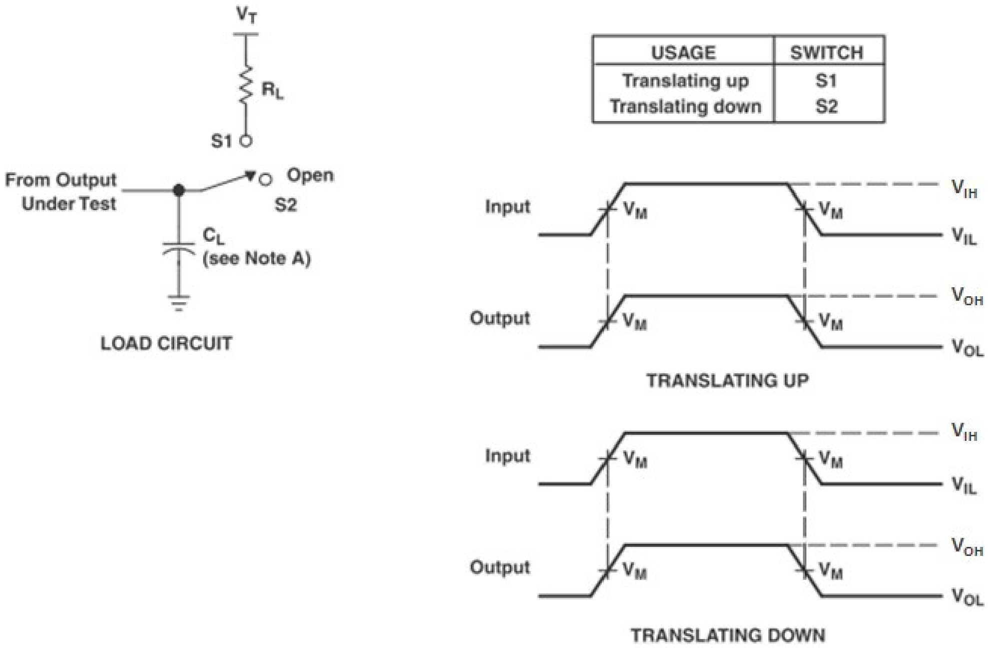
Parameter	Description	Test Conditions(1)		Min	Typ.(2)	Max	Unit
Input and Output SDAB and SCLB							
V_{IK}	Input Clamping Voltage	I_I = -18mA; $V_{I(EN)}$ = 0V		—	—	-1.2	V
I_{IH}	HIGH-Level Input Current	V_I = 5V; $V_{I(EN)}$ = 0V		—	—	5	µA
$C_{i(EN)}$	Input Capacitance on pin EN	V_I = 3V or 0V		—	11	—	pF
$C_{io(off)}$	Off-State Input/Output Capacitance (SCLn, SDAn)	V_O = 3V or 0V; $V_{I(EN)}$ = 0V		—	4	—	pF
$C_{io(on)}$	On-State Input/Output Capacitance (SCLn, SDAn)	V_O = 3V or 0V; $V_{I(EN)}$ = 3V		—	10.5	—	pF
Ron	ON-State Resistance(2) (SCLn, SDAn)	V_I = 0V; I_O = 64mA	$V_{I(EN)}$ = 4.5V	—	3.5	5.5	Ω
			$V_{I(EN)}$ = 3V	—	4.7	7.0	Ω
			$V_{I(EN)}$ = 2.3V	—	6.3	9.5	Ω
			$V_{I(EN)}$ = 1.5V	—	60	140	Ω
		V_I = 2.4V; I_O = 15mA	$V_{I(EN)}$ = 4.5V	1	6	15	Ω
			$V_{I(EN)}$ = 3V	20	60	140	Ω
		V_I = 1.7V; I_O = 15mA	$V_{I(EN)}$ = 2.3V	20	60	140	Ω

Notes:
1. All typical values are at T_A = 25°C.
2. Measured by the voltage drop between the SCL1 and SCL2 or SDA1 and SDA2 terminals at the indicated current through the switch. ON-state resistance is determined by the lowest voltage of the two terminals.

Dynamic Characteristics

T_A = -40°C to +85°C; unless otherwise specified. Values guaranteed by design.

Symbol	Parameter	Conditions	C_L = 50pF		C_L = 30pF		C_L = 15pF		Unit
			Min	Max	Min	Max	Min	Max	
Dynamic Characteristics (Translating Down)									
$V_{I(EN)}$ = 3.3V; V_{IH} = 3.3V; V_{IL} = 0V; V_M = 1.15V									
t_{PLH}	LOW-to-HIGH Propagation Delay	From (Input) SCL2 or SDA2 to (Output) SCL1 or SDA1	0	0.8	0	0.6	0	0.3	ns
t_{PHL}	HIGH-to-LOW Propagation Delay	From (Input) SCL2 or SDA2 to (Output) SCL1 or SDA1	0	1.2	0	1	0	0.5	ns
$V_{I(EN)}$ = 2.5V; V_{IH} = 2.5V; V_{IL} = 0V; V_M = 0.75V									
t_{PLH}	LOW-to-HIGH Propagation Delay	From (Input) SCL2 or SDA2 to (Output) SCL1 or SDA1	0	1	0	0.7	0	0.4	ns
t_{PHL}	HIGH-to-LOW Propagation Delay	From (Input) SCL2 or SDA2 to (Output) SCL1 or SDA1	0	1.3	0	1	0	0.6	ns
Dynamic Characteristics (Translating up)									
$V_{I(EN)}$ = 3.3V; V_{IH} = 2.3V; V_{IL} = 0V; V_T = 3.3V; V_M = 1.15V; R_L = 300Ω									
t_{PLH}	LOW-to-HIGH Propagation Delay	From (Input) SCL1 orSDA1 to (output) SCL2 or SDA2	0	0.9	0	0.6	0	0.4	ns
t_{PHL}	HIGH-to-LOW Propagation Delay	From (Input) SCL1 or SDA1 to (Output) SCL2 or SDA2	0	1.4	0	1.1	0	0.7	ns
$V_{I(EN)}$ = 2.5V; V_{IH} = 1.5V; V_{IL} = 0V; V_T = 2.5V; V_M = 0.75V; R_L = 300Ω									
t_{PLH}	LOW-to-HIGH Propagation Delay	From (Input) SCL1 orSDA1 to (Output) SCL2 or SDA2	0	1	0	0.6	0	0.4	ns
t_{PHL}	HIGH-to-LOW Propagation Delay	From (Input) SCL1 or SDA1 to (Output) SCL2 or SDA2	0	1.3	0	1.3	0	0.8	ns



NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
C. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit for Outputs

Functional Description

The PI6ULS5V9306 can also be used to run two buses—one at 400kHz operating frequency and the other at 100kHz operating frequency. If the two buses are operating at different frequencies, the 100kHz bus must be isolated when the 400kHz operation of the other bus is required. If the master is running at 400kHz, the maximum system operating frequency may be less than 400kHz because of the delays added by the translator.

As with the standard I^2C-bus system, pullup resistors are required to provide the logic HIGH levels on the translator's bus. The PI6ULS5V9306 has a standard open-collector configuration of the I^2C-bus. Each side of the translator must have a pullup resistor though the size of these pullup resistors depends on the system. The device is designed to work with standard mode, fast mode, and fast mode plus I^2C-bus devices in addition to SMBus devices.

When the SDA1 or SDA2 port is LOW, the clamp is in the ON-state and a low-resistance connection exists between the SDA1 and SDA2 ports. When the higher voltage is on the SDA2 port, and the SDA2 port is HIGH, the voltage on the SDA1 port is limited to the voltage set by VREF1. When the SDA1 port is HIGH, the SDA2 port is pulled to the drain pullup supply voltage (VDPU) by the pullup resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user without requiring directional control. The SCL1/SCL2 channel also functions as the SDA1/SDA2 channel.

All channels have the same electrical characteristics, and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete transistor voltage translation solutions because the fabrication of the switch is symmetrical. The translator provides excellent ESD protection to lower voltage devices, and at the same time protects less ESD-resistant devices

Application Information

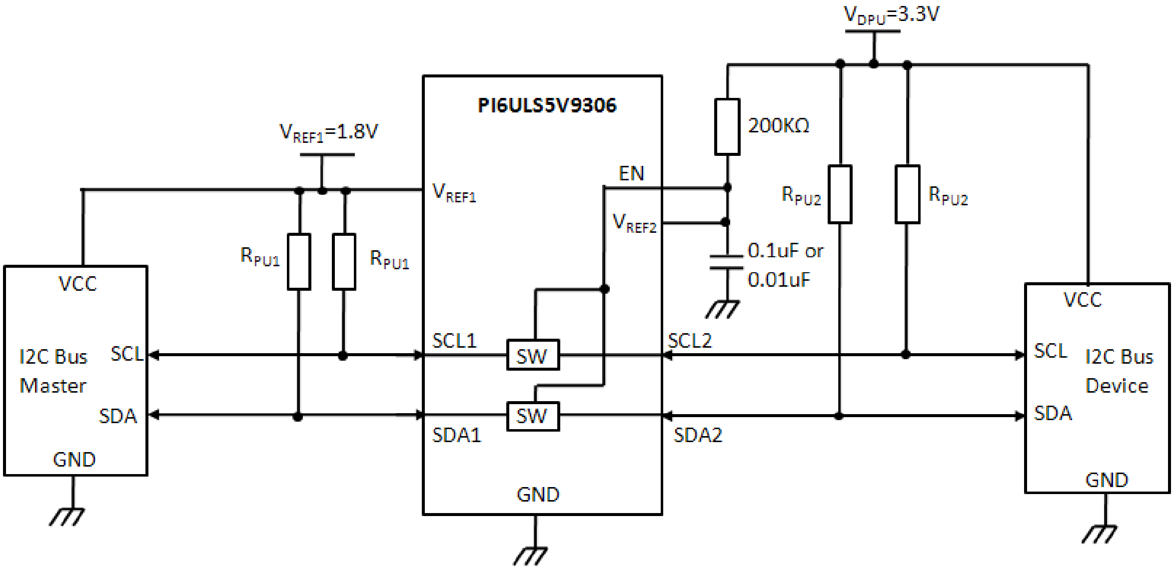


Figure 2. Typical Open-Drain Application Circuit (Switch Always Enabled)

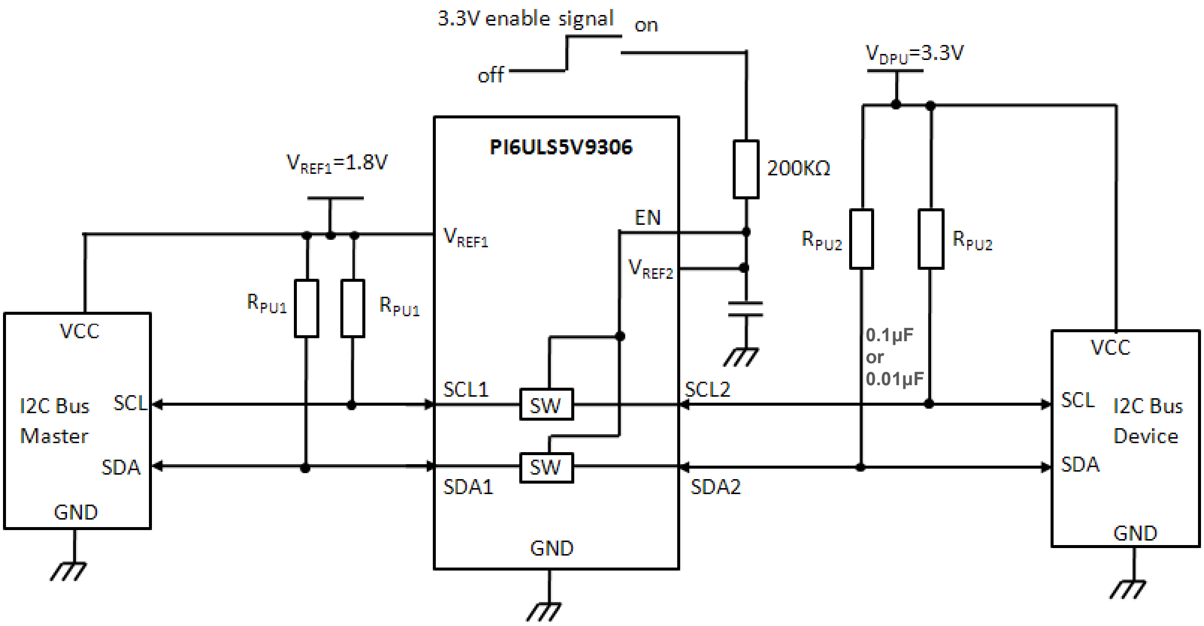


Figure 3. Typical Open-Drain Application Circuit (Switch Enabled Control)

Open-Drain Application

For the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to VREF2 and both pins pulled to high-side VDPU through a pullup resistor (typically 200kΩ). This allows VREF2 to regulate the EN input. A filter capacitor on VREF2 is recommended.

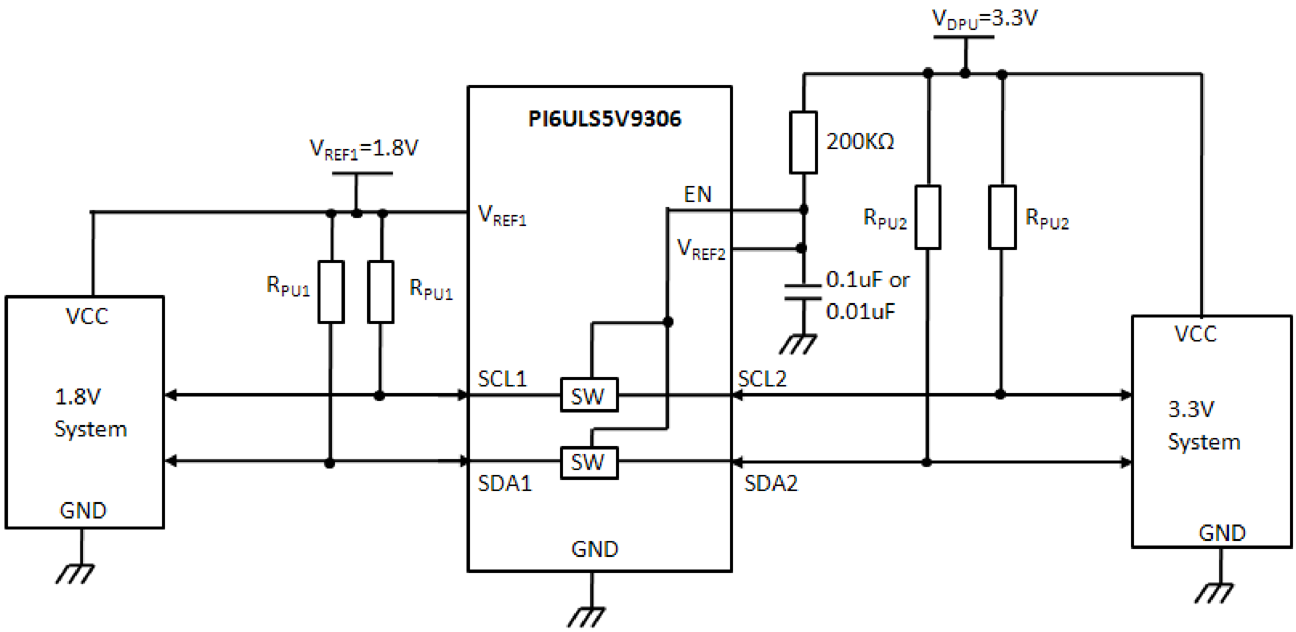


Figure 4. Typical Push-Pull Application Circuit (Switch Enabled Control)

Push-Pull Application

If used in push-pull system, the pullup resistors on REF side are also required. The data must be unidirectional, or the outputs must be 3-stateable and controlled by some direction-control mechanism to prevent high-to-low contentions in either direction.

Operating Voltage

Refer to Figure 2

Symbol	Description	Min	Typ[1]	Max	Unit
VDPU	Ref2 Side Pullup Voltage on 200kΩ	VREF1 + 0.6	2.1	5	V
EN	Enable Input Voltage	VREF1 + 0.6	2.1	5	V
VREF1	Reference Voltage	0	1.5	4.4	V
IPASS	Pass Switch Current	14	—	—	mA
IREF	Reference-Transistor Current	—	—	5	µA
TA	Operating Free-Air Temperature	-40	—	85	°C

The Pass-Through Current: I_pass

I_pass is determined by the pullup and the low voltage added on the PI6LS5V9306.

In Figure 6, I_pass equals (V_{REF1}-V_{OL1_9306})/R_{PU1}.

When V_IN is 0V, the PI6ULS5V9306 can support as large as 64mA pass-through current in theory, but it is recommend to limit the I_pass in 15mA.

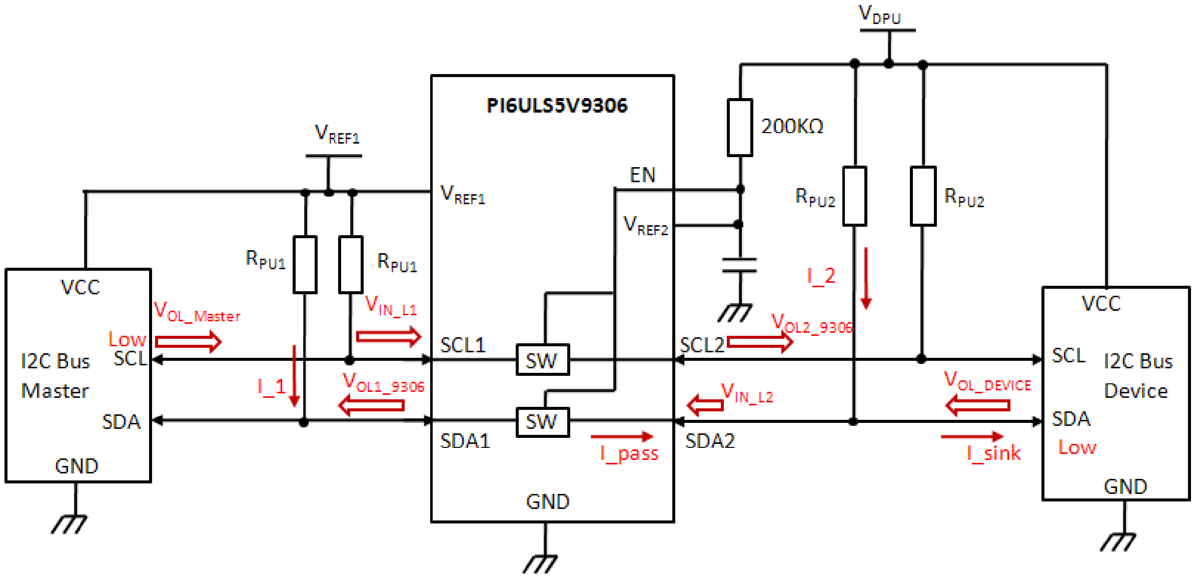


Figure 5. Typical Open-Drain Application Circuit

(1) The Sink Current: I_sink

The device sinks the total current from both pullup resistors. For example, in figure below, when the SDA2 is pulled low by the I2C device, the sink current of the I2C device is I_sink = Ipass+I_2=I_1+I_2. The same thing happens when I2C master pulls low the I2C bus. The I_sink should not be larger than the tolerance of the I2C devices.

(2) V_{IL},V_{OL} of the External Drive and V_{OL} of PI6ULS5V9306

In normal application, the V_{IL} of external devices should always be larger than the V_{OL} of PI6ULS5V9306. The value of PI6ULS5V9306's V_{OL} is determined by the pass-through current and the low voltage added on the SDA, SCL pins. The $V_{OL\_9306} = V_{IN\_L} + V_{UP}$ (V_{UP} is mainly determined by the I_pass, which is always less than 0.35V).

(3) Low VREF Application

The PI6ULS5V9306 can support very-low Vref1 application in theory, but it is recommended no lower than 0.9V. Because when VREF1 is less than 1.8V, the V_{OL} of REF1 side is a concern in system. For example, in Figure 6, if VREF1 = 0.9V, VDPU = 3.3V, the V_{IL} of the REF1 side I2C master is normally 0.3 × VREF1 = 0.25V, but the V_{OL} of REF2 side can up to 0.1 × VDPU=0.36V. The system designer must make sure this situation does not happen. A limit for the V_{OL} of REF2 side devices is required then.

The following table shows the requirements for V_{OL} of VREF2 side devices when using PI6ULS5V9306. Figure 6 shows the requirement for V_{OL_DEVICE}.

The V_{OL} Requirement of V_{REF2} Side External Devices (Temp = 25°C, Assume the V_{IL} of V_{REF1} Side Devices is 0.3 × V_{REF1})			
I_pass / V_{REF1}	≤3mA	10mA	15mA
0.9V	≤0.15V	≤0.1V	Not Recommended
1.2V	≤0.2V	≤0.15V	Not Recommended
1.5V	≤0.3V	≤0.25V	≤0.2V
1.8V	≤0.4V	≤0.35V	≤0.3V

Pullup Resistors and Minimum Values

Sizing the pullup resistor on an open-drain bus is specific to the individual application and is dependent on the following driver characteristics:

- The driver sink current
- The V_{OL} of driver
- The V_{OL} of the PI6ULS5V9306
- The V_{IL} of the driver
- Frequency of operation

The following tables can be used to estimate the pullup resistor value in different use cases so that the minimum resistance for the pullup resistor can be found.

The tables below show suggested minimum values of pullup resistors for the PI6ULS5V9306 with typical voltage translation levels and drive currents. The calculated values assume that both drive currents are the same.

$V_{OL} = V_{IL} = 0.1 \times VCC$ and accounts for a 5% VCC tolerance of the supplies, 1 % resistor values. Note that the resistor chosen in the final application should be equal to or larger than the values shown in the table to ensure that the pass voltage is less than 10% of the VCC voltage, and the external driver should be able to sink the total current from both pullup resistors.

Pullup Resistor Minimum Values, 3mA Driver Sink Current for PI6ULS5V9306

A Side	B Side				
	1.5V	**1.8V**	**2.5V**	**3.3V**	**5.0V**
0.9V	R_{RPU1} = 859Ω R_{RPU2} = 859Ω	R_{RPU1} = 970Ω R_{RPU2} = 970Ω	R_{RPU1} = none R_{RPU2} = 896Ω or both 1.23kΩ	R_{RPU1} = none R_{RPU2} = 1.19kΩ or both 1.53kΩ	R_{RPU1} = none R_{RPU2} = 1.82kΩ or both 2.16kΩ
1.2V	—	R_{RPU1} = 1.07kΩ R_{RPU2} = 1.07kΩ	R_{RPU1} = none R_{RPU2} = 886Ω or both 1.33kΩ	R_{RPU1} = none R_{RPU2} = 1.18kΩ or both 1.63kΩ	R_{RPU1} = none R_{RPU2} = 1.81kΩ or both 2.26kΩ
1.5V	—	—	R_{RPU1} = none R_{RPU2} = 875Ω or both 1.43kΩ	R_{RPU1} = none R_{RPU2} = 1.17kΩ or both 1.73kΩ	R_{RPU1} = none R_{RPU2} = 1.8kΩ or both 2.36kΩ
1.8V	—	—	R_{RPU1} = 1.53kΩ R_{RPU2} = 1.53kΩ	R_{RPU1} = none R_{RPU2} = 1.16kΩ or both 1.82kΩ	R_{RPU1} = none R_{RPU2} = 1.79kΩ or both 2.46kΩ
2.5V	—	—	—	R_{RPU1} = 2.06kΩ R_{RPU2} = 2.06kΩ	R_{RPU1} = none R_{RPU2} = 1.77kΩ or both 2.69kΩ
3.3V	—	—	—	—	R_{RPU1} = none R_{RPU2} = 1.74kΩ or both 2.96kΩ

Pullup Resistor Minimum Values, 10mA Driver Sink Current for PI6ULS5V9306

A Side	B Side				
	1.5V	**1.8V**	**2.5V**	**3.3V**	**5.0V**
0.9V	R_{RPU1} = 258Ω R_{RPU2} = 258Ω	R_{RPU1} = 291Ω R_{RPU2} = 291Ω	R_{RPU1} = none R_{RPU2} = 269Ω or both 369Ω	R_{RPU1} = none R_{RPU2} = 358Ω or both 458Ω	R_{RPU1} = none R_{RPU2} = 546Ω or both 646Ω
1.2V	—	R_{RPU1} = 321Ω R_{RPU2} = 321Ω	R_{RPU1} = none R_{RPU2} = 266Ω or both 399Ω	R_{RPU1} = none R_{RPU2} = 355Ω or both 488Ω	R_{RPU1} = none R_{RPU2} = 543Ω or both 677Ω
1.5V	—	—	R_{RPU1} = none R_{RPU2} = 263Ω or both 429Ω	R_{RPU1} = none R_{RPU2} = 352Ω or both 518Ω	R_{RPU1} = none R_{RPU2} = 540Ω or both 707Ω
1.8V	—	—	R_{RPU1} = 460Ω R_{RPU2} = 460Ω	R_{RPU1} = none R_{RPU2} = 348Ω or both 548Ω	R_{RPU1} = none R_{RPU2} = 537Ω or both 737Ω
2.5V	—	—	—	R_{RPU1} = 619Ω R_{RPU2} = 619Ω	R_{RPU1} = none R_{RPU2} = 521Ω or both 808Ω
3.3V	—	—	—	—	R_{RPU1} = none R_{RPU2} = 522Ω or both 889Ω

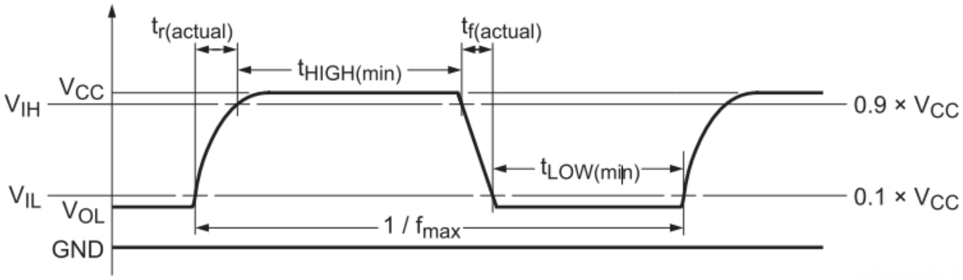
Pullup Resistor Minimum Values, 15mA Driver Sink Current for PI6ULS5V9306

A Side	B Side				
	1.5V	**1.8V**	**2.5V**	**3.3V**	**5.0V**
0.9V	R_{RPU1} = 172Ω R_{RPU2} = 172Ω	R_{RPU1} = 194Ω R_{RPU2} = 194Ω	R_{RPU1} = none R_{RPU2} = 179Ω or both 246Ω	R_{RPU1} = none R_{RPU2} = 238Ω or both 305Ω	R_{RPU1} = none R_{RPU2} = 364Ω or both 431Ω
1.2V	—	R_{RPU1} = 214Ω R_{RPU2} = 214Ω	R_{RPU1} = none R_{RPU2} = 177Ω or both 266Ω	R_{RPU1} = none R_{RPU2} = 236Ω or both 325Ω	R_{RPU1} = none R_{RPU2} = 362Ω or both 451Ω
1.5V	—	—	R_{RPU1} = none R_{RPU2} = 175Ω or both 286Ω	R_{RPU1} = none R_{RPU2} = 234Ω or both 345Ω	R_{RPU1} = none R_{RPU2} = 360Ω or both 471Ω
1.8V	—	—	R_{RPU1} = 306Ω R_{RPU2} = 306Ω	R_{RPU1} = none R_{RPU2} = 232Ω or both 366Ω	R_{RPU1} = none R_{RPU2} =358Ω or both 492Ω
2.5V	—	—	—	R_{RPU1} = 413Ω R_{RPU2} = 413Ω	R_{RPU1} = none R_{RPU2} = 354Ω or both 539Ω
3.3V	—	—	—	—	R_{RPU1} = none R_{RPU2} = 348Ω or both 593Ω

Maximum Frequency Application

The maximum frequency is limited by the minimum pulse width LOW and HIGH as well as rise time and fall time.

$$f(\max) = \frac{1}{\text{tLOW(min)} + \text{tHIGH(min)} + \text{tr(actual)} + \text{tf(actual)}}$$



The rise and fall times are dependent upon translation voltages, the drive strength, the total node capacitance (CL), and the pullup resistors (RPU) that are present on the bus. The node capacitance is the addition of the PCB trace capacitance and the device capacitance that exists on the bus.

Because of the dependency of the external components, PCB layout and the different device operating states the calculation of rise and fall times is complex and has several inflection points along the curve.

The main component of the rise and fall times is the RC time constant of the bus line when the device is in its two primary operating states: when device is in the ON state and it is low-impedance and when the device is OFF isolating the A-side from the B-side.

There are some basic guidelines to follow that will help maximize the performance of the device:

- Keep trace length to a minimum by placing the PI6ULS5V9306 close to the processor.
- The signal round trip time on trace should be shorter than the rise or fall time of signal to reduce reflections.
- The faster the edge of the signal, the higher the chance for ringing.
- The higher drive strength controlled by the pullup resistor (up to 15mA), the higher the frequency the device can use.

The system designer must design the pullup resistor value based on external current drive strength and limit the node capacitance (minimize the wire, stub, connector, and trace length) to get the desired operation frequency result.

Part Marking

W Package Cu

PI6ULS5V
9306WE
ZYWXX

Z: Die Rev
Y: Date Code (Year)
W: Date Code (Workweek)
1st X: Assembly Site Code
2nd X: Wafer Fab Site Code
Bar above fab code means Cu wire

Note: Bar above "I" means Fab3 og MGN

W Package Au

PI6ULS5V
9306WE
ZABKG

Z: Die Rev
AB: Date Code (Year & Workweek)
K: Assembly Site Code
G: Wafer Fab Site Code

U Package

ULS5V9
306UE
ZYWXX

Z: Die Rev
Y: Date Code (Year)
W: Date Code (Workweek)
1st X: Assembly Site Code
2nd X: Wafer Fab Site Code
Bar above fab code means Cu wire

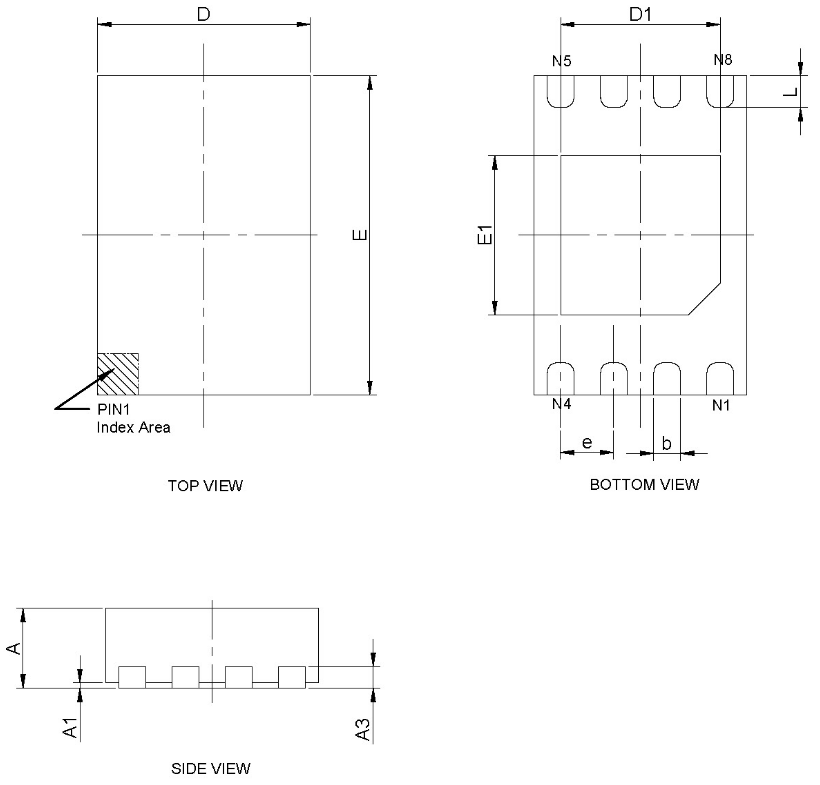
ZE Package

rA
XX
JG

J: Assembly Site Code
G: Fab Site Code
XX: Date Code (Year & Workweek)
Bar above "A" means Fab3 of MGN

Packaging Mechanical

TDFN-8 (ZE)



PKG.	DIMENSIONS(MM)	
SYMBOL	Min	Max
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
D	1.92	2.08
E	2.92	3.07
D1	1.40	1.60
E1	1.40	1.60
k	0.20 MIN	
b	0.20	0.30
e	0.50 TYP	
L	0.22	0.38

Notes:
1. Ref: JEDEC MO-229

PERICOM Enabling Serial Connectivity

DATE: 06/14/13

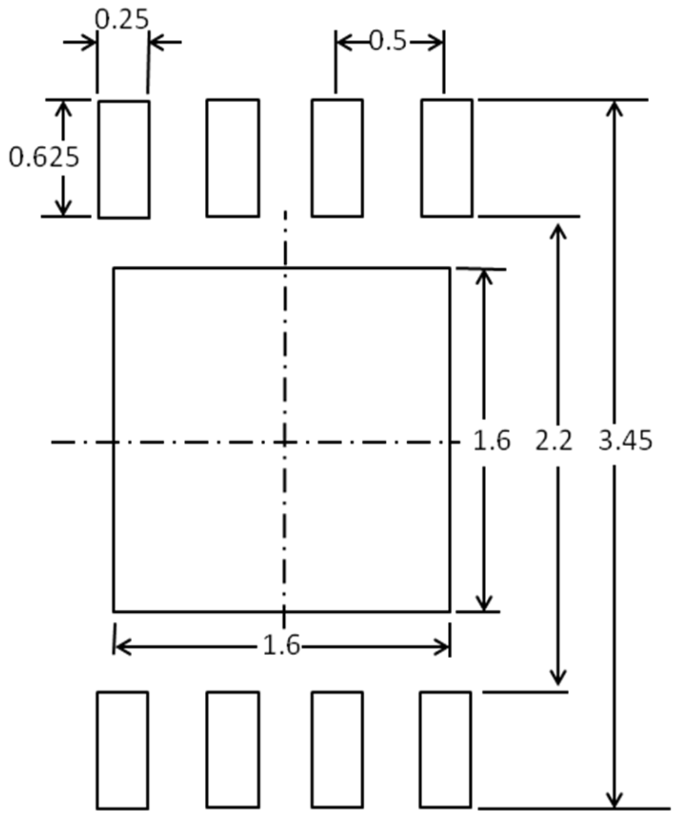
DESCRIPTION: 8-Pin, TDFN, 2X3

PACKAGE CODE: ZE (ZE8)

DOCUMENT CONTROL#: PD-2116 **REVISION: --**

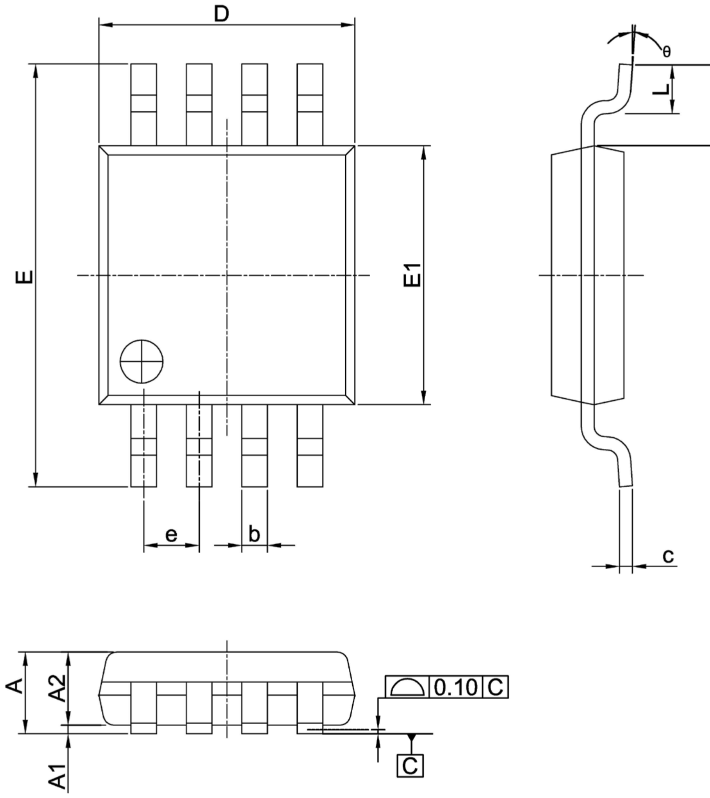
13-0155

Recommended Land Pattern for TDFN2x3-8L



Note:
All linear dimensions are in millimeters.

MSOP-8 (U)



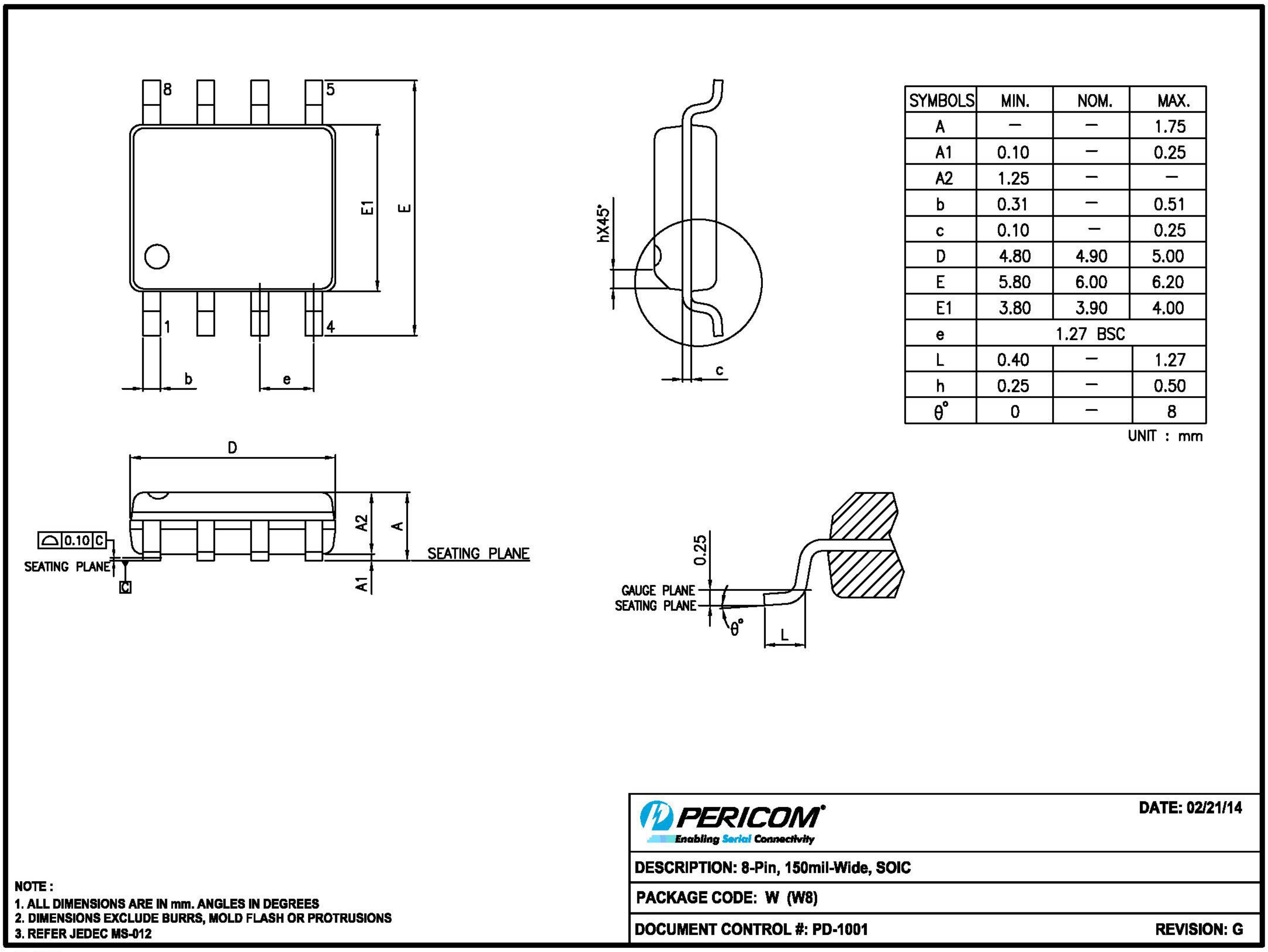
PKG DIMENSIONS(MM)		
SYMBOL	Min.	Max.
A	--	1.10
A1	0.00	0.15
A2	0.75	0.95
b	0.22	0.38
c	0.08	0.23
D	2.80	3.20
E	4.65	5.15
E1	2.80	3.20
e	0.65 BSC	
L	0.40	0.80
L1	0.95 REF	
θ	0°	8°

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES IN DEGREES.
2. REFER JEDEC MO-187F/AA
3. PACKAGE OUTLINE DIMENSIONS DO NOT INCLUDE MOLD FLASH AND METAL BURR.

DIODES INCORPORATED / PERICOM ENABLING SERIAL CONNECTIVITY	**DATE: 11/03/16**
DESCRIPTION: 8-Pin, Mini Small Outline Package, MSOP	
PACKAGE CODE: U (U8)	
DOCUMENT CONTROL #: PD-1261	**REVISION: G**

16-0242

SOIC-8 (W)



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.75
A1	0.10	–	0.25
A2	1.25	–	–
b	0.31	–	0.51
c	0.10	–	0.25
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.40	–	1.27
h	0.25	–	0.50
θ°	0	–	8

UNIT : mm

NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES
2. DIMENSIONS EXCLUDE BURRS, MOLD FLASH OR PROTRUSIONS
3. REFER JEDEC MS-012

PERICOM Enabling Serial Connectivity — DATE: 02/21/14

DESCRIPTION: 8-Pin, 150mil-Wide, SOIC

PACKAGE CODE: W (W8)

DOCUMENT CONTROL #: PD-1001 — REVISION: G

15-0103

For latest package information:

See http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/.

Ordering Information

Part Number	Package Code	Package Description
PI6ULS5V9306ZEEX	ZE	8-Pin, 2X3 (TDFN)
PI6ULS5V9306UEX	U	8-Pin, Mini Small Outline Package (MSOP)
PI6ULS5V9306WEX	W	8-Pin,150 mil Wide (SOIC)

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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