

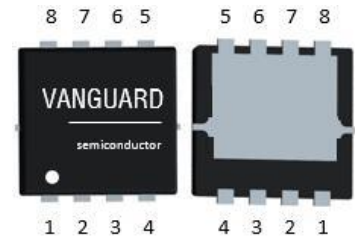
Features

- Enhancement mode
- Low on-resistance $R_{DS(on)}$ @ $V_{GS}=4.5V$
- VitoMOS[®] II Technology
- Fast Switching and High efficiency
- ESD Protection HBM $\pm 1500V$
- Pb-free lead plating; RoHS compliant; Halogen free

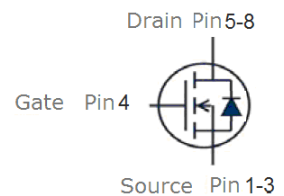


V_{DS}	30	V
$R_{DS(on),TYP}$ @ $V_{GS}=10V$	1.4	m Ω
$R_{DS(on),TYP}$ @ $V_{GS}=4.5V$	2.2	m Ω
I_D	155	A

PDFN3333



Part ID	Package Type	Marking	Tape and reel information
VSE002N03MS-G	PDFN3333	002N03M	5000pcs/Reel



Maximum ratings, at $T_A=25^\circ C$, unless otherwise specified

Symbol	Parameter	Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage	30	V
V_{GS}	Gate-Source voltage	± 20	V
I_S	Diode continuous forward current	$T_C=25^\circ C$	155 A
I_D	Continuous drain current @ $V_{GS}=10V$	$T_C=25^\circ C$	155 A
		$T_C=100^\circ C$	98 A
I_{DM}	Pulse drain current tested ①	$T_C=25^\circ C$	620 A
I_{DSM}	Continuous drain current @ $V_{GS}=10V$	$T_A=25^\circ C$	35 A
		$T_A=70^\circ C$	28 A
E_{AS}	Avalanche energy, single pulsed ②	56	mJ
P_D	Maximum power dissipation	$T_C=25^\circ C$	69 W
		$T_C=100^\circ C$	28 W
P_{DSM}	Maximum power dissipation ③	$T_A=25^\circ C$	3.6 W
		$T_A=70^\circ C$	2.3 W
$T_{STG,TJ}$	Storage and junction temperature range	-55 to 150	$^\circ C$

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.8	2.2	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	35	42	$^\circ C/W$

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
V(BR)DSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	30	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current(T _j =25°C)	V _{DS} =30V, V _{GS} =0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T _j =55°C)	V _{DS} =30V, V _{GS} =0V	--	--	5	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V, V _{DS} =0V	--	--	±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.2	1.6	2.3	V
R _{DS(on)}	Drain-Source On-State Resistance ④	V _{GS} =10V, I _D =20A	1	1.4	1.8	mΩ
		T _j =100°C	--	1.7	2.3	mΩ
R _{DS(on)}	Drain-Source On-State Resistance ④	V _{GS} =4.5V, I _D =10A	1.5	2.2	2.9	mΩ
Dynamic Electrical Characteristics @ T_j= 25°C (unless otherwise stated)						
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz	2080	2450	2820	pF
C _{oss}	Output Capacitance		980	1155	1330	pF
C _{rss}	Reverse Transfer Capacitance		70	80	90	pF
R _g	Gate Resistance	f=1MHz	1.5	2.1	2.7	Ω
Q _{g(10V)}	Total Gate Charge	V _{DS} =15V, I _D =20A, V _{GS} =10V	--	45	58	nC
Q _{g(4.5V)}	Total Gate Charge		--	23	30	nC
Q _{gs}	Gate-Source Charge		--	7.1	9.4	nC
Q _{gd}	Gate-Drain Charge		--	8.8	13	nC
Switching Characteristics						
T _{d(on)}	Turn-on Delay Time	V _{DD} =15V, I _D =20A, R _G =3Ω, V _{GS} =10V	--	8.2	--	ns
T _r	Turn-on Rise Time		--	59	--	ns
T _{d(off)}	Turn-Off Delay Time		--	40	--	ns
T _f	Turn-Off Fall Time		--	23	--	ns
Source- Drain Diode Characteristics @ T_j= 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =20A, V _{GS} =0V	--	0.8	1.2	V
T _{rr}	Reverse Recovery Time	T _j =25°C, I _{sd} =20A, V _{GS} =0V	--	35	70	ns
Q _{rr}	Reverse Recovery Charge	di/dt=100A/μs	--	18	36	nC

NOTE:

- ① Repetitive rating; pulse width limited by max junction temperature.
- ② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 15A, V_{GS} = 10V. Part not recommended for use above this value
- ③ The power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C.
- ④ Pulse width ≤ 380μs; duty cycle ≤ 2%.

Typical Characteristics

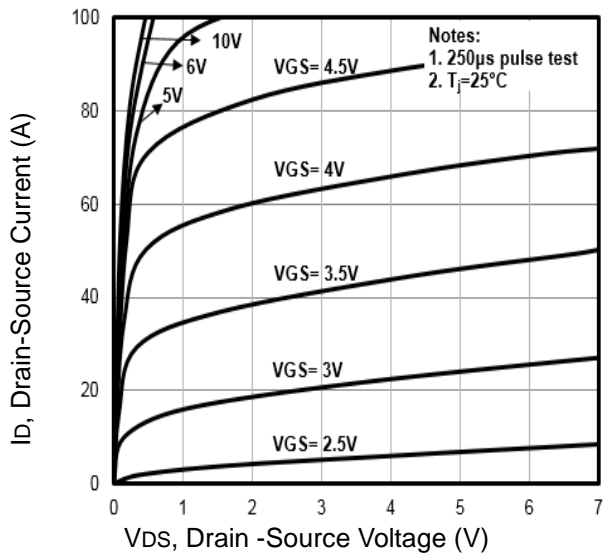


Fig1. Typical Output Characteristics

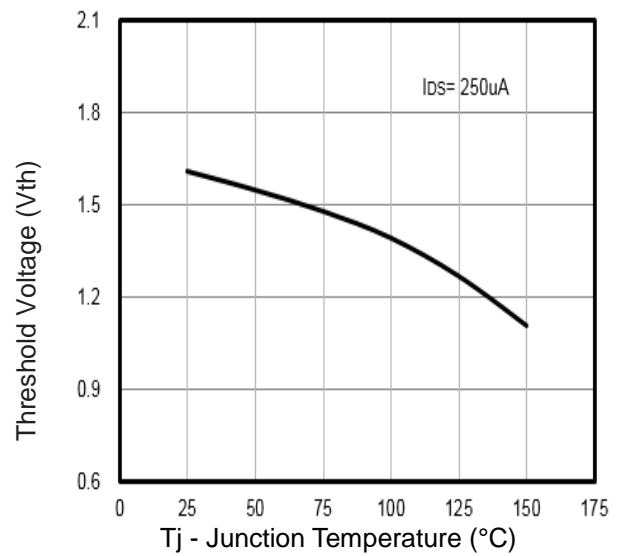


Fig2. Threshold Voltage Vs. Temperature

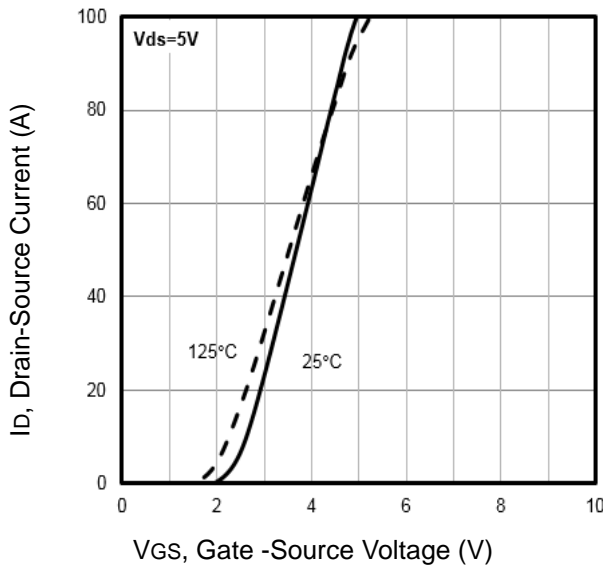


Fig3. Typical Transfer Characteristics

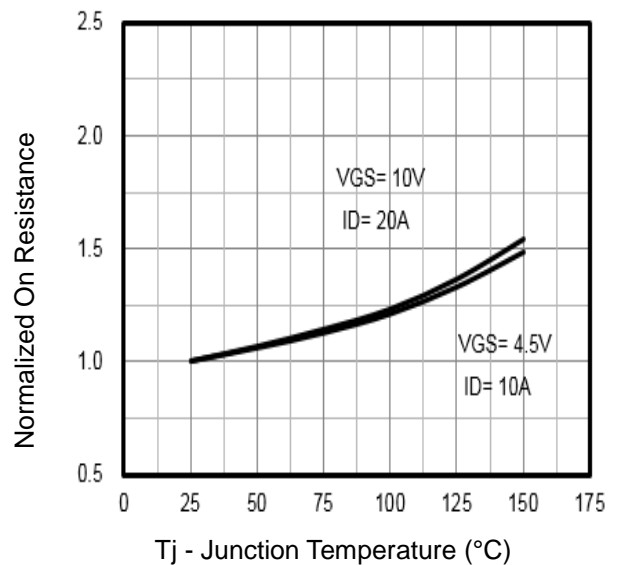


Fig4. Normalized On-Resistance Vs. Temperature

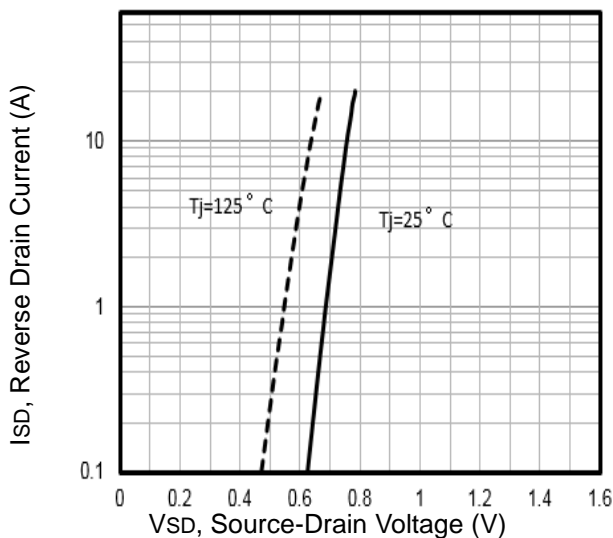


Fig5. Typical Source-Drain Diode Forward Voltage

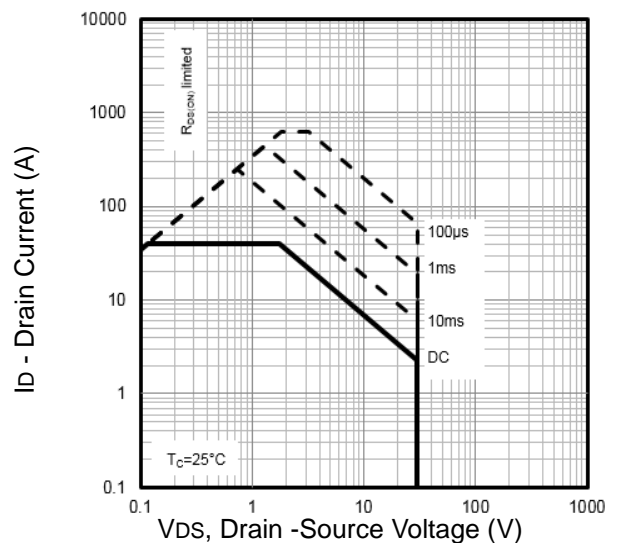


Fig6. Maximum Safe Operating Area

Typical Characteristics

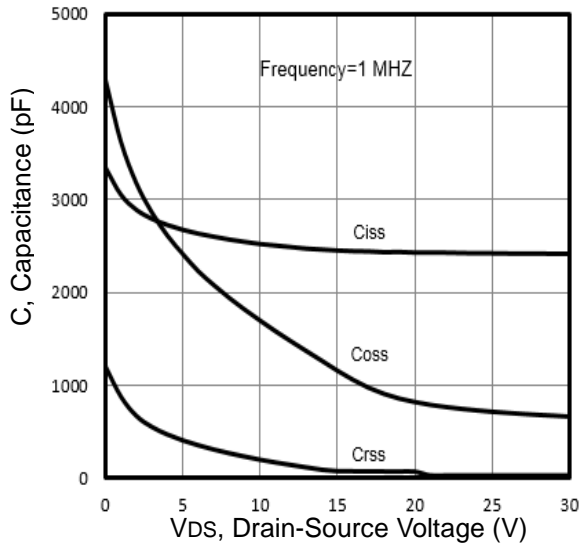


Fig7. Typical Capacitance Vs. Drain-Source Voltage

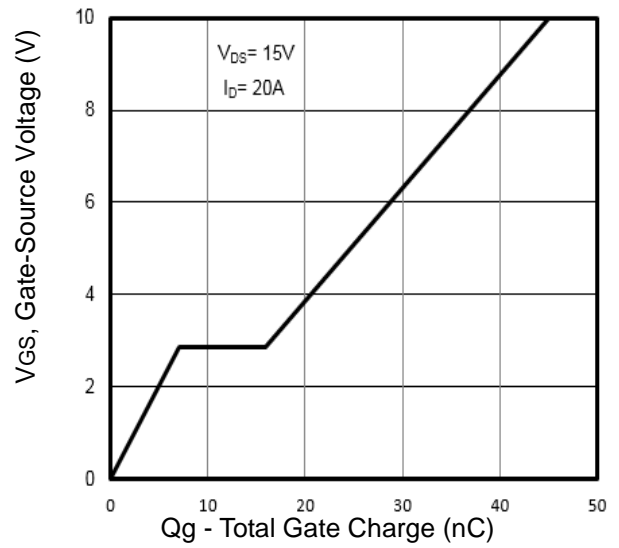


Fig8. Typical Gate Charge Vs. Gate-Source

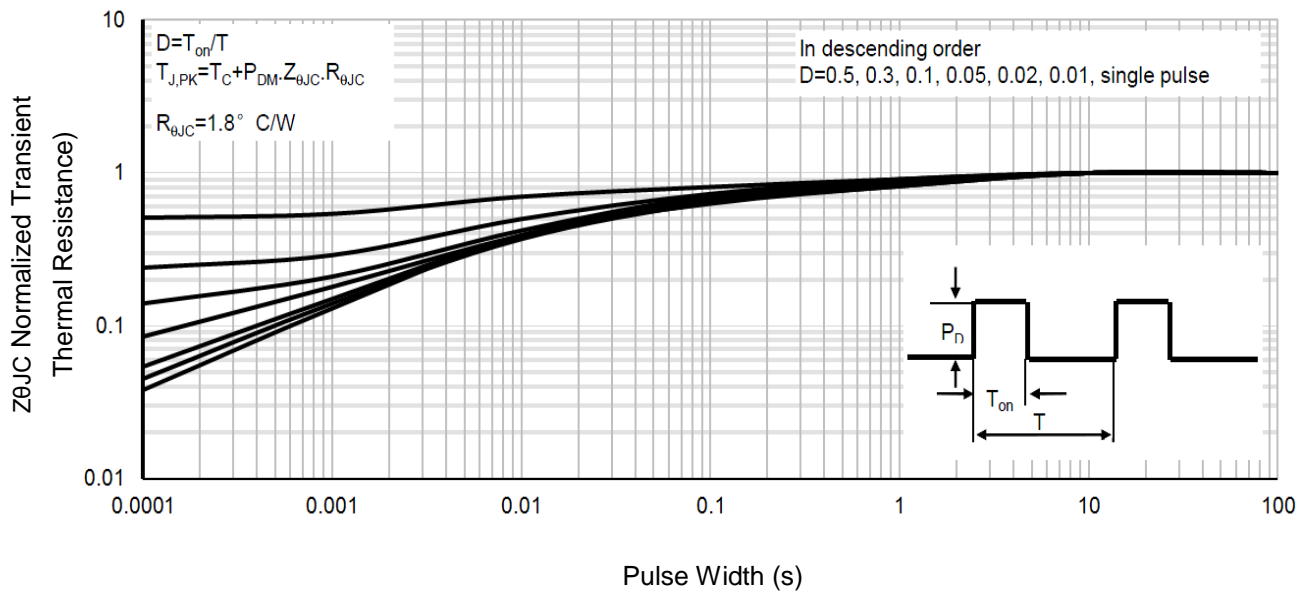


Fig9. Normalized Maximum Transient Thermal Impedance

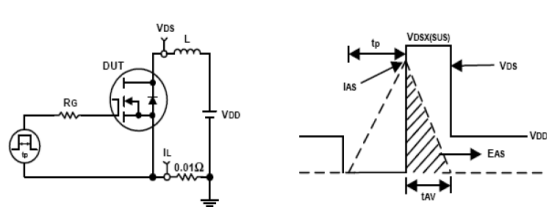


Fig10. Unclamped Inductive Test Circuit and waveforms

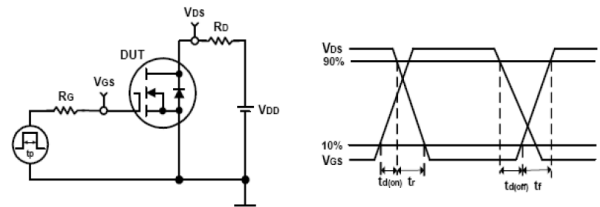
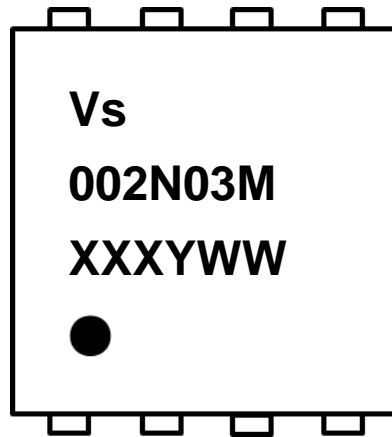


Fig11. Switching Time Test Circuit and waveforms



Marking Information



1st line: Vanguard Code (Vs)

2nd line: Part Number (002N03M)

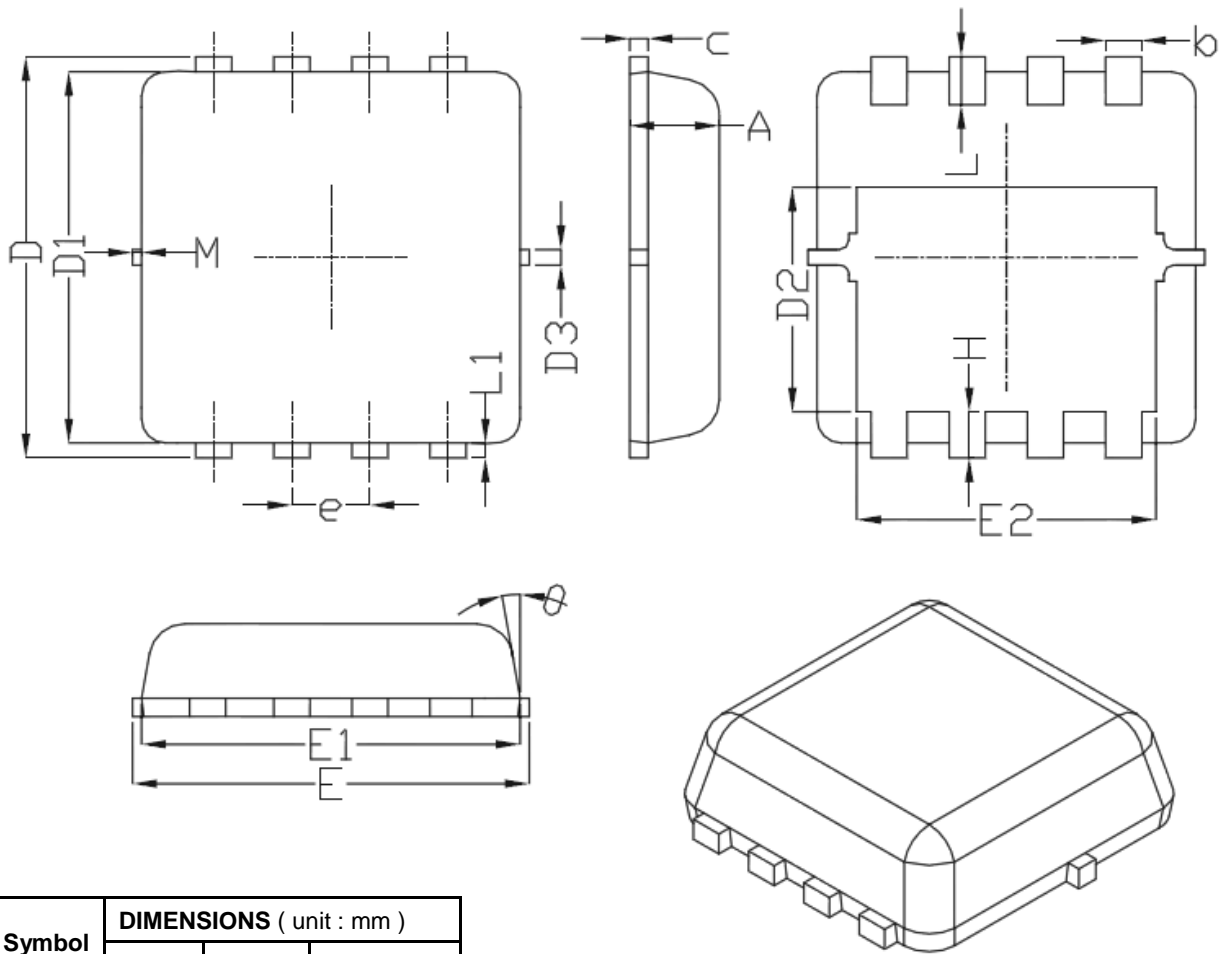
3rd line: Date code (XXXYWW)

XXX: Wafer Lot Number Code, code changed with Lot Number

Y: Year Code (e.g. E=2017, F=2018, G=2019, H=2020, etc)

WW: Week Code (01 to 53)

PDFN3333 Package Outline Data



Symbol	DIMENSIONS (unit : mm)		
	Min	Typ	Max
A	0.7	0.75	0.8
b	0.25	0.3	0.35
C	0.1	0.15	0.25
D	3.25	3.35	3.45
D1	3	3.1	3.2
D2	1.78	1.88	1.98
D3	--	0.13	--
E	3.2	3.3	3.4
E1	3	3.15	3.2
E2	2.39	2.49	2.59
e	0.65 BSC		
H	0.3	0.39	0.5
L	0.3	0.4	0.5
L1	--	0.13	--
θ	--	10°	12°
M	*	*	0.15
* Not specified			

Notes:

1. Follow JEDEC MO-240 variation CA.
2. Dimensions "D1" and "E1" do NOT include mold flash protrusions or gate burrs.
3. Dimensions "D1" and "E1" include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25mm per side.

Customer Service

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