General Description

The EA9103D is designed for portable RF and wireless applications with demanding performance and space requirements. The EA9103D performance is optimized for battery-powered systems to deliver ultra low quiescent current. Regulator ground current increases only slightly in dropout, further prolonging the battery life. The EA9103D also works with low-ESR ceramic capacitors, reducing the amount of board space necessary for power applications, critical in hand-held wireless devices. The EA9103D consumes less than 0.1uA in shutdown mode. The other features include ultra low dropout voltage, high output accuracy, current limiting protection and high ripple rejection ratio. The EA9103D is available in the SOT23-5 and DFN 1x1-4L packages.

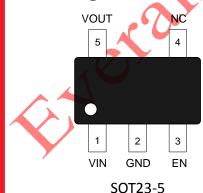
Features

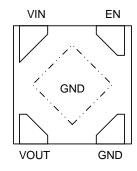
- 0.3uA Ultra-Low Quiescent Current
- 2V to 7V Input Voltage Range
- Low Dropout: 200mV@200mA
- 500mA Output Current
- 1.2V/1.8V/2.8V/2.5V/3.3V Output Voltage
- High PSRR: -70dB at 1KHz
- < 0.1uA Standby Current When Shutdown
- Fast Discharge
- Current Limiting and Thermal Shutdown Protection
- Available in SOT-23-5 and DFN 1x1-4L Packages

Applications

- Reference Power
- Portable Devices
- Bluetooth, Wireless Handsets

Pin Configurations





DFN 1x1-4L

Datasheet

Pin Description

		Pin No.	
Pin Name	Function Description	SOT23-5	DFN 1x1-4L
VIN	Power input voltage pin.	1	4
GND	Ground pin.	2	2, EP
EN	Enable pin. Do not leave this pin floating.	3	3
NC	Not Connect.	4	7,5
VOUT	Output voltage pin.	5	1

Function Block Diagram

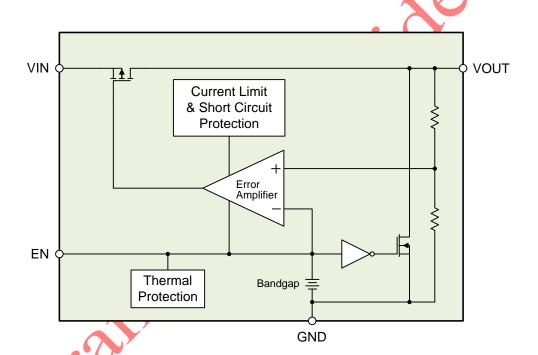


Figure 1. EA9103D internal function block diagram



500mA, Ultra-Low IQ, Ultra-Fast LDO

Absolute Maximum Ratings

Parameter	Value
Input Supply Voltage (V _{IN})	-0.3V to +9V
Output Voltage (V _{OUT})	-0.3V to (V _{IN} +0.3)V
Output Current (I _{OUT})	550mA
Lead Temperature (Soldering, 10 sec)	+260°C
Storage Temperature Range (T _s)	-55°C to +150°C
ESD Susceptibility (HBM)	2kV
ESD Susceptibility (MM)	200V

Note (1):Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

Exposure to "Absolute Maximum Ratings" conditions for extended periods may affect device reliability and lifetime.

Package Thermal Characteristics

Parameter	Value
SOT-23-5/DFN 1x1-4L Thermal Resistance (θ _{JC})	125°C/W
SOT-23-5/DFN 1x1-4L Thermal Resistance (θμ)	220°C/W
SOT-23-5/DFN 1x1-4L Power Dissipation at $T_A=25^{\circ}$ C (P_{Dmax})	0.55W

Note (1): P_{Dmax} is calculated according to the formula: $P_{DMAX}=(T_{JMAX}-T_A)/\theta_{JA}$.

Recommended Operating Conditions

Parameter	Value
Input Operating Voltage Range (V _{IN})	+2V to +7V
Ambient Temperature Range (T _A)	-40°C to +85°C
Junction Temperature Range (T _J)	-40°C to +125°C

Datasheet

Electrical Characteristics

 V_{IN} = V_{OUT} +1V, V_{OUT} = 3.3V, C_{IN} = C_{OUT} =1uF, T_A =25°C, unless otherwise noted

Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
Output Voltage Accuracy	ΔV_{OUT}	$I_{OUT} = 1mA$	-1.5		1.5	%
Output Loading Current	I _{LOAD}	$V_{EN} = V_{IN}, V_{IN}$ >2.2V		500		mA
Current Limit	I _{LI M}			550	• (mA
Short Circuit Current	I _{sc}	$R_{LOAD} = 1\Omega$		90	X	mA
Quiescent Current	I_Q	$V_{EN} \ge 1.2V$, $I_{OUT} = 0$ mA		0.3	0.8	uA
Dropout Voltage	W	$I_{OUT} = 200 \text{mA},$ $V_{OUT} > 2.8 \text{V}$. 2	220	260	mV
Dropout Voltage	V_{DROP}	$I_{OUT} = 300 \text{mA},$ $V_{OUT} > 2.8 \text{V}$	{}	370	410	mV
Line Regulation	ΔV_{LINE}	$V_{IN} = (V_{OUT}+1V)$ to $7V$, $I_{OUT} = 1mA$			0.3	%
Load Regulation	ΔLOAD	1mA < I _{OUT} < 300mA			35	mV
Standby Current	I _{STBY}	V _{EN} = GN D, S hutdown			0.1	uA
EN Leakage Current	I _{EN}				0.1	uA
EN Threshold Low Voltage	VIL	VIN = 3V to 5.5V, Shutdown			0.4	V
EN Threshold High Voltage	VIH	VIN = 3V to 5.5V, Start-up	1.2			V
Output Noise Voltage		10Hz to 100kHz, $I_{OUT} = 200mA$, $C_{OUT} = 1uF$		100		uVRMS
Power Supply Rejection Rate f = 1kHz	PSRR	$C_{OUT} = 1uF, I_{OUT} =$		-70		dB
Power Supply Rejection Rate f = 10kHz	FORK	100mA		-65		dB
Thermal Shutdown Threshold	T _{SD}			165		°C

Note (1): MOSFET on-resistance specifications are guaranteed by correlation to wafer level measurements.

^{(2):} Thermal shutdown specifications are guaranteed by correlation to the design and characteristics analysis.

500mA, Ultra-Low IQ, Ultra-Fast LDO

Application Circuit Diagram

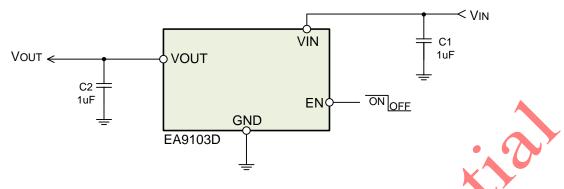


Figure 2. Typical application circuit diagram

Ordering Information

Part Number	Package Type	Packing Information
EA9103DVVT5R	SOT-23-5	Tape & Reel / 3000
EA9103DVVDGR	DFN 1x1-4L	Tape & Reel / 3000

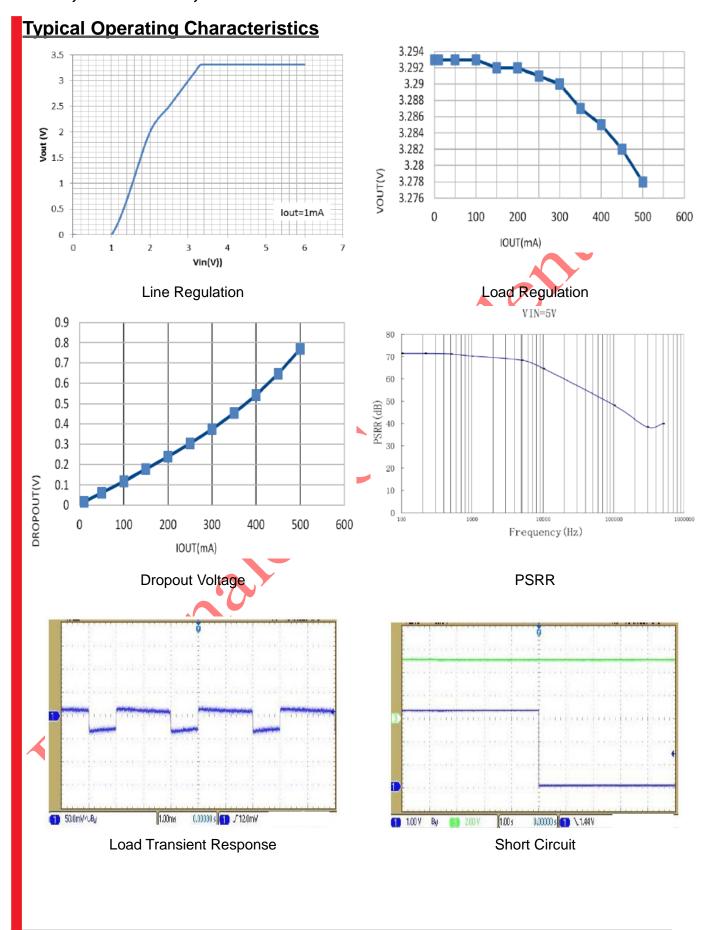
Note (1):"VV": Output voltage version code.

(2): "T5/DG": Package type code.

(3):"R": Tape & Reel.

Output Voltage Version Co	de Output Voltage
12	1.2V
18	1.8V
28	2.8V
25	2.5V
33	3.3V

Datasheet



500mA, Ultra-Low IQ, Ultra-Fast LDO

Application Information

Like any low-dropout regulator, the external capacitors used with the EA9103D must be carefully selected for regulator stability and performance. Using a capacitor whose value is > 1uF on the EA9103D input and the amount of capacitance can be increased without limit. The input capacitor must be located a distance that less than 0.5 inch from the input pin of the device to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line transient response. The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The EA9103D is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least 1uF with ESR is > 25m Ω on the EA9103D output ensures stability. The EA9103D still works well with output capacitor of other types due to the wide stable ESR range. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability and PSRR. The EA9103D features an LDO regulator enable/disable function. To assure the LDO regulator will switch on, the EN turn on control level must be greater than 1.2V. The LDO regulator will go into the shutdown mode when the voltage on the EN pin falls below 0.4V. The EA9103D have a quick-discharge function to protecting the system.

Thermal Considerations

Thermal protection limits power dissipation in EA9103D. When the operation junction temperature exceeds 165°C, the OTP circuit starts the thermal shutdown function turn the pass element off. The pass element turn on again after the junction temperature cools by 30°C. For continue operation, do not exceed absolute maximum operation junction temperature 125°C. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula:

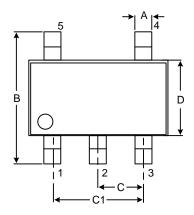
$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance. For recommended operating conditions specification of EA9103D, the $T_{J(MAX)}$ is the maximum junction temperature of the die (125°C) and T_A is the maximum ambient temperature. The junction to ambient thermal resistance θ_{JA} for SOT23-5 package is 220°C/W.

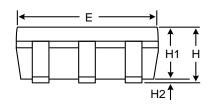
Datasheet

Package Information

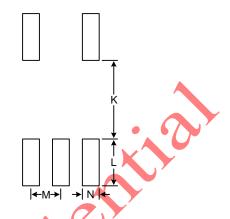
SOT-23-5 Package



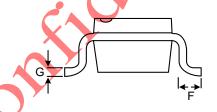
Top View



Side View



Recommended Layout Pattern



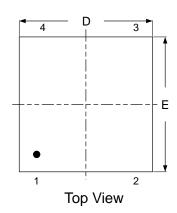
Front View

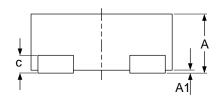
Unit:	mm

Cymphal	Dimension		Cymphol	Dimension
Symbol	Min	Max	Symbol	Тур
Α	0.30	0.50	K	1.40
В	2.65	2.95	L	1.40
С	0.85	1.05	М	0.95
C1	1.80	2.00	N	0.65
D	1.50	1.70		
Е	2,82	3.02		
F	0.30	0.60		
G /	0.10	0.20		
H	1.05	1.25		
H1	1.05	1.15		
H2	0.00	0.10		

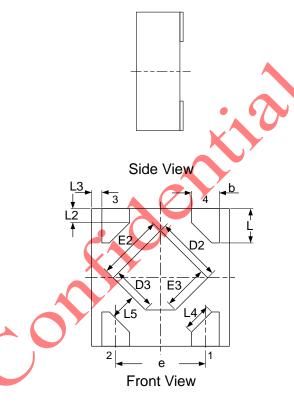
500mA, Ultra-Low IQ, Ultra-Fast LDO

DFN 1mmx1mm-4L Package





Side View



Unit:	mm

Cymphol		Dimension	
Symbol	Min	Nor	Max
Α	0.35		0.40
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
С		0.127	
D	0.95	1.00	1.05
D2	0.38	0.48	0.58
D3	0.23	0.33	0.43
е		0.65	
E .	0.95	1.00	1.05
E 2	0.38	0.48	0.58
E3	0.23	0.33	0.43
L	0.20	0.25	0.30
L2		0.103	
L3		0.075	
L4		0.208	
L5		0.200	