

General Description

The WSD4048DN56 is the highest performance trench N-ch and P-ch MOSFET with extreme high cell density , which provide excellent RDSON and gate charge for most of the synchronous buck converter applications .

The WSD4048DN56 meet the RoHS and Green Product requirement 100% EAS guaranteed with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

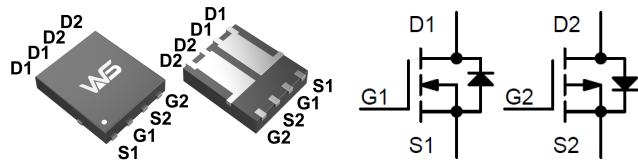
Product Summary

BVDSS	RDS(on)	ID
40V	14mΩ	34A
-40V	32mΩ	-24A

Applications

- High Frequency Point-of-Load Synchronous Buck Converter for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- CCFL Back-light Inverter

DFN5X6C-8-EP2 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-Ch	P-Ch	
V _{DS}	Drain-Source Voltage	40	-40	V
V _{GS}	Gate-Source Voltage	±20	±20	V
I _D @T _C =25°C	Continuous Drain Current, V _{GS} @ 10V ¹	34	-24	A
I _D @T _C =70°C	Continuous Drain Current, V _{GS} @ 10V ¹	22	-18	A
I _{DM}	Pulsed Drain Current ²	46	-40	A
EAS	Single Pulse Avalanche Energy ³	28	66	mJ
I _{AS}	Avalanche Current	17.8	-27.2	A
P _D @T _C =25°C	Total Power Dissipation ⁴	25	31.3	W
T _{STG}	Storage Temperature Range	-55 to 150	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction-Ambient ¹	---	62	°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹	---	5	°C/W

N-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$	40	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BVDSS Temperature Coefficient	Reference to 25°C , $I_D=1\text{mA}$	---	0.034	---	$\text{V}/^\circ\text{C}$
$R_{DS(\text{ON})}$	Static Drain-Source On-Resistance ²	$V_{GS}=10\text{V}$, $I_D=10\text{A}$	---	14	21	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}$, $I_D=5\text{A}$	---	18	25	
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=250\mu\text{A}$	1.5	2.0	2.5	V
$\Delta V_{GS(\text{th})}$	$V_{GS(\text{th})}$ Temperature Coefficient		---	-4.56	---	$\text{mV}/^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=32\text{V}$, $V_{GS}=0\text{V}$, $T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{DS}=32\text{V}$, $V_{GS}=0\text{V}$, $T_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20\text{V}$, $V_{DS}=0\text{V}$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=5\text{V}$, $I_D=10\text{A}$	---	15	---	S
R_g	Gate Resistance	$V_{DS}=0\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$	---	2.5	5.2	Ω
Q_g	Total Gate Charge (4.5V)	$V_{DS}=20\text{V}$, $V_{GS}=4.5\text{V}$, $I_D=12\text{A}$	---	9.5	---	nC
Q_{gs}	Gate-Source Charge		---	1.25	---	
Q_{gd}	Gate-Drain Charge		---	2.5	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=20\text{V}$, $V_{GS}=10\text{V}$, $R_G=3.3\Omega$	---	8.9	---	ns
T_r	Rise Time		---	2.2	---	
$T_{d(off)}$	Turn-Off Delay Time		---	41	---	
T_f	Fall Time		---	2.7	---	
C_{iss}	Input Capacitance	$V_{DS}=15\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$	---	810	---	pF
C_{oss}	Output Capacitance		---	90	---	
C_{rss}	Reverse Transfer Capacitance		---	60	---	

Guaranteed Avalanche Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
EAS	Single Pulse Avalanche Energy ⁵	$V_{DD}=25\text{V}$, $L=0.5\text{mH}$, $I_{AS}=10\text{A}$	10	---	---	mJ

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_s	Continuous Source Current ^{1,6}	$V_G=V_D=0\text{V}$, Force Current	---	---	23	A
I_{SM}	Pulsed Source Current ^{2,6}		---	---	46	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0\text{V}$, $I_s=1\text{A}$, $T_J=25^\circ\text{C}$	---	---	1.2	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating .
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The Min. value is 100% EAS tested guarantee.
- 6.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

P-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}$, $I_D=-250\mu\text{A}$	-40	---	---	V
$\Delta \text{BV}_{\text{DSS}}/\Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to 25°C , $I_D=-1\text{mA}$	---	-0.012	---	$\text{V}/^\circ\text{C}$
$R_{\text{DS}(\text{ON})}$	Static Drain-Source On-Resistance ²	$V_{\text{GS}}=-10\text{V}$, $I_D=-10\text{A}$	---	32	38	$\text{m}\Omega$
		$V_{\text{GS}}=-4.5\text{V}$, $I_D=-4\text{A}$	---	46	62	
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	$V_{\text{GS}}=V_{\text{DS}}$, $I_D=-250\mu\text{A}$	-1.5	-2.0	-2.5	V
$\Delta V_{\text{GS}(\text{th})}$	$V_{\text{GS}(\text{th})}$ Temperature Coefficient		---	4.32	---	$\text{mV}/^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{\text{DS}}=-32\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=25^\circ\text{C}$	---	---	1	uA
		$V_{\text{DS}}=-32\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{\text{GS}}=\pm 20\text{V}$, $V_{\text{DS}}=0\text{V}$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{\text{DS}}=-5\text{V}$, $I_D=-8\text{A}$	---	12.6	---	S
R_g	Gate Resistance	$V_{\text{DS}}=0\text{V}$, $V_{\text{GS}}=0\text{V}$, $f=1\text{MHz}$	---	13	16	Ω
Q_g	Total Gate Charge (-4.5V)	$V_{\text{DS}}=-20\text{V}$, $V_{\text{GS}}=-4.5\text{V}$, $I_D=-12\text{A}$	---	9	---	nC
Q_{gs}	Gate-Source Charge		---	2.54	---	
Q_{gd}	Gate-Drain Charge		---	3.1	---	
$T_{\text{d}(\text{on})}$	Turn-On Delay Time	$V_{\text{DD}}=-15\text{V}$, $V_{\text{GS}}=-10\text{V}$, $R_G=3.3\Omega$, $I_D=-1\text{A}$	---	19.2	---	ns
T_r	Rise Time		---	12.8	---	
$T_{\text{d}(\text{off})}$	Turn-Off Delay Time		---	48.6	---	
T_f	Fall Time		---	4.6	---	
C_{iss}	Input Capacitance	$V_{\text{DS}}=-15\text{V}$, $V_{\text{GS}}=0\text{V}$, $f=1\text{MHz}$	---	1904	--	pF
$-C_{\text{oss}}$	Output Capacitance		---	108	---	
C_{rss}	Reverse Transfer Capacitance		---	80	---	

Guaranteed Avalanche Characteristics

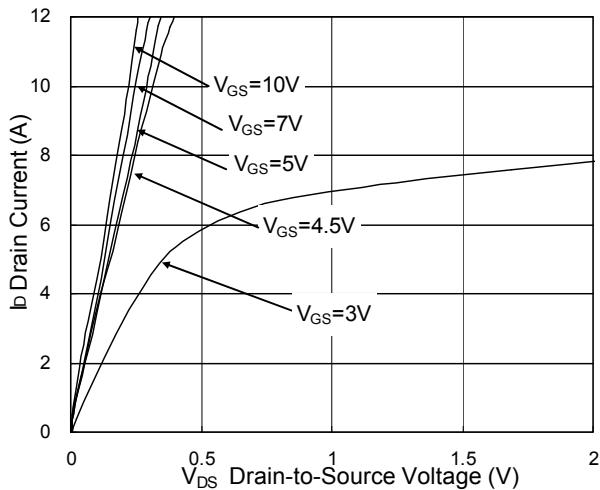
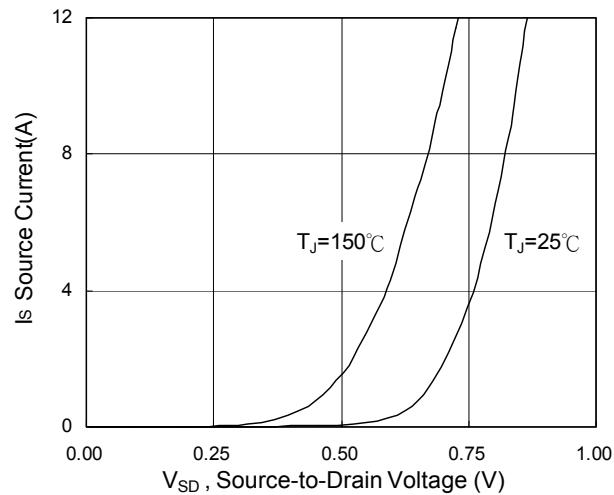
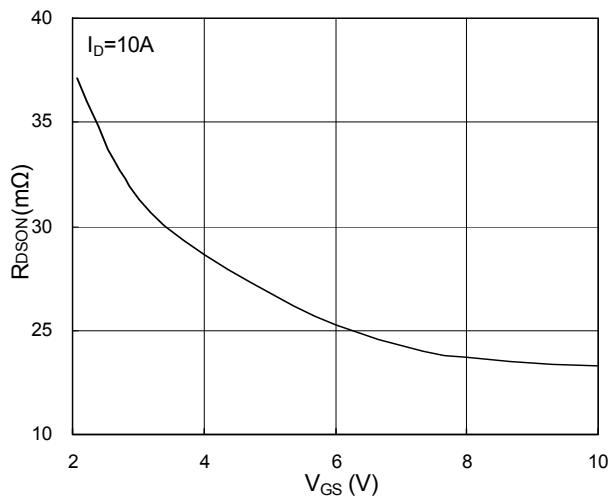
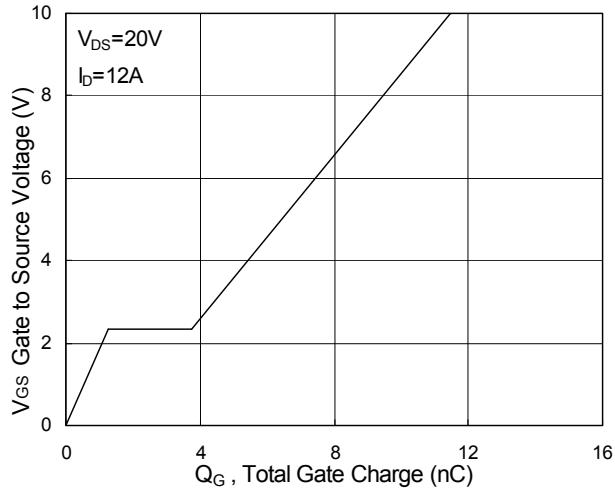
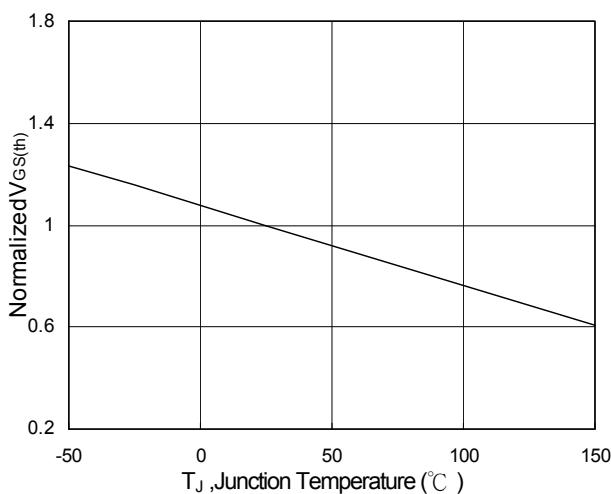
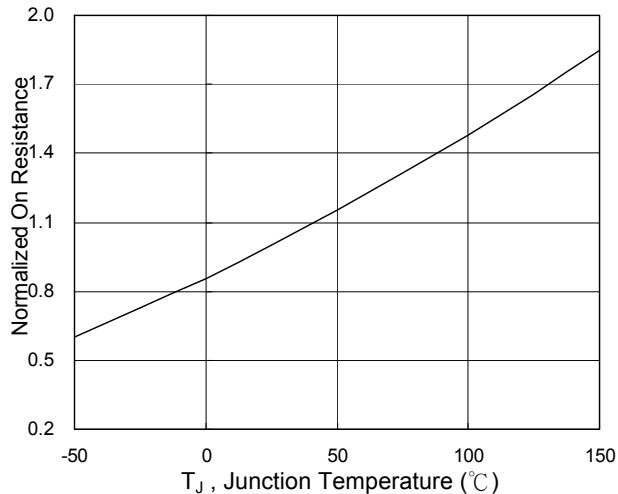
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
EAS	Single Pulse Avalanche Energy ⁵	$V_{\text{DD}}=-25\text{V}$, $L=0.1\text{mH}$, $I_{\text{AS}}=-10\text{A}$	20	---	---	mJ

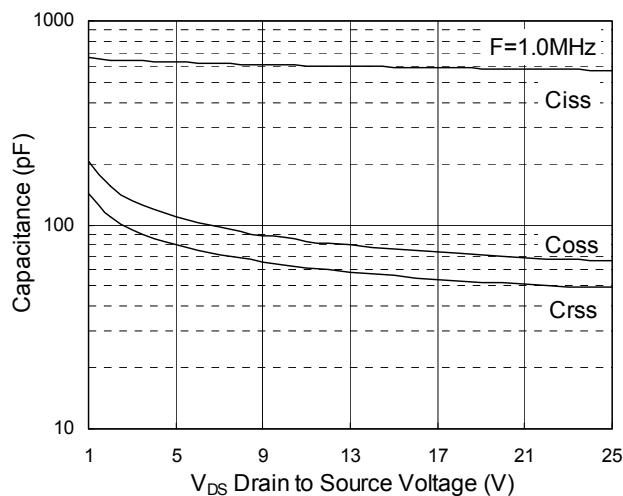
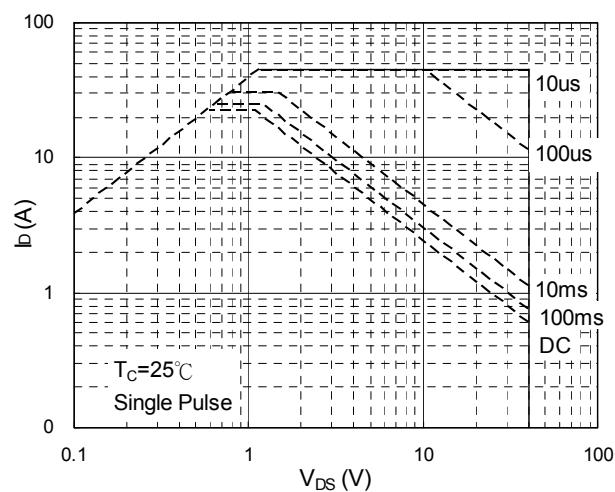
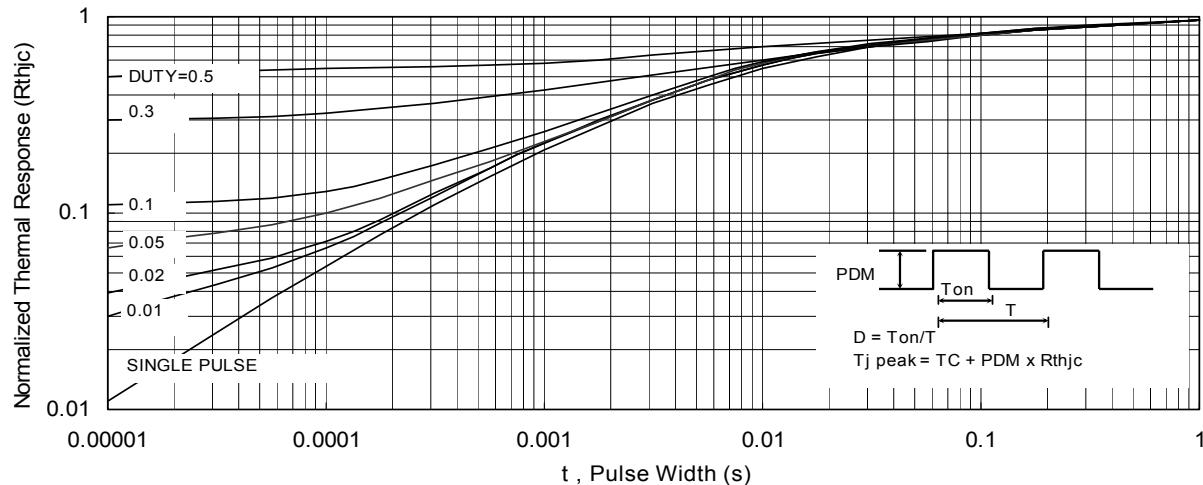
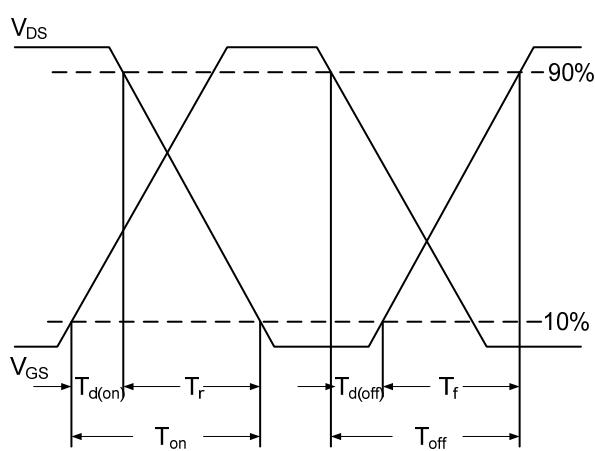
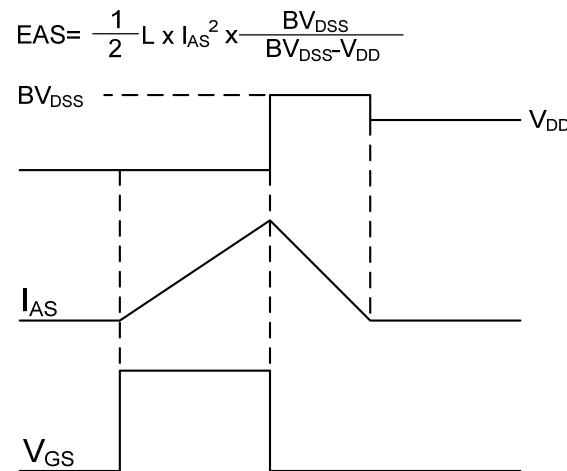
Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_s	Continuous Source Current ^{1,6}	$V_G=V_D=0\text{V}$, Force Current	---	---	-20	A
I_{SM}	Pulsed Source Current ^{2,6}		---	---	-40	A
V_{SD}	Diode Forward Voltage ²	$V_{\text{GS}}=0\text{V}$, $I_s=-1\text{A}$, $T_J=25^\circ\text{C}$	---	---	-1	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating .
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The Min. value is 100% EAS tested guarantee.
- 6.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

N-Channel Typical Characteristics

Fig.1 Typical Output Characteristics

Fig.3 Forward Characteristics of Reverse

Fig.2 On-Resistance vs. G-S Voltage

Fig.4 Gate-Charge Characteristics

Fig.5 Normalized $V_{GS(th)}$ vs. T_J

Fig.6 Normalized $R_{DS(on)}$ vs. T_J


Fig.7 Capacitance

Fig.8 Safe Operating Area

Fig.9 Normalized Maximum Transient Thermal Impedance

Fig.10 Switching Time Waveform

Fig.11 Unclamped Inductive Switching Wave

P-Channel Typical Characteristics

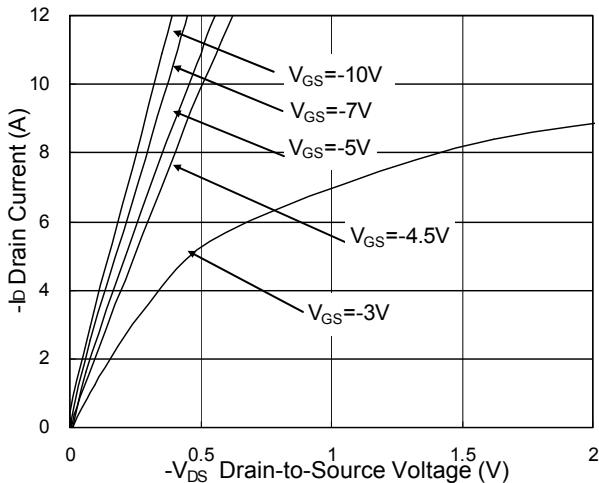


Fig.1 Typical Output Characteristics

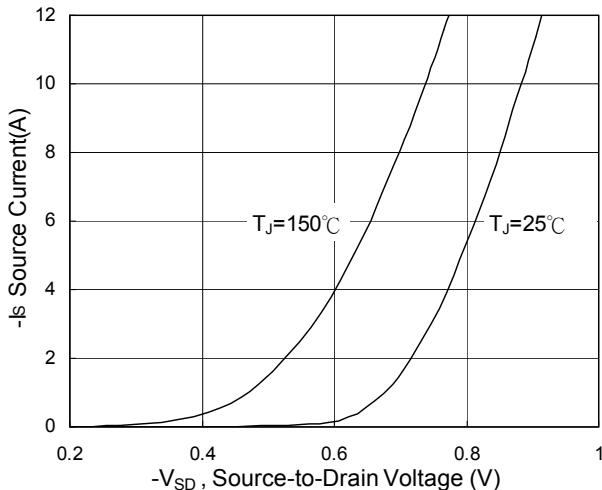


Fig.3 Forward Characteristics of Reverse

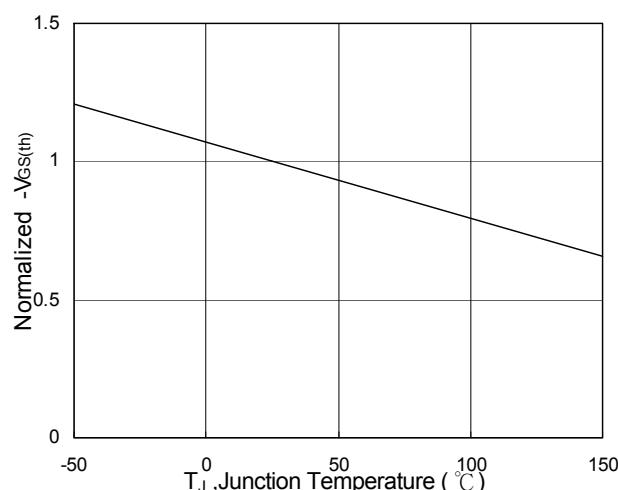


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

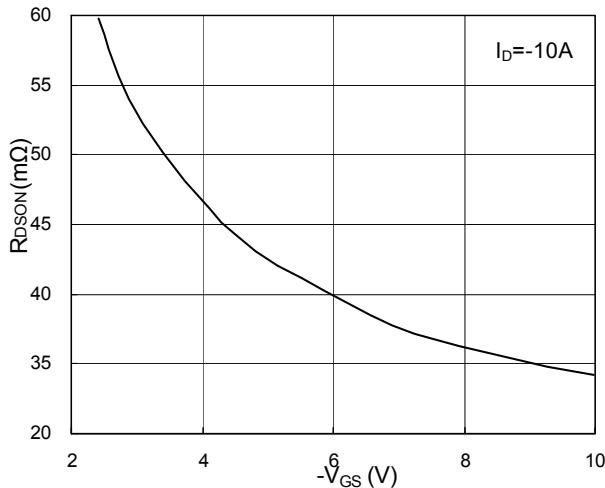


Fig.2 On-Resistance v.s Gate-Source

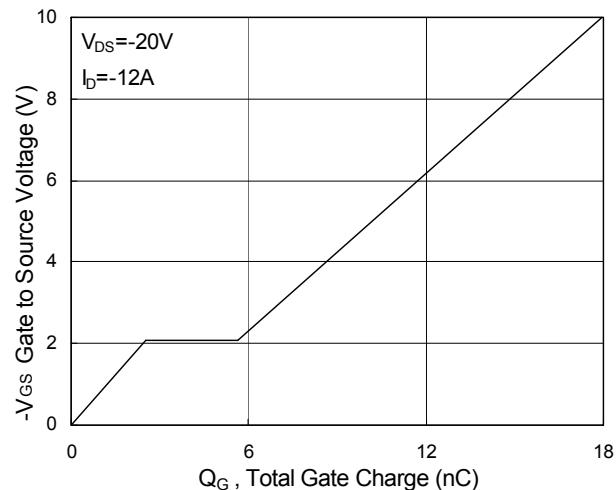


Fig.4 Gate-Charge Characteristics

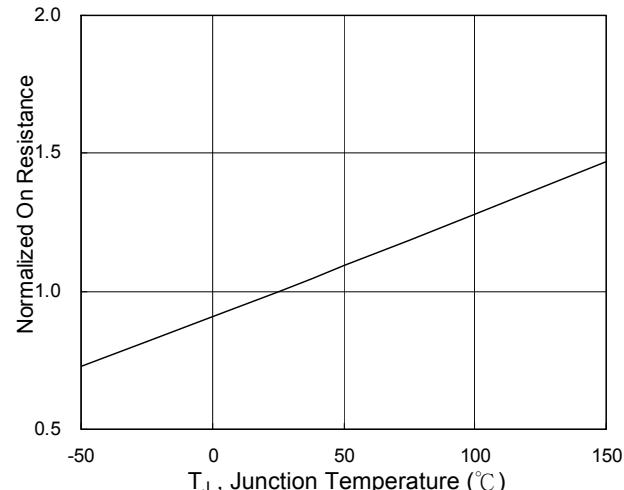


Fig.6 Normalized R_{DSON} v.s T_J

